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Product Specification

Part Number: FDS16x2(75x31)TBP

Revision: Ver 1.0

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Approved By	Review By	Prepared By
	Control Document ☐ Yes ☐ No	
	Confidential Document ☐ Yes ☐ No	

1.Module Basic Specification

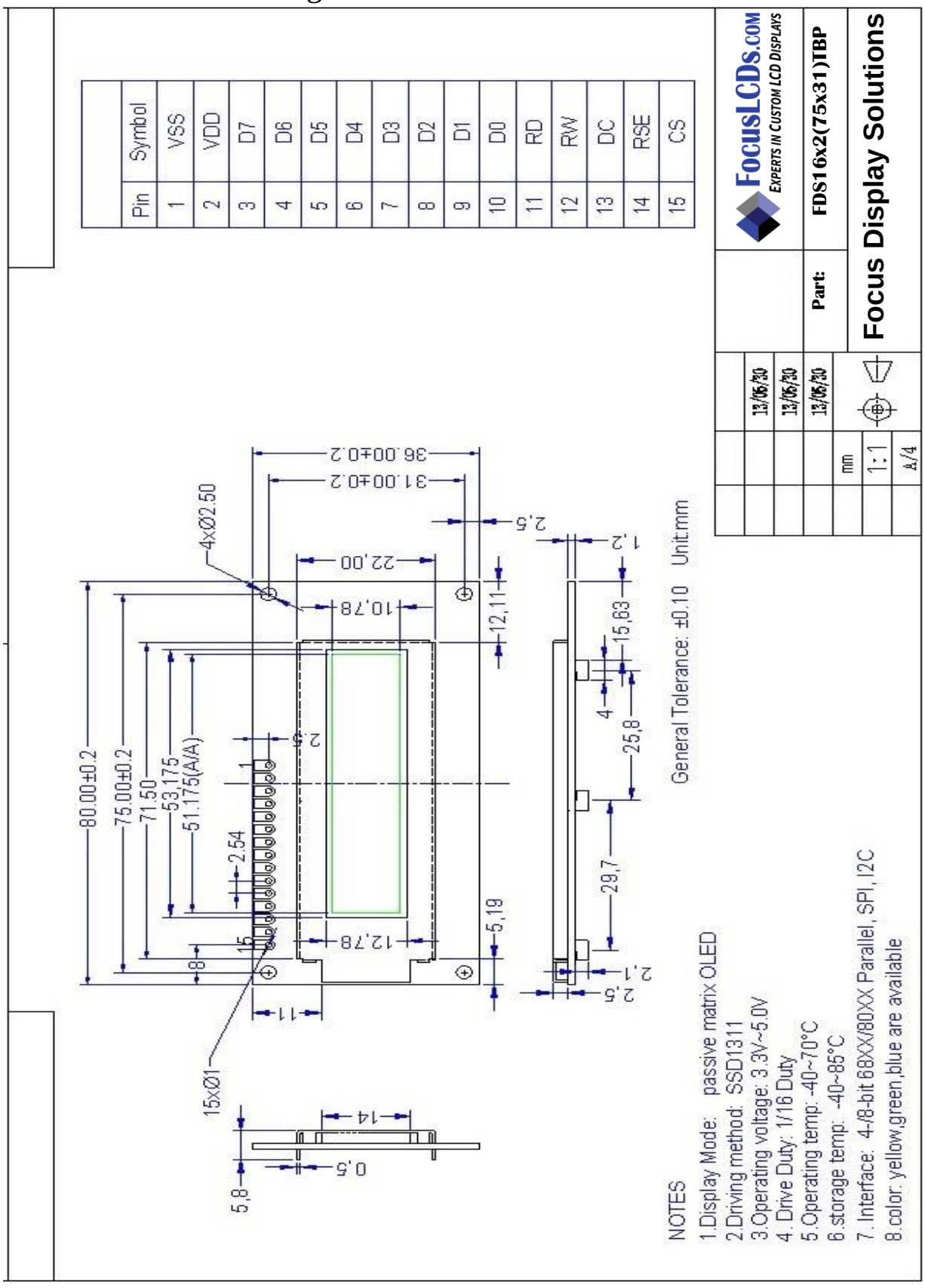
1.1 Display Specifications

1) Display Mode: Passive Matrix OLED
2) Display Color: Blue (monochrome)
3) Drive Duty: 1/16 Duty
4) Controller Driver: SSD1311

1.2 Module Features

Items	Specification	Unit
Diagonal A/A Size	2.06	Inch
Number of dots	16 Characters (5×8 dots)×2 Lines	dot
Module size	80×36×6.3	mm
Active Area	51.175×10.78	mm
viewing Area	53.175×12.78	mm
Character Pitch	3.235×5.71	mm
Character Size	2.65×5.07	mm
Dot Pitch	0.54×0.64	mm
Dot Size	0.49×0.59	mm
General Tolerance	±0.20	mm

1.3 Mechanical Drawing



1.4 Pin Definition

Pin number	Symbol	Type	Function
1	**VSS**	**P**	Power supply ground
2	**VDD**	**P**	3.3V power supply
3~10	**D7~D0**	**I/O**	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
11	**RD**	**I**	When interface to a 6800-series microprocessor, this pin will be used as the Enable(E) signal, When interface to an 8080-microprocessor, this pin receives the Read(RD#)signal.
12	**RW**	**I**	This is read/write control input pin connecting to the MCU interface. When interface to a 6800-series microprocessor, Read mode will be carried out when this pin is pulled HIGH and write mode when low .When interface to an 8080-microprocessor, this pin will be the data Write input. When serial interface is selected, this pin must be connected to Vss
13	**DC**	**I**	This is DATA/COMMAND control pin. When it is pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
14	**RSE**	**I**	This pin is reset signal input (active LOW)
15	**CS**	**I**	This pin is chip select input (active LOW)

1.5 Jump

BS0 /BS1 /BS2:MUC bus interface selection pin.

BS2	BS1	BS0	Interface
1	0	0	8-bit 6800 parallel
1	0	1	4-bit 6800 parallel
1	1	0	8-bit 8080 parallel
1	1	1	4-bit 8080 parallel

Notes: "0"connection GND and "1"connection V_{DD}.

2.Absolute Maximum Ratings.

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for logic	V_{DD}	-0.3	5.5	V	1,2
Supply Voltage for display	V_{CC}	0	13	V	1,2
Operating Temperature	Top	-40	70	°C	-
Storage Temperature	Tstg	-40	85	°C	-
Life time (100cd/m²)(yellow)		50000	-	hour	3
Life time (100cd/m²)(green)		50000	-	hour	3
Life time (100cd/m²)(blue)		50000	-	hour	3

Notes1:

All the above voltages are on the basis of "Vss =0V "

Notes2:

When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur, also for normal operations, it is desirable to use this module under the conditions according to Section 3."Optics and Electrical Characteristics "If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Notes3:

V_{CC} = 7.25V, Ta = 25° C, 50% Checkerboard.
Software configuration follows Section 6.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3.Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note4	120	150	-	cd/m^2
C.I.E(Blue)	(x) (y)	C.I.E 1931	0.46 0.45	0.50 0.49	0.54 0.53	
Dark Room Contrast	CR		-	10,000:1	-	
View Angle			-	Free	-	degree

Optical measurement taken at V_{DD} =2.8V,V_{CC} =7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Note 4: V_{DD} =2.8V,V_{CC} =12V, 30% Display Area Turn on.
Note 5: V_{DD} =2.8V,V_{CC} =12V, 100% Display Area Turn on.
Software configuration follows Section 4.4 Initialization.

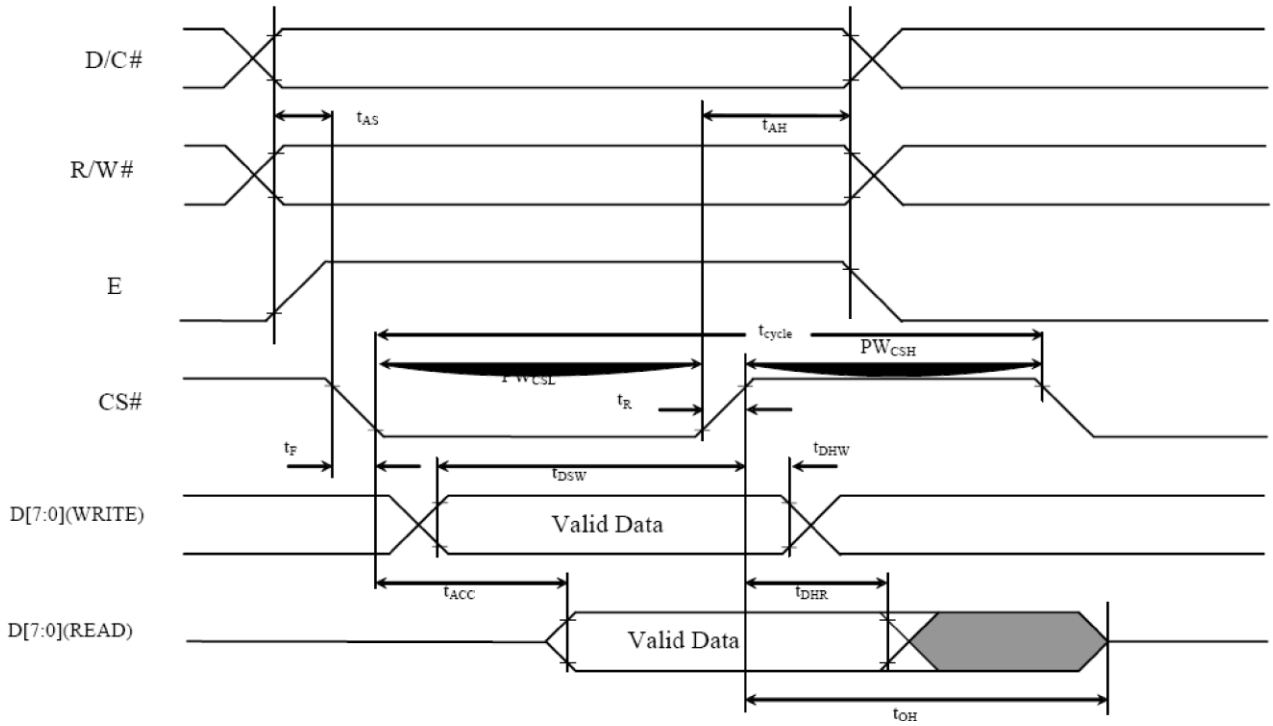
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage fot Logic	V_{DD}	InternalRegulatorEnable(Output)	-	3.3	-	V
		InternalRegulatorDisable(Input)	2.4	-	3.6	V
Supply Voltage for I/O	V_{DDIO}	5V Voltage Mode	4.4	-	5.5	V
		Low Voltage Mode	2.4	-	3.6	V
Supply Voltage for Display	V_{CC}	Note4	7	12	12.5	V
High Level Input	V_{IH}	-	$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}	-	0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{OUT}=100μA,3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT}=100μA,3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{DD}	I_{DD}	-	-	180	300	μA
Operating Currentfor V_{CC} (V_{CC} Supply Externally)	I_{CC}	Note5	-	16	21	mA
		Note6	-	27	32	mA
Sleep Mode Current for V_{DD}	$I_{DD,SLEEP}$	-	-	1	10	μA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$	-	-	2	10	μA

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(T_A=25°C, V_{DD} -V_{SS}=1.65V to 3.3V)

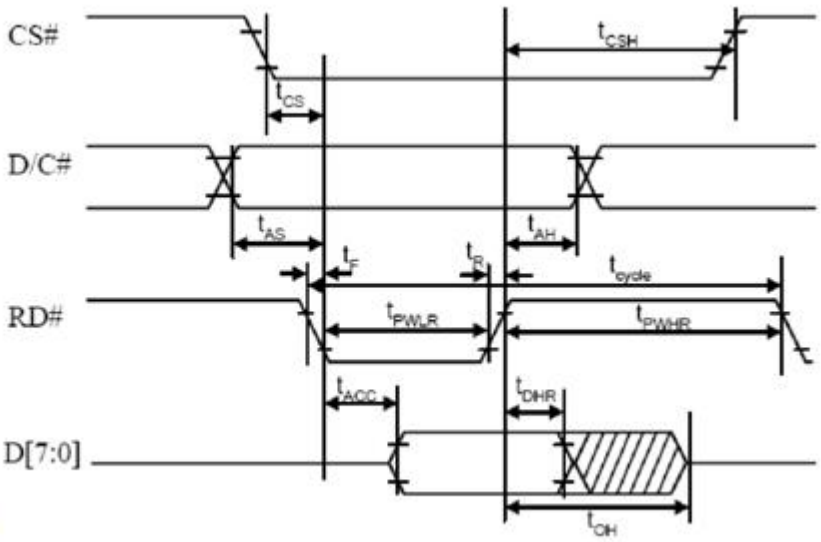
Symbol	parameter	Min	Type	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup time	13	-	-	ns
t_{AH}	Address Hold time	17	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	125	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW_{CSH}	Chip select High Pulse Width (read)	155	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



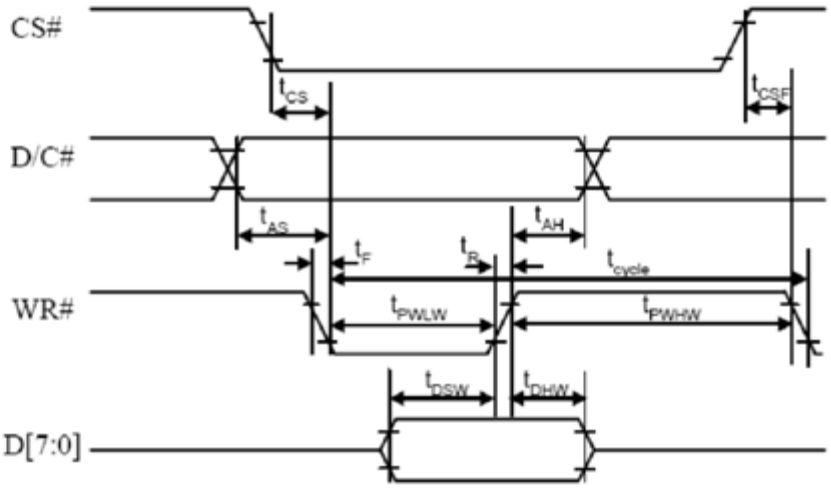
3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(TA=25°C, V_{DD} -V_{SS}=1.65V to 3.3V)

Symbol	parameter	Min	Type	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup time	13	-	-	ns
t_{AH}	Address Hold time	17	-	-	ns
t_{CS}	Chip Select time	0	-	-	ns
t_{CSH}	Chip select Hold Time To read signal	0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	90	ns
t_{ACC}	Access Time	-	-	125	ns
t_{PWLR}	Read Low time	250	-	-	ns
t_{PWLW}	Write Low time	50	-	-	ns
t_{PWHR}	Read High time	155	-	-	ns
t_{PWHW}	Write High time	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



(Read Timing)



(Write Timing)

4. Functional Specification

4.1 Commands

Command	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution time fosc=250khz
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear the screen & return to the address 0	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H", return cursor to its original position, if shifted. The contents of DDRAM are not changed.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address: I/D = "1": cursor/ blink moves to right & DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left & DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR).	40µs
Cursor or Display Shif	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left	40µs
Feature set	0	0	0	0	1	DL	N	F	x	x	Setting the length of the data bus (DL), and display the number of rows (N) and character font (F) DL=1: 8 bits F=0: 5x7 dots DL=0: 4 bits F=1: 5x10 dots N=0: 1 row show N=1: 2 row show	40µs
Set CGRAM address	0	0	0	1	Character Generator (CG) RAM Address						Set CGRAM address in address counter. (POR=00 0000)	40µs
Set DDRAM Address	0	0	1	Display Data (DD) RAM Address / Cursor Address							Set the DD RAM address, DD RAM data to be transmitted and received in this order	40µs
Write data	1	0	Write Data								Write data into internal RAM (DDRAM / CGRAM).	46µs
Read Data	1	1	Read Data								Read data from internal RAM (DDRAM / CGRAM).	46µs

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:
1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms (When V_{CC} is stable)
7. Send Display on command

4.2.2 Power down Sequence:
1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}

Note **:**
1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:
1. Display off, Cursor off, Blink off.
2. Power Down off.
3. 5-dot font is default.
4. Display Shift Disable.
5. CGRAM address is 00h. SEGRAM address is 00h.
6. DDRAM address is 00h.
7. Display start line is set at display RAM address 0
8. Column address counter is set at 0
9. Normal scan direction of the COM outputs
10. Contrast control register is set at 7Fh