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Application Note FAN4219

Working with the E70GE1-RW820-N (Part 1)

This application note will discuss the hardware requirements of driving the E70GE1-RW820-N TFT Display Module with an ST Nucleo-F767ZI microcontroller development board.

Working with the E70GE1-RW820-N Display (Part 1)

This series of application notes will discuss the hardware and software requirements of driving the [E70GE1-RW820-N](#) TFT Display Module with an [ST Nucleo-F767ZI](#) microcontroller development board. The Nucleo-F767ZI has the required bandwidth and I/O pins but lacks enough internal SRAM for a full frame buffer. Part 1 (FAN4219) will walk through the hardware requirements and interfacing with the display. Part 2 (FAN4220) will work on developing the firmware.

1. Introduction

This application note will discuss how to connect the display module to a microcontroller. The E70GE1-RW820-N is supplied with the [parallel RGB interface](#) which poses a challenge to low pin count and low clock frequency microcontrollers (MCU). Below are the reasons for selecting the ST Nucleo-F767ZI MCU board.

The RGB interface has 30 signals, including ground (GND), that must be connected to the MCU of choice. Modern MCUs have several GND and power pins along with an external reset pin. In addition, some MCUs have programming pins that cannot be used for application circuitry. Therefore, a minimum of a 40-pin MCU is necessary.

The display runs on 3.3V logic levels. To make interfacing easier selecting an MCU that can run on 3.3V logic negates the need for logic-level translator circuitry. Most MCUs produced today can operate on 5V and 3.3V logic levels without issue. The STM32F7 series devices run natively on 3.3V.

In general, the controller chips that only have the RGB interface need an external frame buffer as they do not have internal graphics memory (GRAM). This memory can be located internally in an MCU with a large enough RAM. Another option is to select an MCU with an external RAM interface.

In either case, the MCU-controlled RAM will provide the frame buffer for the display. The Nucleo-F767ZI does not have enough internal SRAM for a full frame buffer. In this application note, the display is driven with a smaller frame buffer as driving the display with the RGB interface is the main goal.

Timing and bandwidth are other concerns when [selecting an MCU](#). The dot clock (DCLK) frequency and timing of the display require the use of an MCU with a higher clock frequency. An MCU with a timer that can produce a 50% duty cycle, 33.3MHz clock signal is necessary for proper clocking of the DCLK pin. The general-purpose I/O pins (GPIO) also need to support toggling at this frequency without jitter (changes in timing) or distortion (non-square waveform). [Timing and Bandwidth](#) will be discussed further in Section 5.

FAN4219

The main characteristics of the display are as follows:

- 7.0" TFT, 154.08(H) x 85.92(V) mm Viewing Area
- 800 x 480 Pixels
- 16/18/24-bit RGB Interface for up to 16.7M Colors
- EK9716 & EK73002 Display Controllers
- White LED Backlight
- Transmissive / Normally White
- Typical Operating Voltage 3.3V



Figure 1. E70GE1-RW820-N TFT Display

To connect the display to the Nucleo-F767ZI Development Board, it is necessary to use the [KBB5040A Breakout Board](#). This board adapts from the flexible printed circuit (FPC) cable of the display to pin headers. Jumpers can then connect from the adapter to the MCU board.

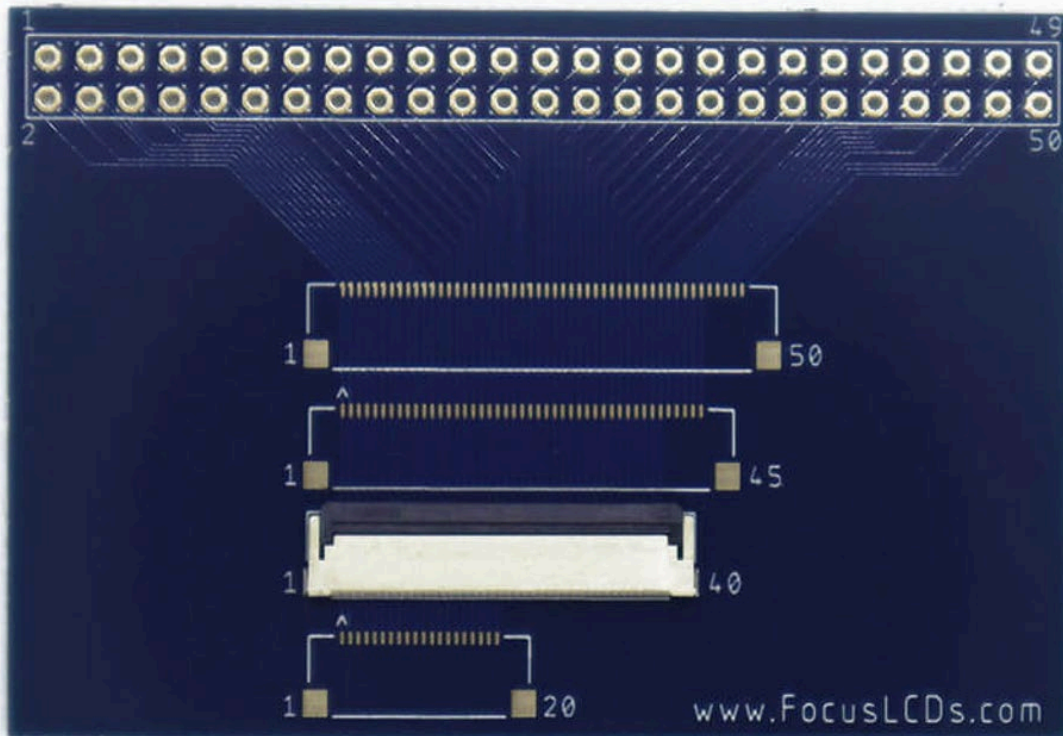


Figure 2. KBB5040 40-pin FPC Breakout Board

The MCU in this application is the [ST Nucleo-F767ZI Development Board](#).

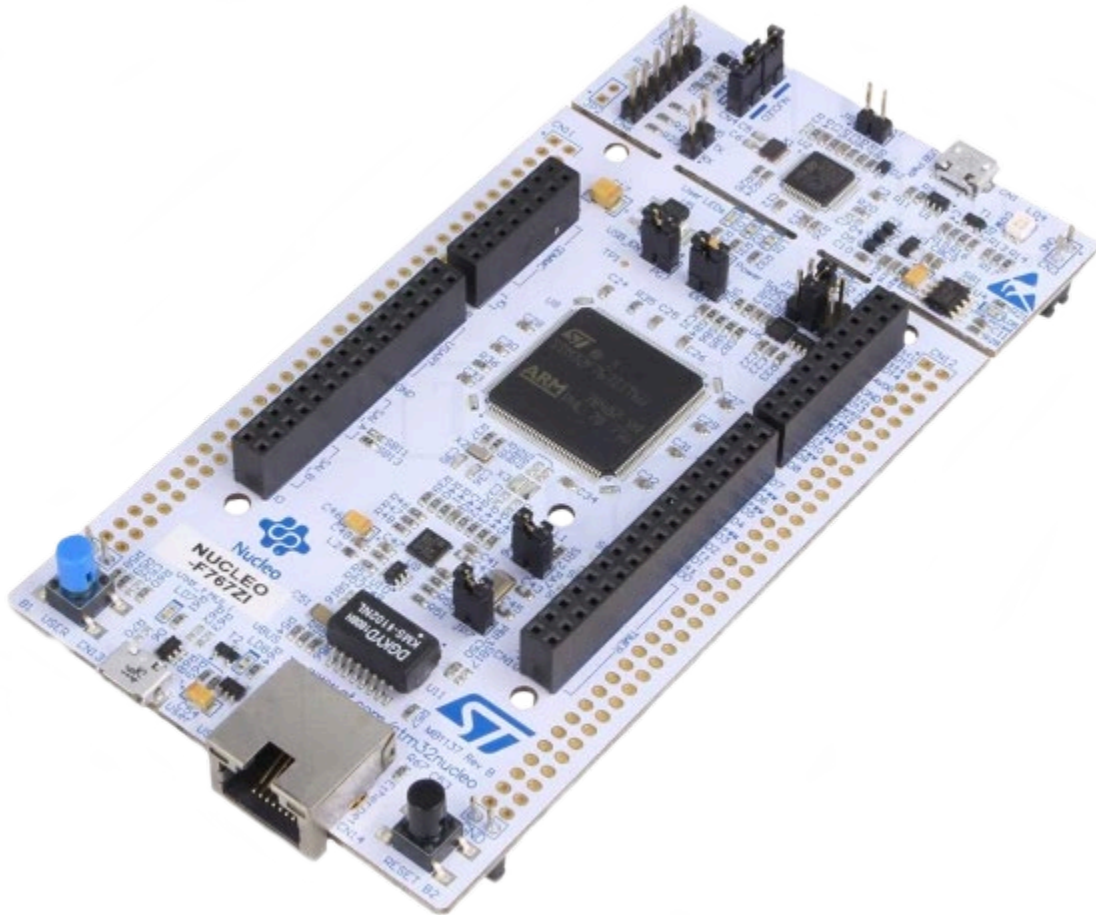


Figure 3. Nucleo-F767ZI MCU Dev Board

2. Required Hardware

The hardware requirements are detailed below.

Table 1. Hardware

Qty	Description	Notes
1	E70GE1-RW820-N TFT Display	FocusLCDs
1	KBB5040A Breakout Board or other 40-pin 0.5mm Pitch FPC Adapter Board	FocusLCDs
1	ST Nucleo-F767Zi MCU Board with Micro USB Cable	ST
1	Jumper Wires	
1	Benchtop Variable Power Supply	

The KBB5040A breakout board adapts the FPC cable from the display to the pin header for connecting to the Nucleo board.

The benchtop power supply is to provide power to the backlight. Another option is to design a constant current, boost mode switching power supply for driving the white LEDs. A pulse-width modulated (PWM) signal from the MCU to the backlight power supply, can be used to control the brightness of the display. Designing a switch-mode power supply is outside the scope of the application note.

3. Hardware Connections

The RGB interface has 29 signals along with several power and ground pins to be connected to the MCU. Connect the display FPC cable to the 40-pin FPC connector on the KBB5040A breakout board. Jumpers will be connected between the breakout board and the MCU board as listed in Section 4 Pin Assignments.

The color depth in bits-per-pixel (bpp) determines which color data signal pins to connect to the MCU. In 16 bpp mode (RGB 565 format) the MCU provides the red R[4:0], green G[5:0], and blue B[4:0] signals. The 18 bpp mode uses 6 bits of data and the 24 bpp mode use 8 bits of data for each color. Refer to Table 2. Pixel Data Format for the number of color data signals per bit depth.

Table 2. Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24-bit	1	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18-bit	1							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16-bit*	1									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

*16-bit format is in RGB 565 color

The backlight will be driven separately from the benchtop power supply. Set the power supply’s output to 9.3V and limit the output current to 180mA. Add a 51 Ohm, 2-Watt resistor in series to limit the current flow if the power supply does not have this feature. Size the resistor up or down to adjust the brightness level. Even if the power supply can limit the current, a resistor in series is a good safety precaution.

4. PIN Assignments

The RGB interface has up to 24 data lines for color, 5 control lines, a 3.3V power, and 2 ground pins that need to be connected to the MCU. Though the DCLK line is running at 33.3Mhz, controlled impedance and trace length are not major concerns when laying out the production PCB. In this instance, using jumper wires to connect the display breakout board to the MCU will not cause any signal degradation if they are kept short.

The 24-color data lines should be connected to parallel GPIO pins preferably on one port or split between 2 ports. This will ease the MCU's data transfer and allow for internal peripherals such as direct memory access (DMA) to handle data movement without CPU intervention. The only critical signal is the DCLK. This can be a divided-down clock output or a timer with a 50% duty cycle PWM running at 33.3 MHz.

The display breakout board pin connections are detailed in the table below.

Table 3. Pin Assignments

Pin No.	Pin Name	Description	Pin Name	Connection
1	LED K	Cathode Pin of Backlight	K	Neg of Power Supply
2	LED A	Anode Pin of Backlight	A	Pos of Power Supply
3	GND	Power Ground	GND	GND on Nucleo board
4	VDD	Power Supply	3V3	3V3 on Nucleo board
5	R0	Red Data Signal	PG13	CN11-68
6	R1	Red Data Signal	PA2	CN12-35
7	R2	Red Data Signal	PA1	CN11-30
8	R3	Red Data Signal	PB0	CN11-34
9	R4	Red Data Signal	PA5	CN12-11
10	R5	Red Data Signal	PC0	CN11-38
11	R6	Red Data Signal	PB1	CN12-24
12	R7	Red Data Signal	PE15	CN12-53
13	G0	Green Data Signal	PE5	CN11-50
14	G1	Green Data Signal	PE6	CN11-62
15	G2	Green Data Signal	PA6	CN12-13
16	G3	Green Data Signal	PE11	CN12-56
17	G4	Green Data Signal	PB10	CN12-25
18	G5	Green Data Signal	PB11	CN12-18
19	G6	Green Data Signal	PC7	CN12-19
20	G7	Green Data Signal	PG8	CN12-66
21	B0	Blue Data Signal	PE4	CN11-48
22	B1	Blue Data Signal	PG12	CN11-65
23	B2	Blue Data Signal	PC9	CN12-1
24	B3	Blue Data Signal	PD10	CN12-65

25	B4	Blue Data Signal	PE12	CN12-49
26	B5	Blue Data Signal	PA3	CN12-37
27	B6	Blue Data Signal	PB8	CN12-3
28	B7	Blue Data Signal	PB9	CN12-5
29	GND	Power Ground	GND	GND on Nucleo board
30	DCLK	Dot Clock (Pixel Clock) signal for data latching and internal timing	PE14	CN12-51
31	DISP	Display Controller Standby Mode Selection DISP = LOW Standby DISP = HIGH Display On	PC10	CN11-1
32	HSYNC	Horizontal Sync Signal	PC6	CN12-4
33	VSYNC	Verticle Sync Signal	PA4	CN11-32
34	DE	Data Input Enable	PF10	CN12-42
35	NC	--		NC
36	GND	Power Ground	GND	GND on Nucleo board
37-40	NC	--		NC

5. Timing and Bandwidth

5.1. Display Timing

When selecting the MCU to drive the display the DCLK period, horizontal resolution, vertical resolution, front porch, and back porch must be taken into consideration. The display has a typical DCLK frequency of 33.3 MHz. Using the formula $T = \frac{1}{f}$ (S), where T is time in seconds and f is the frequency in Hz, DCLK has a period of 30 nS.

This period will be needed when calculating the total frame time or the time to draw one frame. It is a critical measurement as the MCU writes to the frame buffer between frames. The DMA will transfer the contents of the frame buffer to the display during a frame write.

The total frame time is the combination of row (line) time \times vertical resolution + vertical front and back porch. Figure 4 shows how the columns and rows relate to each other in a frame.

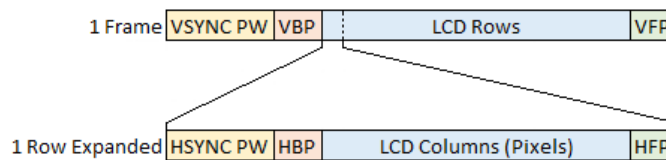


Figure 4. Frame and Row layout

- VSYNC PW is the starting pulse of a frame
- VBP and VFP are the vertical back and front porch
- HSYNC PW is the starting pulse for one line
- HBP and HFP are the horizontal back and front porch

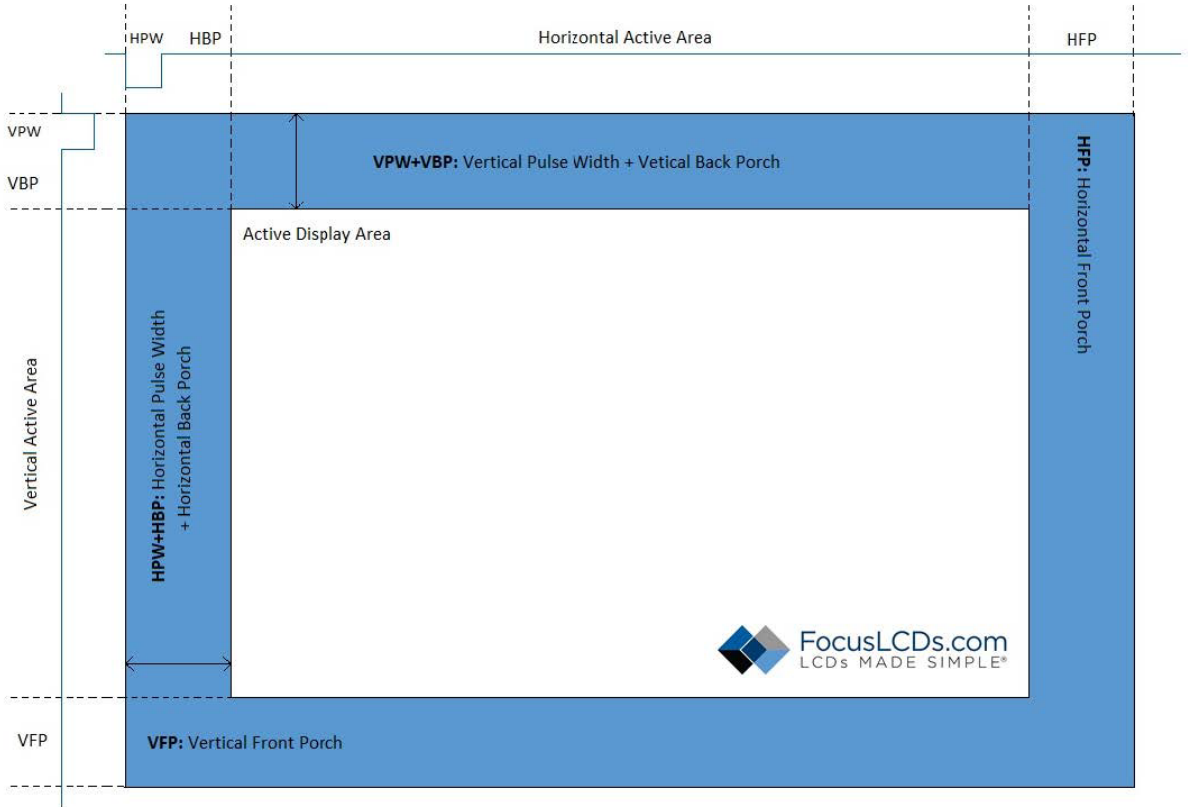


Figure 5. Active Display Area

Reading through the [datasheet](#) Section 5.0 TFT AC Characteristics shows the HSYNC period time (Th) of 1056 DCLKs or 31.68 μ s. This includes the HSYNC pulse (Thw) + horizontal pixel resolution (Thdisp) + horizontal back porch (Thbp) + horizontal front porch (Thfp). The Thw can be from 1 to 40 DCLKs and is adjusted to meet the minimum MCU setup time to prepare to transfer 1 line. Thbp does not have a set number of DCLKs as it is used to fill in the horizontal time to complete the typical horizontal period of 1056 DCLKs. Both Thbp and Thfp are adjusted to center the image horizontally within the active display area. These values should be set only be set up once and do not change while the display is running.

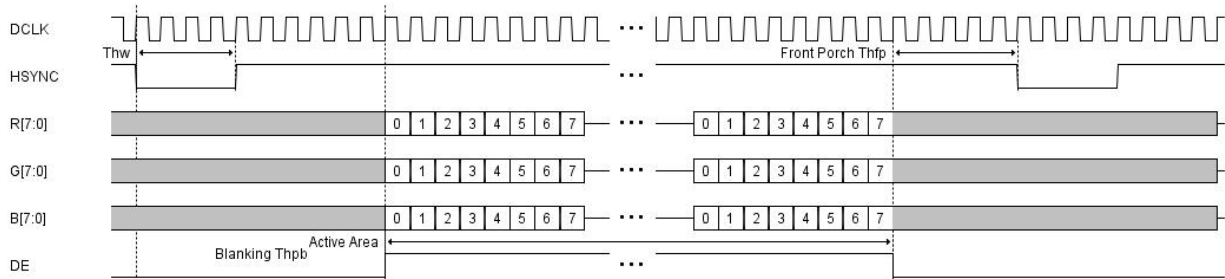


Figure 6. Horizontal Timing Diagram

The VSYNC period time (T_v) is typically 525 TH, while 1 Th is the HSYNC period (1056 DCLKs = 31.68 μ s). The period time is calculated from VSYNC pulse (T_{vw}) + vertical display period (vertical resolution T_{vdisp}) + vertical back porch (T_{vbp}) + vertical front porch (T_{vfp}). T_{vw} can be adjusted between 1 and 20 TH to compensate for MCU timing. The T_{vbp} is modified to complete the timing for 1 frame. Both T_{vbp} and T_{vfp} will be used to center the image vertically within the active display area. Like the horizontal setting, these values do not change during operation and should be set once.

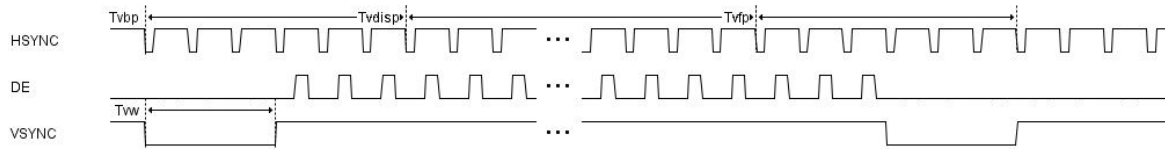


Figure 7. Vertical Timing Diagram

The final timing can then be calculated as HSYNC period time \times VSYNC period time \times DCLK period. In this instance, it will be $1056 \times 525 \times 30 \text{ nS} = 16.632 \text{ mS}$. This means the entire frame buffer will be written to the display in the 16.632 mS period. Inverting the time formula to frequency $f = \frac{1}{T} \text{ (Hz)}$, frames will be written to the display at a rate of 60.125 Hz. The MCU is required to write a full frame of data to the buffer within the 16.632 mS otherwise portions of the previous and current frame will be displayed.

5.2. Bandwidth Requirements

The bandwidth requirements of the MCU are simple to calculate. The formula is the horizontal resolution \times vertical resolution \times color bit depth \times frame rate = bit/second. The result of the E70GE1-RW820-N display is 554.112Mb/s ($800 \times 480 \times 24 \times 60.125$). The single-color pin data rate is less as the color bit depth becomes one, equating to 23.088 Mb/s. As shown, the MCU bandwidth requirements can be high when using the RGB interface.

6. Summary

In this application note, the E70GE1-RW820-N TFT LCD was presented along with how to connect it to an ST Nucleo-F767ZI MCU. Selecting an appropriate MCU was discussed and what parameters should be taken into consideration. Next, the actual hardware connections were listed. The final discussion revolved around the display timing and bandwidth requirements.

In Application Note FAN4220 firmware development will be presented. The ST Nucleo-F767ZI will be programmed utilizing the STM32CubeMX Initialization Code Generator and the STM32CubeIDE Integrated Development Environment. The code developed includes special peripherals features of the MCU.

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