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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

## Character LCD Module

Part Number

C82B-BW-LW63

### Overview:

- 8x2 Character LCD
- STN Blue Negative
- 58mm W x 32mm H
- 4/8-bit Parallel Interface
- White LED Backlight
- Transmissive
- Wide Temperature
- 3.3V Input Voltage
- Controller: ST7066
- RoHS Compliant

## Description

This is a STN (Super-Twisted Nematic) Blue Negative Character LCD (Liquid Crystal Display) that can display eight characters on two lines (8x2). This model is composed of a transmissive type LCD Panel, a built-in driver IC and a backlight unit.

## Character LCD Features

Character Format: 5x8 Dots with Cursor

Display Format: 8 Characters x 2 Lines

Interface: Parallel

Controller: ST7066U (or equivalent)

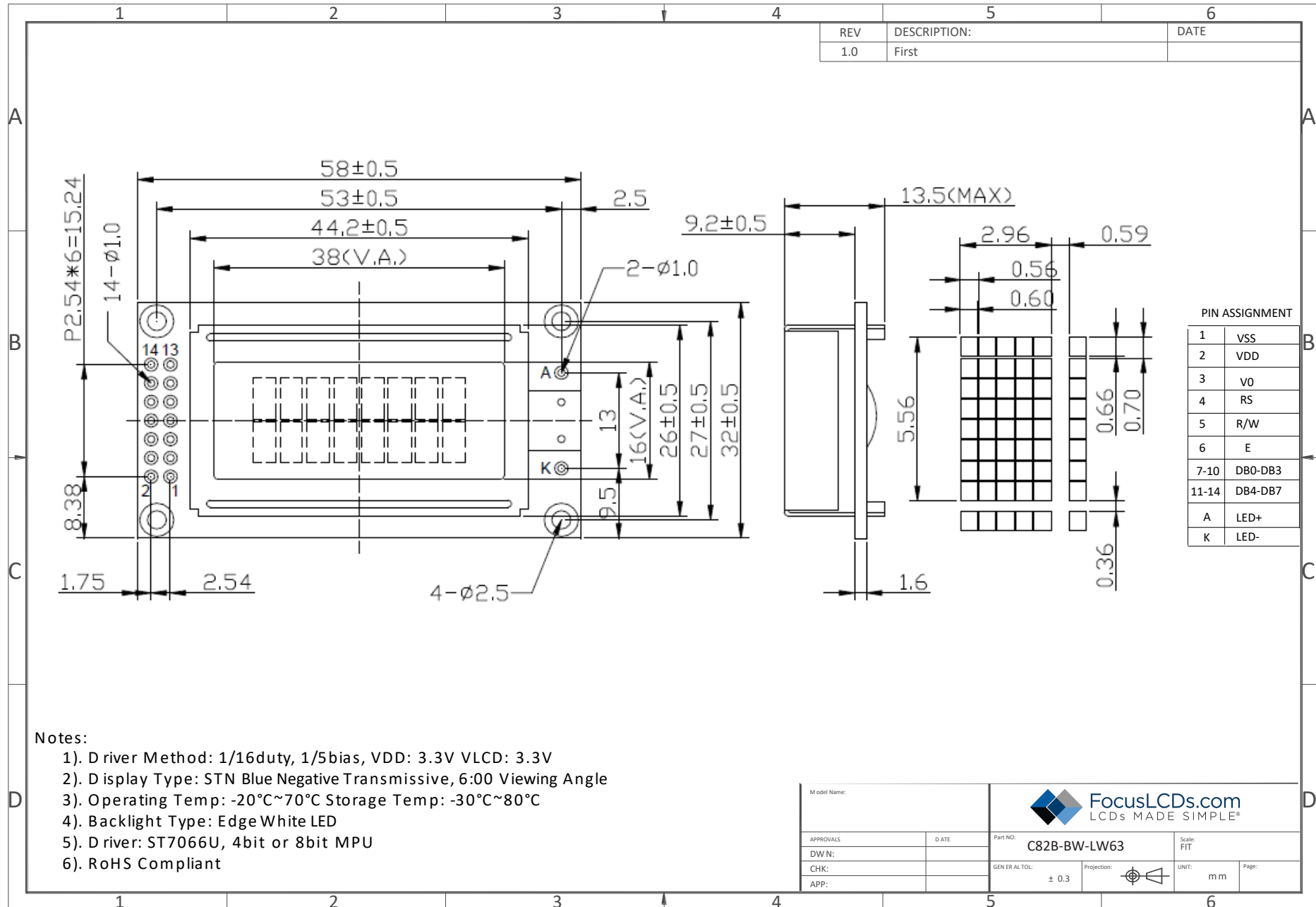
RoHS Compliant

| General Information | Specification | Note           |
|---------------------|---------------|----------------|
| LCD Type            | STN           |                |
| Viewing Direction   | 6 o'clock     |                |
| Rear Polarizer      | Transmissive  |                |
| Backlight Type      | LED Edge      | External Power |
| Backlight Color     | White         |                |
| Temperature Range   | Wide          |                |
| Touch Screen        | None          |                |
| Controller IC       | ST7066U       | Or equivalent  |
| Interface           | Parallel      | 4/8-bit        |

## Mechanical Information

| Item            | Specification                  |
|-----------------|--------------------------------|
| Module Size     | 58.0mm L x 32.0mm W x 13.5mm H |
| Viewing Area    | 38.0mm L x 16.0mm W            |
| Character Size  | 2.96mm L x 5.56mm W            |
| Character Pitch | 3.55mm L x 5.92mm W            |

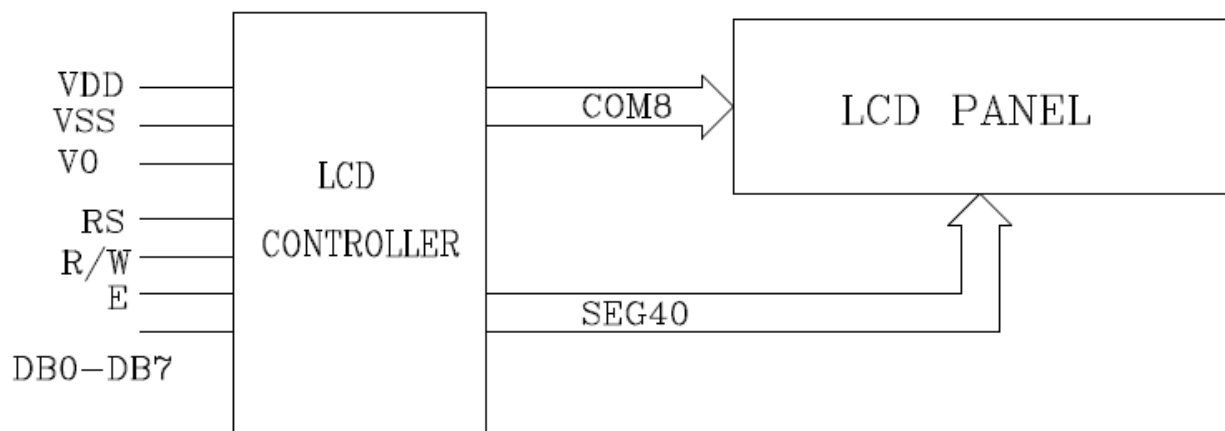
# 1. Outline Dimensions



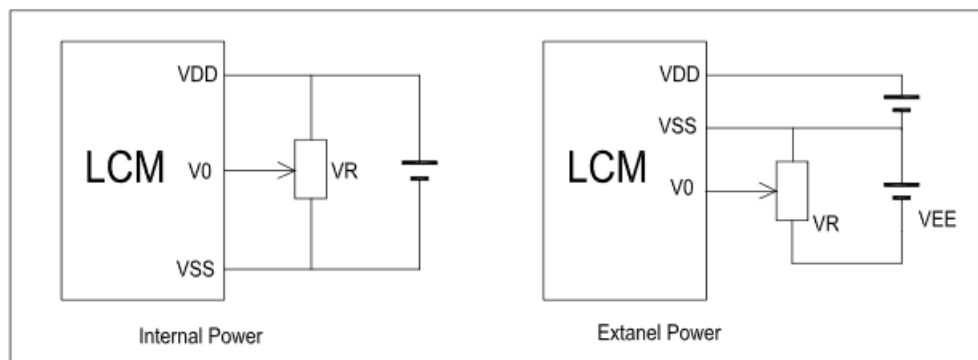
## 2. Input Terminal Pin Assignment

| NO.   | Symbol  | Description                                                                                                                                                    | Connection   |
|-------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| 1     | VSS     | Signal Ground for logic                                                                                                                                        | Power ground |
| 2     | VDD     | Power supply for logic                                                                                                                                         | Power supply |
| 3     | V0      | Contrast adjustment pin                                                                                                                                        | Power supply |
| 4     | RS      | Register select signal                                                                                                                                         | MPU          |
| 5     | R/W     | Read/Write signal                                                                                                                                              | MPU          |
| 6     | E       | Operation (data read/write) enable signal                                                                                                                      | MPU          |
| 7-10  | DB0-DB3 | Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU.                                                              | MPU          |
| 11-14 | DB4-DB7 | Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used in the 4-bit interface. | MPU          |
| 15    | LED+    | Power supply for Backlight                                                                                                                                     | Power supply |
| 16    | LED-    | Power supply for Backlight GND                                                                                                                                 | Power ground |

## 3. Block Diagram



## 4. Contrast Adjusting Circuit



VDD-V0: LCD Driving Voltage  
 VR: 10k-20k

## 5. LCD Optical Characteristics

| Item           | Symbol     | Condition | Min | Typ. | Max | Unit |
|----------------|------------|-----------|-----|------|-----|------|
| Viewing Angle  | $\theta 1$ | Cr>4      | -25 | --   | --  | deg  |
|                | $\Phi 1$   |           | -30 | --   | --  |      |
|                | $\theta 2$ | Cr>2      | -60 | --   | --  | deg  |
|                | $\Phi 2$   |           | -40 | --   | --  |      |
| Response Time  | Rise       | tr        | --  | 120  | 250 | ms   |
|                | Fall       |           | --  | 120  | 250 |      |
| Contrast Ratio | Cr         |           | 2   | 6    | --  | --   |

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

| Characteristics       | Symbol  | Min | Max | Unit |
|-----------------------|---------|-----|-----|------|
| Power Voltage         | VDD-Vss | 0   | 7.0 | V    |
| Input Voltage         | VIN     | VSS | VDD | V    |
| Operating Temperature | TOP     | -20 | +70 | °C   |
| Storage Temperature   | TST     | -30 | +80 | °C   |

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

### 6.2 DC Electrical Characteristics

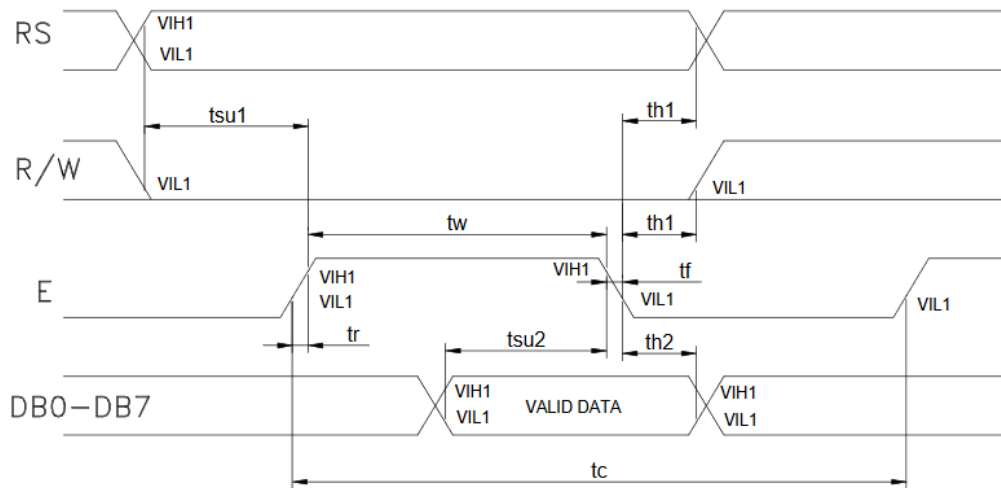
| Parameter                | Symbol | Min | Typ. | Max | Unit | Note                        |
|--------------------------|--------|-----|------|-----|------|-----------------------------|
| Supply Voltage for LCD   | VDD-V0 | 3.1 | 3.3  | 3.5 | V    | Ta=25°C                     |
| Input Voltage            | VDD    | 3.1 | 3.3  | 3.5 | V    |                             |
| Supply Current           | IDD    | 0.5 | 1.5  | 2.0 | mA   | Ta=25°C, VDD=3.3V           |
| Input Leakage Current    | ILKG   | --  | --   | 1.0 | uA   |                             |
| "H" Level Input Voltage  | VIH    | 2.2 | --   | VDD | V    |                             |
| "L" Level Input Voltage  | VIL    | 0   | --   | 0.6 | V    | Twice initial value or less |
| "H" Level Output Voltage | VOH    | 2.4 | --   | --  | V    | LOH=-0.25mA                 |
| "L" Level Output Voltage | VOL    | --  | --   | 0.4 | V    | LOH=1.6mA                   |
| Backlight Supply Voltage | VF     | 2.7 | 2.85 | 3.0 | V    |                             |
| Backlight Supply Current | ILED   | 10  | 15   | 20  | mA   |                             |

## 7. Timing Characteristics

### 7.1 Write Cycle ( $T_a=25^\circ\text{C}$ , $V_{DD}=3.3\text{V}$ )

| Parameter                 | Symbol | Min  | Typ. | Max | Unit | Test Pin |
|---------------------------|--------|------|------|-----|------|----------|
| Enable Cycle Time         | tc     | 1000 | -    | -   | ns   | E        |
| Enable Pulse Width        | tw     | 450  | -    | -   | ns   |          |
| Enable Rise/Fall Time     | tr, tf | --   | -    | 25  | ns   |          |
| RS, R/W Setup Time        | tsu1   | 60   | -    | -   | ns   | RS, R/W  |
| RS, R/W Address Hold Time | th1    | 20   | -    | -   | ns   |          |
| Read Data Output Delay    | tsu2   | 195  | -    | -   | ns   | DB0-DB7  |
| Read Data Hold Time       | th2    | 10   | -    | -   | ns   |          |

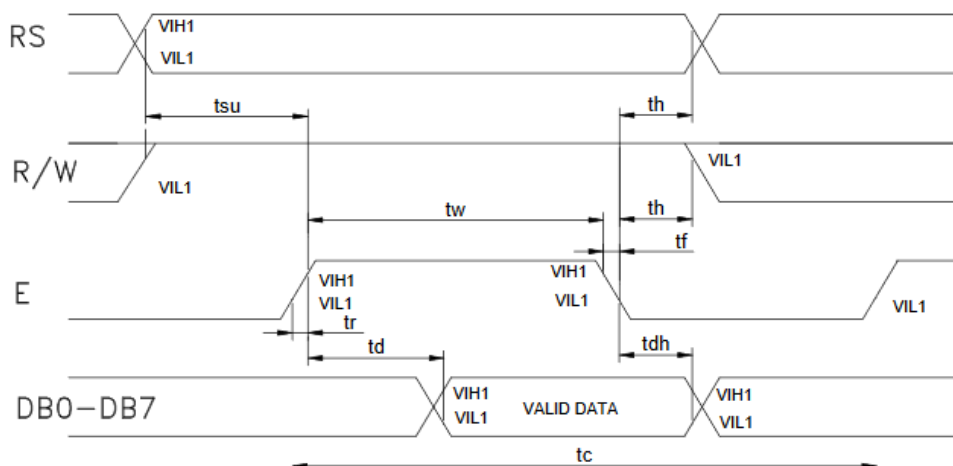
#### Write Mode Timing Diagram



### 7.2 Read Cycle ( $T_a=25^\circ\text{C}$ , $V_{DD}=3.3\text{V}$ )

| Parameter                 | Symbol | Min  | Typ. | Max | Unit | Test Pin |
|---------------------------|--------|------|------|-----|------|----------|
| Enable Cycle Time         | tc     | 1000 | -    | -   | ns   | E        |
| Enable Pulse Width        | tw     | 450  | -    | -   | ns   |          |
| Enable Rise/Fall Time     | tr, tf | --   | -    | 25  | ns   |          |
| RS, R/W Setup Time        | tsu    | 60   | -    | -   | ns   | RS, R/W  |
| RS, R/W Address Hold Time | th     | 20   | -    | -   | ns   |          |
| Read Data Output Delay    | td     | --   | -    | 360 | ns   | DB0-DB7  |
| Read Data Hold Time       | tdh    | 5    | -    | -   | ns   |          |

#### Read Mode Timing Diagram



## 8. Instructions

To overcome the speed difference between the internal clock of ST7066 (or equivalent) and the MPU clock, ST7066 performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instructions can be divided largely into four groups:

- 1) ST7066 function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read "High". Busy flag check must be preceded by the next instruction.

### 8.1 Instruction Table

| Instruction                | Instruction Code |     |     |     |     |     |     |     |     |     | Description                                                                                                              | Exc. Time<br>(fosc = 270kHz) |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--------------------------------------------------------------------------------------------------------------------------|------------------------------|
|                            | RS               | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |                                                                                                                          |                              |
| Clear Display              | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | Write "20H" to DDRAM and set DDRAM address to "00H" from AC                                                              | 1.53ms                       |
| Return Home                | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | -   | Set DDRAM address to "00H" from AC and return cursor to original position if shifted. Contents of DDRAM are not changed. | 1.53ms                       |
| Entry Mode Set             | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | SH  | Assign cursor moving direction and blinking of display                                                                   | 39us                         |
| Display On/Off             | 0                | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   | Set display (D), cursor (C), and blinking of cursor (B) on/off control bit                                               | -                            |
| Cursor or Display Shift    | 0                | 0   | 0   | 0   | 0   | 1   | S/C | R/L | -   | -   | Set cursor moving, shift control bit and direction. Does not change DDRAM data                                           | 39us                         |
| Function Set               | 0                | 0   | 0   | 0   | 1   | DL  | N   | F   | -   | -   | Set interface data length (DL: 8/4-bit), Numbers of display Line (N: 2/1 line) and font type (F:5x11/5x8)                | 39us                         |
| Set CGRAM Address          | 0                | 0   | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter                                                                                     | 39us                         |
| Set DDRAM Address          | 0                | 0   | 1   | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter                                                                                     | 39us                         |
| Read Busy Flag and Address | 0                | 1   | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Read busy flag and address. Can be done during internal operation by reading BF                                          | 0us                          |
| Write Data to Address      | 1                | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Write data into internal RAM (DDRAM/CGRAM)                                                                               | 43us                         |
| Read Data from RAM         | 1                | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Read data from internal RAM (DDRAM/CGRAM)                                                                                | 43us                         |

NOTE: When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

## 8.2 Contents

### 8.2.1 Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

Clear all the display data by writing "20H" (space code) to all DDRAM address and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D="High").

### 8.2.2 Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | -   |

Return home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change

### 8.2.3 Entry Mode Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | I/D | SH  |

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D="high", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D="Low", cursor/blink moves to left and DDRAM address is increased by 1.

CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH="Low", shifting of entire display is not performed. If SH="High" and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D="high". shift left, I/D="Low". Shift right)

### 8.2.4 Display ON/OFF Control

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   |

Control display/cursor/blink ON/OFF 1-bit register.

**D: Display ON/OFF control bit**

When D="High", entire display is turned on.

When D="Low", display is turned off, but display data remains in DDRAM.

**C: cursor ON/OFF control bit**

When D="High", cursor is turned on.

When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

**B: Cursor blink ON/OFF control bit**

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.

When B="Low", blink is off.

### 8.2.5 Cursor or Display Shift

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | S/C | R/L | -   | -   |

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When display data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not change

#### Shift patterns according to S/C and R/L bits

| S/C | R/L | Operation                                                                 |
|-----|-----|---------------------------------------------------------------------------|
| 0   | 0   | Shift cursor to the left. AC is decreased by 1                            |
| 0   | 1   | Shift cursor to the right. AC is increased by 1                           |
| 1   | 0   | Shift all the display to the left. Cursor moves according to the display  |
| 1   | 1   | Shift all the display to the right. Cursor moves according to the display |

### 8.2.6 Function Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | F   | -   | -   |

**DL: Interface data length control bit**

When DL="High", it means 8-bit bus mode with MPU.

When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

**N: Display line number control bit**

When N="Low", 1-line display mode is set.

When N="High", 2-line display mode is set.

**F: Display line number control bit**

When F="Low", 5x8 dots format display mode is set.

When F="High", 5x11 dots format display mode.

### 8.2.7 Set CGRAM address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

### 8.2.8 Set DDRAM address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=LOW), DDRAM address is form "00H" to "4FH". In 2-line display mode (N=High), DDRAM address in the 1st line form "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

### 8.2.9 Read Busy Flag & Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 1   | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether ST7066 is in internal operation or not. If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

### 8.2.10 Write data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

### 8.2.11 Read data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register. After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

*NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation. At this time, AC indicates next address position, but only the previous data can be read by the read instruction.*

## 9. Cautions and Handling

### General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isopropyl alcohol, ethyl alcohol or trichlorotrifluoroethane. Do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting.
5. When mounting the LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

### Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore, operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

### Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature:  $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

### Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage  $V_o$ .
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over  $40^{\circ}\text{C}$  is required, the relative humidity should be kept below 60%, and avoid