AiP31108U
64CH Segment Driver for Dot Matrix LCD

Product Specification

Specification Revision History ：

Version	Data	Description
2010-01-A	2010-01	Replace the new template
2012-01-B1	2012-01	Increase in the number and history

1、GENERAL DESCRIPTION

The AiP31108U is a LCD driver LSl with 64channel output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64bit data latch, 64 bit drivers and decoder logics.

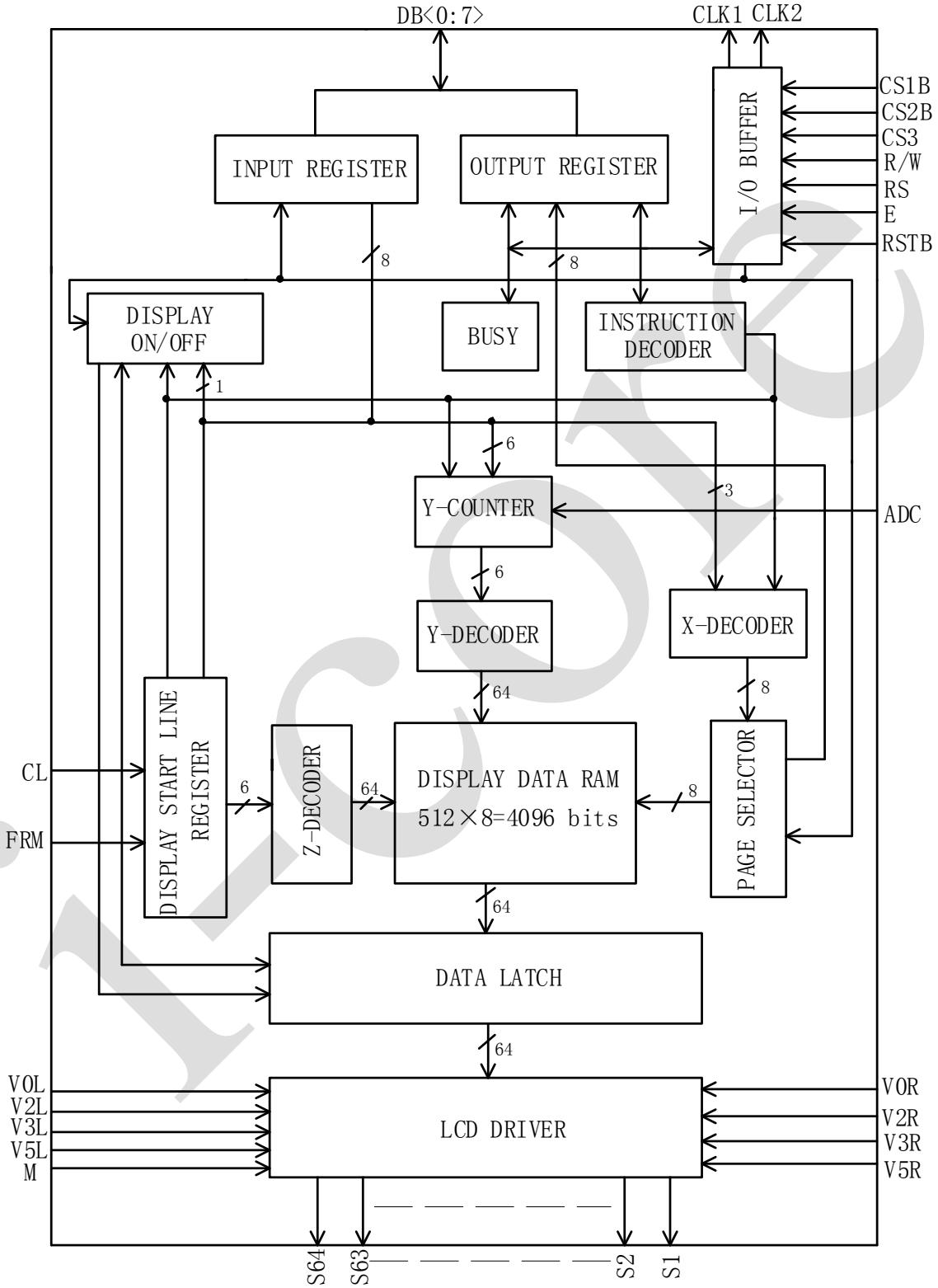
It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The AiP31108U composed of the liquid crystal display system in combination with the AiP31107 (64 channel common driver).

Features

- Dot matrix LCD segment driver with 64 channel output
- Input and Output signal
  - Input: 8 bit parallel display data
    Control signal from MPU
    Divided bias voltage (V0R, V0L, V2R, V2L,V3R,V3L, V5R,V5L)
  - Output: 64 channel for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - Capacity: 512 bytes (4096 bits)
  - RAM bit data: RAM bit data = 1: ON
    RAM bit data = 0: OFF
- Applicable LCD duty: 1/32 ~1/64
- LCD driving voltage: 8V ~17V(VDD-VEE)
- Power supply voltage: 2.7V ~5.5V
- High voltage CMOS process.
- chip size: 2960×2965 (um×um),
- The IC substrate should be connected to VDD or float in the PCB layout artwork.
- 100QFP and bare chip available

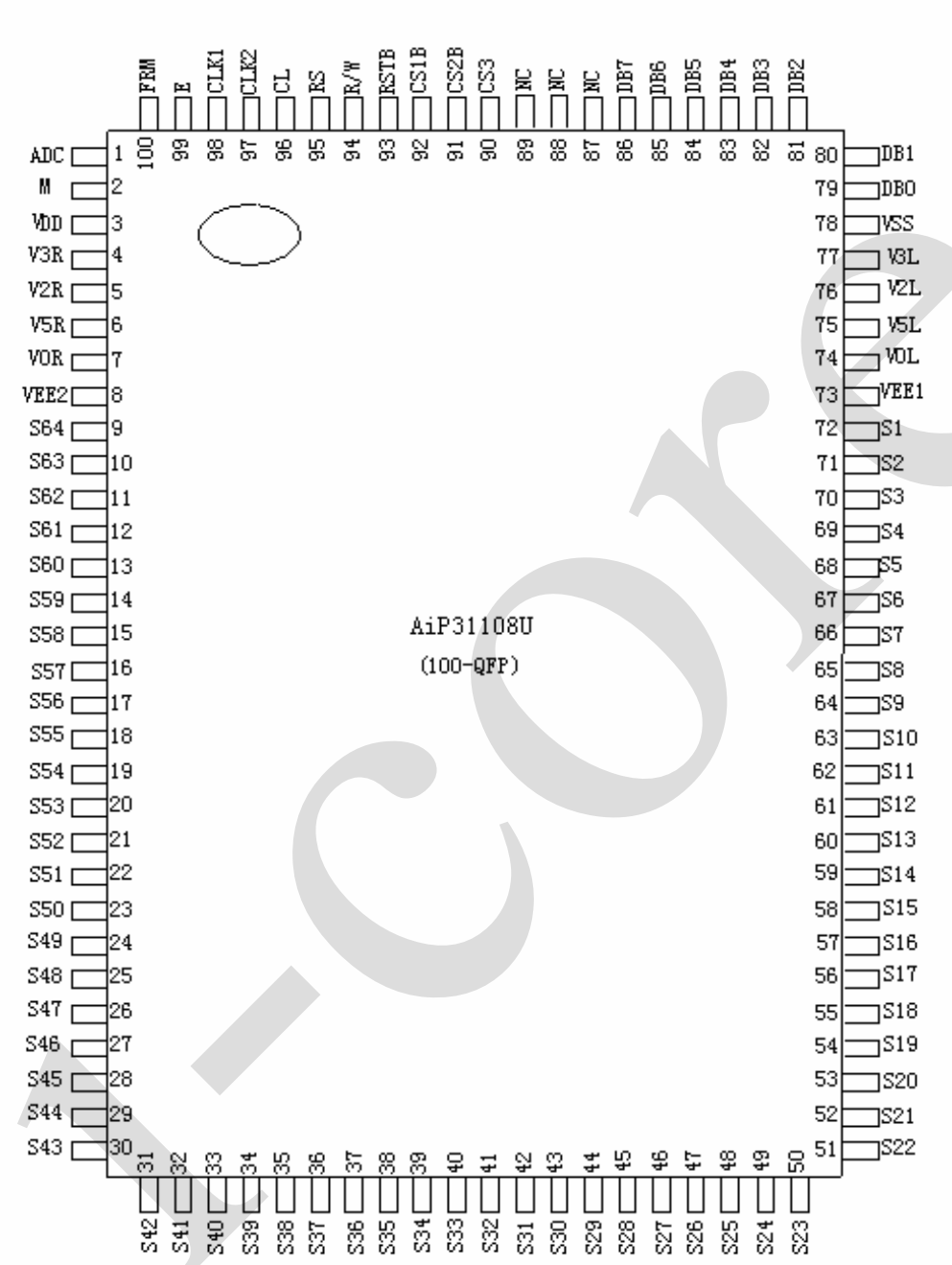
2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM



2.2、PIN CONFIGURATIONS

QFP-100



2.3、PIN DESCRIPTION

<table>
<tr><th>PIN NO.(QFP)</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>3
78
73,8</td><td>VDD
VSS
VEE1，2</td><td>Power</td><td>For internal logic circuit（+5V±10%）
GND(0V)
For LCD driver circuit
VSS=0V,VDD=+5V±10%,VDD-VEE=8V～17V
VEE1 and VEE2 is connected by the same voltage.</td></tr>
<tr><td>74,7
76,5
77,4
75,6</td><td>V0L,V0R
V2L,V2R
V3L,V3R
V5L,V5R</td><td>Power</td><td>Bias supply voltage terminals to drive the LCD.
<table><tr><td>Select Level</td><td>Non-Select Level</td></tr><tr><td>V0L(R),V5L(R)</td><td>V2L(R),V3L(R)</td></tr></table>V0L and V0R(V2L&V2R,V3L&V3R,V5L&V5R) should be connected by the same voltage.</td></tr>
<tr><td>92
91
90</td><td>CS1B
CS2B
CS3</td><td>I</td><td>Chip selection
In order to interface data for input or output, the terminals have to be CS1B=L,CS2B=L,CS3=H</td></tr>
<tr><td>2</td><td>M</td><td>I</td><td>Alternating signal input for LCD driving.</td></tr>
<tr><td>1</td><td>ADC</td><td>I</td><td>Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output.
ADC=H→Y0:S1-Y63: S64
ADC=L→Y0:S64-Y63: S1</td></tr>
<tr><td>100</td><td>FRM</td><td>I</td><td>Synchronous control signal.
Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.</td></tr>
<tr><td>99</td><td>E</td><td>I</td><td>Enable signal.
write mode (R/W=L) →data of DB<0:7> is latched at the falling edge of E.
read mode (R/W=H) →DB<0:7> appears the reading data while E is at high level.</td></tr>
<tr><td>98
97</td><td>CLK1
CLK2</td><td>I</td><td>2 phase clock signal for internal operation.
Used to execute operations for input/output of display RAM data and others.</td></tr>
<tr><td>96</td><td>CL</td><td>I</td><td>Display synchronous signal.
Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.</td></tr>
<tr><td>95</td><td>RS</td><td>I</td><td>Data or Instruction.
RS=H→DB<0:7>: Display RAM Data
RS=L→DB<0:7>: Instruction Data</td></tr>
<tr><td>94</td><td>R/W</td><td>I</td><td>Read or Write.
R/W=H → Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B=L and CS3=H.
R/W=L→Display data DB<0:7> can be written at falling of E</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>when CS1B=L, CS2B=L and CS3=H.</td></tr>
<tr><td>79-86</td><td>DB0-DB7</td><td>I/0</td><td>Data bus. There state I/O common terminal.</td></tr>
<tr><td>72-9</td><td>S1-S64</td><td>0</td><td>LCD Segment driver output.
Display RAM data 1:ON
Display RAM data 0:OFF
(Relation of display RAM data & M)
<table>
<tr><th>M</th><th>Data</th><th>Output Level</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V_2</td></tr>
<tr><td>H</td><td>V_0</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V_3</td></tr>
<tr><td>H</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>93</td><td>RSTB</td><td>I</td><td>Reset signal.
When RSTB=L,
1) ON/OFF register becomes set by 0. (display off)
2) Display start line register becomes set by 0
(Z-address 0 set, display from line 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>87
88
89</td><td>NC</td><td></td><td>connection.(open)</td></tr>
</table>

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to VSS, unless otherwise specified)

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	VDD	-0.3～+7.0	V	（1）
Supply Voltage	VEE	VDD-19.0～VDD+0.3	V	（4）
Driver Supply Voltage	V_B	-0.3～VDD+0.3	V	（1），（3）
	V_{LCD}	VEE-0.3～VDD+0.3	V	（2）
Operating Temperature	T_{OPR}	-30～+85	℃	
Storage Temperature	T_{STG}	-55～+125	℃	
Soldering Temperature	T_L	245(10s)	℃	

*1. Based on V_{SS}=0V.

*2. Applies the same supply voltage to V_{EE1} and V_{EE2}. $V_{LCD}=V_{DD}-V_{EE}$.

*3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.

*4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).

Voltage level: VDD ≥ V0L= V0R ≥ V2L= V2R ≥ V3L= V3R ≥ V5L= V5R ≥ VEE.

3.2、ELECTRICAL CHARACTERISTICS

3.2.1 DC Characteristics（VDD=+5V±10%,VSS=0V,|VDD-VEE|=8～17V,Ta=-30～+85℃,）

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input High Voltage	V_{IH1}	—	0.7VDD	—	VDD	V	(1)
	V_{IH2}	—	2.0	—	VDD	V	(2)
Input Low Voltage	V_{IL1}	—	0	—	0.3VDD	V	(1)
	V_{IL2}	—	0	—	0.8	V	(2)
Output High Voltage	V_{OH}	I_{OH}=-200uA	2.4	—	—	V	(3)
Output Low Voltage	V_{OL}	I_{OL}=1.6mA	—	—	0.4	V	(3)
Input Leakage Current	I_{LKG}	V_{IN}=VSS-VDD	-1.0	—	1.0	uA	(4)
Three-state(OFF) Input Current	I_{TSL}	V_{IN}=VSS-VDD	-5.0	—	5.0	uA	(5)
Driver Input Leakage Current	I_{DIL}	V_{IN}=VEE-VDD	-2.0	—	2.0	uA	(6)
Operating Current	I_{DD1}	During Display	—	—	150	uA	(7)
	I_{DD2}	During Access Access Cycle=1MHz	—	—	600	uA	(7)
On Resistance	R_{ON}	VDD-VEE=15V ILOAD=±0.1mA	—	—	7.5	KΩ	(8)

*1. CL, FRM, M, RSTB, CLK1, CLK2
*2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
*3. DB0~DB7
*4. Except DB0~DB7
*5. DB0~DB7 at High Impedance
*6. V0L(R), V2L(R), V3L(R), V5L(R)
*7. 1/64 duty, FCLK=250KHZ, Frame Frequency=70HZ, Output: No Load
*8. VDD~VEE=15.5V V0L(R)>V2L(R)=VDD-2/7 (V_{DD}-V_{EE})>V3L(R)=V_{EE}+2/7(VDD-VEE)>V5L(R)

3.2.2 AC Characteristics（V_{DD}=+5V±10%,VSS=0V,Ta=-30～+85℃）

Clock Timing

Characteristic	Symbol	Min	Typ	Max	Unit
CLK1, CLK2 Cycle Time	t_{CY}	2.5	—	20	us
CLK1 LOW Level Width	t_{WL1}	625	—	—	ns
CLK2 LOW Level Width	t_{WL2}	625	—	—	
CLK1 HIGH Level Width	t_{WH1}	1875	—	—	
CLK2 HIGH Level Width	t_{WH2}	1875	—	—	
CLK1-CLK2 Phase Difference	t_{D12}	625	—	—	
CLK2-CLK1 Phase Difference	t_{D21}	625	—	—	
CLK1,CLK2 Rise Time	t_R	—	—	150	
CLK1,CLK2 Fall Time	t_F	—	—	150	

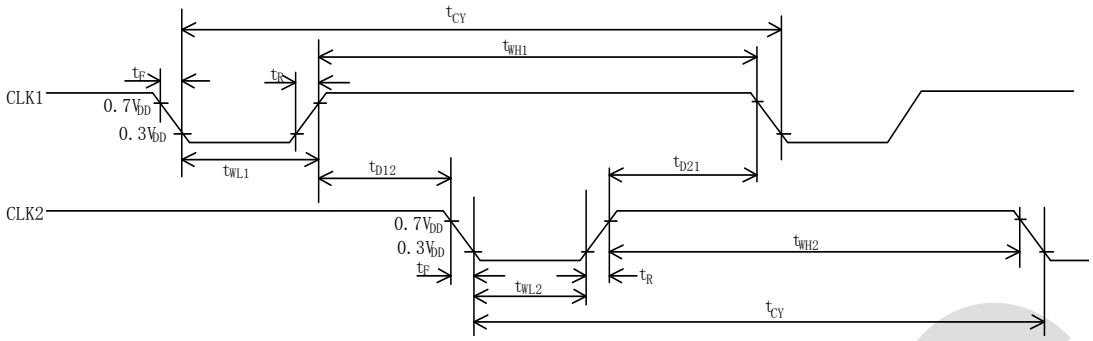


Fig1.External clock waveform

Display Control Timing

Characteristic	Symbol	Min	Typ	Max	Unit
FRM Delay Time	tDF	-2	—	+2	us
M Delay Time	tDM	-2	—	+2	us
CL LOW Level Width	tWL	35	—	—	us
CL HIGH Level Width	tWH	35	—	—	us

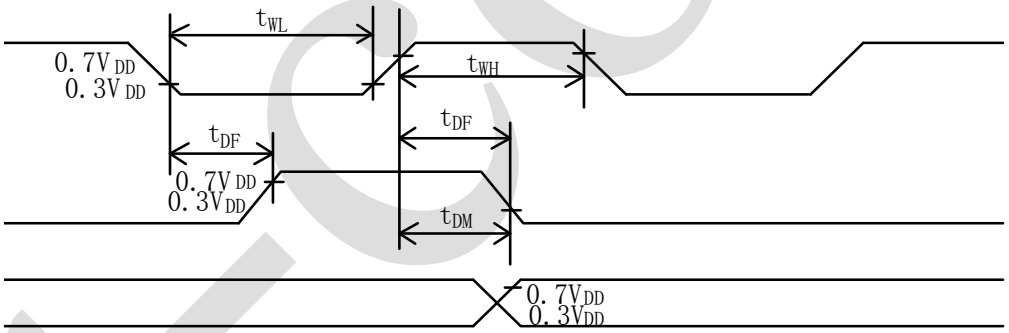


Fig2. Display control signal waveform

MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	tC	1000	—	—	ns
E High Level Width	tWH	450	—	—	ns
E Low Level Width	tWL	450	—	—	ns
E Rise Time	tR	—	—	25	ns
E Fall Time	tF	—	—	25	ns
Address Set-Up Time	tASU	140	—	—	ns
Address Hold Time	tAH	10	—	—	ns
Data Set-Up Time	tDSU	200	—	—	ns
Data Delay Time	tD	—	—	320	ns
Data Hold Time (Write)	tDHW	10	—	—	ns
Data Hold Time (Read)	tDHR	20	—	—	ns

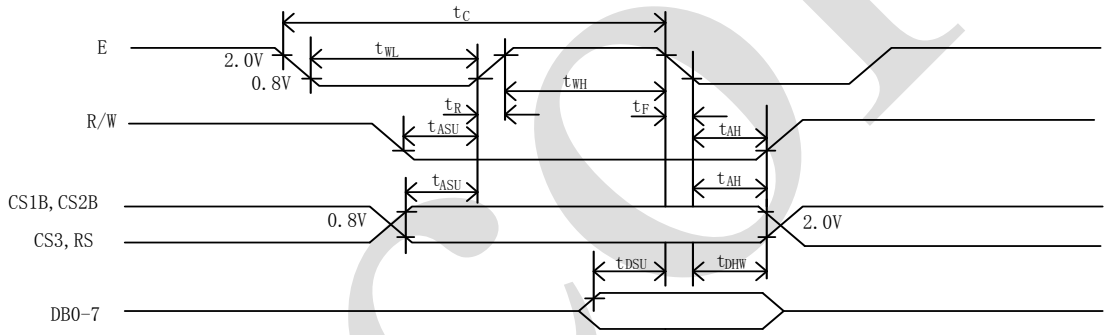


Fig 3. MPU write timing

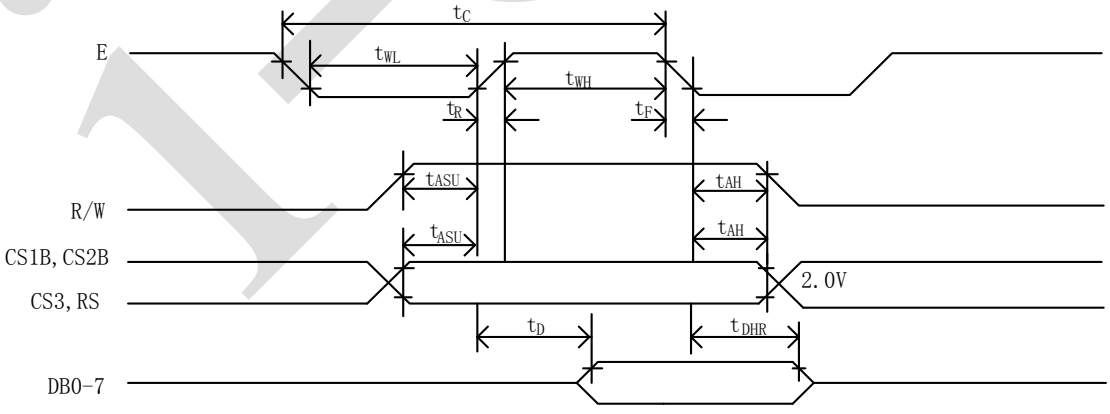
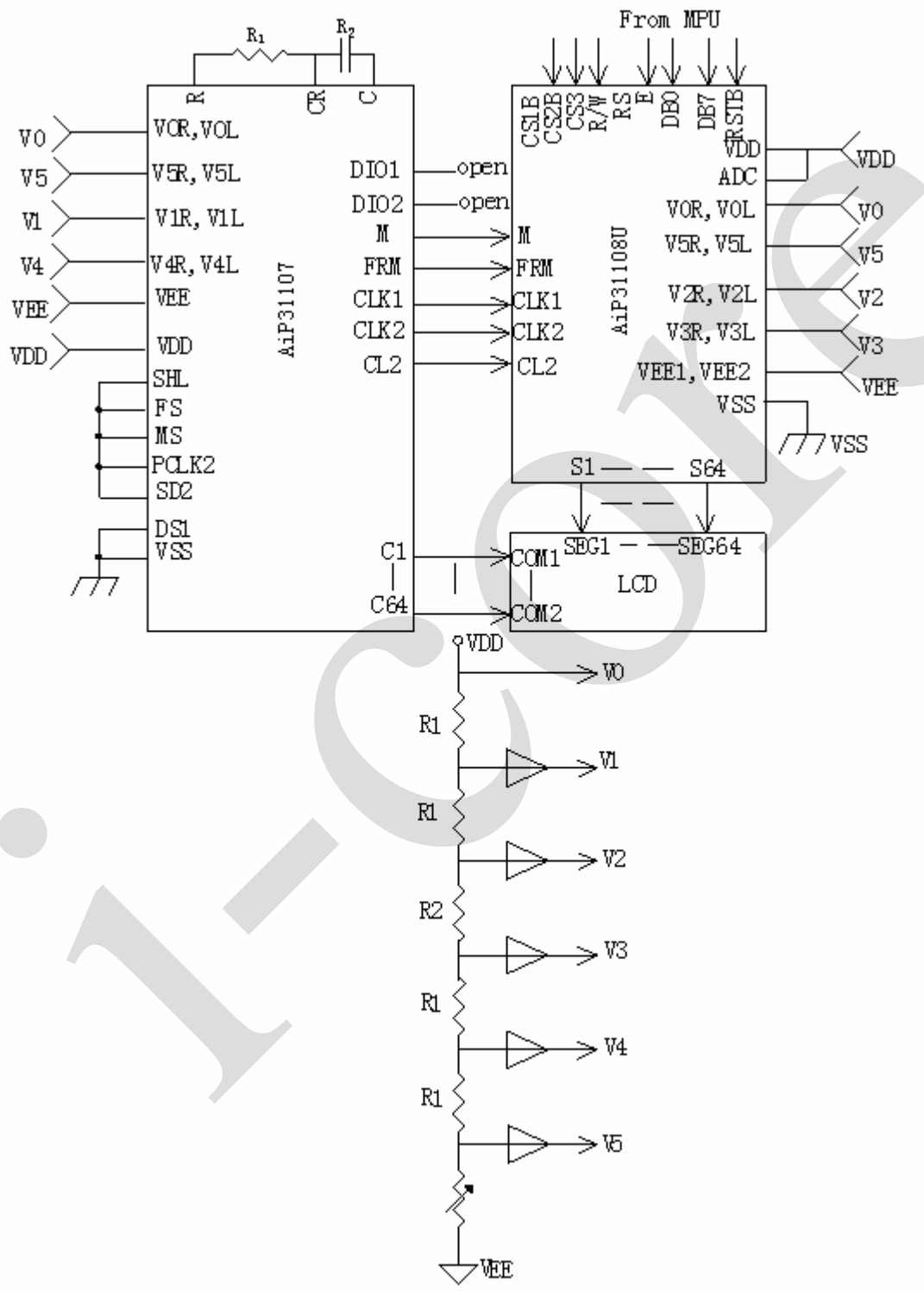


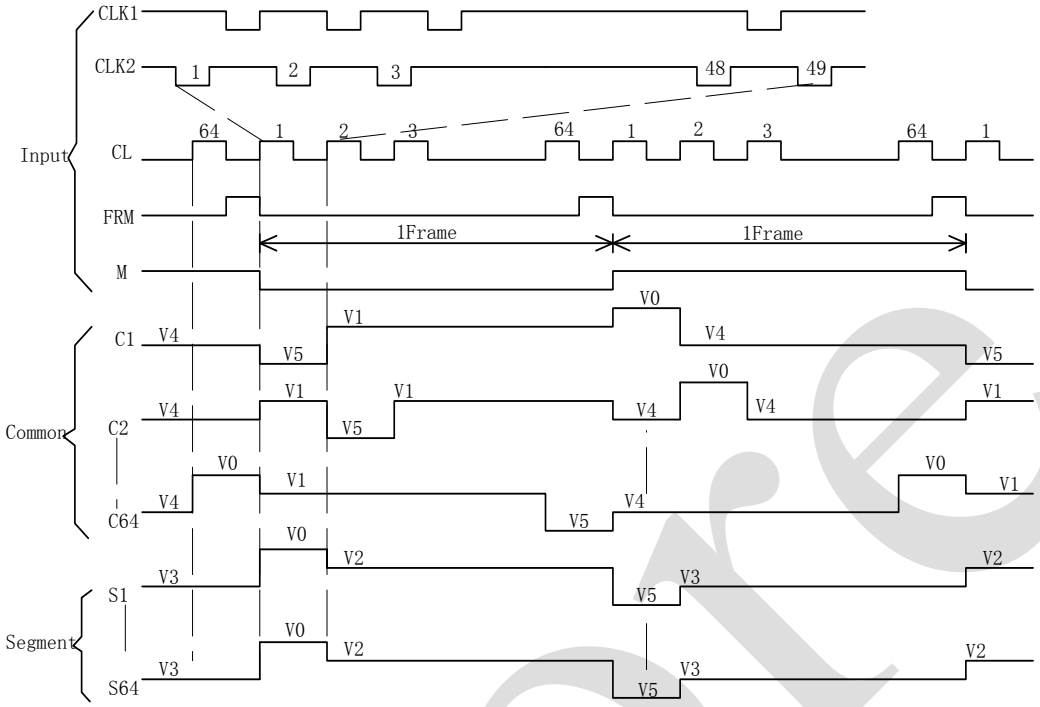
Fig 4. MPU Read timing

4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT

1/64 duty common driver(AiP31107) interface circuit





4. 2、APPLICATION NOTE

OPERATING PRINCIPLES & METHODS

I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But

status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

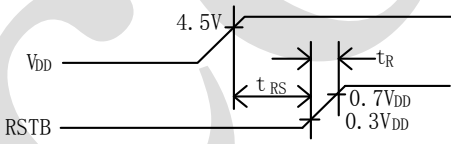
When RSTB becomes low, following procedure is occurred.

1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction.

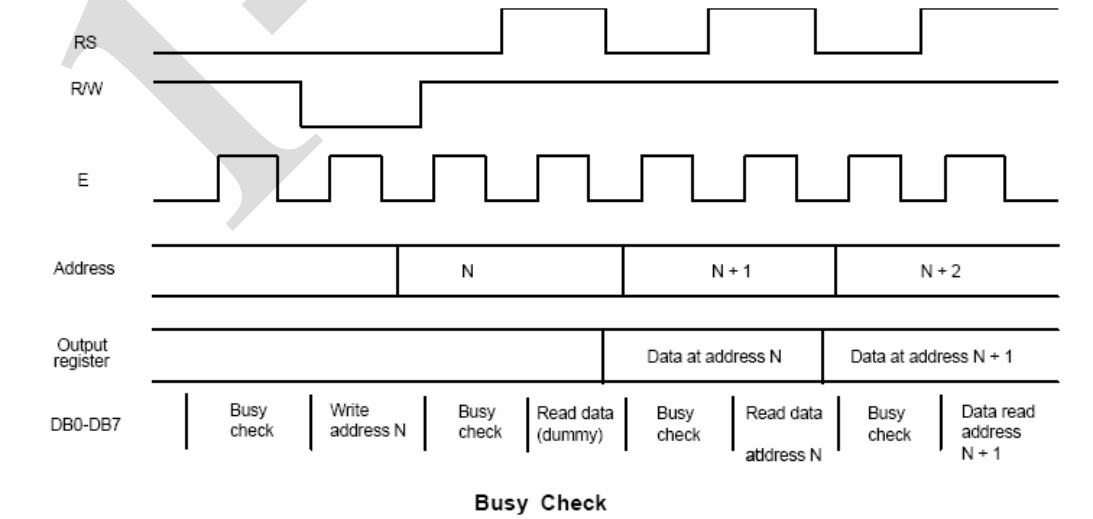
Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	—	—	us
Rise Time	t_R	—	—	200	ns

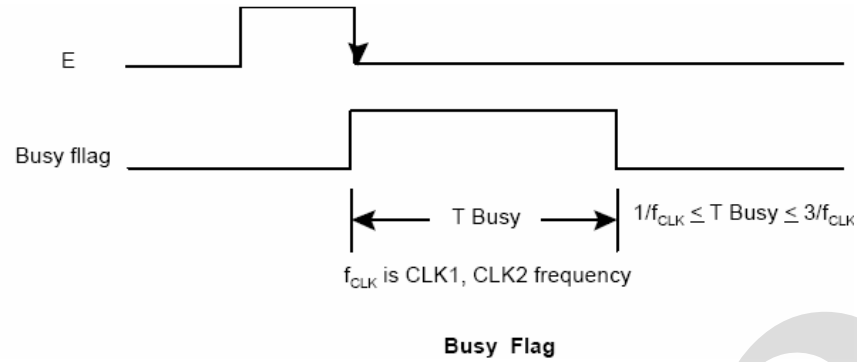


Busy flag

Busy flag indicates that AiP31108U is operating or no operating. When busy flag is high, AiP31108U is in internal operating. When busy flag is low, AiP31108U can accept the data or instruction. DB7 indicates busy flag of the AiP31108U.



Busy Check



Busy Flag

Display On/Off Flip - Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM.

Count function is not available. An address is set by instruction.

Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H → Y- address 0:S1 -Y address 63:64

ADC=L → Y- address 0:S64 -Y address 63:S1

ADC terminal connect the V_{DD} or V_{SS}.

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.

Display Control Instruction

The display control instructions control the internal state of the AiP31108U. Instruction is received from MPU to AiP31108U for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set Address (Y address)	L	L	L	H	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	L	L	H	L	H	H	H	Page（0-7）			Sets the X address at the X address register.
Display Start Line (Z address)	L	L	H	H	Display start line（0-63）						Indicates the display data RAM displayed at the top of the screen.
Status Read	L	H	busy	L	On/off	reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write Display Data	H	L	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.

Though the data is not on the screen with D=0, it remains in the display data RAM.

Therefore, you can make it appear by changing D=0 into D=1.

Set Address (Y Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0 ~ AC5) of the display data RAM is set in the Y address counter.

An address is set by instruction and increased by 1 automatically by read or write operations

of display data.

Set Page (X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address(AC0 ~ AC2) of the display data RAM is set in the X address register.

Writing or reading to or from MPU is executed in this specified page until the next page is set.

Display Start Line (Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0 ~ AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others(1/32 ~ 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY

  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.

  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF

  When ON/OFF is 1, the display is off.

  When ON/OFF is 0, the display is on.
- RESET

  When RESET is 1, the system is being initialized. In this condition, no instructions except status read can be accepted.

  When RESET is 0, initializing has finished and the system is in the usual operation condition.

Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0 ~ D7) into the display data RAM.After writing instruction, Y address is increased by 1 automatically.

Read Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0 ~ D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

4.3 SOFT EXAMPLE

The 128×64 dot matrix LCD module is formed by one AiP31107 and two AIP31108s.AT89C52 will drive the module by indirect controlling method. When CS1B=L，CS2B=L，CS3=H, the AIP31108 is working. Binding the AIP31108, CS1B and CS2B will be connected GND directly, but the CS3B must be connected the module select terminal. The CS3 of two AIP31108s will be defined as CS1 and CS2。

```
RS        EQU     P1.1
RW        EQU     P1.2
E         EQU     P1.0
CS1       EQU     P1.3
CS2       EQU     P1.4
RST       EQU     P1.5
DB0~7     EQU     P0
COM       EQU     5EH          ; Instruction data RAM
DAT       EQU     5FH          ; display data RAM
```

（1）、Read Busy flag subprogram

```
BUSYT:  CLR     RS
        SETB    RW
BUSYT1: MOV     A, #0FFH
        MOV     P0, A
        SETB    E
        NOP
        NOP
        MOV     A, P0
        JB      ACC.7, BUSYT1
        CLR E
        RET
```

（2）、Write instruction subprogram

```
COMW:   SETB    CS1     ; According to the AIP31108, setting CS1 and CS2
        LCALL   BUSYT
        LCALL   COMW1
        CLR     CS1     ; According to the AIP31108, setting CS1 and CS2
        RET
COMW1:  CLR     RW
        CLR     RS
        NOP
        NOP
```

```
        MOV     P0, COM
        SETB    E
        NOP
        NOP
        CLR     E
        RET
```

（3）、Write data subprogram

```
DATW:   SETB    CS1         ; According to the AIP31108, setting CS1 and CS2
        LCALL   BUSYT
        LCALL   DATW1
        CLR     CS1         ; According to the AIP31108, setting CS1 and CS2
        RET
DATW1:  CLR     RW
        SETB    RS
        NOP
        NOP
        MOV     P0, DAT
        SETB    E
        NOP
        NOP
        CLR     E
        RET
```

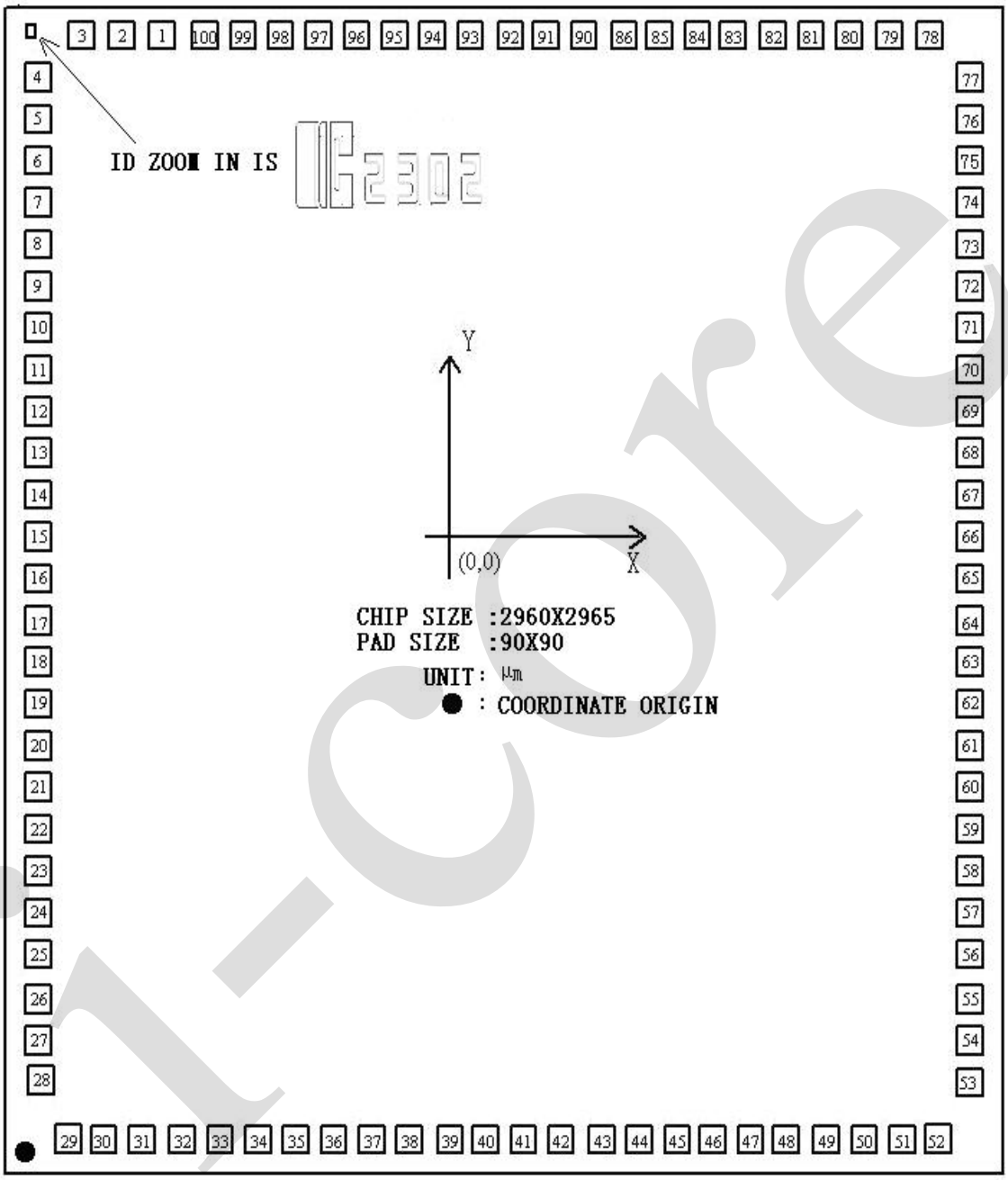
（4）、Read data subprogram

```
DATR:   SETB    CS1         ; According to the AIP31108, setting CS1 and CS2
        LCALL   BUSYT
        LCALL   DATR1
        CLR     CS1         ; According to the AIP31108, setting CS1 and CS2
        RET
DATR1:  MOV     COM, #0B8H      ; According to the reading location, setting
                                ;the page address
        LCALL   COMW
        MOV     COM, #40H       ; According to the reading location, setting
                                ;the column address
        LCALL   COMW
        SETB    CS1             ; According to the AIP31108, setting
CS1 and CS2
```

```
                LCALL   BUSYT
                SETB    RW
                SETB    RS
                SETB    E
                NOP
                NOP
                MOV     A, P0
                CLR     E
                CLR     CS1             ; According to the AIP31108, setting
CS1 and CS2
```

5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM



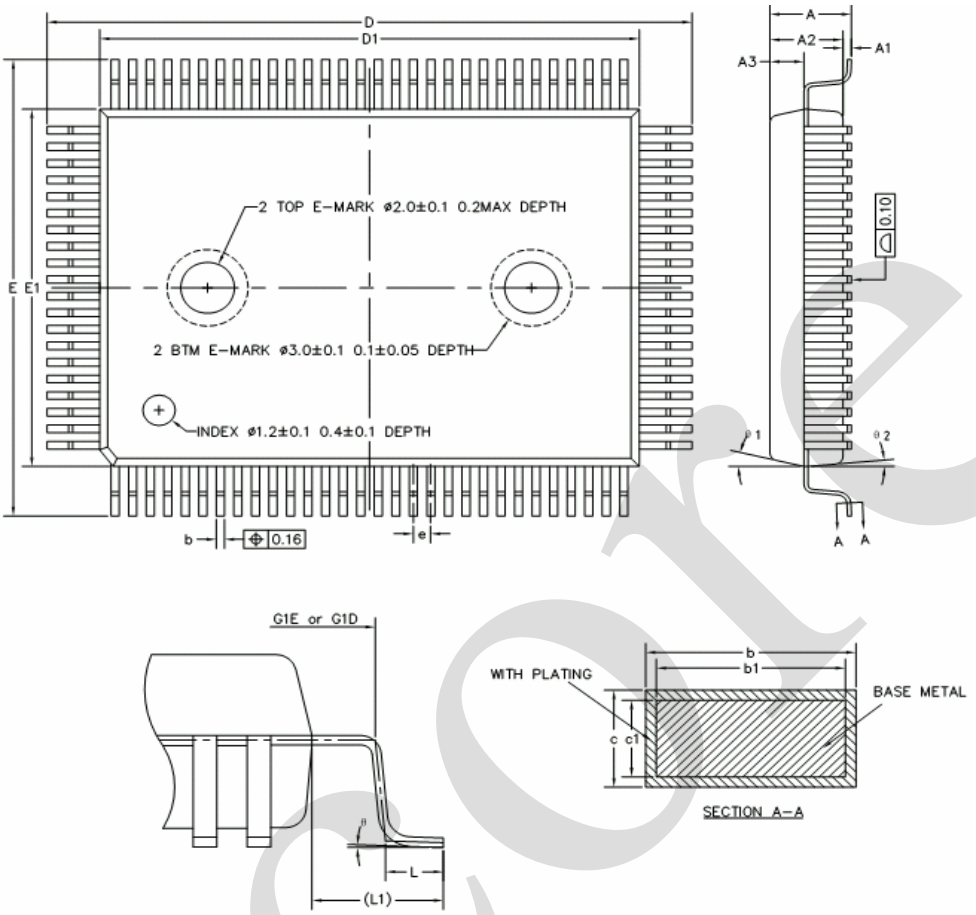
5.2、PAD Location （UNIT:μm）

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
1	ADC	445	2900	51	S22	2635	62.5
2	M	330	2900	52	S21	2760	62.5
3	VDD	215	2900	53	S20	2897.5	162.5
4	V3	62.5	2802.5	54	S19	2897.5	272.5
5	V2	62.5	2692.5	55	S18	2897.5	382.5
6	V5	62.5	2582.5	56	S17	2897.5	492.5
7	V0	62.5	2472.5	57	S16	2897.5	602.5
8	VEE	62.5	2362.5	58	S15	2897.5	712.5
9	S64	62.5	2252.5	59	S14	2897.5	822.5
10	S63	62.5	2142.5	60	S13	2897.5	932.5
11	S62	62.5	2032.5	61	S12	2897.5	1042.5
12	S61	62.5	1922.5	62	S11	2897.5	1152.5
13	S60	62.5	1812.5	63	S10	2897.5	1262.5
14	S59	62.5	1702.5	64	S9	2897.5	1372.5
15	S58	62.5	1592.5	65	S8	2897.5	1482.5
16	S57	62.5	1482.5	66	S7	2897.5	1592.5
17	S56	62.5	1372.5	67	S6	2897.5	1702.5
18	S55	62.5	1262.5	68	S5	2897.5	1812.5
19	S54	62.5	1152.5	69	S4	2897.5	1922.5
20	S53	62.5	1042.5	70	S3	2897.5	2032.5
21	S52	62.5	932.5	71	S2	2897.5	2142.5
22	S51	62.5	822.5	72	S1	2897.5	2252.5
23	S50	62.5	712.5	73	VEE	2897.5	2362.5
24	S49	62.5	602.5	74	V0	2897.5	2472.5
25	S48	62.5	492.5	75	V5	2897.5	2582.5
26	S47	62.5	382.5	76	V2	2897.5	2692.5
27	S46	62.5	272.5	77	V3	2897.5	2802.5
28	S45	62.5	162.5	78	GND	2745	2900
29	S44	200	62.5	79	DB0	2630	2900
30	S43	325	62.5	80	DB1	2515	2900
31	S42	435	62.5	81	DB2	2400	2900

32	S41	545	62.5	82	DB3	2285	2900
33	S40	655	62.5	83	DB4	2170	2900
34	S39	765	62.5	84	DB5	2055	2900
35	S38	875	62.5	85	DB6	1940	2900
36	S37	985	62.5	86	DB7	1825	2900
37	S36	1095	62.5	87	NC		
38	S35	1205	62.5	88	NC		
39	S34	1315	62.5	89	NC		
40	S33	1425	62.5	90	CS3	1710	2900
41	S32	1535	62.5	91	CS2B	1595	2900
42	S31	1645	62.5	92	CS1B	1480	2900
43	S30	1755	62.5	93	RSTB	1365	2900
44	S29	1865	62.5	94	RW	1250	2900
45	S28	1975	62.5	95	RS	1135	2900
46	S27	2085	62.5	96	CL	1020	2900
47	S26	2195	62.5	97	CLK2	905	2900
48	S25	2305	62.5	98	CLK1	790	2900
49	S24	2415	62.5	99	E	675	2900
50	S23	2525	62.5	100	FRM	560	2900

6、PACKAGE INFORMATION

6. 1、QFP100-14×20-0.65



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D		22.00REF	
G1E		16.00REF	
L	0.60	0.80	1.00
L1		1.95REF	
θ	0°	2°	8°
θ 1	11°	13°	15°
θ 2	3°	5°	7°

7、STATEMENTS AND NOTES：

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

8、CONTACT：

Wuxi I-CORE Electronics Co., Ltd.

Addr：2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China http://www.i-core.cn

P.C: 214072 Tel：0510-81888895 Fax：0510-85572700

Marketing Department：2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China

P.C: 214072 Tel：0510-85572708 Fax：0510-85887721

Shenzhen office：26F Building12, xiangli garden hongli west Road, Shenzhen, Guangdong ,China

P.C: 518000 Tel：0755-88370507 Fax：0755-88370507

Guangzhou office：901room-57,ledeGarden, leming fiest street,Guanghua Road, baiyun District,Guangzhou,China

P.C: 510000 Tel：020-36743257 Fax：020-36743257

Applied Technical Services：

Application Department：

2F Building9，100Di cui Road, LiYuan Development Zone, Wuxi, jiangsu, China

P.C：214072 Tel：0510-85572715 Fax：0510-85572700

26F Building12, xiangli garden hongli west Road, Shenzhen, Guangdong ,China

P.C：518000 Tel：0755-88370507 Fax：0755-88370507