AiP31565CR
132 SEG/65 COM Dot Matrix LCD Controller/Driver

Product Specification

Specification Revision History：

Version	Date	Description
2019-03-A1	2019-03	New
2019-12-B1	2019-12	Replace the new template and modify the content

1、General Description

The AiP31565CR is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or 4-line SPI display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the AiP31565CR contain 65×132 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The AiP31565CR chips contain 65 common output circuits and132 segment output circuits, so that a single chip can drive a 65×132 dot display (capable of displaying 8 columns×4 rows of a 16×16 dot kanji font).

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, resistors for LCD driver power voltage adjustment and a display clock CR oscillator circuit, the AiP31565CR can be used to create the lowest power display system with the fewest components for high-performance portable devices.

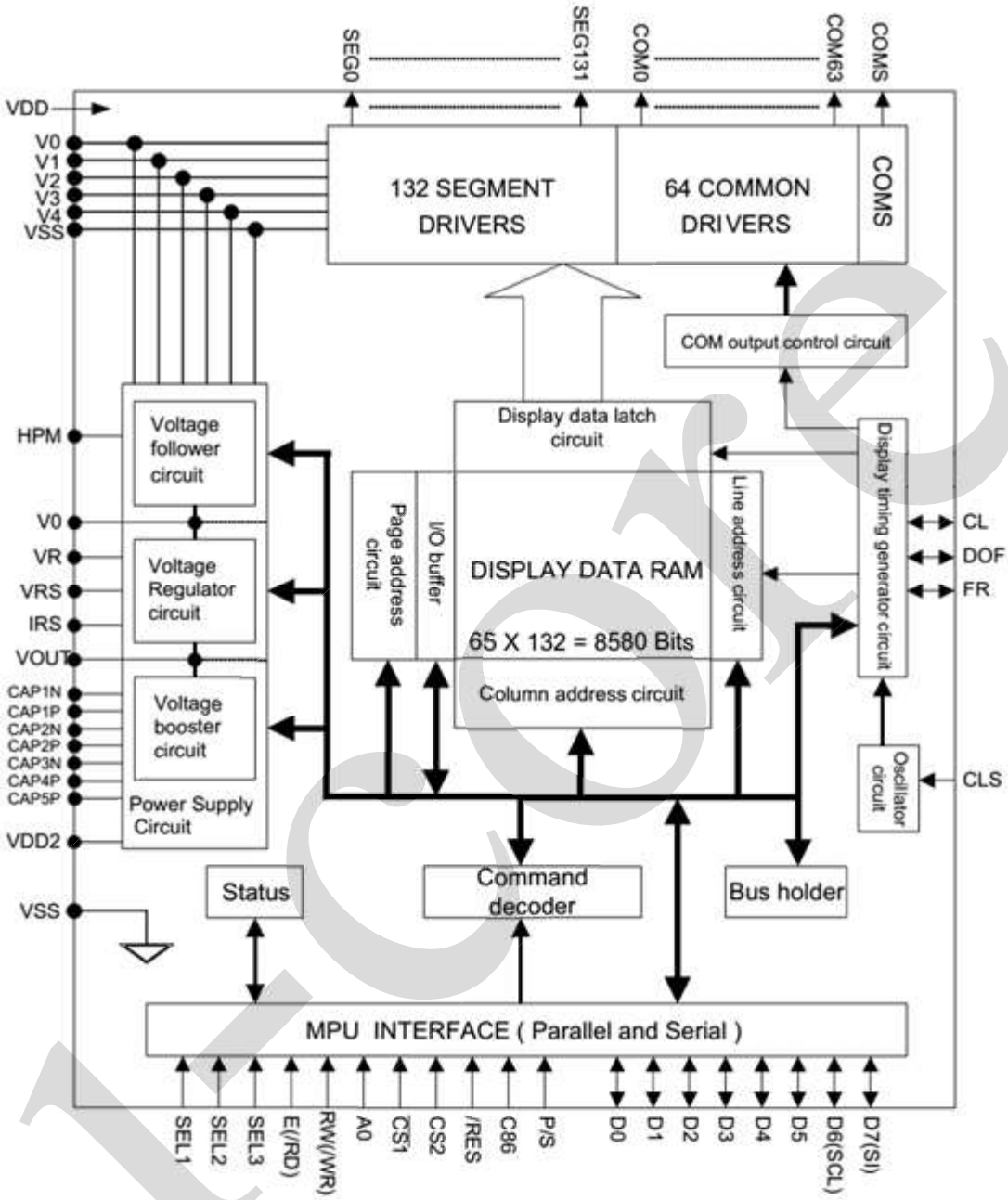
Features:

- Directly display RAM data through Display Data RAM.
- RAM capacity:65×132=8580 bits
- Display duty selectable by select pin
  - 1/65 duty:65 common×132 segment
  - 1/49 duty:49 common×132 segment
  - 1/33 duty:33 common×132 segment
  - 1/55 duty:55 common×132 segment
  - 1/53 duty:53 common×132 segment
- Bidirectional 8-bit parallel interface supports:
  - 8080-series and 6800-series MPU
  - Serial interface (SPI-4) is also supported (write only)
- Abundant command functions
  - Display data Read/Write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction selects, power saver, common output status select, V0 voltage regulation internal resistor ratio set.
- Embedded analog power supply circuits for Liquid Crystal driving: Booster, Regulator and Follower.
- Embedded Booster circuit:
  - 2×,3×,4×,5× and 6× boost ratios are supported.
  - Independent input (VDD2) for boost reference voltage.
- High-accuracy Regulator circuit:
  - Build-in Electronic volume function for the contrast control. Thermal gradient=–0.05%/℃.

- Embedded voltage Follower circuit for LCD driving.
- Embedded R-C oscillator circuit.
  The external clock is also supported.
- Extremely low power consumption:60uA, bare dice (using the internal power).
  Settings:
  VDD–VSS=VDD2–VSS=3.0V,Booster Ratio=4,
  V0–VSS=11.0V. Display OFF and the normal mode is
  selected.
- Logic power supply:VDD–VSS=2.4V to 3.3V
  Analog Power (Boost reference voltage):
  VDD2–VSS=2.4V to 3.3V
  Booster maximum voltage limited
  VOUT=13.5V
  Liquid crystal drive power supply:V0–VSS=3.0V to 12.0V
- Wide range of operating temperatures:–30 to 80℃
- Package type:COG only.
- The chip is not designed to resist the light or to resist
  the radiation.

2、Block Diagram And PAD Description

2.1、Block Diagram



2.2、PAD Description

<table>
<tr><th>PAD No.</th><th>PAD Name</th><th>Description</th></tr>
<tr><td>VDD</td><td>Power</td><td>Power supply</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Power</td><td>Ground</td></tr>
<tr><td>VRS</td><td>Power</td><td>This is the internal-output V_{REG} power supply for the LCD power supply voltage regulator.</td></tr>
<tr><td>V0、V1
V2、V3
V4</td><td>Power</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below.
V0≥V1≥V2≥V3≥V4≥VSS
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 Duty</th><th>1/49 Duty</th><th>1/33 Duty</th><th>1/55 Duty</th><th>1/53 Duty</th></tr>
<tr><td>V1</td><td>8/9V0,6/7V0</td><td>7/8V0,5/6V0</td><td>5/6V0,4/5V0</td><td>7/8V0,5/6V0</td><td>7/8V0,5/6V0</td></tr>
<tr><td>V2</td><td>7/9V0,5/7V0</td><td>6/8V0,4/6V0</td><td>4/6V0,3/5V0</td><td>6/8V0,4/6V0</td><td>6/8V0,4/6V0</td></tr>
<tr><td>V3</td><td>2/9V0,2/7V0</td><td>2/8V0,2/6V0</td><td>2/6V0,2/5V0</td><td>2/8V0,2/6V0</td><td>2/8V0,2/6V0</td></tr>
<tr><td>V4</td><td>1/9V0,1/7V0</td><td>1/8V0,1/6V0</td><td>1/6V0,1/5V0</td><td>1/8V0,1/6V0</td><td>1/8V0,1/6V0</td></tr>
</table></td></tr>
<tr><td>CAP1P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>CAP1N</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.</td></tr>
<tr><td>CAP2P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>CAP2N</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.</td></tr>
<tr><td>CAP3P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>CAP4P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>CAP5P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>VOUT</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.</td></tr>
<tr><td>VR</td><td>I</td><td>Output voltage regulator terminal.Provides the voltage between VSS and V0 through a resistive voltage divider.
IRS=“L”:the V0 voltage regulator internal resistors are not used.
IRS=“H”:the V0 voltage regulator internal resistors are used.</td></tr>
<tr><td>D5~D0
D6(SCL)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.</td></tr>
</table>

<table>
<tr><td>D7(SI)</td><td></td><td>When the serial interface (SPI-4) is selected (P/S="L") :
D7 : serial data input (SI);D6:the serial clock input (SCL).
D0 to D5 should be connected to VDD or floating.
When the chip select is not active, D0 to D7 are set to high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command.
A0="H":Indicates that D0 to D7 are display data.
A0="L":Indicates that D0 to D7 are control data.</td></tr>
<tr><td>/RES</td><td>I</td><td>When /RES is set to "L", the register settings are initialized (cleared).
The reset operation is performed by the /RES signal level.</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>This is the chip select signal. When $\overline{CS1}$="L"and CS2="H",then the chip select becomes active ,and data/command I/O is enabled.</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L".
• When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal.
• When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type:When R/W="H":Read.When R/W="L": Write.</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface selection pin.
C86="H":6800 Series MPU interface.
C86="L":8080 Series MPU interface.</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin configures the interface to be parallel mode or serial mode.
P/S="H":Parallel data input/output.
P/S="L":Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>4-line SPI Clock</th></tr>
<tr><td>H</td><td>A0</td><td>D0 to D7</td><td>/RD,/WR</td><td>X</td></tr>
<tr><td>L</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S="L", D0 to D5 must be fixed to "H".
/RD (E) and /WR (R/W) are fixed to either "H" or "L".
The serial access mode does NOT support read operation.</td></tr>
<tr><td>CLS</td><td>I</td><td>Selection pin to enable or disable the internal display clock oscillator circuit.
CLS="H":use internal oscillator circuit .
CLS="L":use external clock input (internal oscillator is disabled).
When CLS="L",input the external display clock through the CL terminal.</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the CLS status.
<table>
<tr><th>CLS</th><th>CL</th></tr>
<tr><td>"H"</td><td>Output</td></tr>
<tr><td>"L"</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>FR</td><td>O</td><td>This is the liquid crystal alternating current signal terminal.</td></tr>
<tr><td>/DOF</td><td>O</td><td>This is the LCD blanking control terminal.</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS=“H”:Use the internal resistors
IRS=“L”:Do not use the internal resistors. The V0 voltage level is
regulated by an external resistive voltage divider attached to the VR terminal</td></tr>
<tr><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM=“H”:Normal mode
/HPM=“L”:High power mode (suggested)</td></tr>
<tr><td>SEL3
SEL2
SEL1</td><td>I</td><td>These pins are DUTY selection.
<table>
<tr><th>SEL3,2,1</th><th>DUTY</th><th>BIAS</th></tr>
<tr><td>0,0,0</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>0,0,1</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>0,1,0</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>0,1,1</td><td>1/55</td><td>1/8 or 1/6</td></tr>
<tr><td>1,0,0</td><td>1/53</td><td>1/8 or 1/6</td></tr>
<tr><td>1,X,X</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>TEST0~7</td><td>I</td><td>These are terminals for IC testing.
TEST0~6: left them open.
TEST7 must connected to VDD</td></tr>
<tr><td>SEG0~
SEG131</td><td>O</td><td>These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from VSS, V3, V2, and V0.
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COM0~
COM63</td><td>O</td><td>Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VSS, V4, V1 , and V0.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS1，
COMS2
(COMS)</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td></tr>
</table>

2.3、I/O Pin ITO Resister Limitation

PAD Name	ITO Resister
CL,FR,/DOF,C86,P/S,/HPM,SEL1~3,CLS,IRS	No Limitation
TEST0~7,VRS	Floating
VDD,VDD2,VSS,VOUT,VR	<100Ω
V0~4,CAP1P,CAP1N,CAP2P,CAP2N,CAP3P,CAP4P,CAP5P	<300Ω
$\overline{CS1}$,CS2,/RD(E),/WR(R/W),A0,D0~7	<1kΩ
/RES	<10kΩ

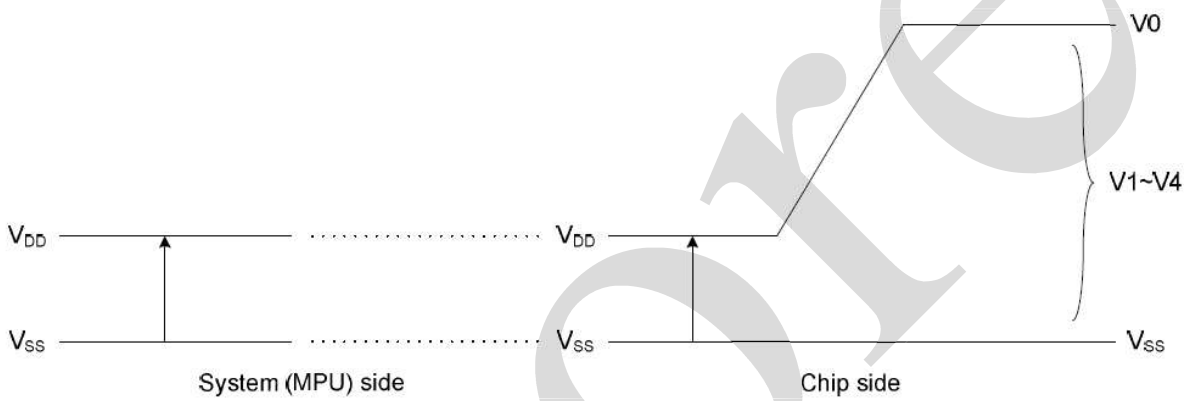
Note:

1. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of /RES signal(add a series resistor or increase ITO resistance). The value is different from modules.
2. The option setting to be “H” should connect to VDD.
3. The option setting to be “L” should connect to VSS.

3、Electrical Parameter

3.1、 Absolute Maximum Ratings (T_{amb}=25℃,VSS=0V, unless otherwise specified)

Characteristic		Symbol	Conditions	Value	Unit
Digital Power Supply Voltage		VDD	-	-0.3~+3.6	V
Analog Power supply voltage		VDD2	-	-0.3~+3.6	V
LCD Power supply voltage		V0,VOUT	-	-0.3~+13.5	V
LCD Power supply voltage		V1,V2,V3,V4	-	-0.3~V0	V
Logic input voltage		V_{IN}		-0.3～VDD+0.3	V
Operating temperature		T_{OPR}	-	-30~+80	℃
Soldering Temperature	Bare chip	T_{STR}	-	-55~+125	℃



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of VOUT,V0,V1,V2,V3,V4 and VSS always match the correct relation: VOUT≥V0≥V1≥V2≥V3≥V4≥VSS

3.2、Electrical Characteristics

3.2.1 DC Characteristics (T_{amb}=-40~+85℃,VDD=3.0V,VSS=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating Voltage(1)	VDD	Note 1		2.4	-	3.3	V
Operating Voltage(2)	VDD2	Relative to VSS,Note 2		2.4	-	3.3	V
High-level Input Voltage	V_{IH}	Note 3		0.8VDD	-	VDD	V
Low-level Input Voltage	V_{IL}	Note 3		VSS	-	0.2VDD	V
High-level Output Voltage	V_{OH}	I_{OH}=-0.5mA,Note 4		0.8VDD	-	VDD	V
Low-level Output Voltage	V_{OL}	I_{OL}=0.5mA,Note 4		VSS	-	0.2VDD	V
Input leakage current	I_{LI}	V_{IN}=VDD or VSS,Note 5		-1.0	-	1.0	uA
Output leakage current	I_{LO}	VOUT=VDD or VSS,Note 6		-3.0	-	3.0	uA
Liquid Crystal Driver ON Resistance	R_{ON}	V0=13.0V,SEG、COM		-	2.0	3.5	kΩ
		V0=8.0V,SEG、COM,Note 7		-	3.2	5.4	kΩ
Static Consumption Current	I_{SS}	V0-VSS=13V,VDD,VDD2		-	0.01	2	uA
Output Leakage Current	I_{OQ}	V0-VSS=13V		-	0.01	10	uA
Input Terminal Capacitance	C_{IN}	25℃,f=1MHz		-	5.0	8.0	pF
Internal Oscillator	f_{OSC}	1/65 and 1/33 duty,Note 8		17	20	24	kHz
		1/49,1/53,1/55 duty		25	30	35	kHz
External Input	f_{CL}	1/65 and 1/33 duty,Note 8		17	20	24	kHz
		1/49,1/53,1/55 duty		25	30	35	kHz
Supply Step-up output voltage Circuit	VOUT	Relative To VSS		-	-	13.5	V
Voltage regulator Circuit Operating Voltage	VOUT	Relative To VSS		6.0	-	13.5	V
Voltage Follower Circuit Operating Voltage	V0	Relative To VSS,Note 9		4.0	-	13.5	V
Base Voltage	VRS	25℃,-0.05%/℃,Note 10		2.07	2.10	2.13	V
Display Pattern OFF (Note 11)	I_{DD}	VDD=3V,V0-VSS=11V, OFF		-	16	27	uA
		VDD=3V,V0-VSS=11V, Checker		-	19	32	uA
Display Pattern Checker (Note 12)	I_{DD}	VDD=3.0V, Quad step-up	Normal Mode	-	90	130	uA
			High-Power	-	128	193	uA

		voltage. V0-VSS=11.0V	Mode				
		VDD=3.0V Quad step-up voltage. V0-VSS=11.0V	Normal Mode	-	100	147	uA
			High-Power Mode	-	135	205	uA
Sleep mode	I_{DD}	VDD=3V		-	0.4	4	uA

Note:

1.While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

2.The operating voltage range for the VSS system and the V0 system is. This applies when the external power supply is being used.

3.The A0,D0 to D5,D6(SCL),D7(SI),/RD(E),/WR(R/W),/CS1,CS2,CLS,CL,FR,C86,P/S,/DOF,/RES,IRS, and /HPM terminals.

4.The D0 to D7, FR, /DOF, and CL terminals.

5.The A0,/RD(E),/WR(R/W),/CS1,CS2,CLS,C86,P/S,/RES,IRS and /HPM terminals.

6.Applies when the D0 to D5,D6(SCL),D7(SI),CL,FR, and /DOF terminals are in a high impedance state.

7.These are the resistance values for when a 0.1V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1,V2,V3 and V4). These are specified for the operating voltage(3) range.R_{ON}=0.1V/ΔI (Where Δ I is the current that flows when 0.1V is applied while the power supply is ON.)

8.The relationship between the oscillator frequency and the frame rate frequency.

9.The V0 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

10.This is the internal voltage reference supply for the V0 voltage regulator circuit.In the AiP31565CR, the temperature range approximately –0.05%/℃.

11.It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.The AiP31565CR is 1/9 biased.Does not include the current due to the LCD panel capacity and wiring capacity.Applicable only when there is no access from the MPU.

12.It is the value on a AiP31565CR having the V_{REG} temperature gradient is –0.05%/℃ when the V0 voltage regulator internal resistor is used.

Current consumption: During Display, without internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Conditions	Min.	Typ.	Max.	Unit
Display Pattern: SNOW (Static)	I_{SS}	VDD=VDD2=3.0V, V0=11.0V, T_{amb}=25℃	-	19	32	uA
Display OFF	I_{SS}	VDD=VDD2=3.0V, V0=11.0V, T_{amb}=25℃	-	16	27	uA

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Conditions	Min.	Typ.	Max.	Unit
Display Pattern: SNOW	I_{SS}	VDD=VDD2=3.0V, V0=11.0V, Booster=×4, T_{amb}=25℃	-	100	147	uA
			-	135	205	uA
Display OFF	I_{SS}	VDD=VDD2=3.0V, V0=11.0V, Booster=×4, T_{amb}=25°C	-	90	130	uA
			-	128	193	uA
Sleep Mode	I_{SS}	VDD=VDD2=3.0V, T_{amb}=25℃	-	0.4	4	uA

Note: The Current Consumption is DC characteristics

The relationship between oscillator frequency f_{OSC}, display clock frequency f_{CL} and liquid crystal frame rate frequency f_{FR}.

Item		f_{CL}	f_{FR}
1/65 Duty	Internal Oscillator Circuit	f_{OSC}/4	f_{OSC}/4/65
	External Display Clock	External Display Clock (f_{CL})	f_{CL}/260
1/49 Duty	Internal Oscillator Circuit	f_{OSC}/8	f_{OSC}/4/49
	External Display Clock	External Display Clock (f_{CL})	f_{CL}/196
1/33 Duty	Internal Oscillator Circuit	f_{OSC}/8	f_{OSC}/4/33
	External Display Clock	External Display Clock (f_{CL})	f_{CL}/264
1/55 Duty	Internal Oscillator Circuit	f_{OSC}/8	f_{OSC}/4/55
	External Display Clock	External Display Clock (f_{CL})	f_{CL}/200
1/53 Duty	Internal Oscillator Circuit	f_{OSC}/8	f_{OSC}/4/53
	External Display Clock	External Display Clock (f_{CL})	f_{CL}/212

3.2.2、AC Characteristics (T_{amb}=-40~+85℃,VDD=3.0V,VSS=0V,unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VDD=2.7V,T_{amb}=25℃						
Address hold time	t_{AH8}、t_{AH6}	A0,FIG 1、2	0	-	-	ns
Address setup time	t_{AW8}、t_{AW6}		0	-	-	ns
System cycle time	t_{CYC8}、t_{CYC6}	/WR(E),FIG 1、2	400	-	-	ns
Enable L pulse width (WRITE)	t_{CCLW}、tew_{LW}		220	-	-	ns
Enable H pulse width (WRITE)	t_{CCHW}、tew_{HW}		180	-	-	ns
Enable L pulse width (READ)	t_{CCLR}、tew_{LR}	RD(E),FIG 1、2	220	-	-	ns
Enable H pulse width (READ)	t_{CCHR}、tew_{HR}		180	-	-	ns
WRITE Data setup time	t_{DS8}、t_{DS6}	D0 to D7 C_L=100pF FIG 1、2	40	-	-	ns
WRITE Address hold time	t_{DH8}、t_{DH6}		0	-	-	ns
READ access time	t_{ACC8}、t_{ACC6}		-	-	140	ns
READ Output disable time	t_{OH8}、t_{OH6}		10	-	100	ns
4-line SPI Clock Period	t_{SCYC}	SCL,FIG 3	100	-	-	ns
SCL “H” pulse width	t_{SHW}		50	-	-	ns
SCL “L” pulse width	t_{SLW}		50	-	-	ns
Address setup time	t_{SAS}	A0,FIG 3	30	-	-	ns
Address hold time	t_{SAH}		20	-	-	ns
Data setup time	t_{SDS}	SI,FIG 3	30	-	-	ns
Data hold time	t_{SDH}		20	-	-	ns
CS-SCL time	t_{CCSS}	CS,FIG 3	30	-	-	ns
	t_{CSH}		60	-	-	ns
Reset time	t_R	FIG 4	-	-	2.0	us
Reset “L” pulse width	t_{RW}	/RES,FIG 4	2.0	-	-	us
VDD=3.3V,T_{amb}=25℃						
Address hold time	t_{AH8}、t_{AH6}	A0,FIG 1、2	0	-	-	ns
Address setup time	t_{AW8}、t_{AW6}		0	-	-	ns
System cycle time	t_{CYC8}、t_{CYC6}	WR(E),FIG 1、2	240	-	-	ns
Enable L pulse width (WRITE)	t_{CCLW}、tew_{LW}		80	-	-	ns
Enable H pulse width (WRITE)	t_{CCHW}、tew_{HW}		80	-	-	ns
Enable L pulse width (READ)	t_{CCLR}、tew_{LR}	RD(E),FIG 1、2	80	-	-	ns
Enable H pulse width (READ)	t_{CCHR}、tew_{HR}		140	-	-	ns
WRITE Data setup time	t_{DS8}、t_{DS6}	D0 to D7 C_L=100pF FIG 1、2	40	-	-	ns
WRITE Address hold time	t_{DH8}、t_{DH6}		0	-	-	ns
READ access time	t_{ACC8}、t_{ACC6}		-	-	70	ns
READ Output disable time	t_{OH8}、t_{OH6}		5	-	50	ns
4-line SPI Clock Period	t_{SCYC}	SCL,FIG 3	50	-	-	ns
SCL “H” pulse width	t_{SHW}		25	-	-	ns
SCL “L” pulse width	t_{SLW}		25	-	-	ns

Address setup time	t_{SAS}	A0,FIG 3	20	-	-	ns
Address hold time	t_{SAH}		10	-	-	ns
Data setup time	t_{SDS}	SI,FIG 3	20	-	-	ns
Data hold time	t_{SDH}		10	-	-	ns
CS-SCL time	t_{CCSS}	CS,FIG 3	20	-	-	ns
	t_{CSH}		40	-	-	ns
Reset time	t_R	FIG 4	-	-	1.0	us
Reset "L" pulse width	t_{RW}	/RES,FIG 4	1.0	-	-	us

4、Testing Circuit

4.1、AC Testing Circuit

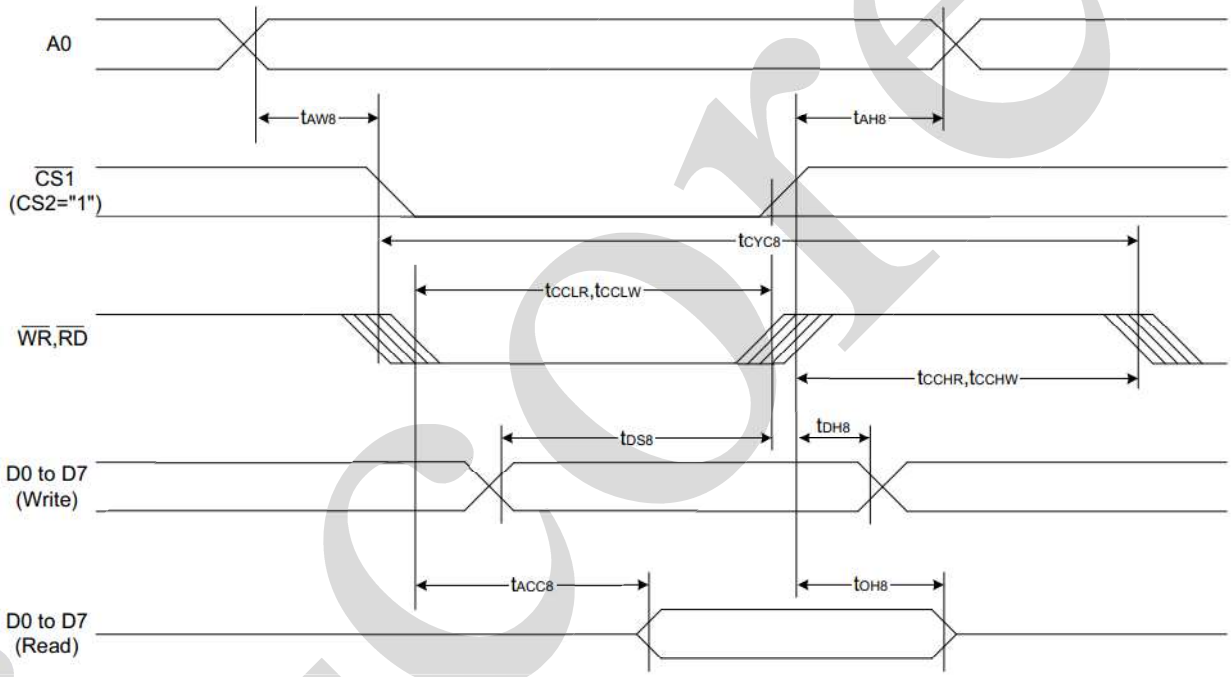


FIG 1、8080MPU

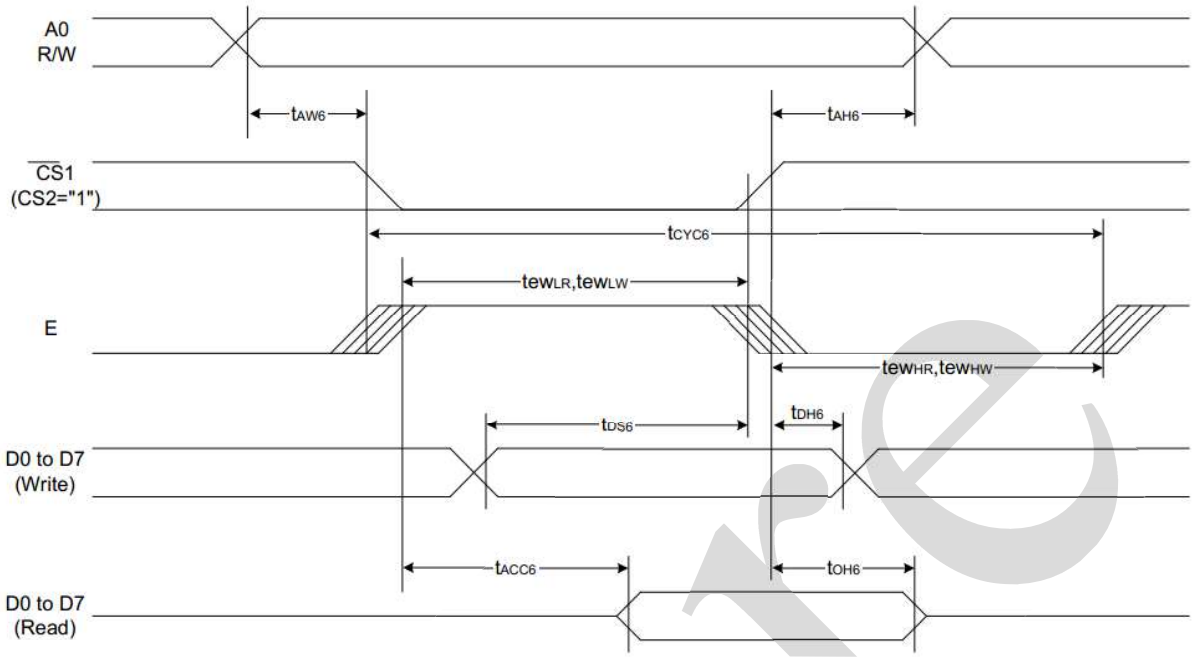


FIG 2、6800MPU

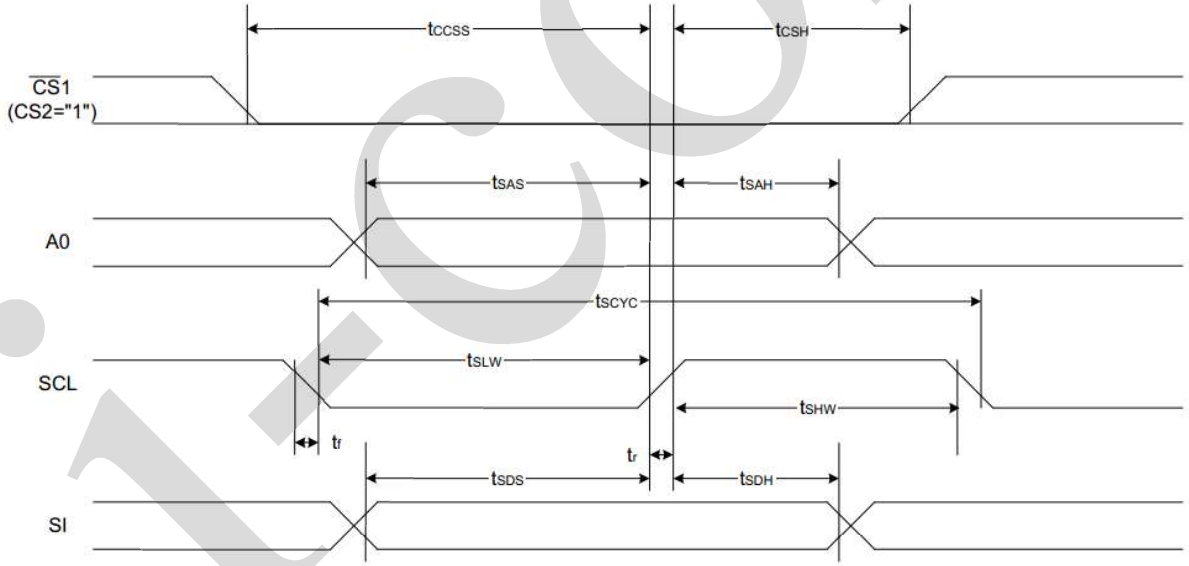


FIG 3、4-Line Serial Interface

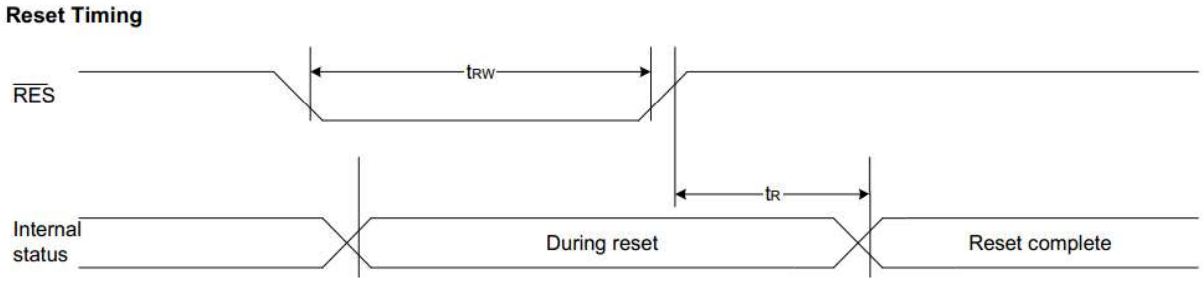


FIG 4、Reset Timing

5、Function Description

5.1、Microprocessor Interface

5.1.1、Chip Select Input

$\overline{CS1}$ and CS2 pins are used for chip selection. When $\overline{CS1}$="L" and CS2="H", the microprocessor interface is enabled and AiP31565CR can interface with an MPU.When $\overline{CS1}$="H" or CS2="L", the inputs of A0, E(/RD) and R/W(/WR) with any combination will be ignored and D7~D0 are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when $\overline{CS1}$="H" or CS2="L".

5.1.2、MCU Interface Selection

The interface selection is controlled by C86 and P/S pins. The selection for parallel or serial interface is shown in Table 1.

Table 1. Parallel/Serial Interface Mode

P/S	C86	$\overline{CS1}$	CS2	A0	E(/RD)	R/W(/WR)	D7~D0	MPU Interface
"H"	"H"	$\overline{CS1}$	CS2	A0	E	R/W	D0~D7	6800-series parallel interface
"H"	"L"				/RD	/WR		8080-series parallel interface
"L"	"X"				-	-	Refer to serial interface.	4-Line SPI interface

Note:The un-used pins are marked as "-" and should be fixed to "H" by VDD.

5.1.3、Parallel Interface

When P/S= "H", the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by "C86" pin as shown in Table 2. The data transfer type is determined by signals on A0, E(/RD) and R/W(/WR) as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

P/S	C86	$\overline{CS1}$	CS2	A0	E(/RD)	R/W(/WR)	D0~D7	MPU Interface
"H"	"H"	$\overline{CS1}$	CS2	A0	E	R/W	D7~D0	6800-series parallel interface
	"L"				/RD	/WR		8080-series parallel interface

Table 3. Parallel Data Transfer Type

Common Pins			6800-Series		8080-Series		Description
$\overline{CS1}$	CS2	A0	E	R/W	/RD	/WR	
"L"	"H"	"H"	"H"	"H"	"L"	"H"	Display data read out
		"H"	"H"	"L"	"H"	"L"	Display data write
		"L"	"H"	"H"	"L"	"H"	Internal status read
		"L"	"H"	"L"	"H"	"L"	Writes to internal register (instruction)

5.1.4、Setting Serial Interface

Serial Mode	P/S	C86	$\overline{CS1}$	CS2	A0	E(/RD)	R/W(/WR)	D7	D6	D5~D0
4-Line SPI interface	"L"	X	$\overline{CS1}$	CS2	A0	-	-	SI	SCL	-

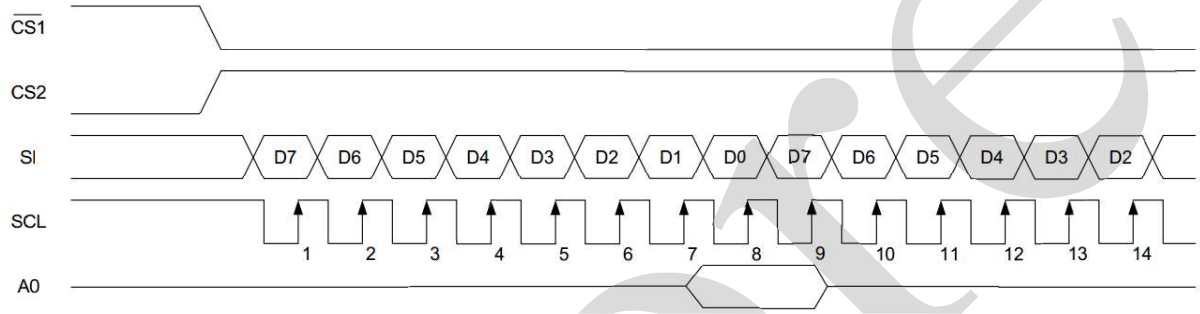
Note: The un-used pins are marked as "-" and should be fixed to "H" by VDD.

C86 is marked as "X" and can be fixed to "H" or "L".

1. The option setting to be "H" should connect to VDD.
2. The option setting to be "L" should connect to VSS.

5.1.5、4-line SPI interface (P/S="L", C86="H" or "L")

When AiP31565CR is active ($\overline{CS1}$="L" and CS2="H"), serial data (SI) and serial clock (SCL) inputs are enabled. When AiP31565CR is not active ($\overline{CS1}$="H" or CS2="L"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SI is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.

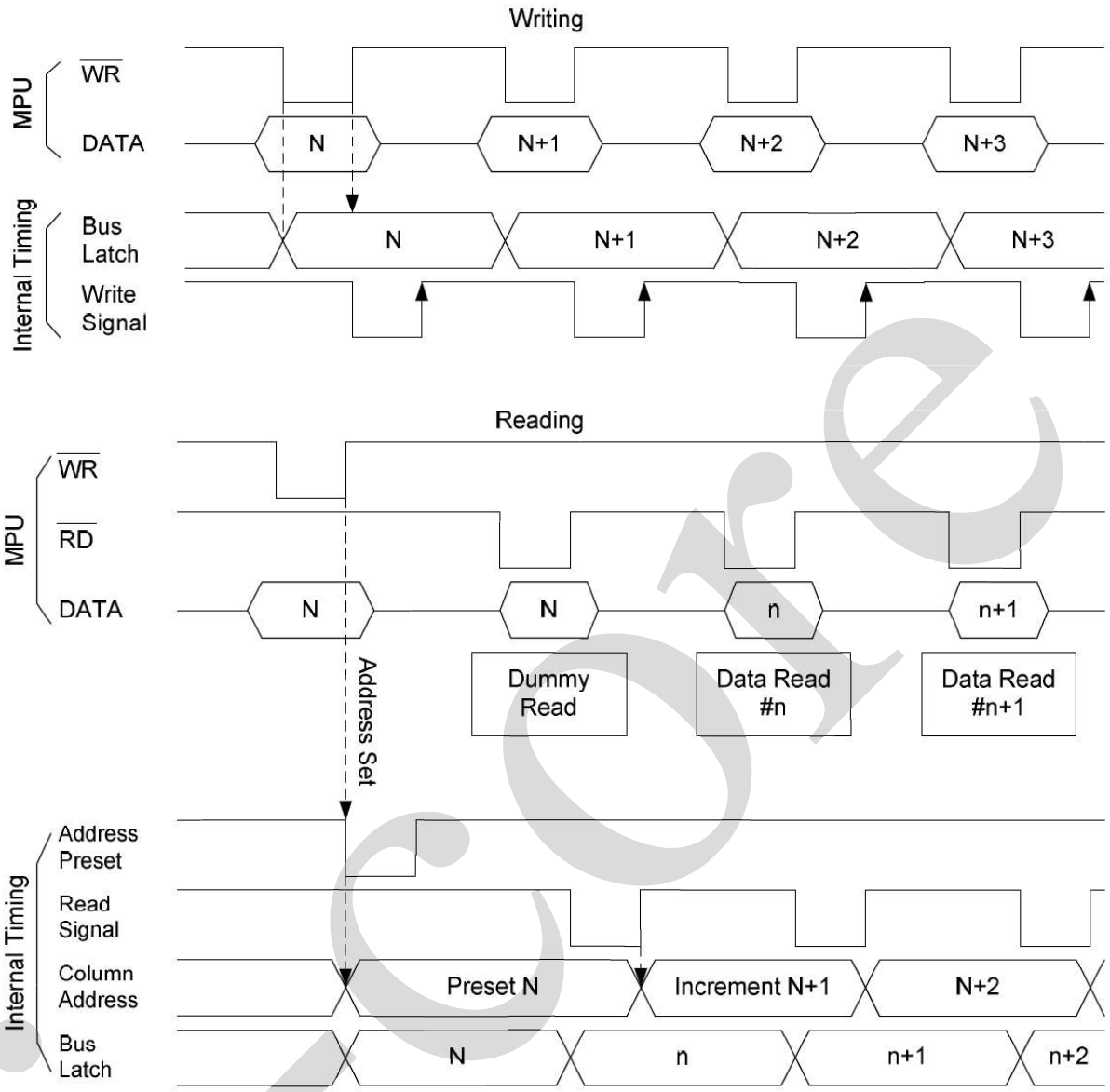


Note:

Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset.This is not allowed when the VDD of AIP31565CR is turned ON. Because the floating input (especially for those control pins such as $\overline{CS1}$, CS2, /RES, R/W(/WR) or E(/RD)…) maybe cause abnormal latch and cause abnormal display.

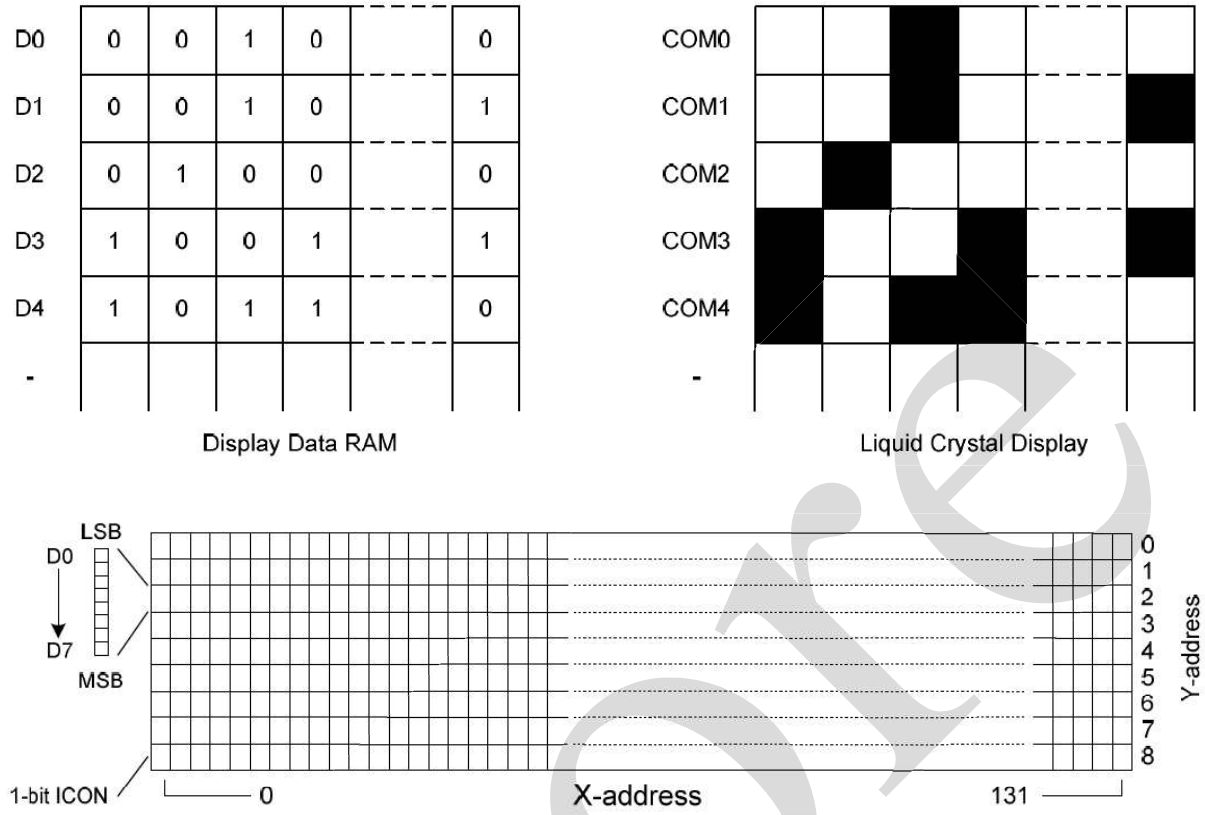
5.1.5、Data Transfer

AiP31565CR uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM.When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle.That means:after setting the target address, a dummy read cycle is required before the following read-operation.Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.



5.2、Display Data RAM (DDRAM)

AiP31565CR is built-in a RAM with 65×132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit).The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified. The rows are divided into: 8 pages (Page-0~Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D7~D0 directly except icon page. Icon RAM uses only 1-bit of data bus (D0). The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



5.3、Addressing

Data is downloaded into the Display Data RAM matrix in AiP31565CR as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131(column address), Y=0~8(page address). Addresses outside these ranges are not allowed.

5.3.1、Page Address Circuit

This circuit provides the page address of DDRAM.It incorporates 4-bit Page Address Register which can be modified by the "Page Address Set" instruction only.The Page Address must be set before accessing DDRAM content. Page Address "8" is a special RAM area for the icons with only one valid bit:D0.

5.3.2、Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address "83h") because the Column Address and Page Address circuits are independent.For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0). Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

5.3.3、Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the "Display Start Line Set" instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore,by setting Line Address repeatedly,AiP31565CR can realize the screen scrolling without changing the contents of DDRAM. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

5.4、Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock.The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

5.5、Oscillation Circuit

The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing AiP31565CR.The clock will not be output to reduce the power consumption.

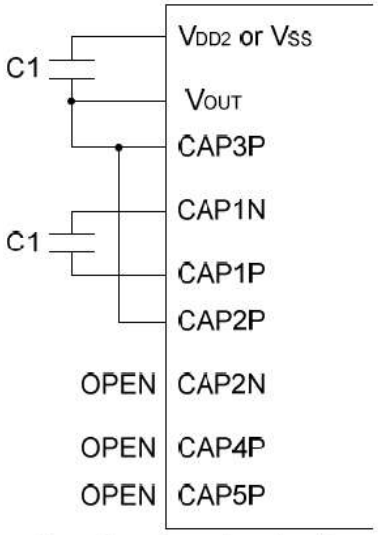
5.6、Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. The built-in power system has voltage booster,voltage regulator and voltage follower circuits.The functionality of voltage booster,voltage regulator and voltage follower circuits can be turned ON and OFF individually.AiP31565CR is possible to use built-in power circuit and external power supply through the command "Power Control Set".The relationship of command setting and power using is shown below. Before power AiP31565CR OFF,a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

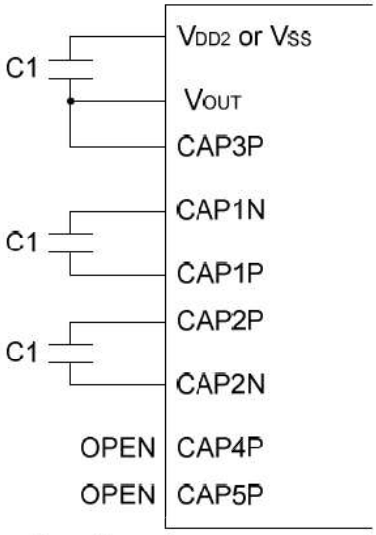
Power Control Set			Built-in Circuit			Power Supply					
VB	VR	VF	Booster	Regulator	Follower	VOUT	V0	V1	V2	V3	V4
1	1	1	ON	ON	ON	Internal	Internal	Internal	Internal	Internal	Internal
0	1	1	OFF	ON	ON	External	Internal	Internal	Internal	Internal	Internal
0	0	1	OFF	OFF	ON	External	External	Internal	Internal	Internal	Internal
0	0	0	OFF	OFF	OFF	External	External	External	External	External	External

5.6.1、Booster Circuit

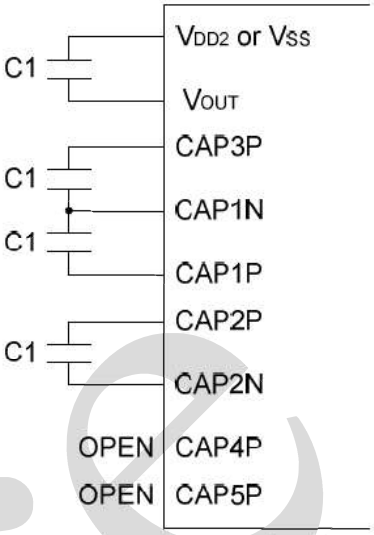
Base on VDD2-VSS,AiP31565CR is able to product step-up voltages of ×2,×3,×4,×5 and ×6 through hardware and software setting.



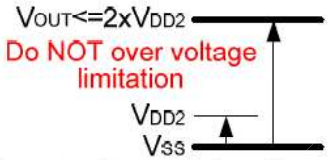
2x voltage booster circuit



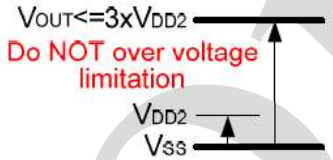
3x voltage booster circuit



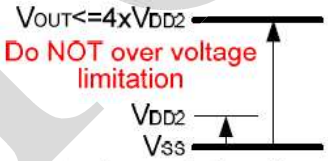
4x voltage booster circuit



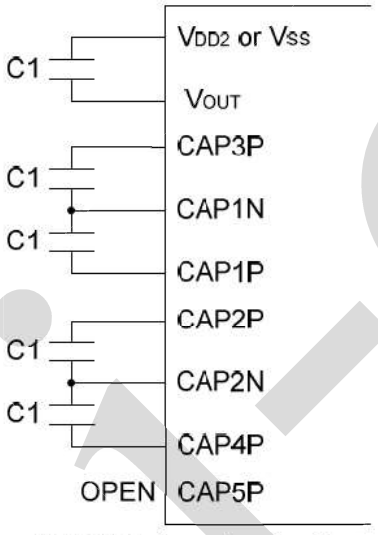
2x boost voltage relationship



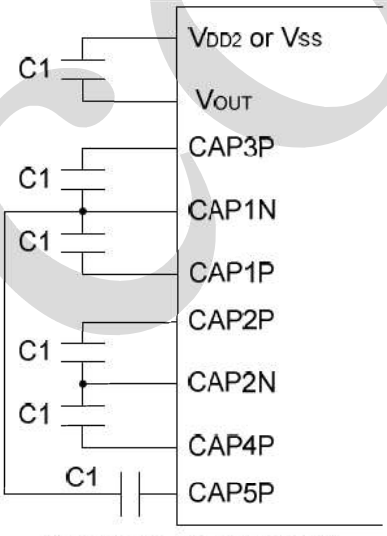
3x boost voltage relationship



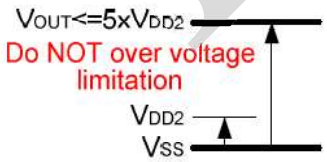
4x boost voltage relationship



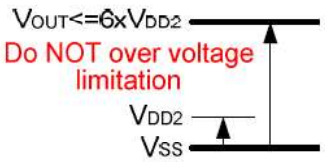
5x voltage booster circuit



6x voltage booster circuit



5x boost voltage relationship



6x boost voltage relationship

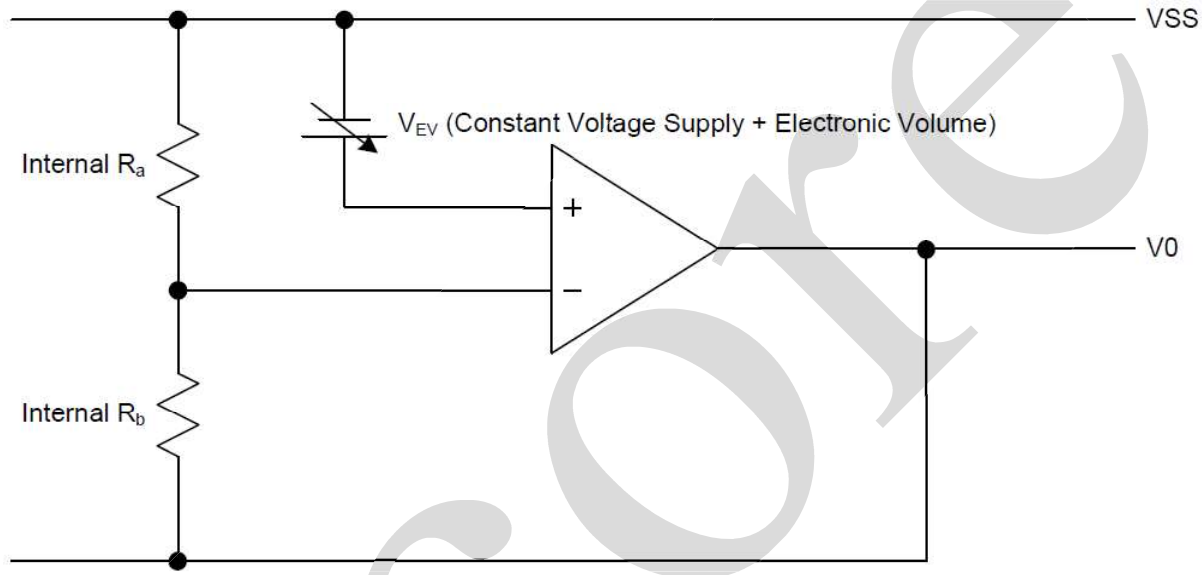
External Component of Booster Circuit

5.6.2、Regulator Circuit

AiP31565CR provides two kinds power supply for LCD driving voltage V0. Built-in regulator circuit or external power supply for V0 is available for LCD driving. The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as “Regulation Ratio” and “Set EV”. The detailed setting method can be found in the Instruction Description section.

- **Built-in Resistor Is Used For Regulator Circuit**

The internal regulator circuit can be controlled by built-in regulation ratio and the electronic volume setting.



$$V0=(1+R_b/R_a)\times V_{EV}$$
$$=(1+R_b/R_a)\times(1-\alpha/162)\times V_{REG}$$
$$V_{EV}=(1-\alpha/162)\times V_{REG}$$

V_{REG} is built-in constant voltage supply for regulator circuit. The voltage level of V_{REG} is 2.1V at temperature 25℃. α is determined by command "Set EV". Base on command "Set EV", the relationship between EV5~EV0 and α is shown below.

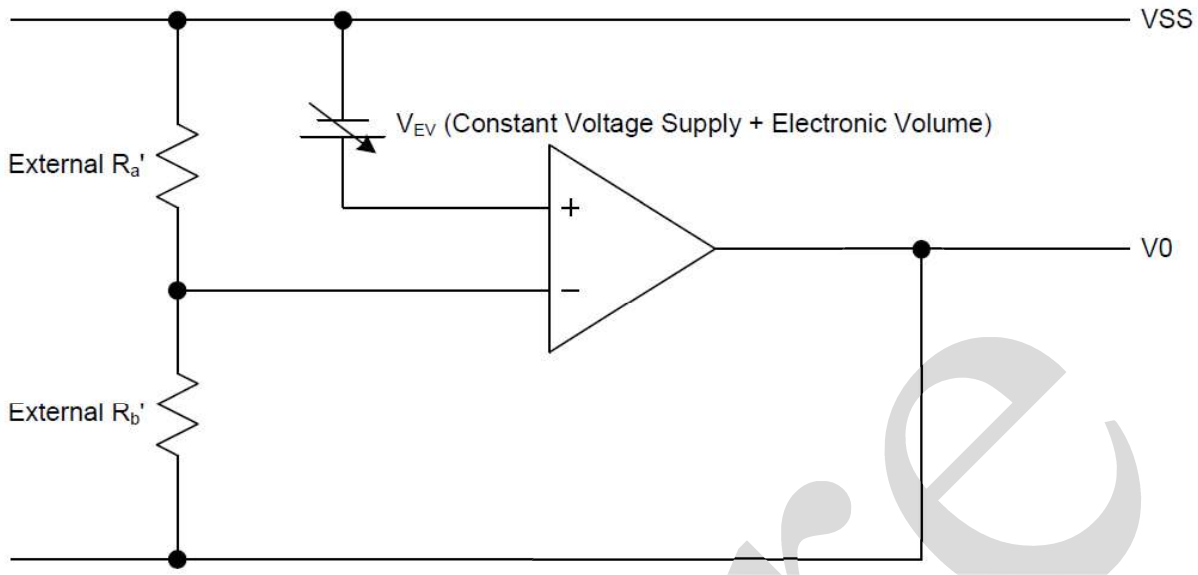
EV5	EV4	EV3	EV2	EV1	EV0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
0	0	0	0	1	1	60
…	…	…	…	…	…	…
1	1	1	1	0	0	3
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

$(1+R_b/R_a)$ is internal regulation ratio for regulator circuit. The relationship between regulation ratio and RR2~RR0 is shown below.

RR2	RR1	RR0	$1+R_b/R_a$
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

- **External Resistor Is Used For Regulator Circuit**

Through hardware setting IRS="L" and external resistor, AiP31565CR is able to use external regulation ratio to control the voltage level of V0.



$$V0=(1+R_b'/R_a')\times V_{EV}$$
$$=(1+R_b'/R_a')\times(1-\alpha/162)\times V_{REG}$$
$$V_{EV}=(1-\alpha/162)\times V_{REG}$$

The setting condition of AiP31565CR for external regulation ratio is V0=8.0V, α=31 and V_{REG}=2.1V. The current consumption through R_a' and R_b' is limited to 5uA. Base on above condition, the relationship of R_a' and R_b' is R_a'+R_b'=1.6MΩ.

$$V0=(1+R_b'/R_a')\times(1-\alpha/162)\times V_{REG} \quad (1.1)$$
$$8V=(1+R_b'/R_a')\times(1-31/162)\times 2.1 \quad (1.2)$$
$$R_a'+R_b'=1.6M\Omega \quad (1.3)$$

According to equation (1.2) and (1.3)

$$R_b'/R_a'=3.71$$
$$R_a'=340k\Omega$$
$$R_b'=1260k\Omega$$

5.6.3、High Power Mode

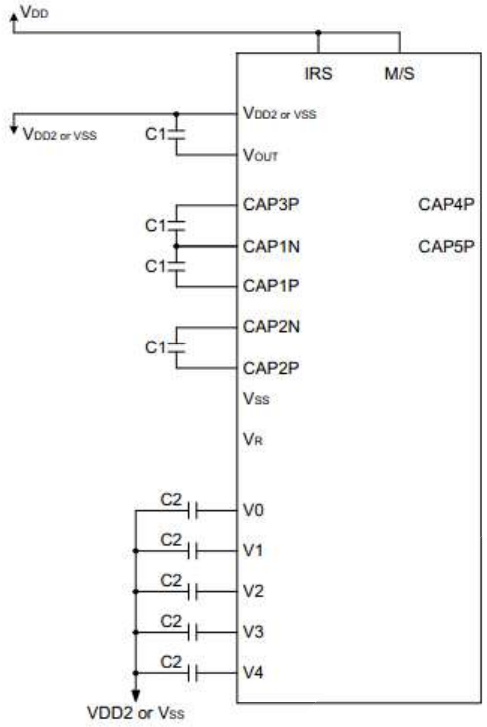
AiP31565CR has two kinds of power mode for driving LCD. When /HPM pin is connected to “H” by VDD,AiP31565CR will enter normal power mode. Normal power mode has lower power consumption for driving. If the panel loading or size is larger,normal power mode may cause display quality to reduce. For improve display quality,AiP31565CR provides high power mode through connect /HPM pin to “L” by VSS.I-CORE recommends that whether using high power mode or normal power mode is determined by actually display quality. Besides, if improvement is unsatisfactory after using high power mode, external power supply for LCD driving is necessary.

5.6.4、Power System Set

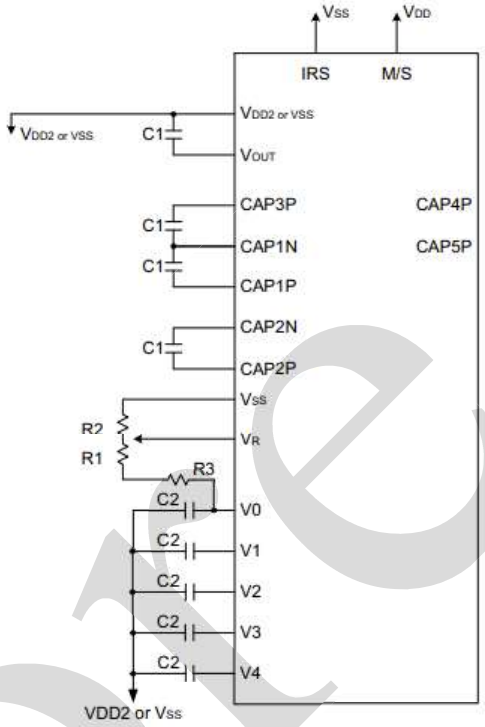
The following sections illustrate the connection of typical application.

- **Built-in Booster, Regulator and Follower Circuit are used**

1.Built-in regulation ratio is used with ×4 step-up

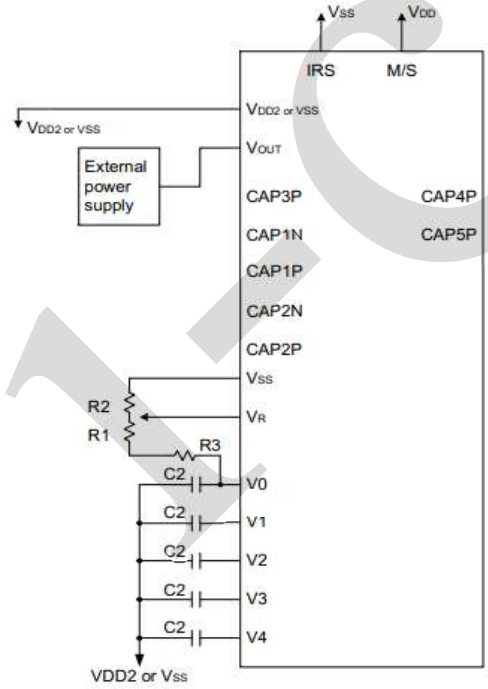


2. Built-in regulation ratio is not used with ×4 step-up

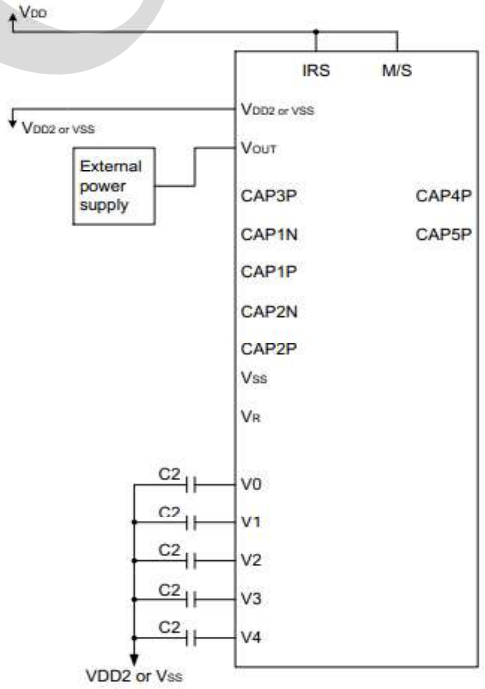


- **Built-in Regulator and Follower Circuit are alone used**

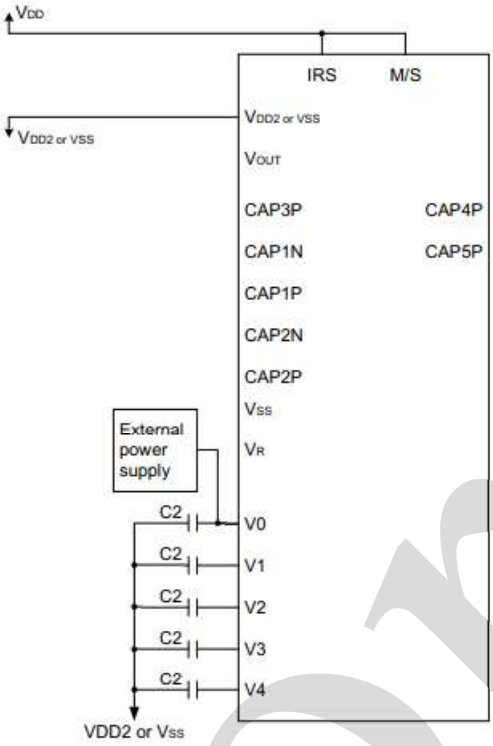
1. Built-in regulation ratio is used



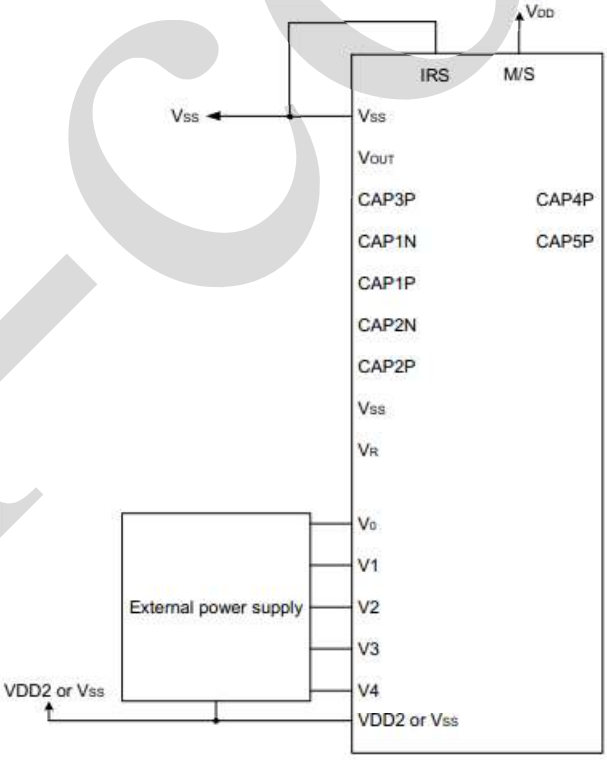
2. Built-in regulation ratio is not used



- **Built-in Follower Circuit is alone used**



- **Built-in Booster, Regulator and Follower Circuit are not used**



The optimum values of C1 and C2 are determined by panel loading and actually display quality. The values of capacitor should be determined by user. User should check display quality of used pattern and power stability after capacitor value is determined. The following table is a quick reference for the initial setting.

Symbol	Type	Reference Value (uF)
C1	Capacitor for step-up and LCD voltage stabilization	1.0 ~ 4.7
C2	Capacitor for LCD voltage stabilization	0.1~ 4.7

5.7、Reset Circuit

Setting /RES to "L" can initialize internal function. While /RES is "L", no instruction except read status can be accepted./RES pin must connect to the reset pin of MPU and initialization by /RES pin is essential before operating. Please note the hardware reset is not same as the software reset. When /RES becomes "L", the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Display OFF:D=0, all SEGs/COMs output at VSS	V	X
Normal Display:INV=0, AP=0	V	X
SEG Normal Direction:MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection:BS=0	V	X
Booster Level BL=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF:VB=0, VR=0, VF=0	V	X
Exit Read-modify-Write mode	V	V
Static Indicator OFF	V	V
Static Indicator Register SIR[1:0]=(0,0)	V	V
Start Line S[5:0]=0	V	V
Column Address X[7:0]=0	V	V
Page Address Y[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V0 Regulation Ratio RR[2:0]=(1,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V
Exit Test Mode	V	V

After power-on, RAM data are undefined and the display status is "Display OFF". It's better to initialize whole DDRAM (ex:fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

5.8、Instruction Table

Instruction	A0	R/W	Command Byte								Description
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
Read Status	0	1	BUSY	MX	D	RST	0	0	0	0	Read IC Status
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode

RESET	0	0	1	1	1	0	0	0	1	0	Software reset
COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
Power Save Mode Set	0	0	1	0	1	0	1	1	0	MD	MD=0, sleep mode MD=1, normal
	0	0	0	0	0	0	0	0	0	0	
Power Save	0	0	Compound Command								Display OFF + All Pixel ON
Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL[1:0]=(0,0),×2,×3,×4 BL[1:0]=(0,1),×5 BL[1:0]=(1,1),×6
	0	0	0	0	0	0	0	0	BL1	BL0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test	0	0	1	1	1	1	-	-	-	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

5.9、Instruction Description

- **Display ON/OFF**

The D flag selects the display mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	0

Note:

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

- **Set Start Line**

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
…	…	…	…	…	…	…
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

- **Set Page Address**

Y [3:0] defines the Y address vector address of the display RAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Page address	Valid bit
0	0	0	0	Page0	D0~D7
0	0	0	1	Page1	D0~D7
0	0	1	0	Page2	D0~D7
…	…	…	…	…	…
0	1	1	0	Page6	D0~D7
0	1	1	1	Page7	D0~D7
1	0	0	0	Page8 (icon page)	D0

- **Set Column Address**

The range of column address is 0…131. The parameter is separated into 2 instructions. The column address is increased (+1) after each byte of display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	X3	X2	X1	X0

X7	X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
		…	…	…	…	…	…	…
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

- **Read Status**

Read the internal status of AiP31565CR. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BUSY	MX	0	RST	0	0	0	0

Flag	Description
BUSY	BUSY=0: Command can be accepted BUSY=1: Command or reset procedure is executed
MX	MX=0: Reverse direction (SEG131->SEG0) MX=1: Normal direction (SEG0->SEG131)
D	D=0: Display ON D=1: Display OFF
RST	RST=1: During reset (hardware or software reset) RST=0: Normal operation

- **Write Data**

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

- **Read Data**

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor. The read function is not available in serial interface mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

- **SEG Direction**

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG131) MX=1: Reverse direction (SEG131->SEG0)

- **Inverse Display**

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white ->Black, Black->White) while the display data in the Display Data RAM is never changed.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV=1: Inverse display

- **All Pixel ON**

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP=0: Normal display AP=1: All pixels ON

- **Bias Select**

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	BS

Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6
1/53	1/8	1/6

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

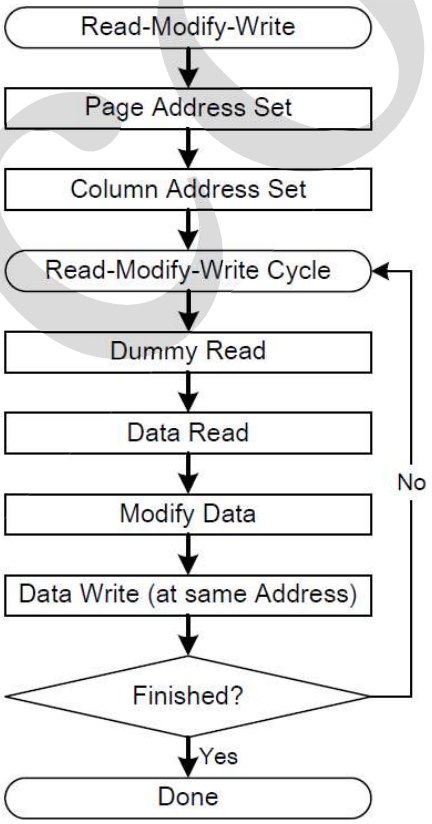
Symbol	Bias Voltage
V0	V0
V1	8/9×V0
V2	7/9×V0
V3	2/9×V0
V4	1/9×V0
VSS	VSS

- **Read-modify-Write**

This command is used paired with the "END" instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

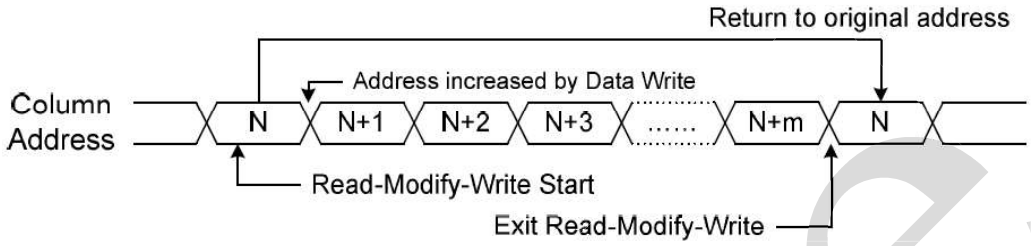
Note: In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.



- **END**

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0



- **RESET**

This instruction resets Start Line (S[5:0]), Column Address (X[7:0]), Page Address (Y[3:0]) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset (/RES=L) and cannot initialize the built-in power circuit which is initialized by the /RES pin. The detailed information is in "Section RESET CIRCUIT".

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

- **COM Direction**

This instruction controls the common output status which changes the vertical display direction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	-	-	-

Flag	Description
MY	MY=0: Normal direction (COM0->COM63) MY=1: Reverse direction (COM63->COM0)

- **Power Control**

This instruction controls the built-in power circuits.Typically, these 3 flags are turned ON at the same time.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VB	VR	VF

Flag	Description
VB	VB=0: Built-in Booster OFF VB=1: Built-in Booster ON
VR	VR=0: Built-in Regulator OFF VR=1: Built-in Regulator ON
VF	VF=0: Built-in Follower OFF VF=1: Built-in Follower ON

- **Regulation Ratio**

This instruction controls the regulation ratio of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	RR2	RR1	RR0

RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

The operation voltage (V0) calculation formula is shown below:(RR comes from Regulation Ratio, EV comes from EV[5:0])

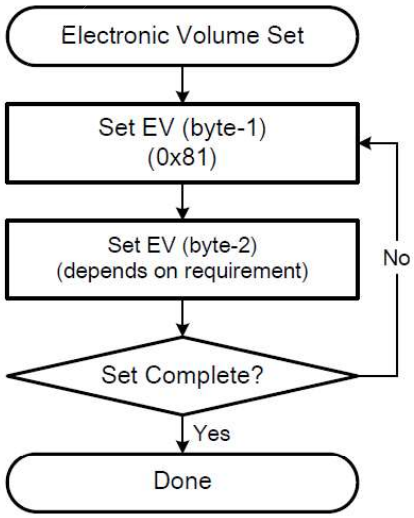
V0=RR×[1-(63-EV)/162]×2.1, or V0=RR×[(99+EV)/162]×2.1

Symbol	Register	Value
RR	RR2~RR0	3.0,3.5,4.0,4.5,5.0,5.5,6.0 and 6.5
EV	EV5~RV0	0~63

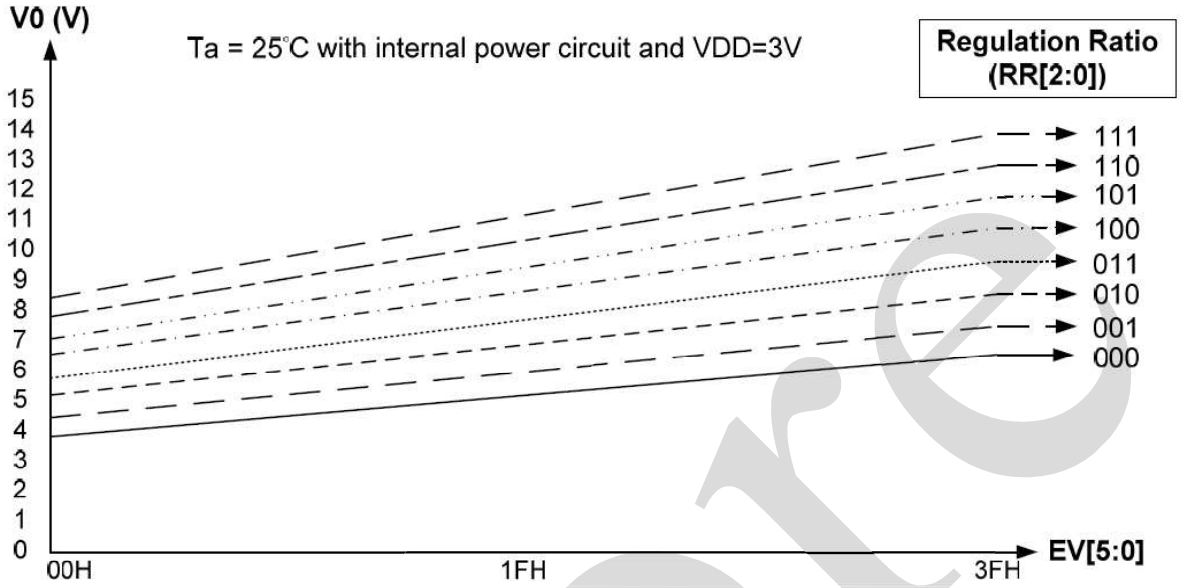
- **Set EV**

This is double byte instruction. The first byte set AiP31565CR into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0



The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment. Please refer to the "Selection of Application Voltage" section for detailed information.



- **Power Save Mode Set**

This is double byte instruction to set power save mode. This instruction used to set mode of power save only. AiP31565CR can not enter sleep mode after this instruction is executed.

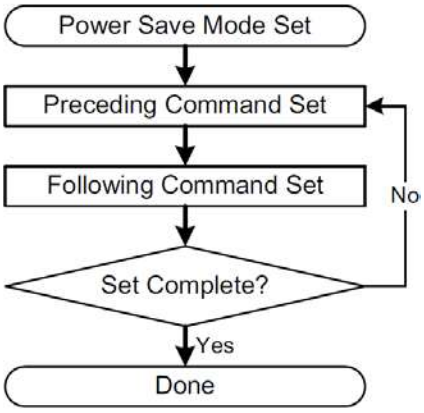
A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	0	MD
0	0	0	0	0	0	0	0	0	0

Flag	Description
MD	MD=0: Sleep Mode MD=1: Normal Mode

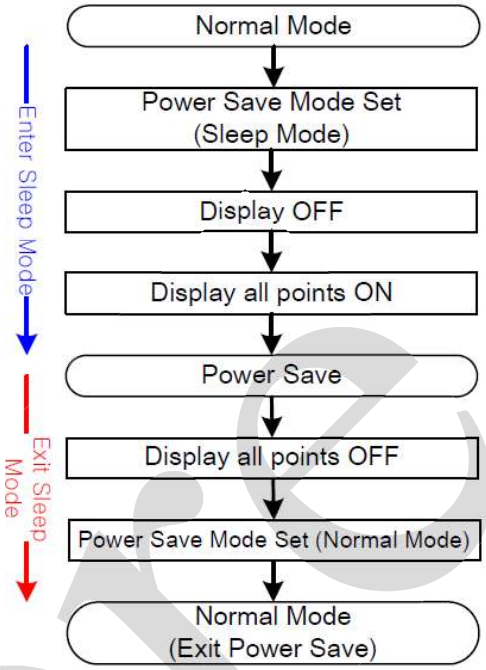
- **Power Save (Compound Instruction)**

This is compound instruction. The 1st instruction is Display OFF (D=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.



Power Save Mode Set Procedure



Power Save Procedure

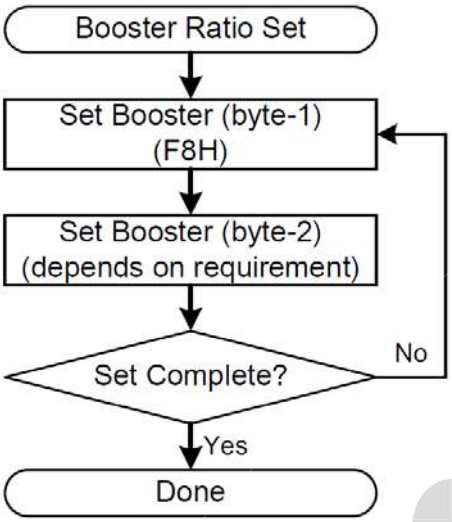
After exiting Power Save, the settings will return to be as they were before.

- **Set Booster**

This is double byte instruction. The first byte set AiP31565CR into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. Hardware connection should be changed according to booster level setting. If the hardware connection and software setting is not corresponding, AiP31565CR will cause extra power consumption. AiP31565CR will not damage through the extra power consumption.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	BL1	BL0

BL1	BL0	Boost Level
0	0	×2,×3,×4
0	1	×5
1	1	×6



- **NOP**

"No Operation" instruction. AiP31565CR will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

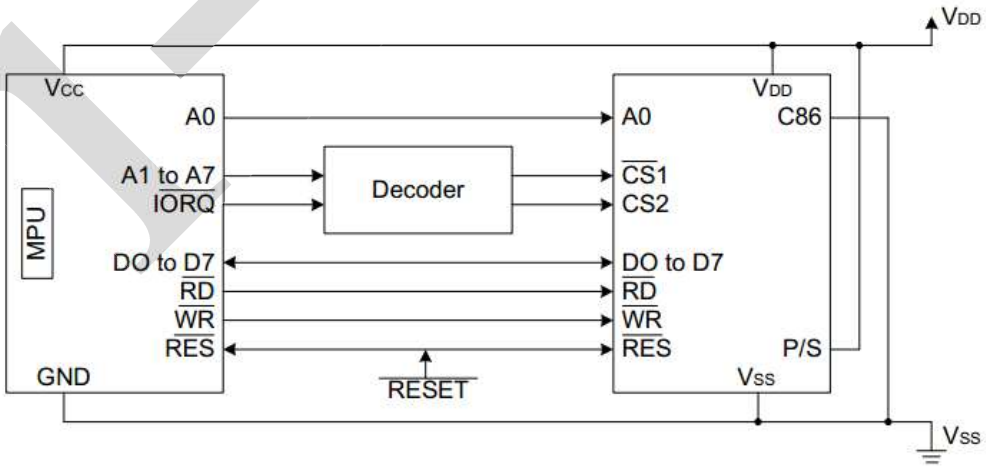
- **Test**

The test mode is reserved for IC testing. Please don't use this instruction. If the test mode is enabled accidentally, it can be cleared by: issuing an "L" pulse on /RES pin, issuing RESET instruction or issuing NOP instruction.

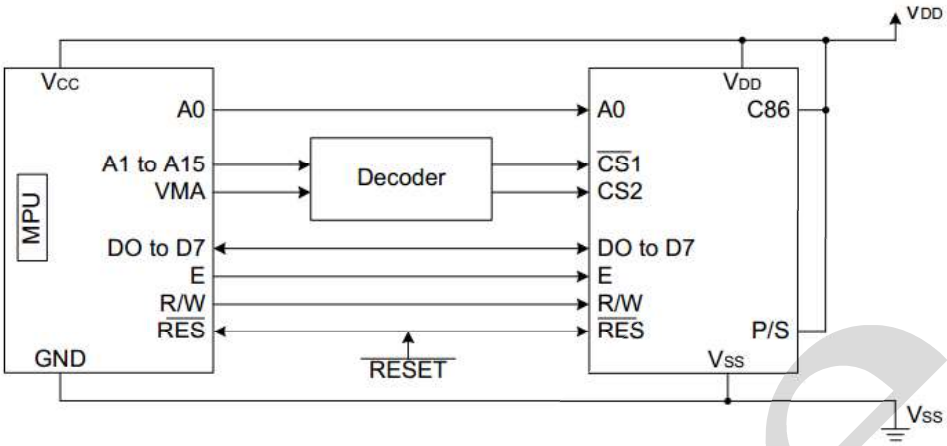
A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	-	-	-	-

Note: "-" means "1" or "0".

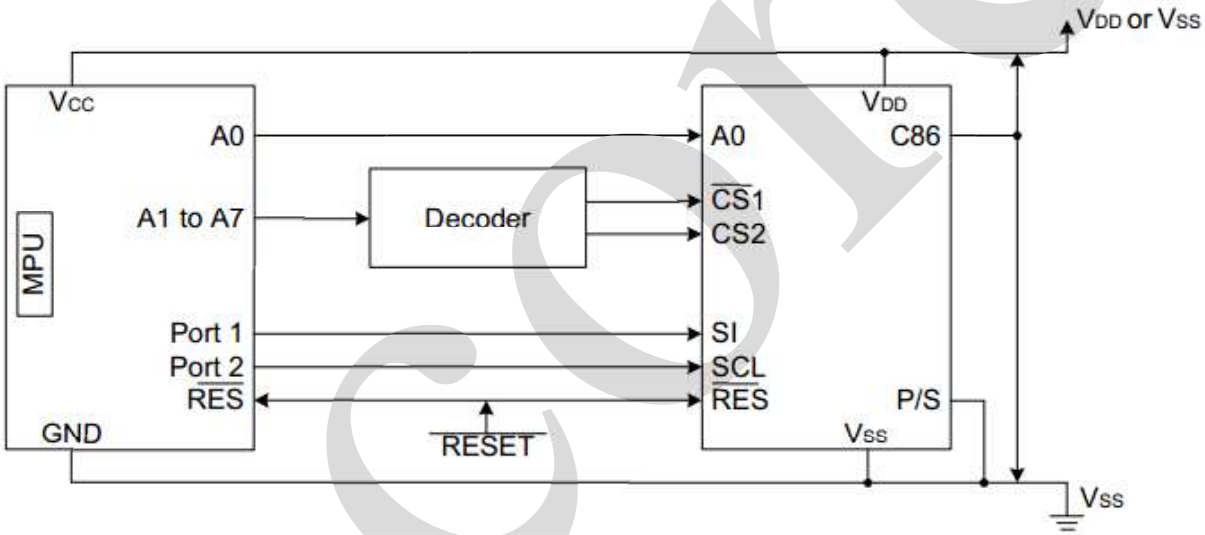
5.10、The MPU Interface



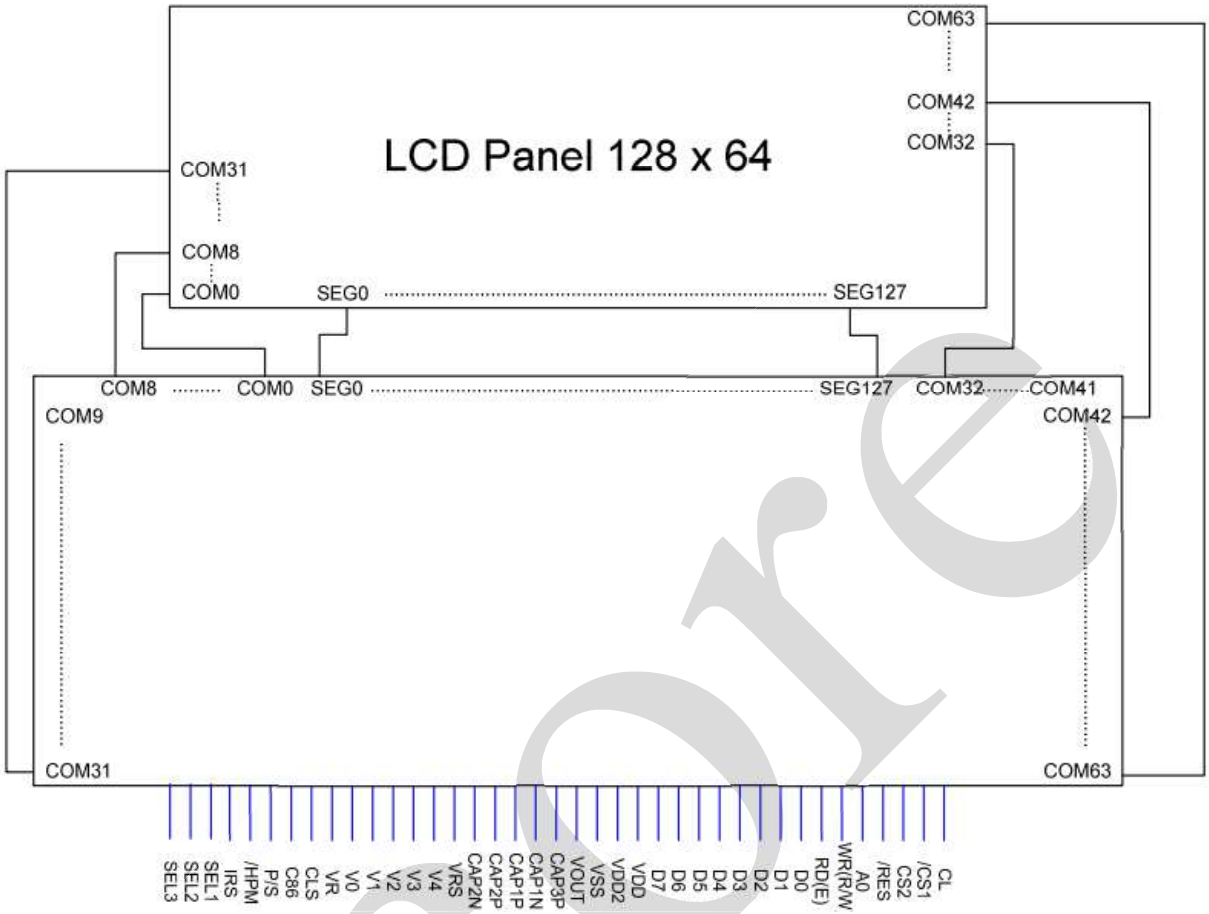
8080 Series MPUs



6800 Series MPUs



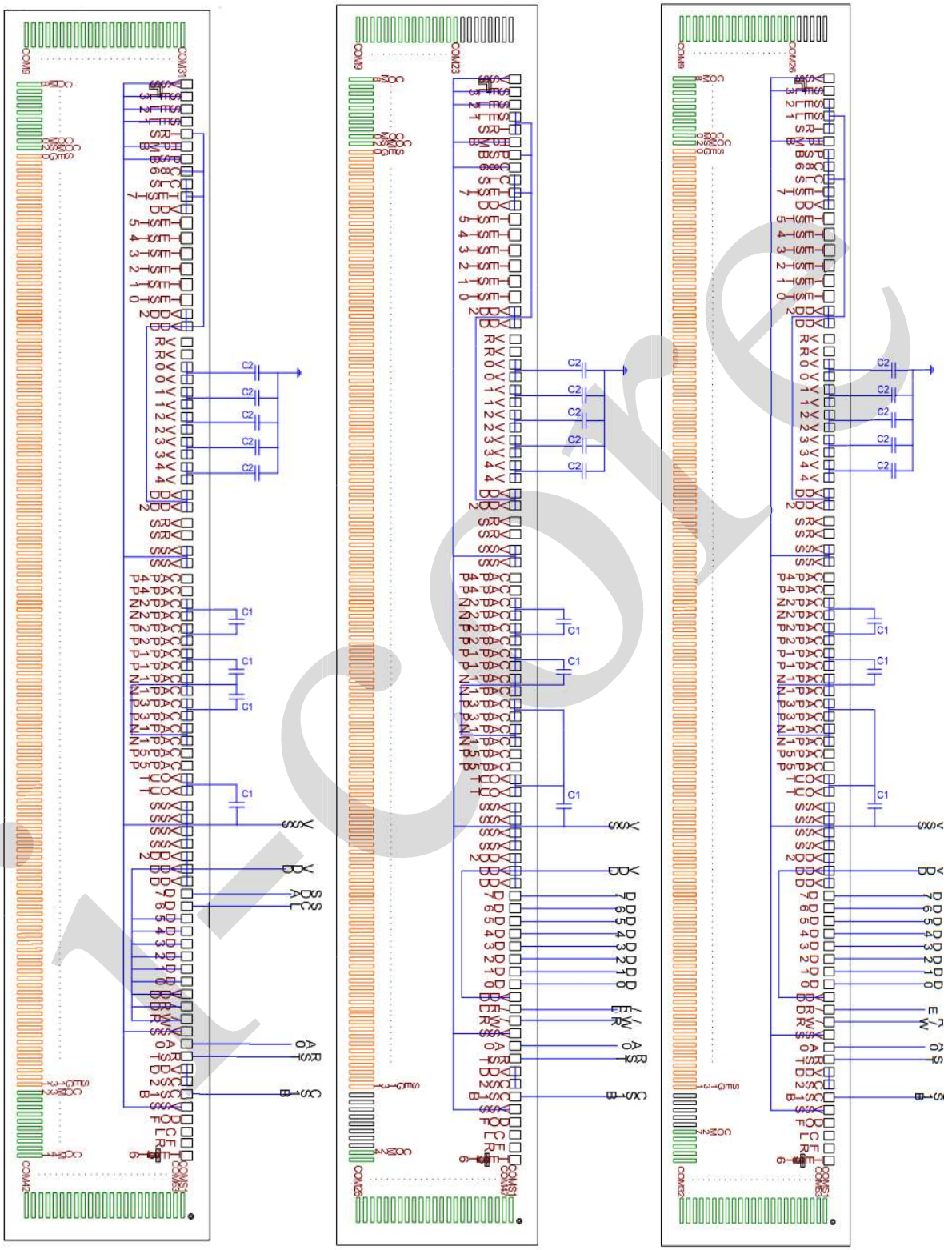
Using the 4-line SPI Interface



Connections Between LCD Drivers

6、Typical Application Circuit And Application Note

6.1、Application Circuits



4-line interface **8080 interface** **6800 interface**

7、Recommend LCD Setting

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 5.5~6.7V
Duty = 1/33

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/5
Vop = 5.0~6.1V
Duty = 1/33

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting 1:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 6.0~7.0V
Duty = 1/49

Recommend Setting 2:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/8
Vop = 7.0~8.5V
Duty = 1/49

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting 1:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 6.0~7.5V
Duty = 1/55

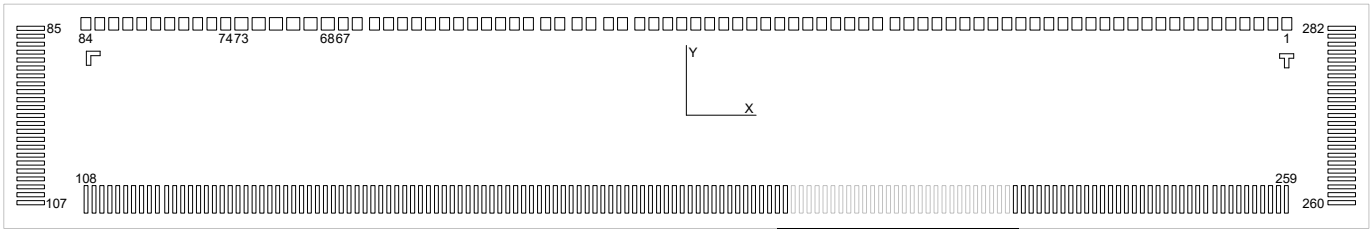
Recommend Setting 2:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/8
Vop = 7.0~8.5V
Duty = 1/55

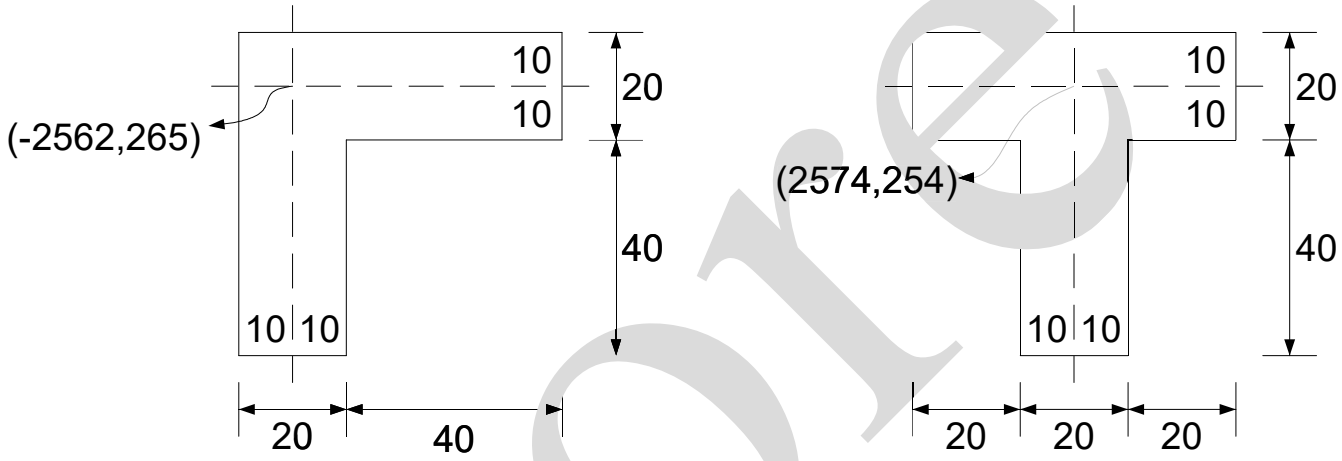
Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/7
Vop = 7.0~8.5V
Duty = 1/65

8、PAD Diagram And PAD Location

8.1、PAD Diagram





单位：um

PAD Size：

PAD NO.	PAD Size
001~067	42um×54um
068~073	56um×54um
074~084	42um×54um
085~282	17um×118um

Bump Pitch：34um（Min.）

Bump Height：9um

Chip Thickness：480um

Chip Size：5852um×962um

8.2、PAD Location

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	TEST[6]	2575	392	**142**	SEG[24]	-1411	-360
2	FR	2515	392	**143**	SEG[25]	-1377	-360

3	CL	2455	392	**144**	SEG[26]	-1343	-360
4	/DOF	2395	392	**145**	SEG[27]	-1309	-360
5	VSS	2335	392	**146**	SEG[28]	-1275	-360
6	$\overline{CS1}$	2275	392	**147**	SEG[29]	-1241	-360
7	CS2	2215	392	**148**	SEG[30]	-1207	-360
8	VDD	2155	392	**149**	SEG[31]	-1173	-360
9	/RES	2095	392	**150**	SEG[32]	-1139	-360
10	A0	2035	392	**151**	SEG[33]	-1105	-360
11	VSS	1975	392	**152**	SEG[34]	-1071	-360
12	/WR(R/W)	1915	392	**153**	SEG[35]	-1037	-360
13	/RD(E)	1855	392	**154**	SEG[36]	-1003	-360
14	VDD	1795	392	**155**	SEG[37]	-969	-360
15	D0	1735	392	**156**	SEG[38]	-935	-360
16	D1	1675	392	**157**	SEG[39]	-901	-360
17	D2	1615	392	**158**	SEG[40]	-867	-360
18	D3	1555	392	**159**	SEG[41]	-833	-360
19	D4	1495	392	**160**	SEG[42]	-799	-360
20	D5	1435	392	**161**	SEG[43]	-765	-360
21	D6	1375	392	**162**	SEG[44]	-731	-360
22	D7	1315	392	**163**	SEG[45]	-697	-360
23	VDD	1255	392	**164**	SEG[46]	-663	-360
24	VDD2	1195	392	**165**	SEG[47]	-629	-360
25	VDD2	1135	392	**166**	SEG[48]	-595	-360
26	VSS	1075	392	**167**	SEG[49]	-561	-360
27	VSS	1015	392	**168**	SEG[50]	-527	-360
28	VSS	955	392	**169**	SEG[51]	-493	-360
29	VSS	895	392	**170**	SEG[52]	-459	-360
30	VOUT	821	392	**171**	SEG[53]	-425	-360
31	VOUT	761	392	**172**	SEG[54]	-391	-360
32	CAP5P	701	392	**173**	SEG[55]	-357	-360
33	CAP5P	641	392	**174**	SEG[56]	-323	-360
34	CAP1N	581	392	**175**	SEG[57]	-289	-360
35	CAP1N	521	392	**176**	SEG[58]	-255	-360
36	CAP3P	461	392	**177**	SEG[59]	-221	-360
37	CAP3P	401	392	**178**	SEG[60]	-187	-360
38	CAP1N	341	392	**179**	SEG[61]	-153	-360
39	CAP1N	281	392	**180**	SEG[62]	-119	-360
40	CAP1P	221	392	**181**	SEG[63]	-85	-360
41	CAP1P	161	392	**182**	SEG[64]	-51	-360
42	CAP2P	101	392	**183**	SEG[65]	-17	-360
43	CAP2P	41	392	**184**	SEG[66]	17	-360
44	CAP2N	-19	392	**185**	SEG[67]	51	-360

45	CAP2N	-79	392	**186**	SEG[68]	85	-360
46	CAP4P	-139	392	**187**	SEG[69]	119	-360
47	CAP4P	-199	392	**188**	SEG[70]	153	-360
48	VSS	-273	392	**189**	SEG[71]	187	-360
49	VSS	-333	392	**190**	SEG[72]	221	-360
50	VRS	-408	392	**191**	SEG[73]	255	-360
51	VRS	-468	392	**192**	SEG[74]	289	-360
52	VDD2	-542	392	**193**	SEG[75]	323	-360
53	VDD	-602	392	**194**	SEG[76]	357	-360
54	V4	-676	392	**195**	SEG[77]	391	-360
55	V4	-736	392	**196**	SEG[78]	425	-360
56	V3	-796	392	**197**	SEG[79]	459	-360
57	V3	-856	392	**198**	SEG[80]	493	-360
58	V2	-916	392	**199**	SEG[81]	527	-360
59	V2	-976	392	**200**	SEG[82]	561	-360
60	V1	-1036	392	**201**	SEG[83]	595	-360
61	V1	-1096	392	**202**	SEG[84]	629	-360
62	V0	-1156	392	**203**	SEG[85]	663	-360
63	V0	-1216	392	**204**	SEG[86]	697	-360
64	VR	-1276	392	**205**	SEG[87]	731	-360
65	VR	-1336	392	**206**	SEG[88]	765	-360
66	VDD	-1410	392	**207**	SEG[89]	799	-360
67	VDD2	-1470	392	**208**	SEG[90]	833	-360
68	TEST[0]	-1537	392	**209**	SEG[91]	867	-360
69	TEST[1]	-1611	392	**210**	SEG[92]	901	-360
70	TEST[2]	-1685	392	**211**	SEG[93]	935	-360
71	TEST[3]	-1759	392	**212**	SEG[94]	969	-360
72	TEST[4]	-1833	392	**213**	SEG[95]	1003	-360
73	TEST[5]	-1907	392	**214**	SEG[96]	1037	-360
74	VDD	-1974	392	**215**	SEG[97]	1071	-360
75	TEST[7]	-2034	392	**216**	SEG[98]	1105	-360
76	CLS	-2094	392	**217**	SEG[99]	1139	-360
77	C86	-2154	392	**218**	SEG[100]	1173	-360
78	P/S	-2214	392	**219**	SEG[101]	1207	-360
79	/HPM	-2274	392	**220**	SEG[102]	1241	-360
80	IRS	-2334	392	**221**	SEG[103]	1275	-360
81	SEL1	-2394	392	**222**	SEG[104]	1309	-360
82	SEL2	-2454	392	**223**	SEG[105]	1343	-360
83	SEL3	-2514	392	**224**	SEG[106]	1377	-360
84	VSS	-2574	392	**225**	SEG[107]	1411	-360
85	COM[31]	-2810	373	**226**	SEG[108]	1445	-360
86	COM[30]	-2810	339	**227**	SEG[109]	1479	-360

87	COM[29]	-2810	305	**228**	SEG[110]	1513	-360
88	COM[28]	-2810	271	**229**	SEG[111]	1547	-360
89	COM[27]	-2810	237	**230**	SEG[112]	1581	-360
90	COM[26]	-2810	203	**231**	SEG[113]	1615	-360
91	COM[25]	-2810	169	**232**	SEG[114]	1649	-360
92	COM[24]	-2810	135	**233**	SEG[115]	1683	-360
93	COM[23]	-2810	101	**234**	SEG[116]	1717	-360
94	COM[22]	-2810	67	**235**	SEG[117]	1751	-360
95	COM[21]	-2810	33	**236**	SEG[118]	1785	-360
96	COM[20]	-2810	-1	**237**	SEG[119]	1819	-360
97	COM[19]	-2810	-35	**238**	SEG[120]	1853	-360
98	COM[18]	-2810	-69	**239**	SEG[121]	1887	-360
99	COM[17]	-2810	-103	**240**	SEG[122]	1921	-360
100	COM[16]	-2810	-137	**241**	SEG[123]	1955	-360
101	COM[15]	-2810	-171	**242**	SEG[124]	1989	-360
102	COM[14]	-2810	-205	**243**	SEG[125]	2023	-360
103	COM[13]	-2810	-239	**244**	SEG[126]	2057	-360
104	COM[12]	-2810	-273	**245**	SEG[127]	2091	-360
105	COM[11]	-2810	-307	**246**	SEG[128]	2125	-360
106	COM[10]	-2810	-341	**247**	SEG[129]	2159	-360
107	COM[9]	-2810	-375	**248**	SEG[130]	2193	-360
108	COM[8]	-2573	-360	**249**	SEG[131]	2227	-360
109	COM[7]	-2539	-360	**250**	COM[32]	2267	-360
110	COM[6]	-2505	-360	**251**	COM[33]	2301	-360
111	COM[5]	-2471	-360	**252**	COM[34]	2335	-360
112	COM[4]	-2437	-360	**253**	COM[35]	2369	-360
113	COM[3]	-2403	-360	**254**	COM[36]	2403	-360
114	COM[2]	-2369	-360	**255**	COM[37]	2437	-360
115	COM[1]	-2335	-360	**256**	COM[38]	2471	-360
116	COM[0]	-2301	-360	**257**	COM[39]	2505	-360
117	COMS2	-2267	-360	**258**	COM[40]	2539	-360
118	SEG[0]	-2227	-360	**259**	COM[41]	2573	-360
119	SEG[1]	-2193	-360	**260**	COM[42]	2810	-375
120	SEG[2]	-2159	-360	**261**	COM[43]	2810	-341
121	SEG[3]	-2125	-360	**262**	COM[44]	2810	-307
122	SEG[4]	-2091	-360	**263**	COM[45]	2810	-273
123	SEG[5]	-2057	-360	**264**	COM[46]	2810	-239
124	SEG[6]	-2023	-360	**265**	COM[47]	2810	-205
125	SEG[7]	-1989	-360	**266**	COM[48]	2810	-171
126	SEG[8]	-1955	-360	**267**	COM[49]	2810	-137
127	SEG[9]	-1921	-360	**268**	COM[50]	2810	-103
128	SEG[10]	-1887	-360	**269**	COM[51]	2810	-69

129	SEG[11]	-1853	-360	**270**	COM[52]	2810	-35
130	SEG[12]	-1819	-360	**271**	COM[53]	2810	-1
131	SEG[13]	-1785	-360	**272**	COM[54]	2810	33
132	SEG[14]	-1751	-360	**273**	COM[55]	2810	67
133	SEG[15]	-1717	-360	**274**	COM[56]	2810	101
134	SEG[16]	-1683	-360	**275**	COM[57]	2810	135
135	SEG[17]	-1649	-360	**276**	COM[58]	2810	169
136	SEG[18]	-1615	-360	**277**	COM[59]	2810	203
137	SEG[19]	-1581	-360	**278**	COM[60]	2810	237
138	SEG[20]	-1547	-360	**279**	COM[61]	2810	271
139	SEG[21]	-1513	-360	**280**	COM[62]	2810	305
140	SEG[22]	-1479	-360	**281**	COM[63]	2810	339
141	SEG[23]	-1445	-360	**282**	COMS1	2810	373

Unit:um

9、Statements And Notes

9.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。									

9.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.