AiP31567
132 SEG/65 COM Dot Matrix LCD Controller/Driver

Product Specification

Specification Revision History ：

Version	Data	Description
2016-10-A1	2016-10	New-made

1、General Description

AiP31567 is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. AiP31567 can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4). Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 65x132 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. AiP31567 contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, AiP31567 generates LCD driving signal without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

Features:

- Single-chip LCD Controller & Driver
- On-chip Display Data RAM (DDRAM)
  - Capacity: 65x132=8580 bits
  - Directly display RAM pattern from DDRAM
- Selectable Display Duty (by SEL2 & SEL1)
  - 1/65 duty(00) : 65 common x 132 segment
  - 1/55 duty (11): 55 common x 132 segment
  - 1/49 duty (01): 49 common x 132 segment
  - 1/33 duty(10) : 33 common x 132 segment
- Microprocessor Interface
  - Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
  - Serial interface (SPI-4) is also supported (write only)
- Abundant Functions
  - Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction, Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).
- External Hardware Reset Pin (RSTB)
- Built-in Oscillation Circuit
  - No external component required
- Low Power Consumption Analog Circuit
  - Voltage Booster (4X, 5X)
  - High-accuracy Voltage Regulator for LCD V_{OP}:
  - Voltage Follower for LCD Bias Voltage
- Wide Operation Voltage Range
  - VDD1-VSS1=1.8V~3.3V (+/-5%)
  - VDD2-VSS2=2.4V~3.3V (+5%)
  - VDD3-VSS3=2.4V~3.3V (+5%)
- Temperature Range: -30~85℃
- Chip proportion: 4840um*660um
- Package Type: COG

2、Block Diagram And Pin Description

2.1、Block Diagram

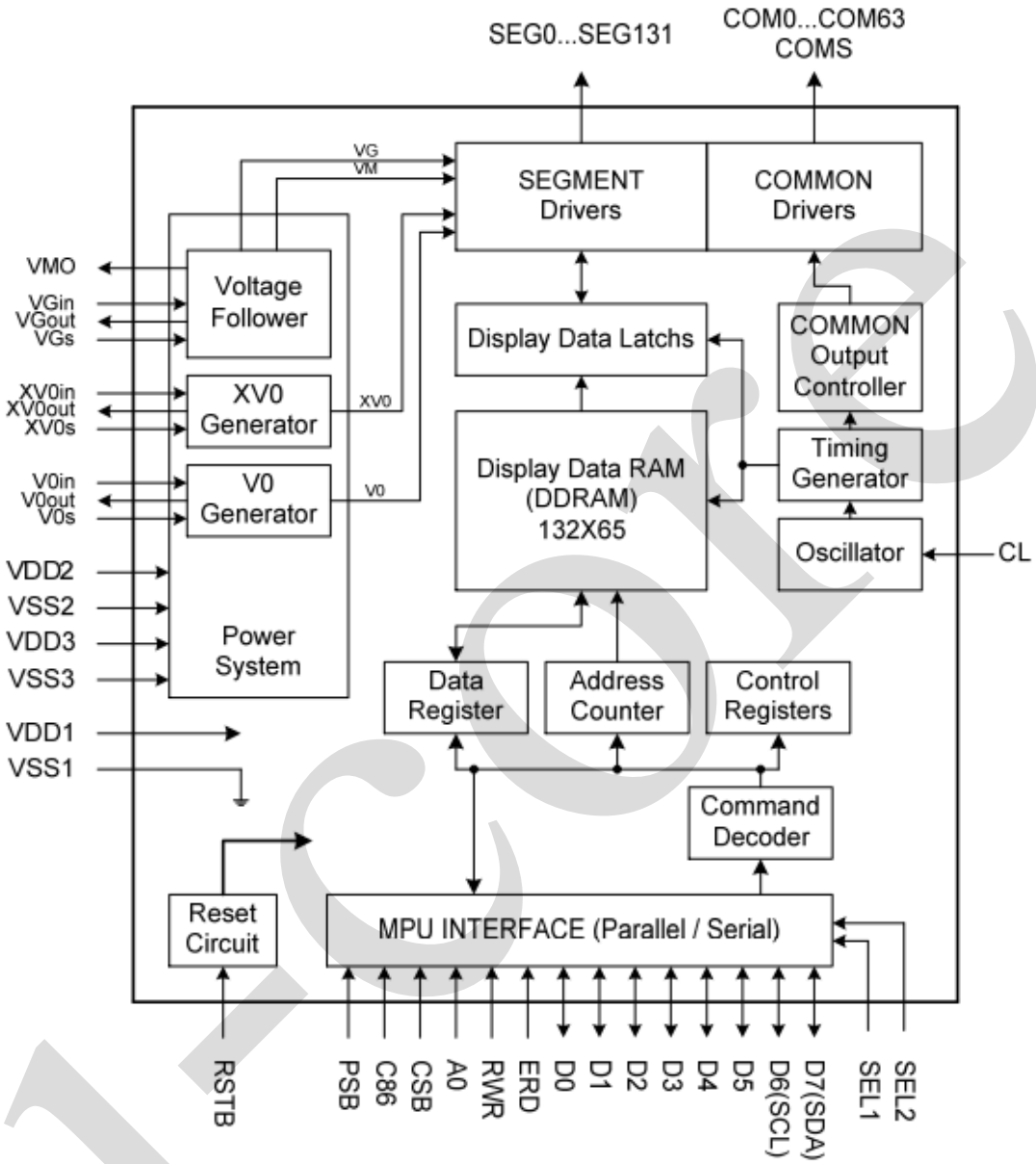
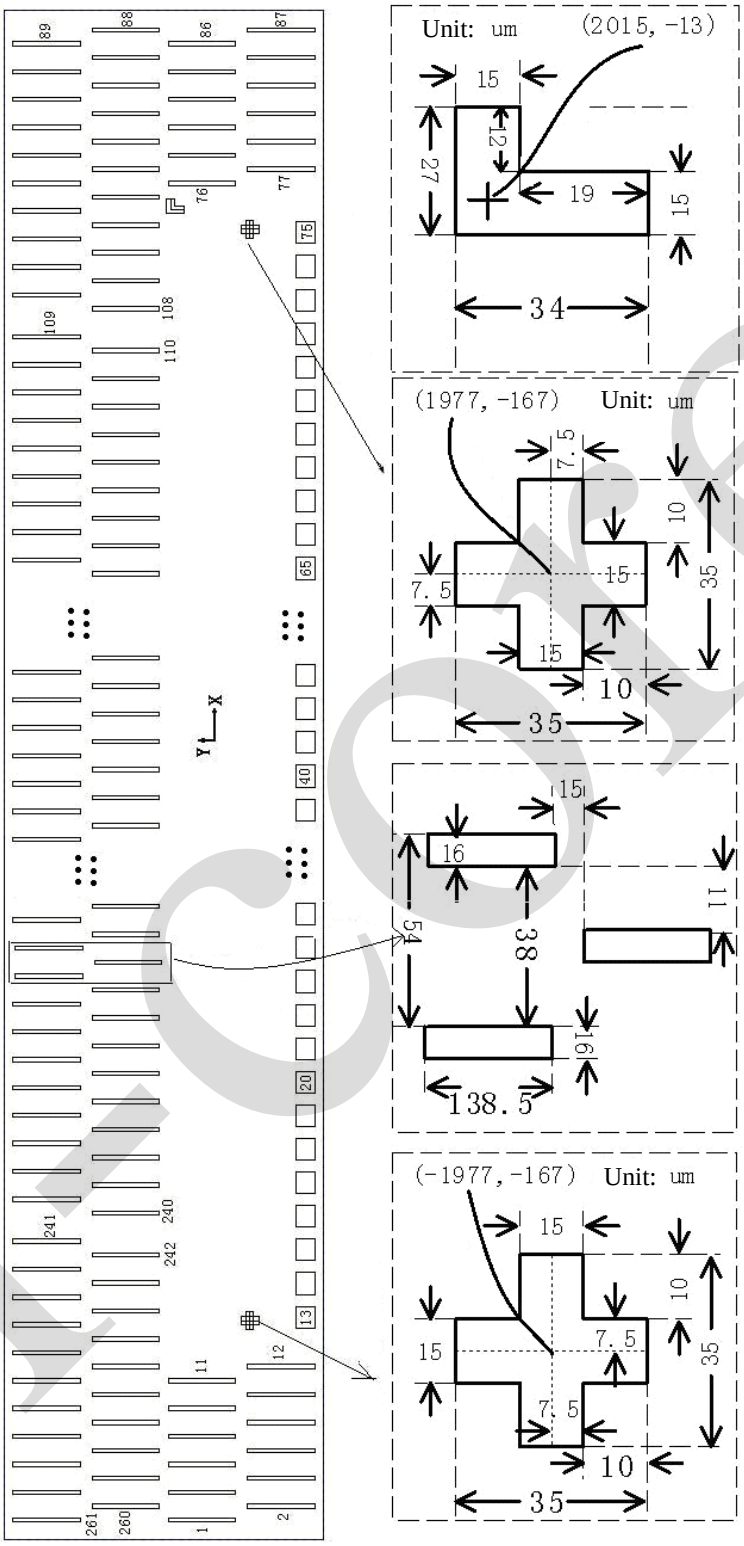


Fig1. Block Diagram

2.2、PAD Configurations



Chip Size: 4840*600 Bump Height: 15 Unit: μm

Fig2. PAD Location

Part Number	Chip Thickness
AiP31567	300
Bump Size	
PAD NO.	Size
1~12，76~261	16*138.5
13~55，65~75	50*45
56~64	45*45
Bump Space（minimum）	
PAD NO.	Space
1~12，76~87，88~108，109~240，241~261	Refer to Fig 2
13~55，65~75	15
56~64	10
55~56，64~65	12.5

2.3、PAD Location

PAD NO.	PIN Name	X	Y	PAD.NO	PIN Name	X	Y
1	COM[53]	-2363	-74.25	132	SEG[23]	1147.5	74.25
2	COM[54]	-2336	-227.75	133	SEG[24]	1120.5	227.75
3	COM[55]	-2309	-74.25	134	SEG[25]	1093.5	74.25
4	COM[56]	-2282	-227.75	135	SEG[26]	1066.5	227.75
5	COM[57]	-2255	-74.25	136	SEG[27]	1039.5	74.25
6	COM[58]	-2228	-227.75	137	SEG[28]	1012.5	227.75
7	COM[59]	-2201	-74.25	138	SEG[29]	985.5	74.25
8	COM[60]	-2174	-227.75	139	SEG[30]	958.5	227.75
9	COM[61]	-2147	-74.25	140	SEG[31]	931.5	74.25
10	COM[62]	-2120	-227.75	141	SEG[32]	904.5	227.75
11	COM[63]	-2093	-74.25	142	SEG[33]	877.5	74.25
12	COMS1	-2066	-227.75	143	SEG[34]	850.5	227.75
13	CL	-1970	-274.5	144	SEG[35]	823.5	74.25
14	CSB	-1905	-274.5	145	SEG[36]	796.5	227.75
15	RSTB	-1840	-274.5	146	SEG[37]	769.5	74.25
16	A0	-1775	-274.5	147	SEG[38]	742.5	227.75
17	RWR	-1710	-274.5	148	SEG[39]	715.5	74.25
18	ERD	-1645	-274.5	149	SEG[40]	688.5	227.75
19	VDDH	-1580	-274.5	150	SEG[41]	661.5	74.25
20	D0	-1515	-274.5	151	SEG[42]	634.5	227.75
21	D1	-1450	-274.5	152	SEG[43]	607.5	74.25
22	D2	-1385	-274.5	153	SEG[44]	580.5	227.75

23	D3	-1320	-274.5	154	SEG[45]	553.5	74.25
24	D4	-1255	-274.5	155	SEG[46]	526.5	227.75
25	D5	-1190	-274.5	156	SEG[47]	499.5	74.25
26	D6	-1125	-274.5	157	SEG[48]	472.5	227.75
27	D7	-1060	-274.5	158	SEG[49]	445.5	74.25
28	VDD1	-995	-274.5	159	SEG[50]	418.5	227.75
29	VDD1	-930	-274.5	160	SEG[51]	391.5	74.25
30	VDD2	-865	-274.5	161	SEG[52]	364.5	227.75
31	VDD2	-800	-274.5	162	SEG[53]	337.5	74.25
32	VDD2	-735	-274.5	163	SEG[54]	310.5	227.75
33	VDD3	-670	-274.5	164	SEG[55]	283.5	74.25
34	VSS1	-605	-274.5	165	SEG[56]	256.5	227.75
35	VSS1	-540	-274.5	166	SEG[57]	229.5	74.25
36	VSS3	-475	-274.5	167	SEG[58]	202.5	227.75
37	VSS2	-410	-274.5	168	SEG[59]	175.5	74.25
38	VSS2	-345	-274.5	169	SEG[60]	148.5	227.75
39	VSS2	-280	-274.5	170	SEG[61]	121.5	74.25
40	V0in	-215	-274.5	171	SEG[62]	94.5	227.75
41	V0in	-150	-274.5	172	SEG[63]	67.5	74.25
42	V0s	-85	-274.5	173	SEG[64]	40.5	227.75
43	V0out	-20	-274.5	174	SEG[65]	13.5	74.25
44	V0out	45	-274.5	175	SEG[66]	-13.5	227.75
45	XV0out	110	-274.5	176	SEG[67]	-40.5	74.25
46	XV0out	175	-274.5	177	SEG[68]	-67.5	227.75
47	XV0s	240	-274.5	178	SEG[69]	-94.5	74.25
48	XV0in	305	-274.5	179	SEG[70]	-121.5	227.75
49	XV0in	370	-274.5	180	SEG[71]	-148.5	74.25
50	VMO	435	-274.5	181	SEG[72]	-175.5	227.75
51	VMO	500	-274.5	182	SEG[73]	-202.5	74.25
52	VGin	565	-274.5	183	SEG[74]	-229.5	227.75
53	VGin	630	-274.5	184	SEG[75]	-256.5	74.25
54	VGs	695	-274.5	185	SEG[76]	-283.5	227.75
55	VGout	760	-274.5	186	SEG[77]	-310.5	74.25
56	T[6]	820	-274.5	187	SEG[78]	-337.5	227.75
57	T[7]	875	-274.5	188	SEG[79]	-364.5	74.25
58	T[8]	930	-274.5	189	SEG[80]	-391.5	227.75
59	TFCOM	985	-274.5	190	SEG[81]	-418.5	74.25
60	T[1]	1040	-274.5	191	SEG[82]	-445.5	227.75

61	T[2]	1095	-274.5	192	SEG[83]	-472.5	74.25
62	T[3]	1150	-274.5	193	SEG[84]	-499.5	227.75
63	T[4]	1205	-274.5	194	SEG[85]	-526.5	74.25
64	T[5]	1260	-274.5	195	SEG[86]	-553.5	227.75
65	Vref	1320	-274.5	196	SEG[87]	-580.5	74.25
66	VSSL	1385	-274.5	197	SEG[88]	-607.5	227.75
67	VDDH	1450	-274.5	198	SEG[89]	-634.5	74.25
68	C86	1515	-274.5	199	SEG[90]	-661.5	227.75
69	PSB	1580	-274.5	200	SEG[91]	-688.5	74.25
70	SEL1	1645	-274.5	201	SEG[92]	-715.5	227.75
71	VSSL	1710	-274.5	202	SEG[93]	-742.5	74.25
72	SEL2	1775	-274.5	203	SEG[94]	-769.5	227.75
73	VDD1	1840	-274.5	204	SEG[95]	-796.5	74.25
74	VDD2	1905	-274.5	205	SEG[96]	-823.5	227.75
75	VDD3	1970	-274.5	206	SEG[97]	-850.5	74.25
76	COM[31]	2066	-74.25	207	SEG[98]	-877.5	227.75
77	COM[30]	2093	-227.75	208	SEG[99]	-904.5	74.25
78	COM[29]	2120	-74.25	209	SEG[100]	-931.5	227.75
79	COM[28]	2147	-227.75	210	SEG[101]	-958.5	74.25
80	COM[27]	2174	-74.25	211	SEG[102]	-985.5	227.75
81	COM[26]	2201	-227.75	212	SEG[103]	-1012.5	74.25
82	COM[25]	2228	-74.25	213	SEG[104]	-1039.5	227.75
83	COM[24]	2255	-227.75	214	SEG[105]	-1066.5	74.25
84	COM[23]	2282	-74.25	215	SEG[106]	-1093.5	227.75
85	COM[22]	2309	-227.75	216	SEG[107]	-1120.5	74.25
86	COM[21]	2336	-74.25	217	SEG[108]	-1147.5	227.75
87	COM[20]	2363	-227.75	218	SEG[109]	-1174.5	74.25
88	COM[19]	2363	74.25	219	SEG[110]	-1201.5	227.75
89	COM[18]	2336	227.75	220	SEG[111]	-1228.5	74.25
90	COM[17]	2309	74.25	221	SEG[112]	-1255.5	227.75
91	COM[16]	2282	227.75	222	SEG[113]	-1282.5	74.25
92	COM[15]	2255	74.25	223	SEG[114]	-1309.5	227.75
93	COM[14]	2228	227.75	224	SEG[115]	-1336.5	74.25
94	COM[13]	2201	74.25	225	SEG[116]	-1363.5	227.75
95	COM[12]	2174	227.75	226	SEG[117]	-1390.5	74.25
96	COM[11]	2147	74.25	227	SEG[118]	-1417.5	227.75
97	COM[10]	2120	227.75	228	SEG[119]	-1444.5	74.25
98	COM[9]	2093	74.25	229	SEG[120]	-1471.5	227.75

99	COM[8]	2066	227.75	230	SEG[121]	-1498.5	74.25
100	COM[7]	2039	74.25	231	SEG[122]	-1525.5	227.75
101	COM[6]	2012	227.75	232	SEG[123]	-1552.5	74.25
102	COM[5]	1985	74.25	233	SEG[124]	-1579.5	227.75
103	COM[4]	1958	227.75	234	SEG[125]	-1606.5	74.25
104	COM[3]	1931	74.25	235	SEG[126]	-1633.5	227.75
105	COM[2]	1904	227.75	236	SEG[127]	-1660.5	74.25
106	COM[1]	1877	74.25	237	SEG[128]	-1687.5	227.75
107	COM[0]	1850	227.75	238	SEG[129]	-1714.5	74.25
108	COMS2	1823	74.25	239	SEG[130]	-1741.5	227.75
109	SEG[0]	1768.5	227.75	240	SEG[131]	-1768.5	74.25
110	SEG[1]	1741.5	74.25	241	COM[32]	-1823	227.75
111	SEG[2]	1714.5	227.75	242	COM[33]	-1850	74.25
112	SEG[3]	1687.5	74.25	243	COM[34]	-1877	227.75
113	SEG[4]	1660.5	227.75	244	COM[35]	-1904	74.25
114	SEG[5]	1633.5	74.25	245	COM[36]	-1931	227.75
115	SEG[6]	1606.5	227.75	246	COM[37]	-1958	74.25
116	SEG[7]	1579.5	74.25	247	COM[38]	-1985	227.75
117	SEG[8]	1552.5	227.75	248	COM[39]	-2012	74.25
118	SEG[9]	1525.5	74.25	249	COM[40]	-2039	227.75
119	SEG[10]	1498.5	227.75	250	COM[41]	-2066	74.25
120	SEG[11]	1471.5	74.25	251	COM[42]	-2093	227.75
121	SEG[12]	1444.5	227.75	252	COM[43]	-2120	74.25
122	SEG[13]	1417.5	74.25	253	COM[44]	-2147	227.75
123	SEG[14]	1390.5	227.75	254	COM[45]	-2174	74.25
124	SEG[15]	1363.5	74.25	255	COM[46]	-2201	227.75
125	SEG[16]	1336.5	227.75	256	COM[47]	-2228	74.25
126	SEG[17]	1309.5	74.25	257	COM[48]	-2255	227.75
127	SEG[18]	1282.5	227.75	258	COM[49]	-2282	74.25
128	SEG[19]	1255.5	74.25	259	COM[50]	-2309	227.75
129	SEG[20]	1228.5	227.75	260	COM[51]	-2336	74.25
130	SEG[21]	1201.5	74.25	261	COM[52]	-2363	227.75
131	SEG[22]	1174.5	227.75				

NOTE: 1. Unit: μm

2. This is the default PAD Center Coordinate Table with 1/65 Duty. Other duty output mapping can be found in Section FUNCTION DESCRIPTION.

3. Tolerance: ±0.05μm.

2.4 、Pin Description

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">LCD Driver Output Pins（Note 1）</td></tr>
<tr><td>110～240</td><td>SEG0
～
SEG131</td><td>O</td><td>LCD SEG Driver Outputs
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">SEG Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>1～11
76～107
241～261</td><td>COM0
～
COM63</td><td>O</td><td>LCD COM Driver Outputs
The internal scanning signal and the frame control the output voltage
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>12、108</td><td>COMS1,
COMS2
（COMS
）</td><td>O</td><td>LCD common driver outputs for icons.
The output signals of these two pins are the same.
When icon feature is not used, these pins should be left open.</td></tr>
<tr><td colspan="4">Microprocessor Interface Pins</td></tr>
<tr><td>15</td><td>RSTB</td><td>I</td><td>Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized.</td></tr>
<tr><td>14</td><td>CSB</td><td>I</td><td>Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>16</td><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0="H”: Indicates that signals on D[7:0] are display data.
A0=“L”: Indicates that signals on D[7:0] are command.</td></tr>
<tr><td>17</td><td>RWR</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to “H” by VDD1 or VDDH.</td></tr>
<tr><td>18</td><td>ERD</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”
<table>
<tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td></td><td></td><td></td><td>“H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin. When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is not used in serial interface and should fix to “H” by VDD1 or VDDH</td></tr>
<tr><td rowspan="2">20～27</td><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I</td><td>When using serial interface: 4-LINE
D7=SDA : Serial data input.
D6=SCL : Serial clock input.
D[5:0] are not used and should connect to “H” by VDD1 or VDDH.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td colspan="4">Configuration Pins</td></tr>
<tr><td>19、67</td><td>VDDH</td><td>I</td><td>Logic “1” level for option pins which should connected to “H”.</td></tr>
<tr><td>66、71</td><td>VSSL</td><td>I</td><td>Logic “0” level for option pins which should connected to “L”</td></tr>
<tr><td>69</td><td>PSB</td><td>I</td><td>PSB selects the interface type: Serial or Parallel.</td></tr>
<tr><td>68</td><td>C86</td><td>I</td><td>C86 selects the microprocessor type in parallel interface mode
<table>
<tr><th>PSB</th><th>C86</th><th>Selected Interface</th></tr>
<tr><td>H</td><td>H</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>H</td><td>L</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>L</td><td>X</td><td>Serial 4-Line SPI Interface</td></tr>
</table></td></tr>
<tr><td>70、72</td><td>SEL[2:1]</td><td>I</td><td>These pins select the display duty and bias of AiP31567.
<table>
<tr><th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr>
<tr><td>L</td><td>L</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>H</td><td>L</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>H</td><td>H</td><td>1/55</td><td>1/8 or 1/6</td></tr>
</table></td></tr>
<tr><td colspan="4">Power System Pins</td></tr>
<tr><td>28、29、73</td><td>VDD1</td><td>P</td><td>Digital power. If VDD1=VDD2, connect to VDD2 externally</td></tr>
<tr><td>30、31、32、74</td><td>VDD2</td><td>P</td><td>Analog power. If VDD1=VDD2, connect to VDD1 externally</td></tr>
<tr><td>33、75</td><td>VDD3</td><td>P</td><td>Power for reference voltage circuit</td></tr>
<tr><td>34、35</td><td>VSS1</td><td>P</td><td>Digital ground. Connect to VSS2 externally</td></tr>
<tr><td>37、38、39</td><td>VSS2</td><td>P</td><td>Analog ground. Connect to VSS1 externally</td></tr>
<tr><td>36</td><td>VSS3</td><td>P</td><td>Ground for reference voltage circuit.</td></tr>
<tr><td>43、44
40、41
42</td><td>V0out
V0in
V0s</td><td>P</td><td>V0 is the LCD driving voltage for common circuits at negative frame.
V0out is the output of V0 regulator. V0s is the feedback of V0 regulator.
V0in is the V0 input of common circuits.
Be sure that: V0 ≥ VG > VM > VSS ≥ XV0 (under operation).</td></tr>
</table>

			V0out, V0in & V0s should be separated in ITO layout. V0out, V0in & V0s should be connected together in FPC layout.
45、46 48、49 47	XV0out XV0in XV0s	P	XV0 is the LCD driving voltage for common circuits at positive frame. XV0out is the output of XV0 regulator. XV0s is the feedback of XV0 regulator. XV0in is the V0 input of common circuits. XV0out, XV0in & XV0s should be separated in ITO layout. XV0out, XV0in & XV0s should be connected together in FPC layout
55 52、53 54	VGout VGin VGs	P	VG is the LCD driving voltage for segment circuits. Vgout is the output of VG regulator. VGs is the feedback of VG regulator. Vgin is the VG input of segment circuits. Vgout, Vgin & VGs should be separated in ITO layout. Vgout, Vgin & VGs should be connected together in FPC layout. 1.6 ≤ VG < VDD2.
50、51	VMO	P	VM is the LCD driving voltage for common circuits. 0.8V ≤ VM < VDD2.
Test Pins			
65	Vref	T	Test pin for power system. This pin must be left open (without any kinds of connection).
56～58 60～64	T1~T8	T	Do NOT use. Reserved for testing. Must be floating.
59	TFCOM	T	Do NOT use. Reserved for testing. Must be floating
13	CL	T	Do NOT use. Reserved for testing. Must be floating.

Note: 1. After VDD1 is turned ON, any MPU interface pins cannot be left floating .

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Tamb=25℃, All voltage referenced to V_{SS}, unless otherwise specified)

Parameter	Symbol		Conditions	Unit
Digital Power Supply Voltage	VDD1		-0.3 ~ 3.6	V
Analog Power supply voltage	VDD2, VDD3		-0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0		-0.3 ~ 16	V
LCD Power supply voltage	VG		-0.3 ~ 3.6	V
LCD Power supply voltage	VM		-0.3 ~ VDD2	V
Input Voltage	Vi		-0.3 ~ VDD1+0.3	V
Operating temperature	T_{amb}		–30 to +85	℃
Storage temperature	T_{stg}		–55 to +125	℃

Note: Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation: VDD2 > VG > VM > VSS ≥ XV0

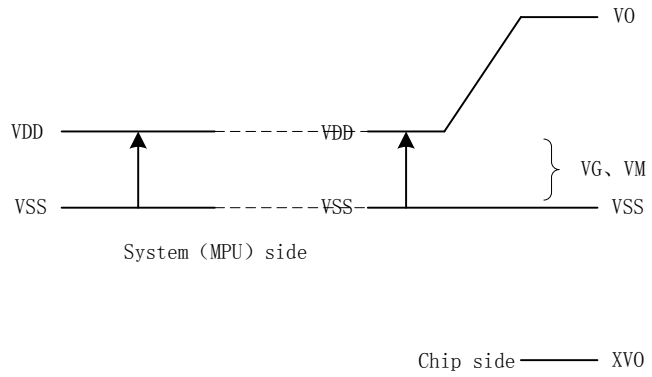


Fig3. Voltage relation

3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(Tamb=25□ C , VDD=2.5V, fosc=3.579545MHz, unless otherwise specified)

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.7	-	3.3	V	VDD1
Operating Voltage (2)	VDD2			2.4	-	3.3	V	VDD2
Operating Voltage (3)	VDD3			2.4	-	3.3	V	VDD3
Input High-level Voltage	V_{IHC}			0.7VDD1	-	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}			VSS1	-	0.3VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA,VDD1=1.8V		0.8VDD1	-	VDD1	V	D[7：0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA,VDD1=1.8V		VSS1	-	0.2VDD1	V	D[7：0]
Input Leakage Current	I_{LI}			-1.0	-	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}			-3.0	-	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	T_a=25℃	VOP=8.5V, ΔV=0.85V	-	0.6	0.8	KΩ	COMX
			VG=1.9V, ΔV=0.19V	-	1.3	1.5	KΩ	SEGX
Frame Frequency	FR	Duty=1/65, OP=8.5V, T_a=25℃		70	75	80	Hz	

3.2.2、DC Characteristics 2

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Pattern: SNOW(Static)	ISS	VDD1=VDD2=VDD3=3.0V，Booster X5 ，VOP= 8.5 V, Bias=1/9，Ta=25℃	-	150	300	μA
Display OFF	ISS	VDD1=VDD2=VDD3=3.0V，Booster X5 ，VOP= 8.5 V, Bias=1/9，Ta=25℃	-	95	190	μA
Power Down	ISS	VDD1=VDD2=VDD3=3.0V，Ta=25℃	-	8	16	μA

3.2.3、TIMING CHARACTERISTICS 1

System Bus Timing for 6800 Series MPU

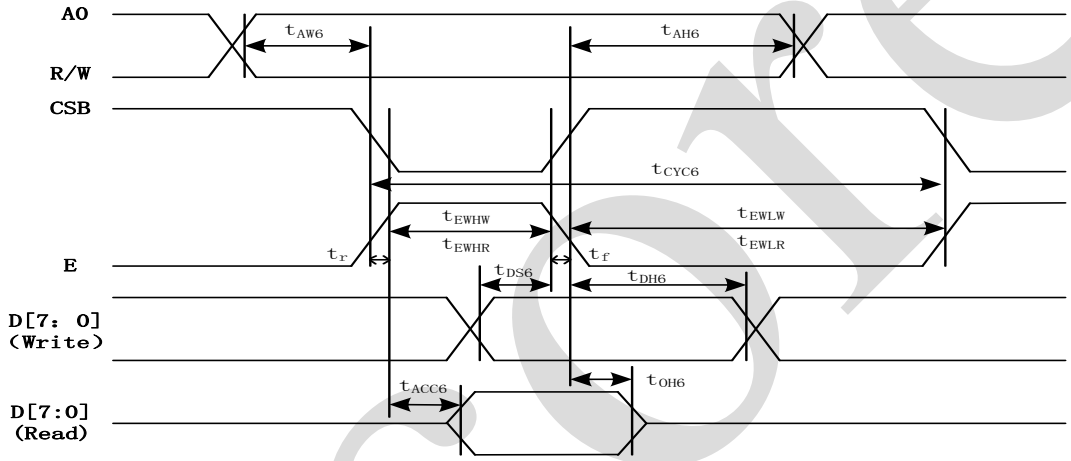


Fig4. Timing characteristics 1

(VDD1 = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW6}		0	—	ns
Address hold time		t_{AH6}		10	—	
System cycle time	E	t_{CYC6}		240	—	
Enable L pulse width (WRITE)		t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
.		t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
Write data setup time	D[7:0]	t_{DS6}		40	—	
Write data hold time		t_{DH6}		10	—	
Read data access time		t_{ACC6}	C_L = 16 pF	—	70	
Read data output disable time		t_{OH6}	C_L = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW6}		0	—	ns
Address hold time		t_{AH6}		0	—	
System cycle time	E	t_{CYC6}		400	—	
Enable L pulse width (WRITE)		t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)		t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
Write data setup time	D[7:0]	t_{DS6}		40	—	
Write data hold time		t_{DH6}		20	—	
Read data access time		t_{ACC6}	CL = 16 pF	—	140	
Read data output disable time		t_{OH6}	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW6}		0	—	ns
Address setup time		t_{AH6}		0	—	
System cycle time	E	t_{CYC6}		640	—	
Enable L pulse width (WRITE)		t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)		t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
Write data setup time	D[7:0]	t_{DS6}		80	—	
Write data hold time		t_{DH6}		20	—	
Read data access time		t_{ACC6}	C_L = 16 pF	—	240	
Read data output disable time		t_{OH6}	C_L = 16 pF	10	200	

Notes：

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – t_{EWLW} – t_{EWHW}) for (tr + tf) ≦ (tCYC6 – t_{EWLR} – t_{EWHR}) are specified.：(tr + tf) ≦ (tCYC6 – t_{EWLW} – t_{EWHW}) for (tr + tf) ≦ (tCYC6 – t_{EWLR} – t_{EWHR})。
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. t_{EWLW} and t_{EWLR} are specified as the overlap between CSB being “L” and E.

3.2.4、TIMING CHARACTERISTICS 2

System Bus Timing for 8080 Series MPU

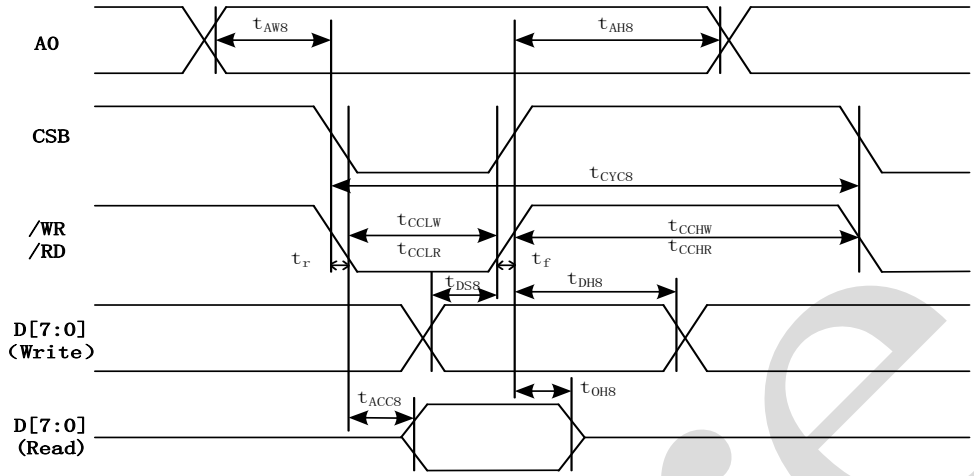


Fig5. Timing characteristics 2

(VDD1 = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		10	—	
System cycle time	/WR	t_{CYC8}		240	—	
/WR L pulse width (WRITE)		t_{CCLW}		80	—	
/WR H pulse width (WRITE)		t_{CCHW}		80	—	
/RD L pulse width (READ)	RD	t_{CCLR}		140	—	
/RD H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D[7:0]	t_{DS8}		40	—	
WRITE Data hold time		t_{DH8}		20	—	
WRITE Data hold time		t_{ACC8}	C_L = 16 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time	/WR	t_{CYC8}		400	—	
/WR L pulse width (WRITE)		t_{CCLW}		220	—	
/WR H pulse width (WRITE)		t_{CCHW}		180	—	
/RD L pulse width (READ)	RD	t_{CCLR}		220	—	
/RD H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D[7:0]	t_{DS8}		40	—	

WRITE Data hold time		t_{DH8}		20	—	
READ access time		t_{ACC8}	C_L = 16 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time	/WR	t_{CYC8}		640	—	
/WR L pulse width (WRITE)		t_{CCLW}		360	—	
/WR H pulse width (WRITE)		t_{CCHW}		280	—	
/RD L pulse width (READ)	RD	t_{CCLR}		360	—	
/RD H pulse width (READ)		t_{CCHR}		280	—	
WRITE Data setup time	D[7:0]	t_{DS8}		80	—	
WRITE Data hold time		t_{DH8}		20	—	
READ access time		t_{ACC8}	C_L = 16 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 16 pF	10	200	

Notes:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,: $(tr + tf) \leqq (tCYC8 - t_{CCLW} - t_{CCHW})$ for $(tr + tf) \leqq (tCYC8 - t_{CCLR} - t_{CCHR})$。
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

3.2.5、TIMING CHARACTERISTICS 3

System Bus Timing for 4-Line Serial Interface

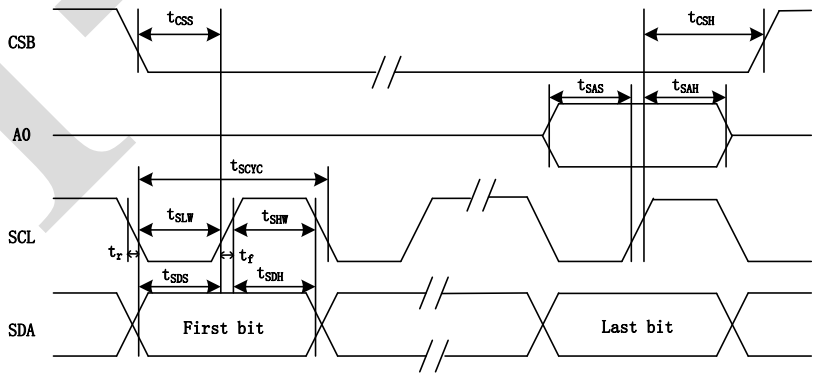


Fig6. Timing characteristics3

(VDD1 = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	t_{SCYC}		50	—	ns
SCLK “H” pulse width		t_{SHW}		25	—	
SCLK “L” pulse width		t_{SLW}		25	—	
Address setup time	A0	t_{SAS}		20	—	
Address hold time		t_{SAH}		10	—	
Data setup time	SDA	t_{SDS}		20	—	
Data hold time		t_{SDH}		10	—	
CSB-SCLK time	CSB	t_{CSS}		20	—	
CSB-SCLK time		t_{CSH}		40	—	

(VDD1 = 2.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	t_{SCYC}		100	—	ns
SCLK “H” pulse width		t_{SHW}		50	—	
SCLK “L” pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		30	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SDA	t_{SDS}		30	—	
Data hold time		t_{SDH}		20	—	
CSB-SCLK time	CSB	t_{CSS}		30	—	
CSB-SCLK time		t_{CSH}		60	—	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	t_{SCYC}		200	—	ns
SCLK “H” pulse width		t_{SHW}		80	—	
SCLK “L” pulse width		t_{SLW}		80	—	
Address setup time	A0	t_{SAS}		60	—	
Address hold time		t_{SAH}		30	—	
Data setup time	SDA	t_{SDS}		60	—	
Data hold time		t_{SDH}		30	—	
CSB-SCLK time	CSB	t_{CSS}		40	—	
CSB-SCLK time		t_{CSH}		100	—	

Notes：1、The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

2、All timing is specified using 20% and 80% of VDD1 as the standard.

3.2.6、TIMING CHARACTERISTICS 4

Hardware Reset Timing

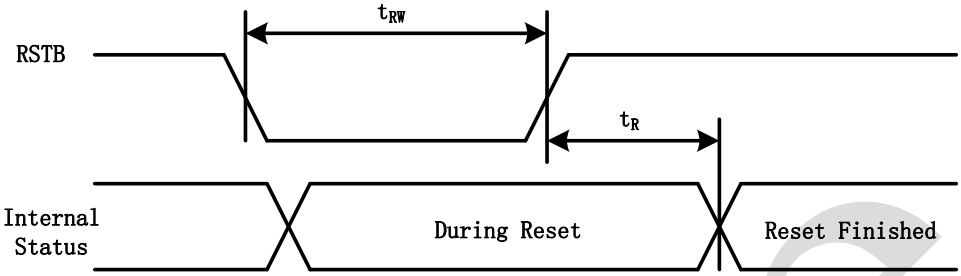


Fig7. Timing characteristics 4

(VDD1 = 3.3V , Ta =25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset “L” pulse width	tRW		1.0	—	

(VDD1 = 2.8V , Ta =25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0	—	

(VDD1 = 1.8V , Ta =25℃)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

4、Testing Circuit

4.1、MPU communicate

PSB	C86	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
H	H	CSB	A0	E	R/W	D[7:0]	6800- series parallel interface
H	L			/RD	/WR		8080- series parallel interface
L	×			--	--	Refer to serial interface	4 Line SPI interface

Note: 1.The un-used pins are marked as “---” and should be fixed to “H” by VDD1 or VDDH.
2. C86 is marked as “X” and can be fixed to “H” or “L”.

4.1.1、Data Transfer

AiP31567 uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig 8. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig 9. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

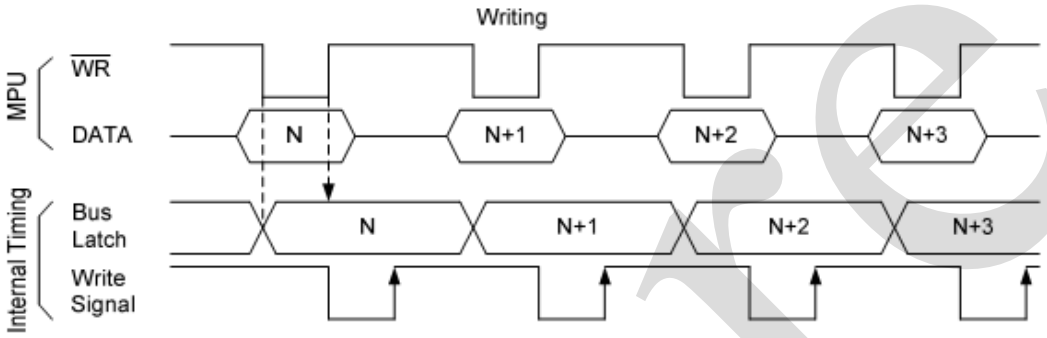


Fig8. Data Transfer: Write

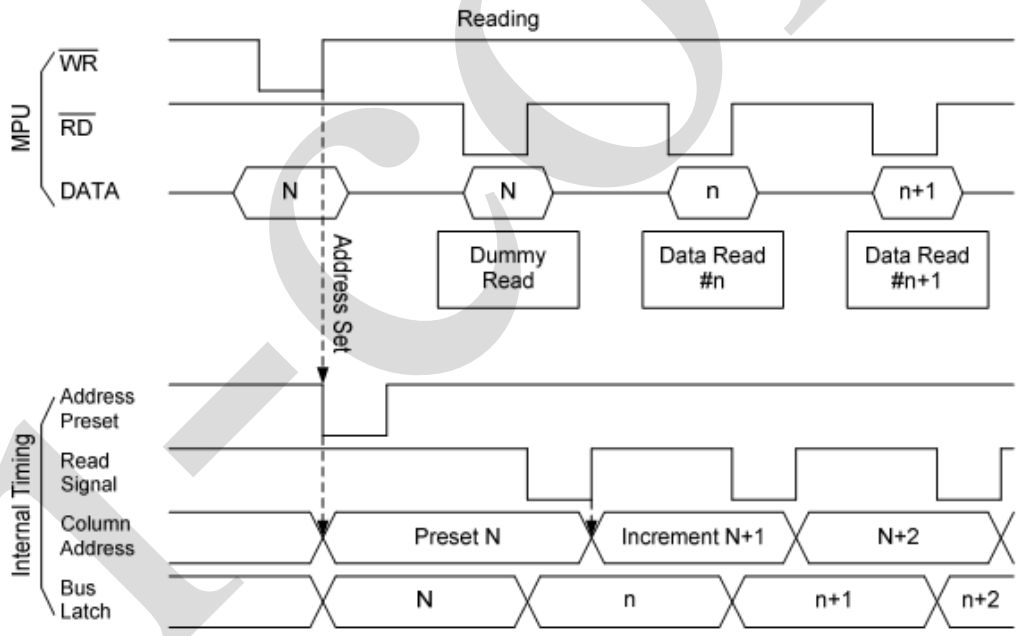


Fig9. Data Transfer: Read

4.2、External Components of Power Circuit

The recommended external power components need only 2 capacitors. The detailed values of these two capacitors are determined by the panel size and loading.

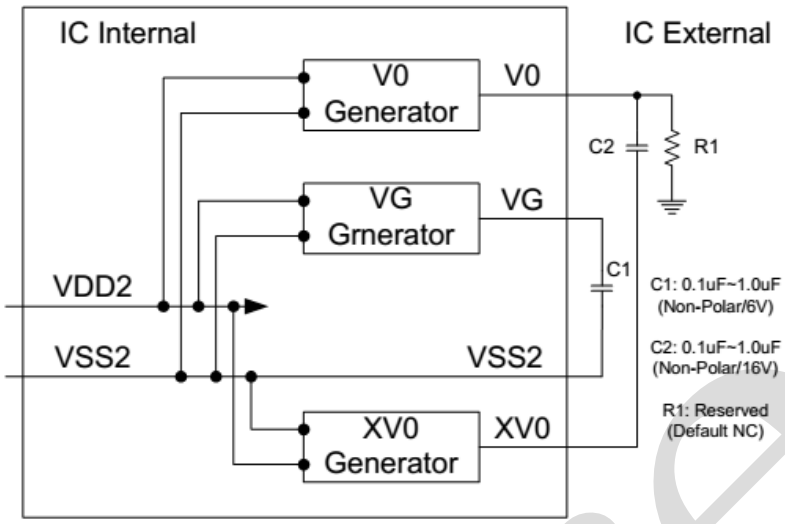


Fig10. Power Circuit

4.3、INSTRUCTION DESCRIPTION

4.3.1、INSTRUCTION TABLE

Num.	INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
				D7	D6	D5	D4	D3	D2	D1	D0	
1	Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
2	Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
3	Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
4	Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
		0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
5	Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
6	Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
7	Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
8	SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
9	Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
10	All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
11	Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)

12	Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0, Write:+1
13	END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
14	RESET	0	0	1	1	1	0	0	0	1	0	Software reset
15	COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
16	Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OF
17	Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
18	Set EV	0	0	1	0	0	0	0	0	0	1	Double command Set electronic volume (EV) level
		0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
19	Set Booster	0	0	1	1	1	1	1	0	0	0	Double command Set booster level: BL=0: 4X BL=1: 5X
		0	0	0	0	0	0	0	0	0	BL	
20	Power Save	0	0	复用指令								Display OFF + All Pixel ON
21	NOP	0	0	1	1	1	0	0	0	1	1	No operation
22	Test	0	0	1	1	1	1	1	1	1	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Symbol	Bias
V0	V0
VG	2/9×V0
VM	1/9×V0
VSS	VSS

Please Note:

VG range: 1.24V ≤ VG < VDD2.

VM range: 0.62V ≤ VM < VDD2.

4.3.2、Power Control

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VB	VR	VF

Flag	Description
VB	VB=0: Built-in Booster OFF VB=1: Built-in Booster ON
VR	VR=0: Built-in Regulator OFF VR=1: Built-in Regulator ON
VF	VF=0: Built-in Follower OFF VF=1: Built-in Follower ON

4.3.3、Regulation Ratio

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	RR2	RR1	RR0

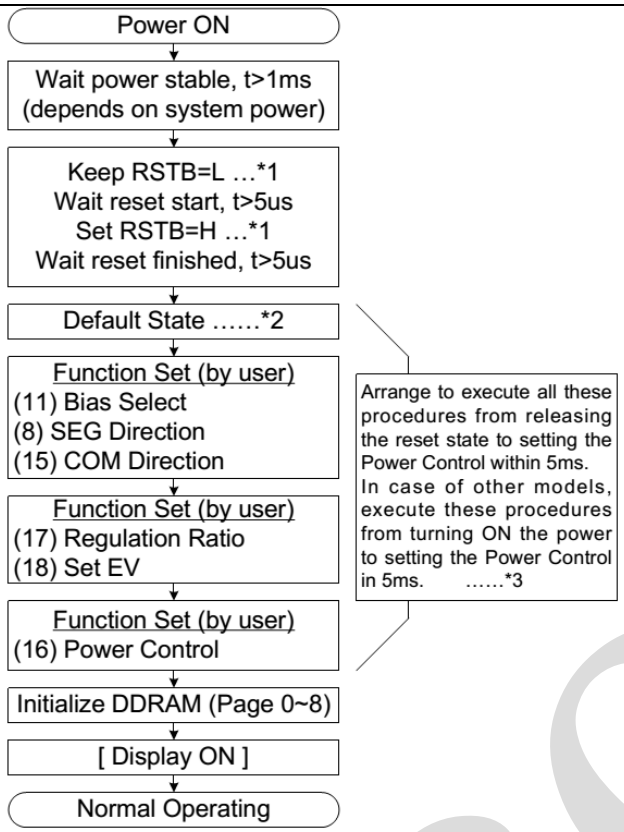
RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])

V0=RR*[1-(63-EV)/162]*2.1，or V0=RR*[(99+EV)/162]*2.1

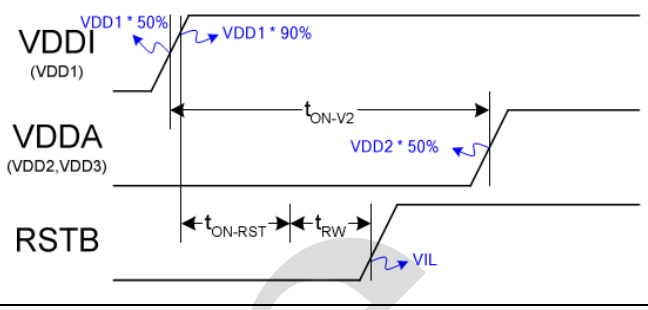
4.4、OPERATION FLOW

Referential Operation Flow

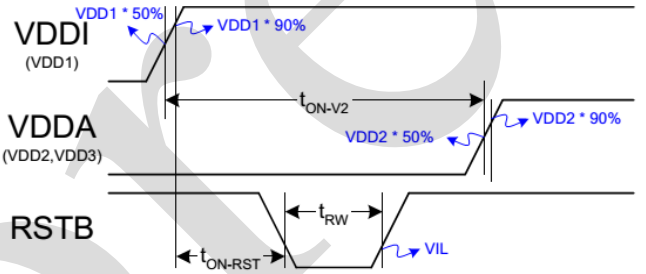


Operation Sequence

Case 1: RSTB=L while Power ON



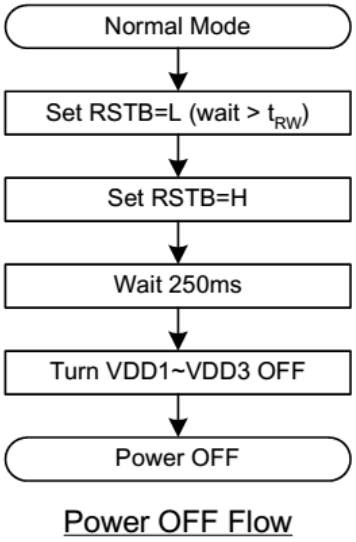
Case 2: RSTB=H while Power ON



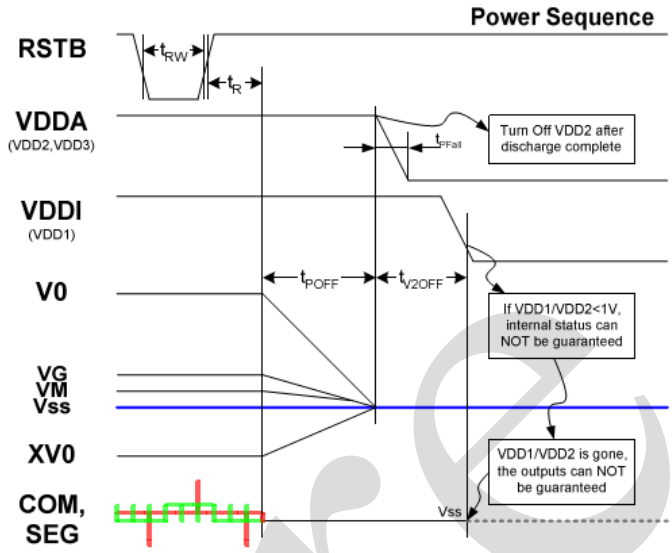
Note: The detailed description can be found in the respective sections listed below.

1. Please refer to the timing specification of t_{RW} and t_R.
2. Refer to Section 4.5.
3. The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.
4. The detailed instruction functionality is described in Section 4.3. INSTRUCTION DESCRIPTION;
5. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

4.5、Use Hardware Reset Function



Power OFF Flow



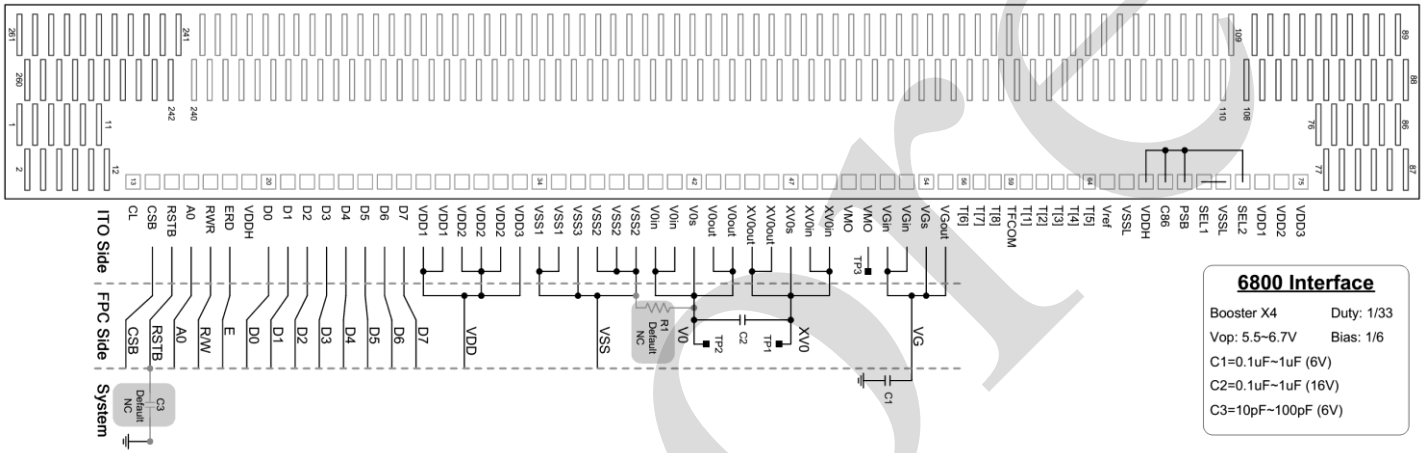
After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.

Note:

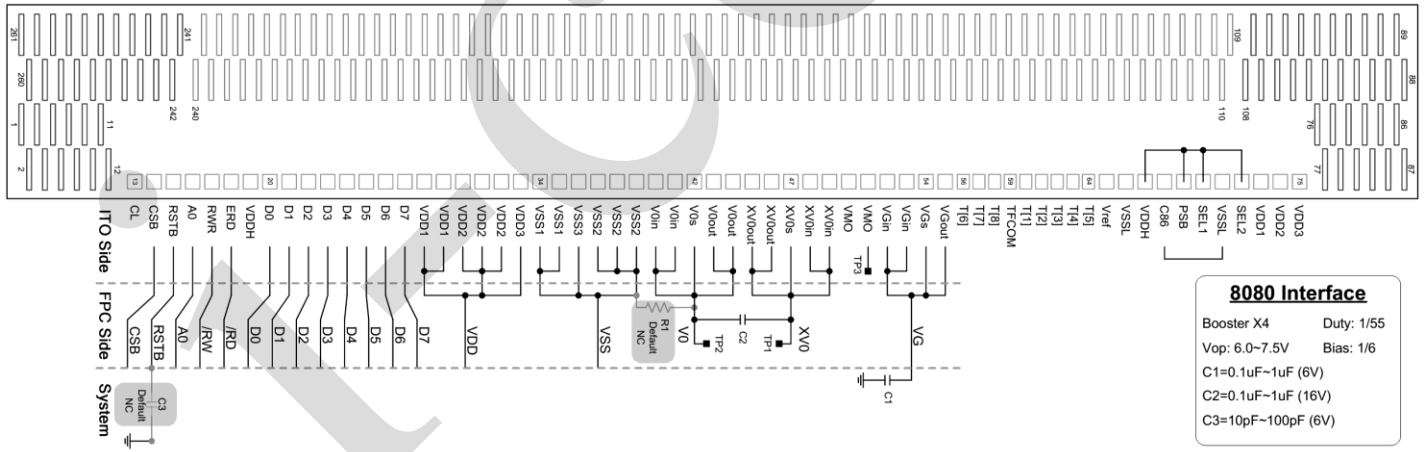
1. t_{POFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process may be stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4” with C1=1uF, C2=1uF.
7. When turning VDDA OFF, the falling time should follow the specification: 20ms ≤ t_{Pfall} ≤ 0.2sec

5、Typical Application Circuit And Application Note

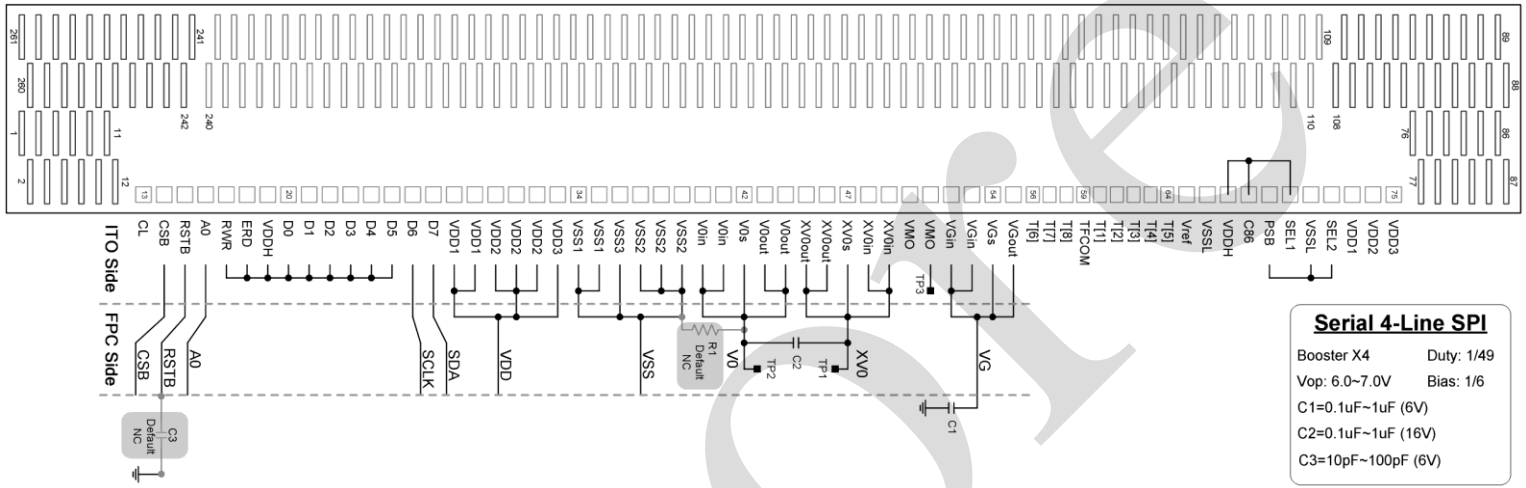
5.1、Application Circuit 1: 6800 Interface



5.2、Application Circuit 2: 8080 Interface



5.3、Application Circuit 3: Serial 4-Line SPI



5.4、Application Note

- **Selection of Application Voltage**

Referential LCD Module Setting: VDD1=2.8V, VDD2=VDD3=2.8V, Panel Size=1.4”, Ta=25°C

Duty	Booster	Vop	Bias
1/65	X5	8.5 ~ 9.5	1/9
		6.5 ~ 7.5	1/7
1/55	X5	7.5 ~ 8.5	1/8
		5.5 ~ 6.5	1/6
1/49	X5	7.5 ~ 8.5	1/8
		5.5 ~ 6.5	1/6
1/33	X5	5.5 ~ 6.5	1/6
		4.5 ~ 5.5	1/5
It is recommended to reserve some range for user adjustment and temperature effect			

Note:

- Positive Booster: (VDD2 * BL * BE) ≥ V0 or (VDD2 * BL * BE) ≥ V_{OP};
- Negative Booster: [–VDD2 * (BL – 1) * BE] ≤ XV0 or [VDD2 * (BL – 1) * BE] ≥ (V_{OP} – VG), where VG = V_{OP} * 2 / N;
- V_{OP} requirement: [VDD2 * (BL – 1) * BE] ≥ [V_{OP} * (N – 2) / N] or [V_{OP} ≤ VDD2 * (BL – 1) * BE *N / (N – 2)].
- BL is the booster stage and BE is the booster efficiency. Referential values are listed below: (assume VDD2=VDD3=2.8V)
  Module Size ≤ 1.4”: BE=80% (Typical);
  Module Size = 1.4”~1.8”: BE=76% (Typical).
  Actual BE should be determined by module loading and ITO resistance value.
- 1.6 ≤ VG < VDD2. Recommend VG is: VDD2-VG around 0.5~0.8V.
- VM=VG/2 and 0.8V ≤ VM < VDD2.
- The worse condition should be considered: Low temperature effect and display on with snow pattern on panel (max: 1.8”).

6、Statements And Notes：

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

6.2、Notion:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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