Datasheet for
Chipsemi CHSC5448

DS-CHSC5448

Ver1.0.3

Features:

- Capacitive touch panel controller, highly integrated with analog transceivers and digital Processer (SOC)
- Support mutual-capacitance ,self-capacitance, hybrid sense also with noise detect
- 17 TX channels, 31 RX channels, with displays size up to 7 inches
- Reporting rate up to 250Hz
- Support moisture detection
- Strong filtering for noise from AC charger/ common mode noise or LCD/OLED
- Low power consumption for battery application
- 32bits MCU and Software Developing Environment
- I2C interface to host
- In-system reprogrammability(reflash) support
- High ESD endurance :
  HBM>+-7KV
  CDM>+-2kV
- Supports advanced sensor/display architecture with:
  - On-cell metal mesh and ITO sensor designs
  -Curved lens designs
  -Sensor ITO pattern on lens
  - Touch controller IC on sensor Flexible Printed Circuit (FPC) tail

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Revision History

Version	Major Changes	Date	Author
1.0.0	Initial release	2020/6	yinyu

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1. Introduction

1.1. General description

CHSC5448 is highly integrated single-chip mutual-capacitive touch panel controller SoC developed by Chipsemi, which is designed to work with mutual-capacitance type sensor, and supports user-friendly gesture control and up to ten-point touch with a capacitive touch panel. Single-chip CHSC5448EU56 supportsup to 7'' touch panel.

With built-in 32-bit RISC processor and CDSP module, the CHSC5448 is featured with outstanding noise immunity, fast response, low power consumption, excellent accuracy and linearity, as well as perfect waterproof performance.

CHSC5448, which operates in the -40℃~+125℃ industrial temperature range,can be applied to a diverse group of portable devices, such as cellular phones, tablets, and GPS navigator.

CHSC5448EU56 offers high-volume-assembly and high integration level. Few external components are needed to satisfy customers' ultra-low cost requirement. It's completely RoHS-compliant and 100% lead (Pb)-free.

1.2. Key features

Table 1- 1 Key features of CHSC5448

Features	CHSC5448
Package	QFN-56, 6X6X0.55mm
Touch sensor	G/G, G/FF,P/FF,OGS,Ultra-thin G/F, On cell **(Support ITO traces; support direct bonding; support frameless TP; support single layer multipoint)**
Touch panel size	4.3''~7''
Response time	Power-on time: <75ms; Latency time for first touch: <12ms. Reporting rate up to 250Hz
Operating voltage	2.6V~3.6V

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Features	CHSC5448
Operating temperature	-40℃~+125℃
Supported channel number	17 TX channels and 31 RX channels
Power consumption	Current-active: 12mA @200Hz FPS, Idle : 500uA @ 50Hz FPS Sleep mode: 10uA
ESD/latch up	HBM 7000V (min.), CDM 2000V (min.), latch up 200mA(min.)
Multi-point touch	Up to 10points
Glove mode	Support
Anti-interference performance	Immune to noise from RF, LCD and power supply

1.3. Sensor pin characteristics

Table 2-1 sensor pin characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Mutual capacitance	Ct	Mutual capacitance Per node		1.5	4	pF
Self-capacitance	Cb	Self-capacitance Per Tx or RX node		20	500	pF
RX impendence	Rs	trace +pattern resistance for RX sensor		20		Kohm
TX impendence	Rt			20		Kohm

Note：for large self-capacitance ， recommend combine with low TRX impendence For better performance. RC constant for TRX sensor is recommended below 500nS.

1.4. Key benefits

(1) Anti-Interference and excellent noise-cancellation performance:

Immune to RF interferences, robust operation in noisy RF environment;

Insensitive to capacitance and environmental variety via auto calibration

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function;

Chipsemi's innovative adaptive-noise-cancellation technology and specially designed data processing unit can detect and silence the two noise sources which capacitive touch screen usually suffers from: display noise and charger noise. With the powerful 32bit MCU and specific built-in hardware, both the periodic and broadband noise can be eliminated to obtain unmatched noise immunity.

(2) Fast response time:

The power-on time for the CHSC5448EU56 is less than 75ms;

When it is powered up, the latency time for first touch is less than 12ms;

Reporting rate up to 250Hz makes fast response available, which is especially useful for the highly demanding applications for the responding speed, such as handwriting and game.

(3) Low power consumption:

The average current in typical case is 12mA at active state, and 11uA in deep sleep mode.

(4) Excellent waterproof performance:

Water mist even droplets on the surface will not influence normal operation of touch panel based on the CHSC5448.

When water mist or droplets are wiped off, the touch screen can also be operated normally without extra delays.

No malfunction or dummy points will be reported during water spurting and wiping process.

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2. Pin Information

2.1. Pin layout

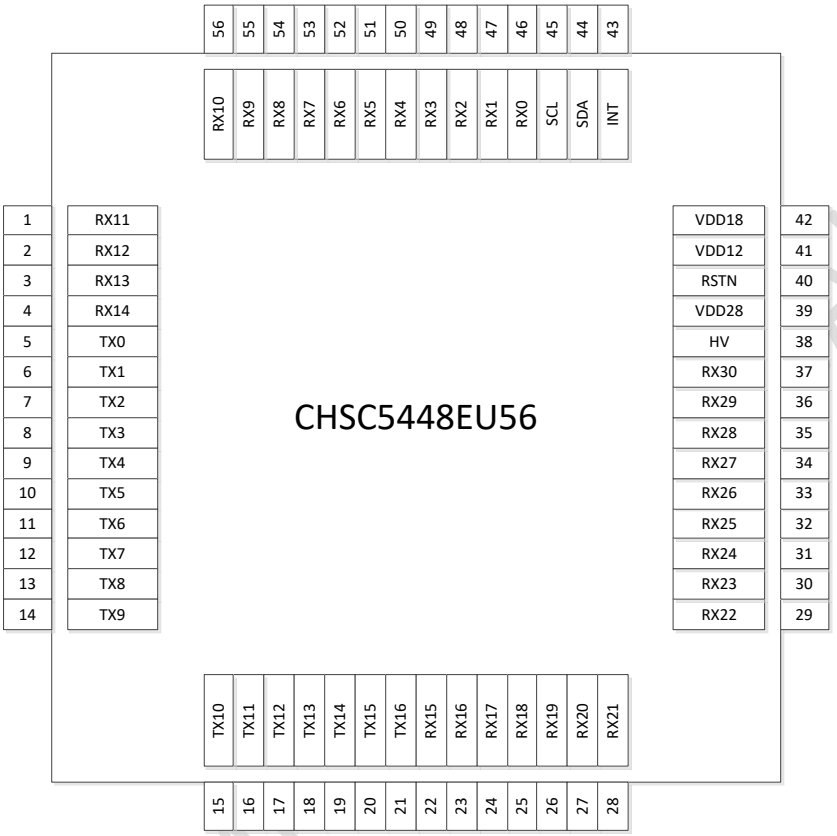

Figure 2-1 Pin assignment for the CHSC5448EU56

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2.2. Pin list

Table 1- 2 Pin functions for the CHSC5448EU56

Pin Name	Pin No.	Type	Description
TX0~TX16	5~21	O	Drive output
RX0~RX30	46~56 1~4 22~37	I	Sense input
HV	38	O	High Voltage Pump. Connect a 1μF ceramic capacitor to ground.
VDD28	39	PWR	Chip power supply, 2.8V or 3.3V. A 1uF ceramic capacitor to ground is required.
RSTN	40	I	Reset Pin, zero voltage active, A 0.1uF capacitor to ground is required.
VDD12	41	PWR	Digital power supply, 1uF capacitor to ground is required.
VDD18	42	PWR	IO power supply, 1uF capacitor to ground is required.
INT	43	I/O	External interrupt to the host
SDA	44	I/O	I2C data input and output
SCL	45	I/O	I2C clock input
GND	ePAD	G	Ground

*Note: INT Pin can be used as GPIO, SDA/SCL Pins are open drain outputs.

3. Absolute maxim rating & ESD

VDD28 to GND	-0.3V to +3.6V
VDD18 to GND	-0.3V to +3.6V
VDD12 to GND	-0.3V to +1.32V
INT/SDA/SCL to GND	-0.3V to +3.6V
RX0~RX30 to GND	-0.3V to +3.6V
TX0~TX10 to GND	-0.3V to +3.6V
Maxim Power dissipation	250mW
Maxim Junction Temperature	150℃
Operating Temperature	-40℃ to 125 ℃
Storage Temperature	-60℃ to 150 ℃
HBM	+/-7000V (min.)
CDM	+/-2000V (min.),

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4. System Description

4.1. Block diagram

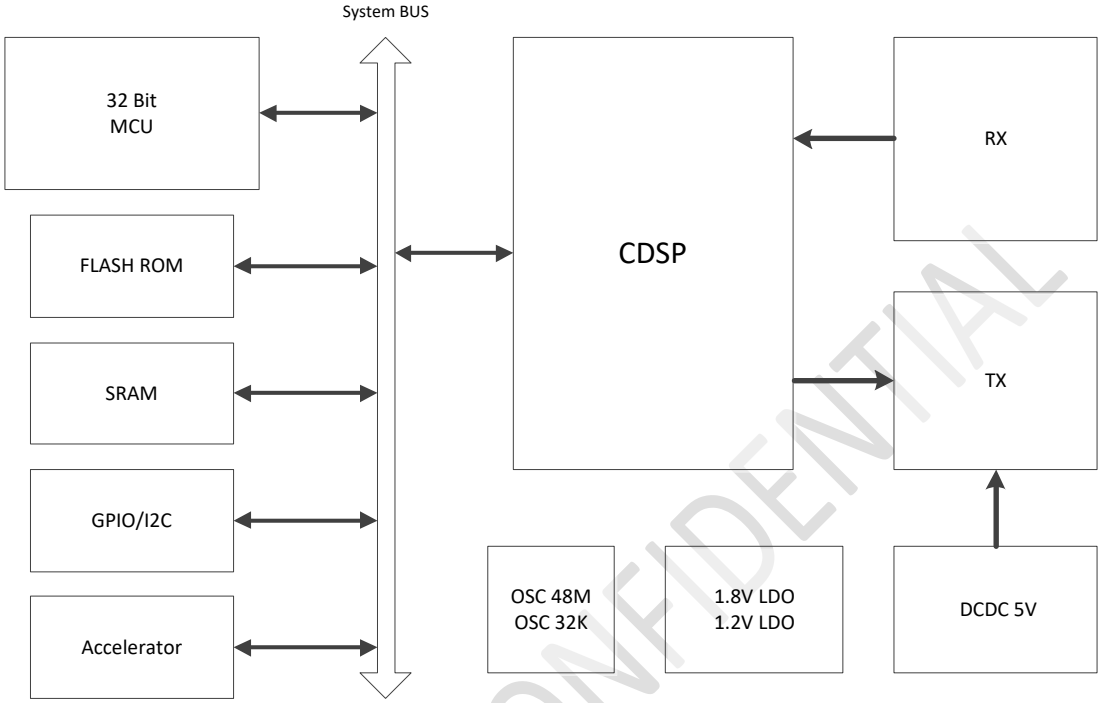

Figure 4- 1 Block diagram

4.2. Block description

- **32bit MCU**

CHSC5448EU56 integrates a 32bit high performance, low Power CPU. It's Harvard structure CPU core, with a 32×32 multiplier and a 32/32 divider.

- **Memory**

64KB RAM and 128KB FLASH ROM

- **GPIO/I2C interface**

INT PIN can be used as GPIO for user define, also INT Pin could generate interrupt signal.

SCL/SDA are I2C interface pins, open drain outputs.

- **Accelerator**

Hardware accelerates CTP computing.

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- **CDSP**

The CHSC5448 embeds CDSP and includes 31 sensing lines and 17 drive lines, and supports channel exchangeable. Calculation for accurate touch point coordinate information is implemented via firmware.

The CDSP configures analog front-end parameters, control analog-to-digital conversion and channel switch for flexible scanning time and sensor usage. The collected sampling data from ADC will be stored into internal SRAM and will be translated into accurate touch position information using advanced algorithms.

The CDSP integrates four control modes: mutual capacitance detection, self capacitance detection, noise detection and short detection, also it has temperature following technique.

- **RX**

The RX module is mutual capacitive senses channels, including high performance capacitive-sense amplifier and ADC that makes the capacitor quantized.

CHSC5448 has 31 channels for CTP sensing.

- **TX**

The TX module is capacitive drive channels. TX generates ordered serial signals to drive mutual capacitance panel.

CHSC5448 has 17 channels for CTP driving.

- **Oscillator**

The CHSC5448EU56 embeds a 48MHz RC oscillator and 32K RC oscillator.

The 48M oscillator is the clock source for MCU and CTP driving, the oscillator clock has a wide adjustment; by tuning frequency CTP will avoid the frequency of the noise interference. The 48M oscillator supports boost clock mode up to 64MHz that increases CTP scan rate.

The 32K oscillator is the clock source for working mode conversion timer and watch-dog monitor

- **Regulator**

The CHSC5448 embeds two groups LDO (Low Dropout) regulators to provide

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lower voltage power. One is for digital core supply, and the other one is for 1.8V IO driving. Each group has two LDOs, large current driving for active mode and week current driving for suspend and sleep mode.

- **DCDC**

The DCDC generates high voltage over supply power for TX driving, higher voltage can provide higher dynamic range for RX sensing, gets better SNR. The DCDC is recommended setting to 5V.

4.3. Power management

The CHSC5448 is optimized for power consumption, inside the chip it embedded PMU (power management unit) to reduce power consumption at off working state. The CHSC5448 has three working states: active/idle/deep sleep mode.

Program would control the system enter suspend or deep sleep mode, and return to active mode by interrupt signal.

Table 4-1 CHSC5448 nominal power consumption

Operation mode	**Total current(AVDD)**
Active	12mA
Idle	500uA
Sleep	10uA

Note: the power consumption only show as reference.actual power consumption depend on system design requirement and the real application case.

4.4. Chip operation modes

For the CHSC5448, there are three operation modes available as follows: active mode, suspend mode and deep sleep mode.

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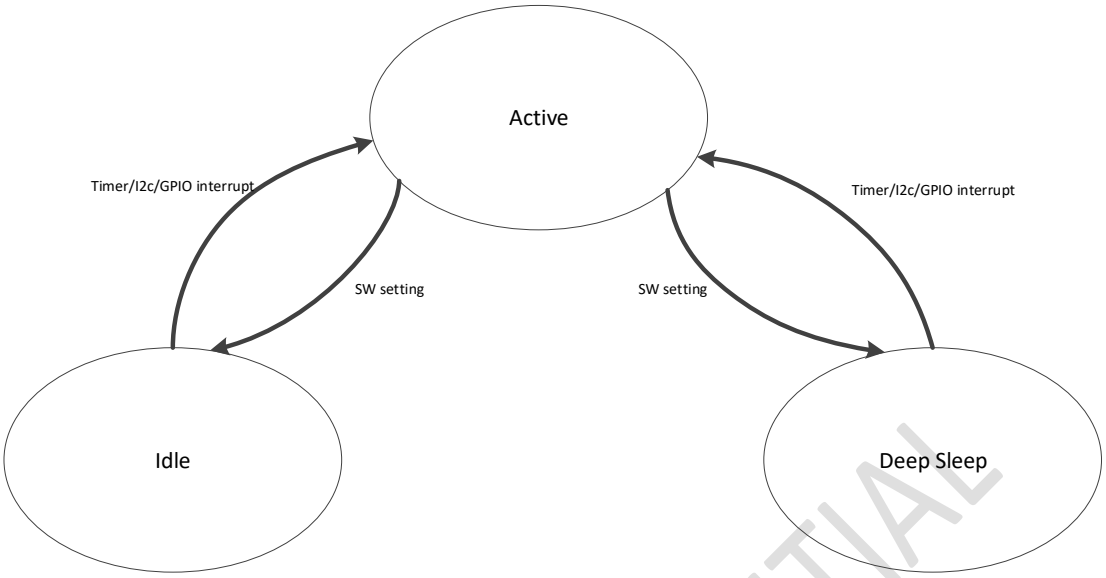

Figure 4-2 Operation mode conversion

- **Active mode**

At active mode, all module will power on, the system work at full speed with high frame report rate.

- **Idle mode**

At this mode, system detect the touch event with fast response ability, Once Touch event is detected, the system recover to active mode. The responding time can be programed from 10mS~100mS by firmware.

- **Deep Sleep mode**

At deep sleep mode, the CHSC5448 will power down MCU and CTP functions , and provide minimum current to maintain necessary state without loss. At this mode, the CHSC5448 will consume less then 10uA current at 2.8V power supply.

I2C, INT , or inner timer can be used to wake up the system

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5. CTP function

The CTP is the core of capacitance detection, with high accuracy analog front end (RX, TX) and powerful computation of CDSP. The CTP provides mutual capacitance detection, self capacitance detection, noise detection and short detection mode. Also the CTP has temperature following technology to fit temperature variation.

5.1. Mutual capacitance mode

At mutual capacitance detection mode, the TX module outputs pulse signal, and the RX module receive it via mutual capacitance on the panel. The CTP will detect capacitance changing when touching, then mark it as contrast.

Mutual capacitance detection supports large range from 2pF to 20pF, it has enough sensitive circuit to ensure the detection accuracy. It also integrate smooth filter to reduce random noise.

5.2. Self capacitance mode

CHSC5448 has high performance self-cap detect technique, and the self-cap detection with 4 sub-mode can adaptive numerous application, with strong noise immunity and high sensitivity. Also can support large self-cap range

5.3. Noise detection

The CTP can scan large frequency range and get noise power density of touch screen, and then system can choose a working frequency with less noise.

5.4. Short detection

At short detection mode, the CTP will sense the resistance of RX Pin, and it is very helpful to factory production.

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6. I2C interface

6.1. Description

I2C module of the CHSC5448EU56 acts as slave. Its related registers are as follows:

By default, I2C Master can read any internal register and RAM space of the CHSC5448EU56 via I2C.

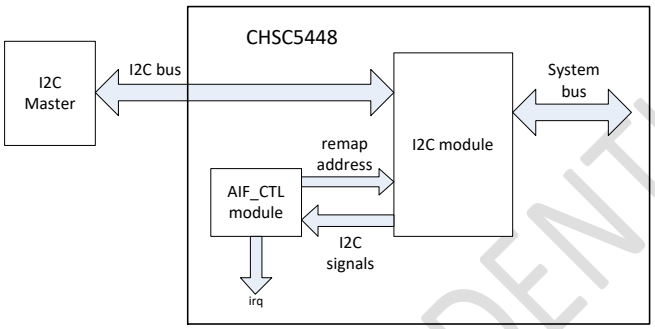

Figure 6-1 Connection schematic between I2C and AIF_CTL module

The AIF_CTL module embedded in the CHSC5448EU56 serves to implement I2C address mapping, and provide cmd register to generate interrupt signal for I2C communication.

6.2. I2C timing

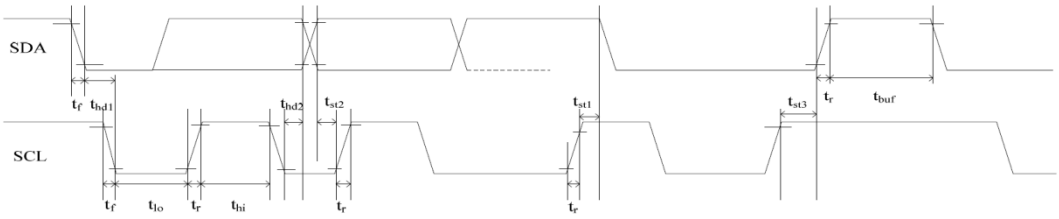

Figure 6-2 I2C timing sequence

Table 6-1

parameter	symbol	MIN	MAX	unit
SCL low period	t_{lo}	1.3		us
SCL high period	t_{hi}	0.6		us
SCL setup time for START condition	t_{st1}	0.6		us
SCL setup time for STOP condition	t_{st3}	0.6		us

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SCL hold time for START condition	t_{hd1}	0.6		us
SDA setup time	t_{st2}	0.1		us
SDA hold time	t_{hd2}	0		us

6.3. AC characteristics

Table6.2 AC Characteristics

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Digital inputs/outputs						
IO voltage(*)	VDDIO	1.6	1.8	2	V	
IO voltage(**)	VDDIO	3.0	3.3	3.6	V	
Input high voltage	VIH	0.7VDDIO		VDDIO	V	
Input low voltage	VIL	VSS		0.3VDDIO	V	
Output high voltage	VOH	VDDIO-0.3		VDD	V	
Output low voltage	VOL	VSS		0.3	V	

(*)VDDIO = 1.8V @ VDD28 = 2.8V
(*)VDDIO =1.8V/3.3V @ VDD28=3.3V

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7. Power on reset sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn’t be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after ini- tializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

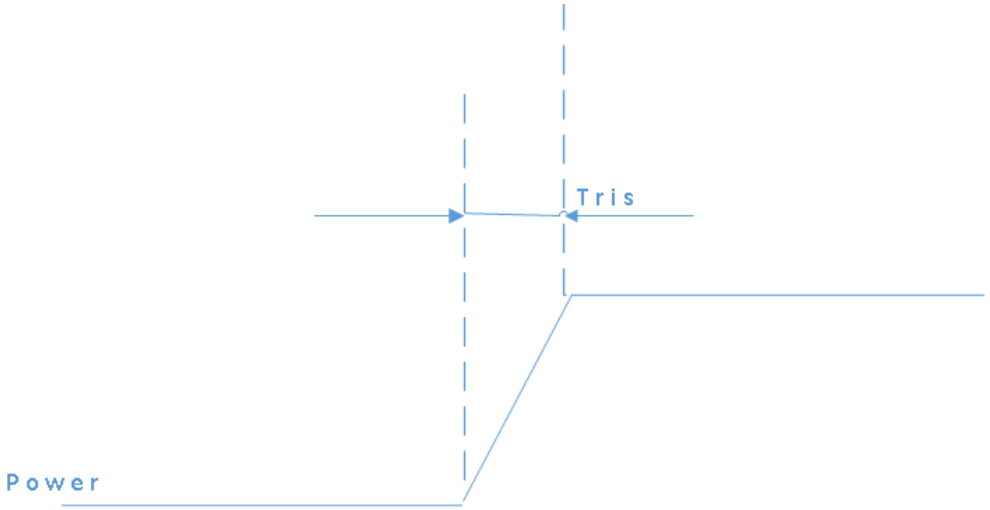

Figure 7-1 power on time

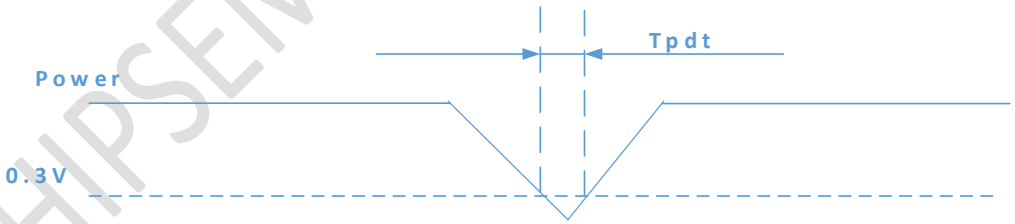

Figure 7-2 Power Cycle requirement

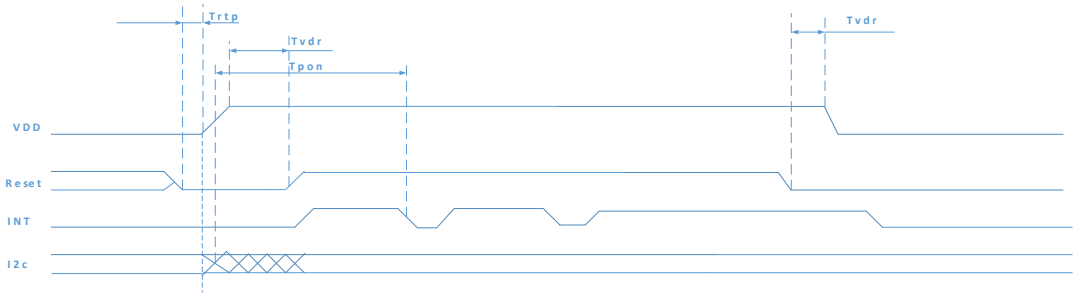

Figure 7-3 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

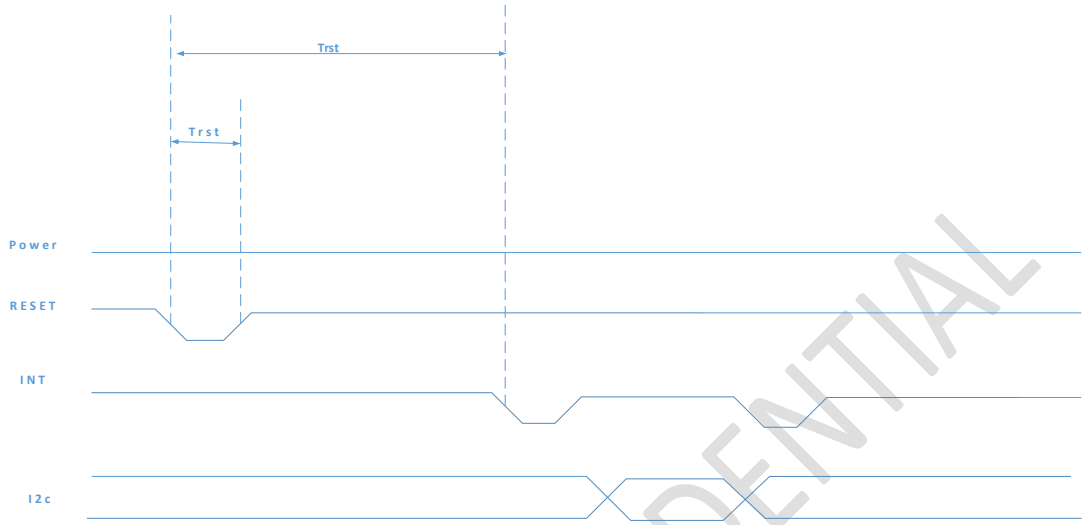

Figure 7-4 Reset Sequence

Table 7-1 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	2	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	500	--	us

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8. System application guide

The CHSC5448 supply voltage can use 2.8V or 3.3V, and support 1.8V or 3.3V IO voltage to system. This circuit has a 1.8V LDO internally, user can use it to pull up I2C resister or not.

If VDD18 pin connects to VDD28, the 1.8V LDO will be disabled automatically.

8.1. Application 1

VDD28 = 2.8V, I2C communication voltage = 1.8V, using CHSC5448 internal 1.8V pull up

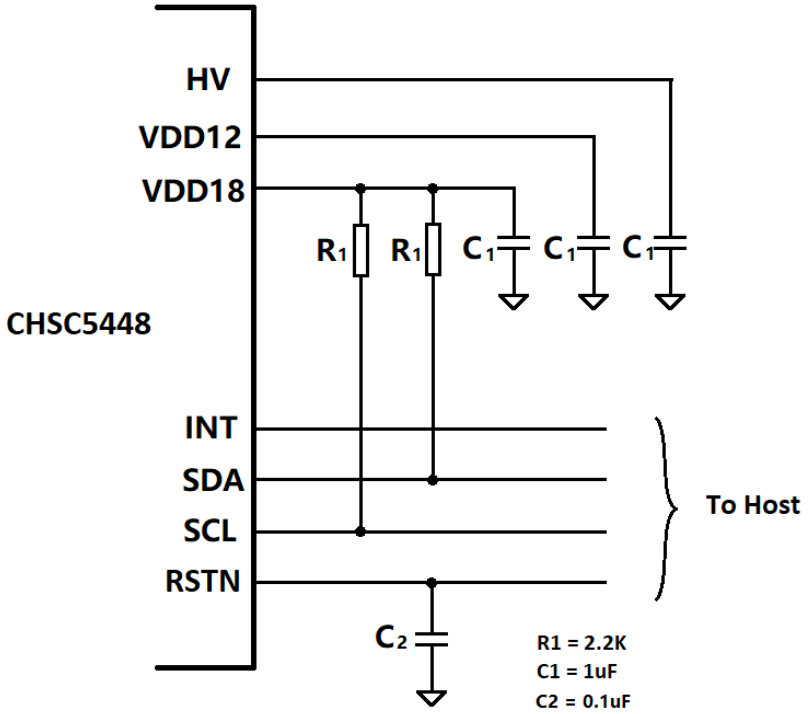

Figure 8-1 I2C with internal 1.8V pull up

8.2. Application 2

VDD28 = 2.8V, I2C communication voltage = 1.8V, using system 1.8V pull up

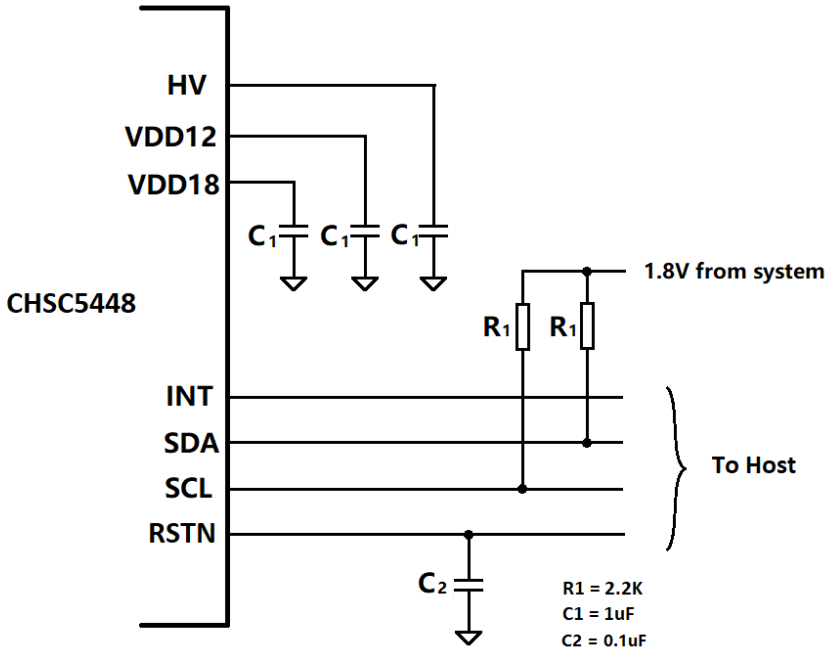

Figure 8-2 I2C with external 1.8V pull up

8.3. Application 3

VDD28 = 3.3V, I2C communication voltage = 3.3V, VDD18 Pin and VDD28 Pin are connected together.

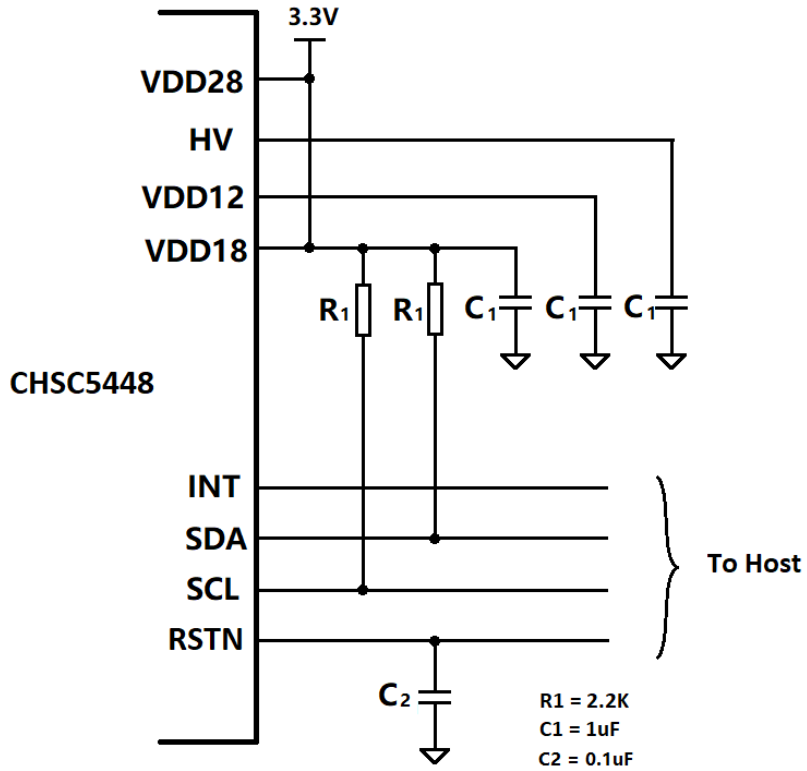

Figure 8-3 I2C with 3.3V pull up

Note : the C2 at RSTN pin can be removed if no serious noise couple to RSTN pin.

9. Package information

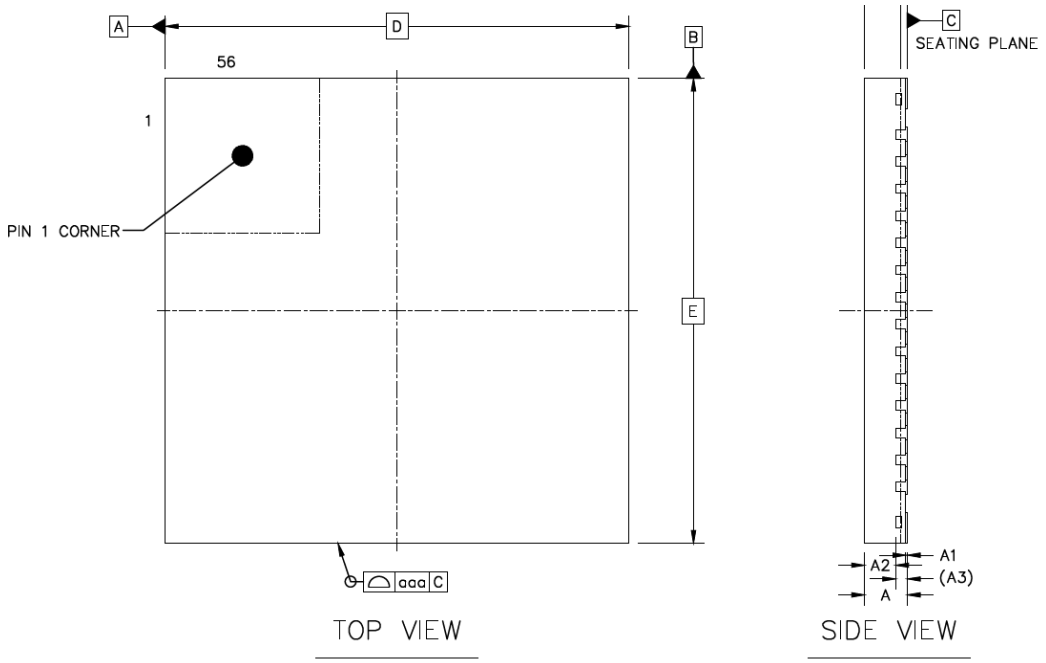

Figure 9-1 Package top view and side view

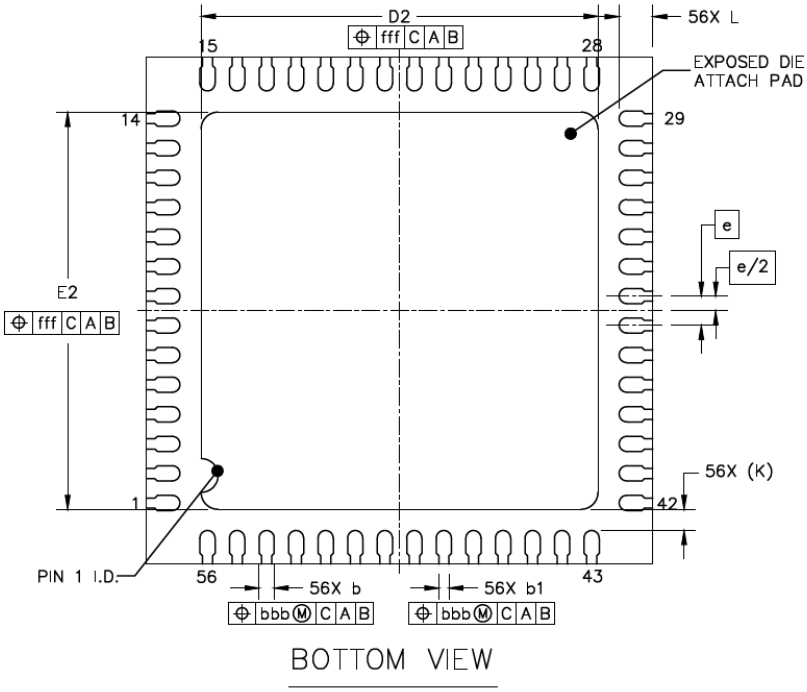

Figure 9-2 Package bottom view

Table 8-1 specific dimension Unit: mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	4.6	4.7	4.8
	Y	E2	4.6	4.7	4.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES

1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP·Sn8~20s

Table 9-2 Ordering information of the CHSC5448

Product Series	Package Type	Temperature Range	Product Part No.	Packing Method	Ordering Number	MinimumOrder Quantity
CHSC5448	56-pin 6x6x0.55mm QFN	-40℃~+125℃	CHSC5448EU56	TR	CHSC5448EU56R	3000

*Note: Packing method “TR” means tape and reel.