fiti

EK9716

Rev. 0.2

PRELIMINARY DATA SHEET

1200CH TFT LCD
Source Driver with TCON

fitipower integrated technology Inc.

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1200CH TFT LCD Source Driver with TCON

1. GENERAL DESCRIPTION

EK9716 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. EK9716 integrated source driver, timing controller and pin control interface.

EK9716 input timing support TTL digital 24bit parallel RGB data format, and source output support 8-bit resolution 256 gray scales with dithering features. Operating parameters can be set via pin control for all control features. Special circuit architecture is designed for lower power dissipation.

EK9716 support two chip cascade operation mode to reduce the FPC amount and save the cost. Configure able Master and Slave configuration increase the flexibility for different panel design. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

2. FEATURES

- Special design for small-sized color TFT LCD source drivers with timing controller
- Integrated 1200 channel source driver
- Support display resolutions : 800(RGB)x600、800(RGB)x480、400(RGB)x480、400(RGB)x240
- 8-bit resolution 256 gray scale with 2-bits dithering (6bits DAC + 2bits HFRC)
- Support TTL 24-bit parallel (RGB) input timing
- Support cascade function with bidirectional shift control (CMOS signal)
- Support single or dual-gate operation mode
- Support Delta or Stripe color filter configuration
- Support stand-by mode for low power consumption
- Support dot inversion driving scheme (Cascade mode)
- Support 2 dot one inversion driving scheme (Dual Gate mode)
- V1 ~ V14 for adjusting Gamma correction
- Output dynamic range: 0.1V ~ VDDA-0.1V (Dual Gate mode)
- Power for source driver voltage VDDA: 6.5V ~ 13.5V
- Power for digital interface circuit VDD: 2.7 ~ 3.6V
- Max. operating frequency: 50 MHz
- Minimum operating frequency: 20 MHz (800(RGB)x600 and 800(RGB)x480 display resolution)
- Built-in CABC function
- Built-in AUTO pattern
- COG package
- Chip Size: 22572um X 938um, Output Pad Pitch: 17um

3. BLOCK DIAGRAM
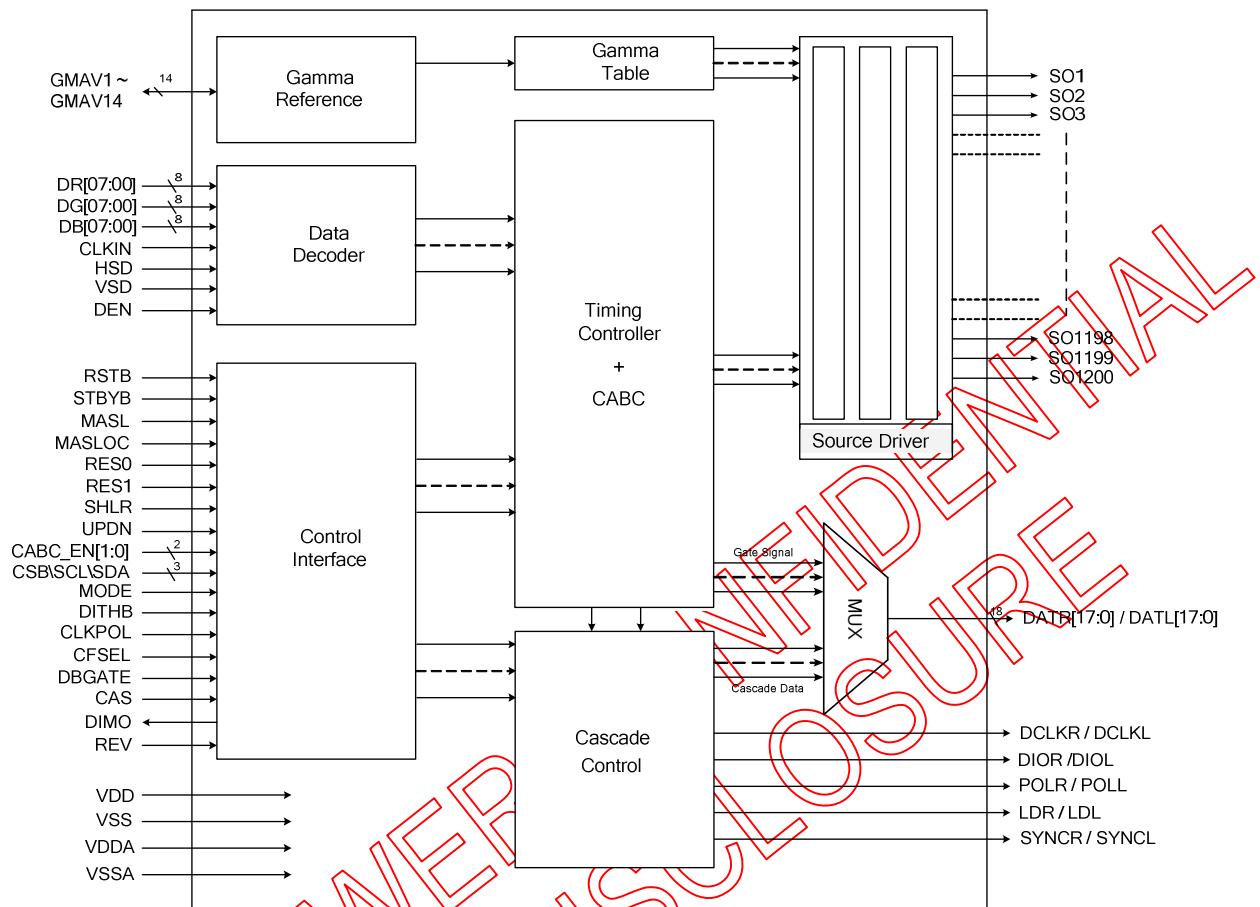
Figure 1. Block Diagram
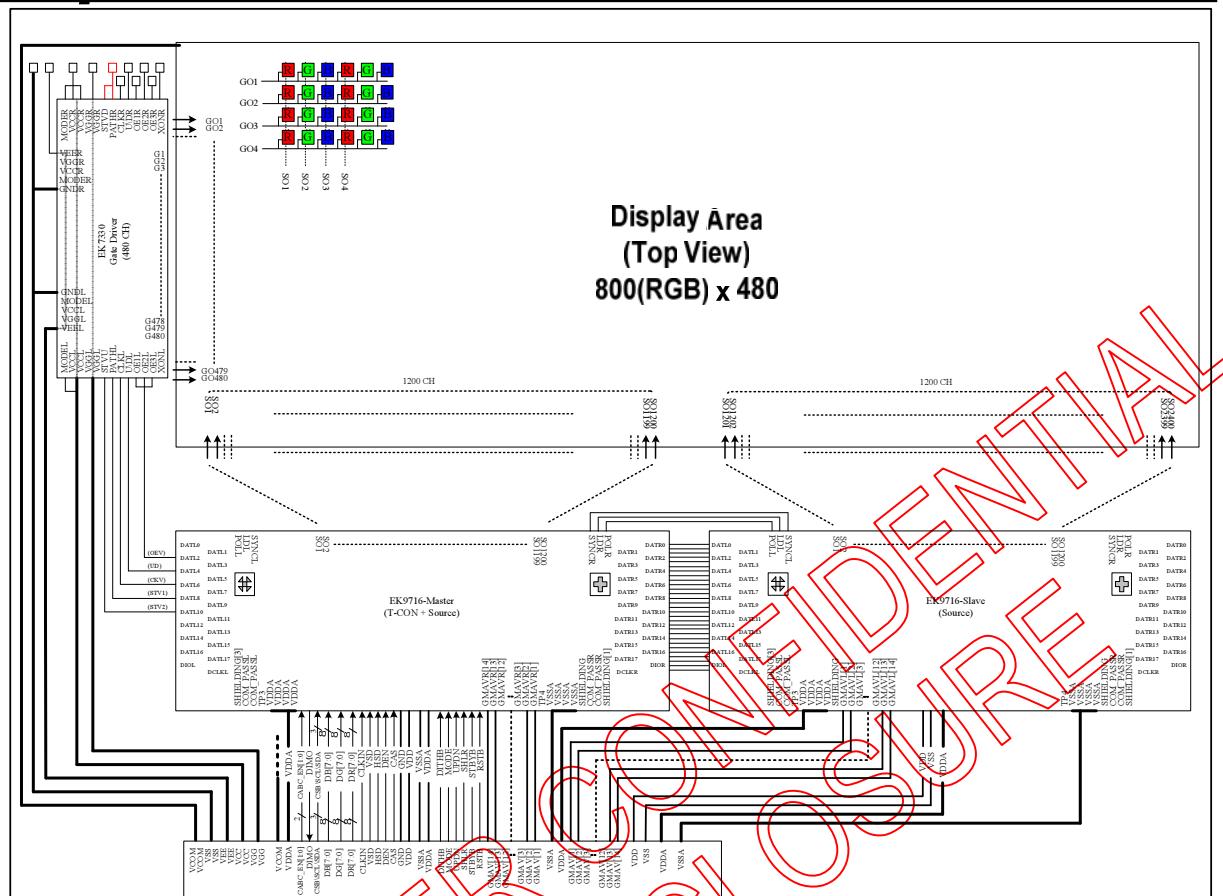
Figure 2. Application Block Diagram – 2 Chip Cascade
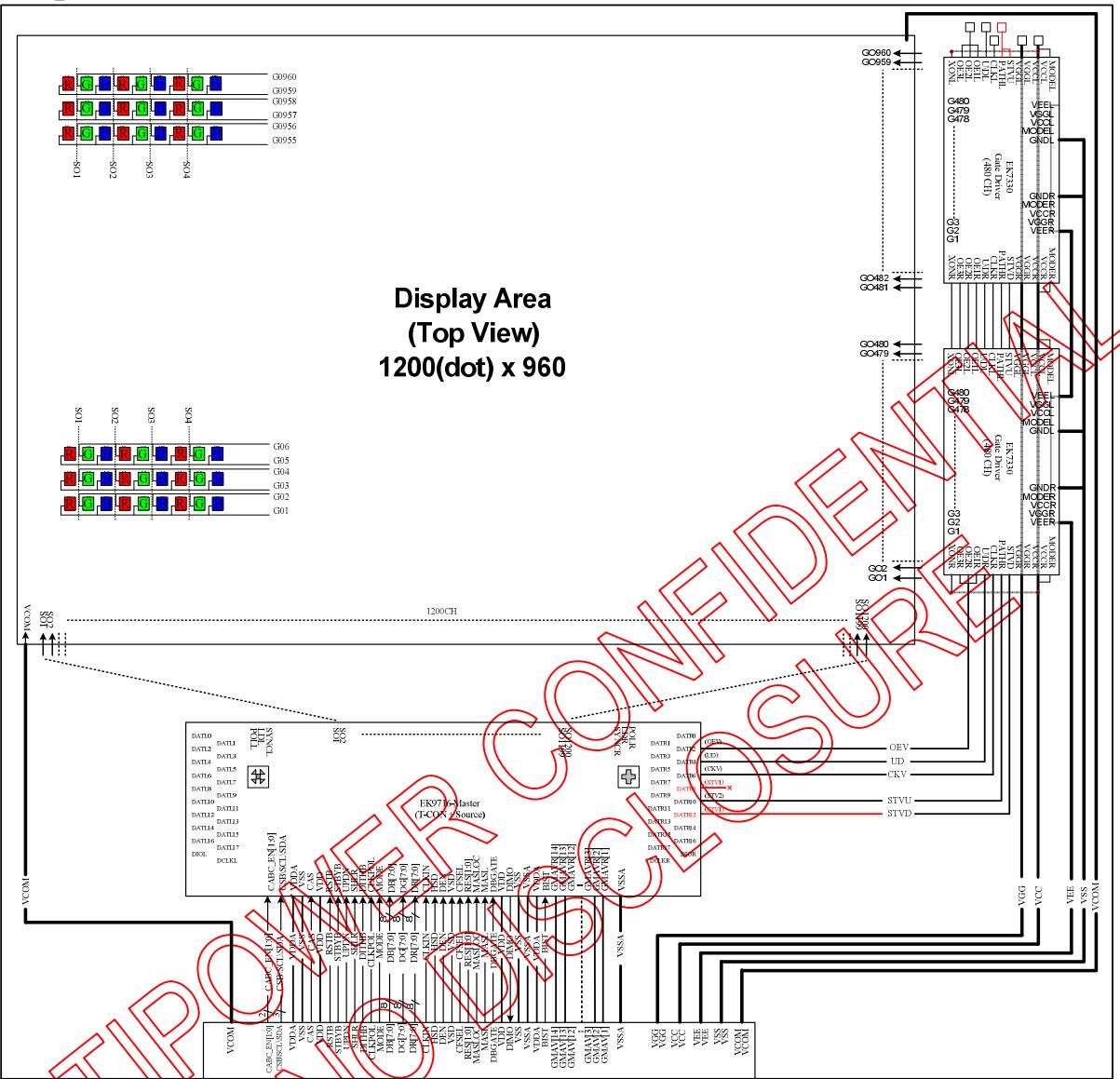
Figure 3. Application Block Diagram – Dual Gate Application

Figure 4. Pad Sequence (Bump Side)
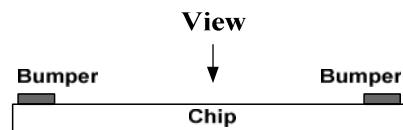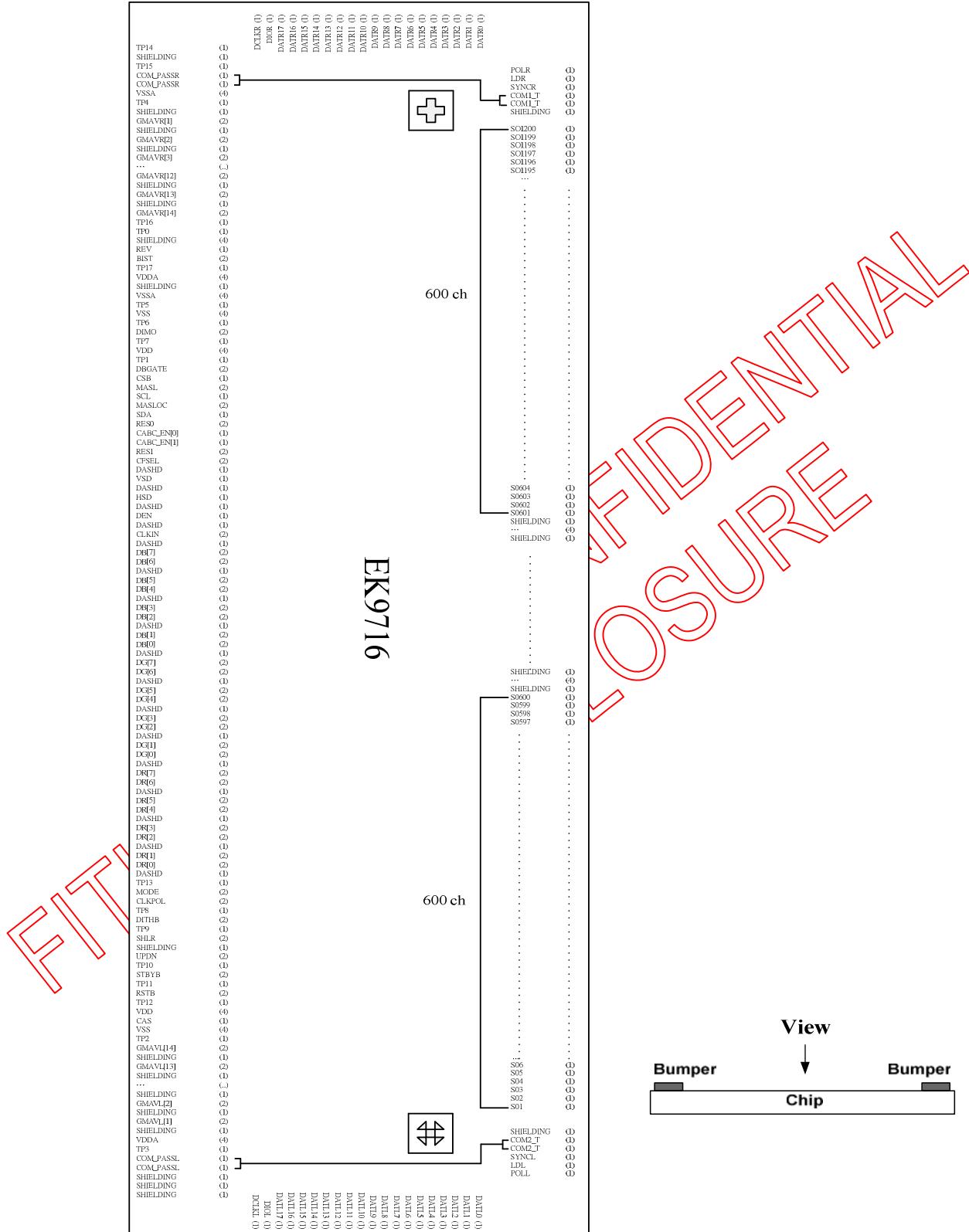
4. PIN DESCRIPTION

Table 1. Pin Description

Pin Name	Pin Type	Description
DR[07:00] DG[07:00] DB[07:00]	Input	Parallel data Input. For TTL 24-bit parallel RGB image data input. DR[07:00]=R[7:0] data; DG[07:00]=G[7:0] data; DB[07:00]=B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to VSS.
CLKIN	Input	Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.
HSD	Input	Horizontal Sync input. Negative polarity.
VSD	Input	Vertical Sync input. Negative polarity.
DEN	Input	Data Input Enable. Active High to enable the data input bus under "DE Mode". Normally pull low.
MODE	Input	DE / SYNC mode select. Normally pull high H: DE mode.(Default) L: HSD/VSD mode.
RES[1:0]	Input	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution RES[1:0] = "10", for 400(RGB)*480 display resolution RES[1:0] = "11", for 400(RGB)*240 display resolution
DITHB	Input	Dithering function enable control. Normally pull high DITHB = "1", Disable internal dithering function(Default) DITHB = "0", Enable internal dithering function
CLKPOL	Input	Input clock edge selection. Normally pull low CLKPOL = "1", Latch data at CLKIN rising edge. CLKPOL = "0", Latch data at CLKIN falling edge. (Default)
DIMO	Output	Backlight dimmer signal for CABC application DIMO = "0", Turn off external backlight controller DIMO = "1", Logical control signal to turn on external backlight controller Note: Refer to the Power On/Off Sequence for the detail information
CABC_EN[1:0]	Input	CABC H/W enable pin. Normally pull low When CABC_EN = "00", CABC OFF.(Default mode) When CABC_EN = "01", User interface Image When CABC_EN = "10", Still Picture When CABC_EN = "11", Moving Image
CFSEL	Input	Color Filter type selection. Normally pull high CFSEL = "1", Stripe mode. (Default) CFSEL = "0", Delta mode
DBGATE	Input	Dual Gate function enables control. Normally pull low DBGATE = "1", Enable Dual Gate Function. DBGATE = "0", Disable Dual Gate Function (Default) Note: Cascade function will be disabled under "dual gate" mode
GMAV1 ~ GMAV14	Input/Output	Gamma correction reference voltage. These input voltage must be offered by user. VSSA+0.1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-0.1 (Dual Gate) VSSA+1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-1 (Cascade mode) V2, V6, V9, V13 pads are disabled.
RSTB	Input	Global reset pin. Active Low to enter Reset State. Suggest to connecting with an RC reset circuit for stability. Normally pull high.

Pin Name	Pin Type	Description
STBYB	Input	Standby mode, Normally pull high. STBYB = "1", normal operation(Default) STBYB = "0", timing controller, source driver will turn off, all output are High-Z
MASL	Input	Master and Slave Mode selection. Normally pull high. MASL = "H", for Master mode. (Default Mode) MASL = "L", for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	Input	Master location definition pin. Normally pull low. MASLOC = "L", Master locate on right side (Panel top view). (Default Mode) MASLOC = "H", Master locate on left side (Panel top view).
CSB	Input	Serial communication chip select. Normally pull high
SDA	Input/Output	Serial communication data input. Normally pull low
SCL	Input	Serial communication clock input. Normally pull low
SHLR	Input	Source Right or Left sequence control. Normally pull high. SHLR = "L", shift left: last data = S1←S2←S3........←S1200 = first data. SHLR = "H", shift right: first data = S1→S2→S3......→S1200 = last data.
UPDN	Input	Gate Up or Down scan control. Normally pull low. UPDN = "L", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver.(Default) UPDN = "H", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
BIST	Input	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
CAS	Input	Cascade function select. Normally pull high. CAS = "H", Enable cascade function.(Default) CAS = "L", Disable cascade function.
REV	Input	Controls whether the data of D00~D27 are inverted or not, normally pulled low. When "REV"=1 these data will be inverted. EX. "00" → " 3F", "07"→ " 38", "15"→ "2A", and so on.
DATR[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKR	Input/Output	Master and Slave cascade control signal.
DIOR	Input/Output	Master and Slave cascade control signal..
POLR	Input/Output	Master and Slave cascade control signal.
LDR	Input/Output	Master and Slave cascade control signal.
SYNCR	Input/Output	Master and Slave cascade control signal.
DATL[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKL	Input/Output	Master and Slave cascade control signal.
DIOL	Input/Output	Master and Slave cascade control signal.
POLL	Input/Output	Master and Slave cascade control signal.
LDL	Input/Output	Master and Slave cascade control signal.
SYNCL	Input/Output	Master and Slave cascade control signal.
VDDA	Power Input	Power supply for analog circuits
VSSA	Power Input	Ground pins for analog circuits
VDD	Power Input	Power supply for digital circuits
VSS	Power Input	Ground pins for digital circuits
SO1~SO1200	Output	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
ALIGN	Mark	For assembly alignment.

Pin Name	Pin Type	Description
COM_PASSR COM_PASSL	Shorted line	Internal link together between input side and output side.
COM1_T COM2_T	Shorted line	Internal link together between input side and output side.
TP17~0	Testing	Float these pins for normal operation.
SHIELDING	Shielding	IC Shielding pads. Those pins are internally connected to the VSSA. DO NOT connect to any WOA on the panel.
DASHD	Shielding	Data Bus Shielding pad. Those pins are internally connected to the VSS. RECOMMAND to add shielding lines on the FPC to reduce EMI.

Table 2. EK9716 Pass Line Description:

Pass Line No:	Pad Name	
1	COM_PASSR	COM1_T
2	COM_PASSL	COM2_T

4.1. Chip Driver configuration examples of the EK9716

Two pieces of EK9716 driver are cascaded application for 800RGB x480
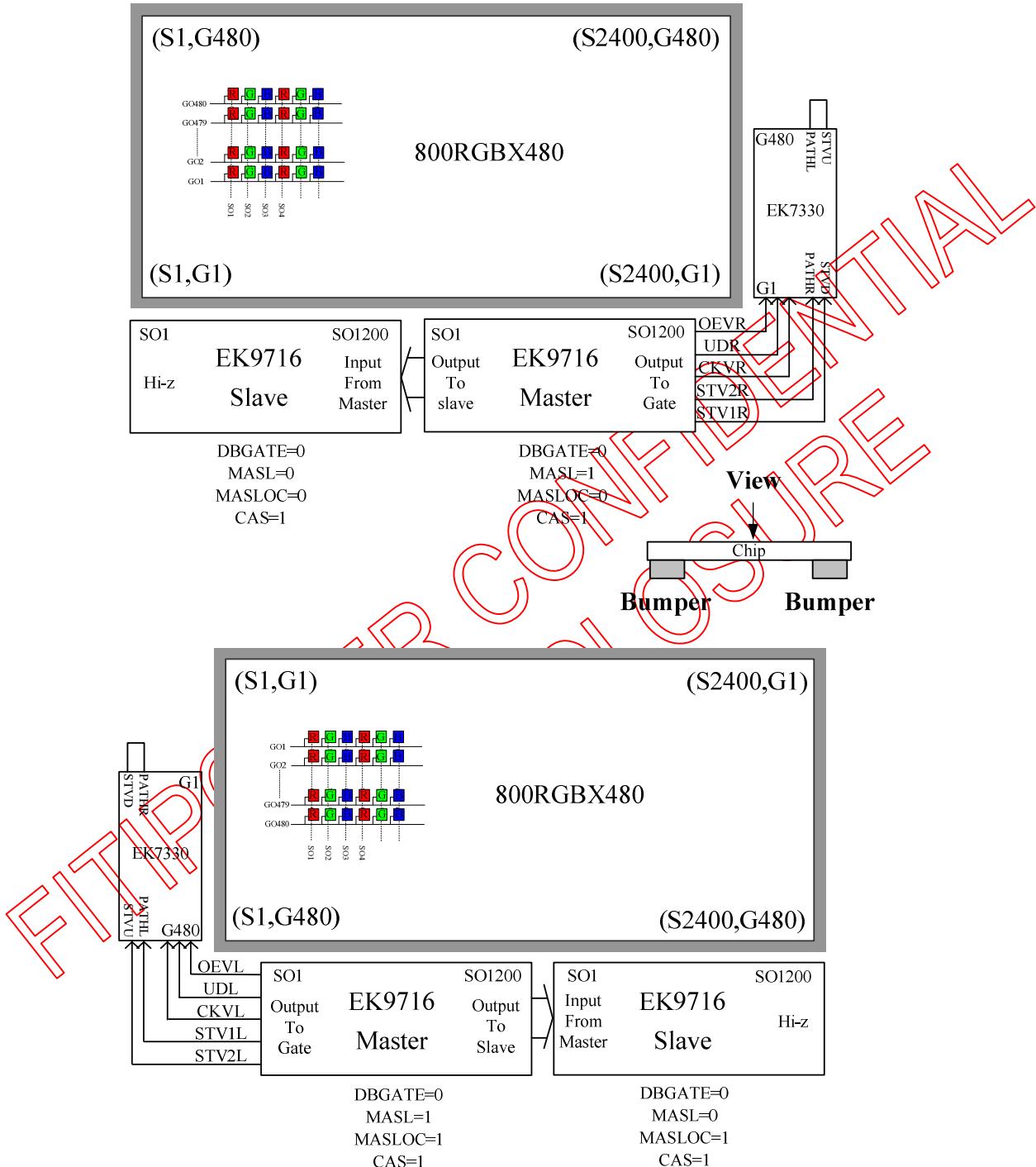
4.2. EK9716 put down and EK7330 put left side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK9716 will be illustrated as figure.
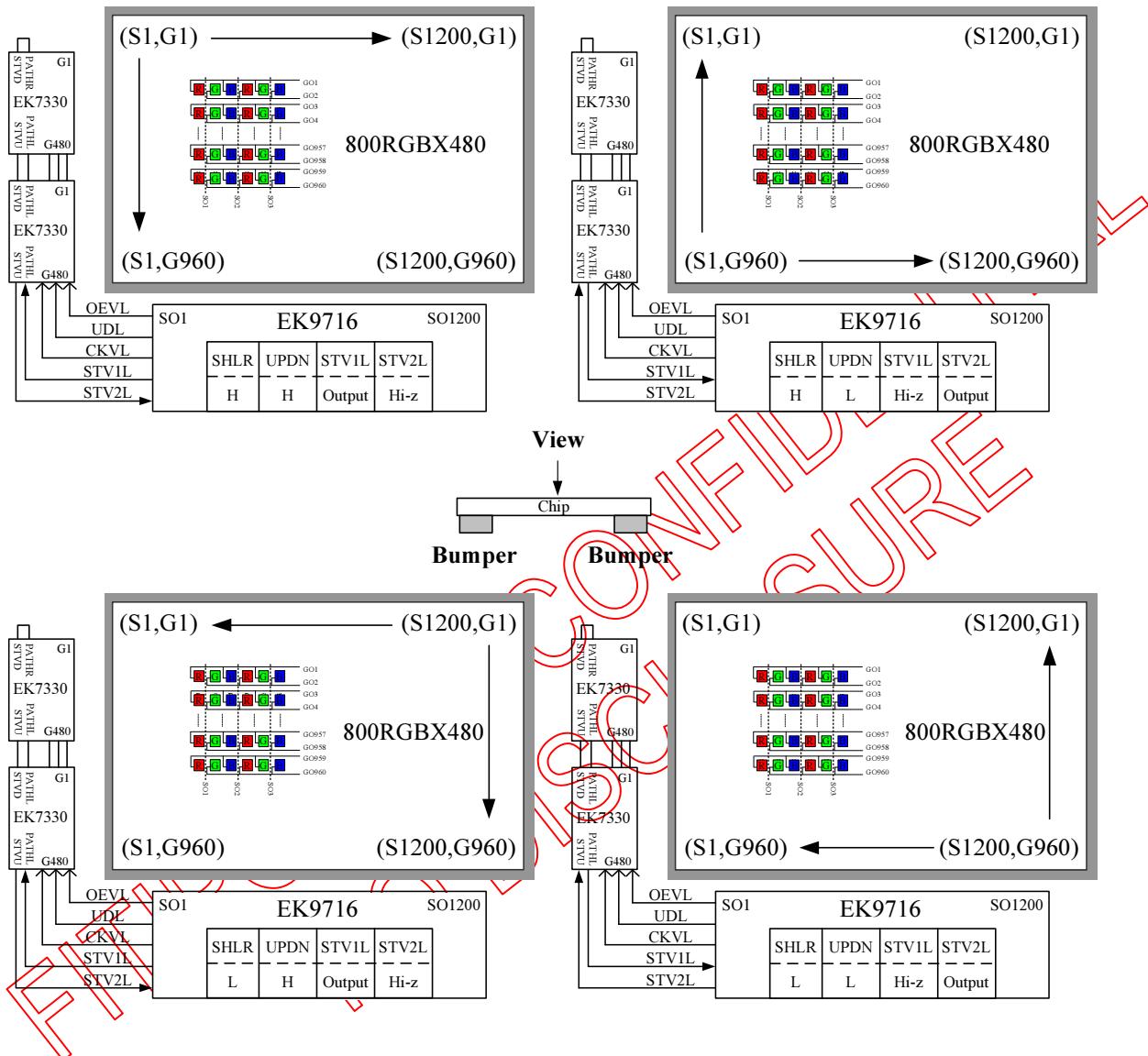
4.3. EK9716 put down and EK7330 put right side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK9716 will be illustrated as figure.
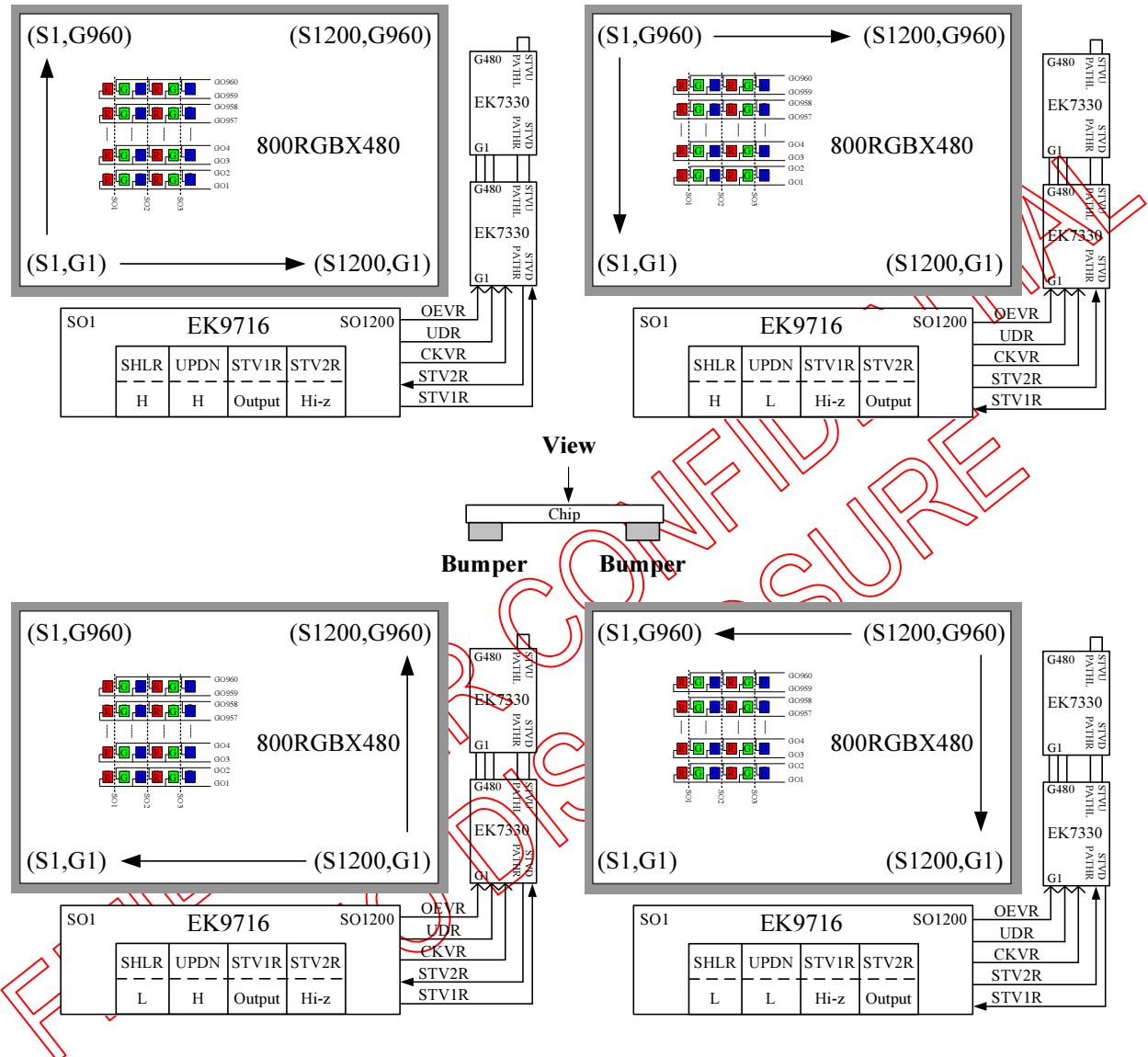
4.4. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Table 3. wiring resistance

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value (Ω)
VDD	<25	BIST	<1K
VDDA	<5	CAS	<1K
VSS	<25	CABC_EN[1:0]	<1K
VSSA	<5	CSB/SCL/SDA	<200
GMAV1~GMAV14	<10	DATR[17:0]	<200 & 20 pf
DR[07:00]	<200	DCLKR	<200 & 20 pf
DG[07:00]	<200	DIOR	<200 & 20 pf
DB[07:00]	<200	POLR	<200 & 20 pf
DEN	<200	LDR	<200 & 20 pf
MODE	<1K	SYNCR	<200 & 20 pf
RES[1:0]	<1K	DATL[17:0]	<200 & 20 pf
DITHB	<1K	DCLKL	<200 & 20 pf
CLKPOL	<1K	DIOL	<200 & 20 pf
DIMO	<1K	POLL	<200 & 20 pf
CFSEL	<1K	LDL	<200 & 20 pf
DBGATE	<1K	CASCADE GMAV1~GMAV14	<30
RSTB	<1K	CLKIN	<50
MASL	<1K	HSD	<200
MASLOC	<1K	VSD	<200
SHLR	<1K		
UPDN	<1K		

Table 4. DATR[17:0] / DATL[17:0] pin mapping Table:

DATR[17:0]	DBGATE = "0" MASL = "1" MASLOC = "0" CAS = "1"	DBGATE = "0" MASL = "1" MASLOC = "1" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "0" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "1" CAS = "1"	DBGATE = "1" MASL = "1" MASLOC = "X" CAS = "0"	DBGATE = "0" MASL = "1" MASLOC = "X" RES[1:0]="1X" CAS = "0"
Description	Master for cascade. Master locate on panel right side	Master for cascade. Master locate on panel left side	Slave for cascade. Master locate on panel right side	Slave for cascade. Master locate on panel left side	Dual Gate Mode	Single Source Mode
DATR0	X	DAT0	DAT0	X	X	X
DATR1	X	DAT1	DAT1	X	X	X
DATR2	OEV	DAT2	DAT2	X	OEV	OEV
DATR3	X	DAT3	DAT3	X	X	X
DATR4	UD	DAT4	DAT4	X	UD	UD
DATR5	X	DAT5	DAT5	X	X	X
DATR6	CKV	DAT6	DAT6	X	CKV	CKV
DATR7	X	DAT7	DAT7	X	X	X
DATR8	STV1	DAT8	DAT8	X	STV1	STV1
DATR9	X	DAT9	DAT9	X	X	X
DATR10	STV2	DAT10	DAT10	X	STV2	STV2
DATR11	X	DAT11	DAT11	X	X	X
DATR12	STV1	DAT12	DAT12	X	STV1	STV1
DATR13	X	DAT13	DAT13	X	X	X
DATR14	X	DAT14	DAT14	X	X	X
DATR15	X	DAT15	DAT15	X	X	X
DATR16	STBN	DAT16	DAT16	X	STBN	STBN
DATR17	X	DAT17	DAT17	X	X	X
DCLKR	X	DCLK	DCLK	X	X	X
DIOR	X	DIO	DIO	X	X	X
LDR	X	LD	LD	X	X	X
SYNCR	X	SYNC	SYNC	X	X	X
DATL0	DAT0	X	X	DAT0	X	X
DATL1	DAT1	X	X	DAT1	X	X
DATL2	DAT2	OEV	X	DAT2	OEV	OEV
DATL3	DAT3	X	X	DAT3	X	X
DATL4	DAT4	UD	X	DAT4	UD	UD
DATL5	DAT5	X	X	DAT5	X	X
DATL6	DAT6	CKV	X	DAT6	CKV	CKV
DATL7	DAT7	X	X	DAT7	X	X
DATL8	DAT8	STV1	X	DAT8	STV1	STV1
DATL9	DAT9	X	X	DAT9	X	X
DATL10	DAT10	STV2	X	DAT10	STV2	STV2
DATL11	DAT11	X	X	DAT11	X	X
DATL12	DAT12	STV1	X	DAT12	STV1	STV1
DATL13	DAT13	X	X	DAT13	X	X
DATL14	DAT14	X	X	DAT14	X	X
DATL15	DAT15	X	X	DAT15	X	X
DATL16	DAT16	STBN	X	DAT16	STBN	STBN
DATL17	DAT17	X	X	DAT17	X	X
DCLKL	DCLK	X	X	DCLK	X	X
DIOL	DIO	X	X	DIO	X	X
LDL	LD	X	X	LD	X	X
SYNCL	SYNC	X	X	SYNC	X	X

5. 3-WIRE SERIAL PORT INTERFACE

5.1. 3-Wire Command Format

EK9716 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. EK9716 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of "3-Wire Timing Diagram" for the detail timing.
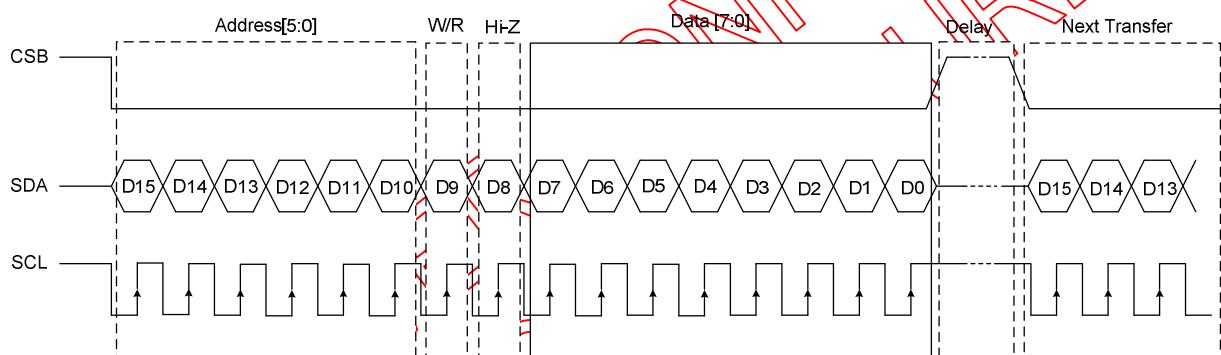
Figure 5. 3-Wire timing chart

Table 5. 3-Wire Command Format

Bit	Description
D15 – D10	Register Address [5:0].
D9	W/R control bit. "0" for Write; "1" for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7 – D0	Data for the W/R operation to the address indicated by Address phase

Table 6. 3-Wire Writer Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	DATA (Issue by external controller)							

Table 7. 3-Wire Read Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	DATA (Issue by 3-Wire engine)							

5.2. 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for EK9716. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

5.3. 3-Wire Control Register List

NO.	Address						R/W	D8	MSB			Initial value				LSB
	D15	D14	D13	D12	D11	D10	D9		D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	R/W(0)	X	RES[1]	RES[0]	SHLR	UPDN	STBYB	GRB	DCLKP	MODE
									0	0	1	0	1	1	0	1
R1	0	0	0	0	0	1	R/W(0)	X	NBWB	CFSEL	SCI_ON	CABC_E N[1]	CABC_ EN[0]	HFRC	DITHB	BIST
									1	1	0	0	0	1	1	0

Note:
1. The register except upper list was for testing use, to write test register was not allowed.

Table 8. R0: System Control Register

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control and driver are off. All outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S1200=First data. SHLR="1", Shift right: First data=S1->S2->S3 … ->S1200=Last data. (Default)
RES[1:0]	R0[7:6]	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution.(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution. RES[1:0] = "10", for 400(RGB)*480 display resolution. RES[1:0] = "11", for 400(RGB)*240 display resolution.

Table 9. R1: System Control Register

Designation	Address	Description
BIST	R1[0]	Normal Operation/BIST pattern select. BIST = "0" : Normal Operation (Default) BIST = "1" : BIST(DCLK input is not needed)
DITHB	R1[1]	Dithering function enable control. Normally pull high DITHB = "0", Enable internal dithering function. DITHB = "1", Disable internal dithering function.(Default)
HFRC	R1[2]	H-FRC selection. HFRC = "0" : FRC enable. (Default) HFRC = "1" : HiFRC enable. If DITHER = "0" , disable dithering function(HiFRC and FRC disable)
CABC_EN[1:0]	R1[4:3]	CABC H/W enable pin. Normally pull low. When CABC_EN="00", CABC OFF. (Default mode) When CABC_EN="01", User interface Image. When CABC_EN="10", Still Picture. When CABC_EN="11", Moving Image.
SCI_ON	R1[5]	Enable 3-wire control function. Normally pull low SCI_ON = "0" : Base on pin control function. (Default) SCI_ON = "1" : Base on 3-wire register.
CFSEL	R1[6]	Color Filter type selection. Normally pull high CFSEL = "0", Delta mode CFSEL = "1", Stripe mode. (Default)
NBWB	R1[7]	Normally black or normally white setting. NBWB = "0" : Normally black NBWB = "1" : Normally white (Default)

6. FUNCTION DESCRIPTION

6.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to "AC Characteristics" for more detail on timing.
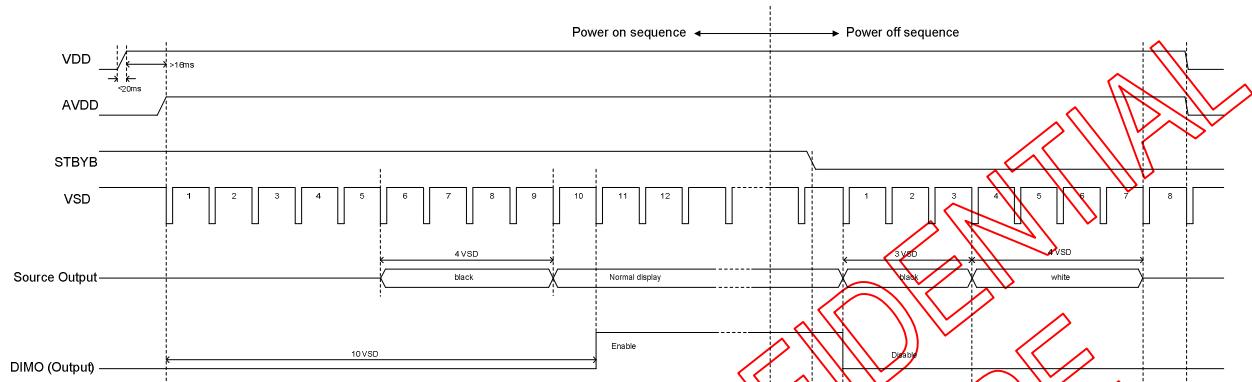
Figure 6. Power-On/Off Timing Sequence
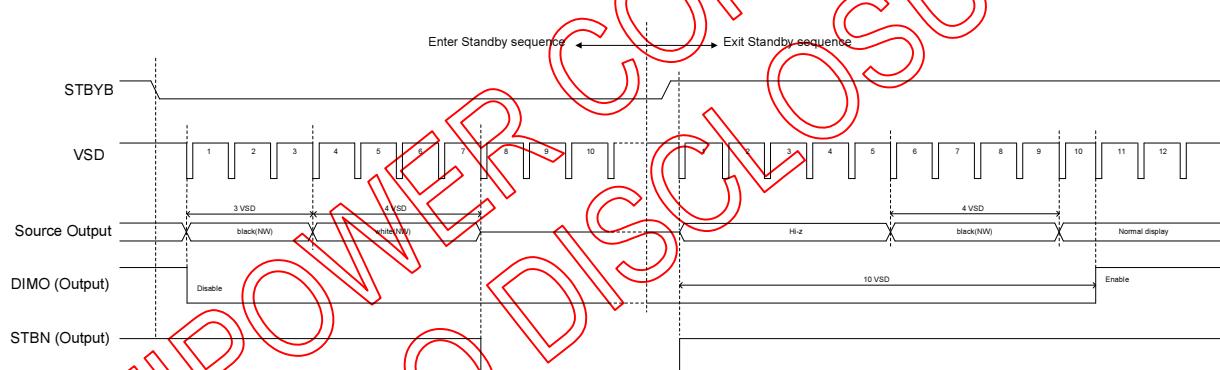
Figure 7. Enter and Exit Standby Mode Sequence

6.2. Input Data VS Output Channels

6.2.1. DBGATE="0", CFSEL="1", Stripe Mode

Table 10. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

Table 11. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

6.2.2. DBGATE="0", CFSEL="0", Delta Mode

Table 12. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DG[07:00]	DB[07:00]	DR[07:00]	---	DG[07:00]	DB[07:00]	DR[07:00]

Table 13. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DG[07:00]	DB[07:00]	DR[07:00]	---	DG[07:00]	DB[07:00]	DR[07:00]

6.2.3. DBGATE="1", CFSEL="1", Stripe Mode

Table 14. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]		DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

Table 15. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]		DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

6.2.4. DBGATE="1", CFSEL="0", Delta Mode

Table 16. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order		First data		→		Last data	
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn+1	DB[07:00]	DG[07:00]	DR[07:00]	---	DB[07:00]	DG[07:00]	DR[07:00]

Table 17. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order		Last data		←		First data	
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn+1	DB[07:00]	DG[07:00]	DR[07:00]	---	DB[07:00]	DG[07:00]	DR[07:00]

6.3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.
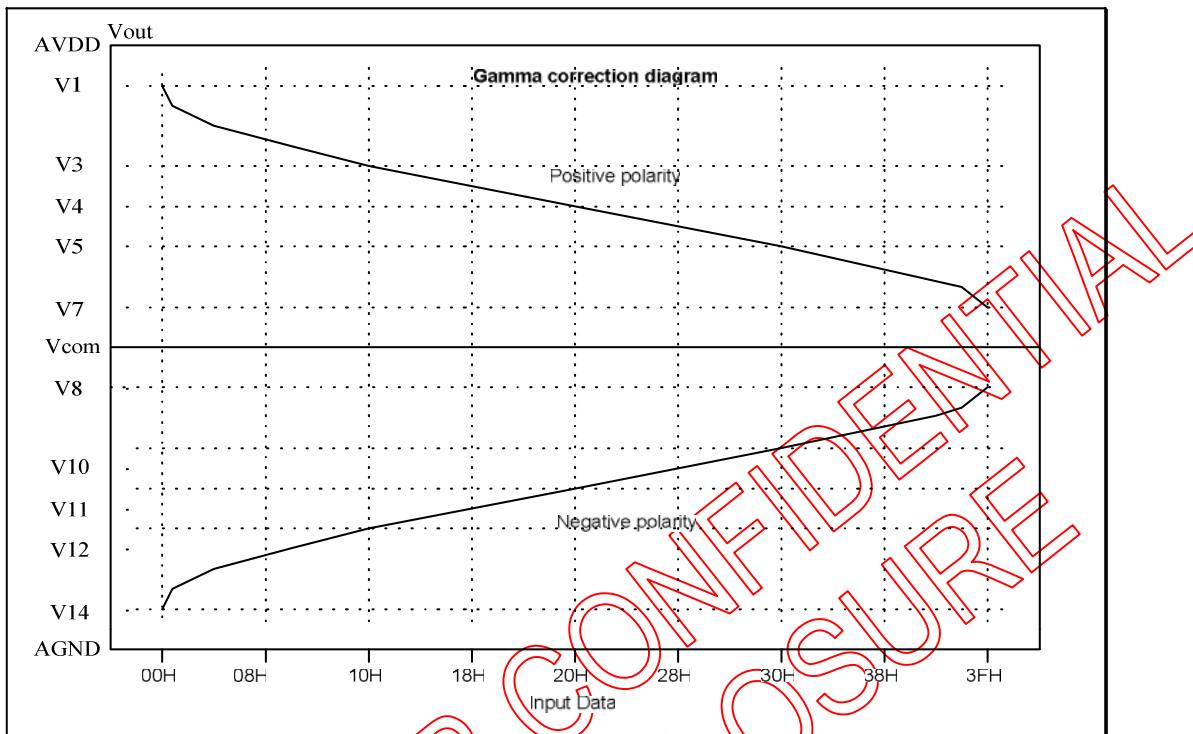
Remark:
Dual Gate：VDDA-0.1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+0.1V
Cascade：VDDA-1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+1V

6.4. Input Data and Output Voltage Reference Table

Table 18. Gamma correction resistor ratio

V1, V14 →

V4, V11 ←

Name	Resistor	Name	Resistor
R0	8.0	R32	0.63
R1	7.11	R33	0.63
R2	6.22	R34	0.63
R3	5.33	R35	0.62
R4	4.45	R36	0.62
R5	3.56	R37	0.62
R6	2.97	R38	0.62
R7	2.48	R39	0.61
R8	2.14	R40	0.61
R9	1.89	R41	0.61
R10	1.69	R42	0.62
R11	1.54	R43	0.63
R12	1.39	R44	0.64
R13	1.28	R45	0.64
R14	1.21	R46	0.65
R15	1.14	R47	0.67
R16	1.05	R48	0.68
R17	1	R49	0.69
R18	0.94	R50	0.71
R19	0.91	R51	0.75
R20	0.87	R52	0.78
R21	0.84	R53	0.82
R22	0.81	R54	0.89
R23	0.78	R55	0.98
R24	0.76	R56	1.08
R25	0.73	R57	1.21
R26	0.71	R58	1.36
R27	0.7	R59	1.59
R28	0.68	R60	1.98
R29	0.67	R61	3.44
R30	0.66	R62	27.28
R31	0.64		

V3, V12 → (at R15)

V5, V10 ← (at R47)

V7, V8 ← (at R62)

V4, V11 → (at R31)

Table 19. Output Voltage VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	V3 + (V1 − V3) X 44.4 / 52.4	V14+ (V12 − V14) X 8 / 52.4
02H	V3 + (V1 − V3) X 37.29 / 52.4	V14+ (V12 − V14) X 15.11 / 52.4
03H	V3 + (V1 − V3) X 31.06 / 52.4	V14+ (V12 − V14) X21.34 / 52.4
04H	V3 + (V1 − V3) X 25.73 / 52.4	V14+ (V12 − V14) X 26.67 / 52.4
05H	V3 + (V1 − V3) X 21.28 / 52.4	V14+ (V12 − V14) X 31.12 / 52.4
06H	V3 + (V1 − V3) X 17.73 / 52.4	V14+ (V12 − V14) X 34.67 / 52.4
07H	V3 + (V1 − V3) X 14.76 / 52.4	V14+ (V12 − V14) X 37.64 / 52.4
08H	V3 + (V1 − V3) X 12.28 / 52.4	V14+ (V12 − V14) X 40.11 / 52.4
09H	V3 + (V1 − V3) X 10.14 / 52.4	V14+ (V12 − V14) X 42.26 / 52.4
0AH	V3 + (V1 − V3) X 8.25 / 52.4	V14+ (V12 − V14) X 44.15 / 52.4
0BH	V3 + (V1 − V3) X 6.56 / 52.4	V14+ (V12 − V14) X 45.84 / 52.4
0CH	V3 + (V1 − V3) X 5.02 / 52.4	V14+ (V12 − V14) X 47.38 / 52.4
0DH	V3 + (V1 − V3) X 3.64 / 52.4	V14+ (V12 − V14) X 48.76 / 52.4
0EH	V3 + (V1 − V3) X 2.36 / 52.4	V14+ (V12 − V14) X 50.04 / 52.4
0FH	V3 + (V1 − V3) X 1.14 / 52.4	V14+ (V12 − V14) X 51.26 / 52.4
10H	V3	V12
11H	V4 + (V3 − V4) X 11.7 / 12.75	V12 + (V11 − V12) X 1.05 / 12.75
12H	V4 + (V3 − V4) X 10.7 / 12.75	V12 + (V11 − V12) X 2.05 / 12.75
13H	V4 + (V3 − V4) X 9.76 / 12.75	V12 + (V11 − V12) X 2.99 / 12.75
14H	V4 + (V3 − V4) X 8.85 / 12.75	V12 + (V11 − V12) X 3.9 / 12.75
15H	V4 + (V3 − V4) X 7.98 / 12.75	V12 + (V11 − V12) X 4.77 / 12.75
16H	V4 + (V3 − V4) X 7.14 / 12.75	V12 + (V11 − V12) X 5.61 / 12.75
17H	V4 + (V3 − V4) X 6.33 / 12.75	V12 + (V11 − V12) X 6.41 / 12.75
18H	V4 + (V3 − V4) X 5.55 / 12.75	V12 + (V11 − V12) X 7.19 / 12.75
19H	V4 + (V3 − V4) X 4.8 / 12.75	V12 + (V11 − V12) X 7.95 / 12.75
1AH	V4 + (V3 − V4) X 4.06 / 12.75	V12 + (V11 − V12) X 8.68 / 12.75
1BH	V4 + (V3 − V4) X 3.35 / 12.75	V12 + (V11 − V12) X 9.4 / 12.75
1CH	V4 + (V3 − V4) X 2.65 / 12.75	V12 + (V11 − V12) X10.09/ 12.75
1DH	V4 + (V3 − V4) X 1.97 / 12.75	V12 + (V11 − V12) X10.78/ 12.75
1EH	V4 + (V3 − V4) X 1.3 / 12.75	V12 + (V11 − V12) X11.44/ 12.75
1FH	V4 + (V3 − V4) X 0.65 / 12.75	V12 + (V11 − V12) X 12.1 / 12.75

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	V5 + (V4 – V5) X 9.37 / 10	V11 + (V10 – V11) X 0.63 / 10
22H	V5 + (V4 – V5) X 8.74 / 10	V11 + (V10 – V11) X 1.26 / 10
23H	V5 + (V4 – V5) X 8.11 / 10	V11 + (V10 – V11) X 1.89 / 10
24H	V5 + (V4 – V5) X 7.49 / 10	V11 + (V10 – V11) X 2.51 / 10
25H	V5 + (V4 – V5) X 6.87 / 10	V11 + (V10 – V11) X 3.13 / 10
26H	V5 + (V4 – V5) X 6.25 / 10	V11 + (V10 – V11) X 3.75 / 10
27H	V5 + (V4 – V5) X 5.63 / 10	V11 + (V10 – V11) X 4.36 / 10
28H	V5 + (V4 – V5) X 5.02 / 10	V11 + (V10 – V11) X 4.98 / 10
29H	V5 + (V4 – V5) X 4.41 / 10	V11 + (V10 – V11) X 5.59 / 10
2AH	V5 + (V4 – V5) X 3.8 / 10	V11 + (V10 – V11) X 6.2 / 10
2BH	V5 + (V4 – V5) X 3.18 / 10	V11 + (V10 – V11) X 6.82 / 10
2CH	V5 + (V4 – V5) X 2.55 / 10	V11 + (V10 – V11) X 7.45 / 10
2DH	V5 + (V4 – V5) X 1.91 / 10	V11 + (V10 – V11) X 8.08 / 10
2EH	V5 + (V4 – V5) X 1.27 / 10	V11 + (V10 – V11) X 8.72 / 10
2FH	V5 + (V4 – V5) X 0.62 / 10	V11 + (V10 – V11) X 9.38 / 10
30H	V5	V10
31H	V7 + (V5 – V7) X 43.58 / 44.25	V10 + (V8 – V10) X 0.8 / 44.25
32H	V7 + (V5 – V7) X 42.89 / 44.25	V10 + (V8 – V10) X 1.37 / 44.25
33H	V7 + (V5 – V7) X 42.18 / 44.25	V10 + (V8 – V10) X 2.08 / 44.25
34H	V7 + (V5 – V7) X 41.42 / 44.25	V10 + (V8 – V10) X 2.83 / 44.25
35H	V7 + (V5 – V7) X 40.64 / 44.25	V10 + (V8 – V10) X 3.61 / 44.25
36H	V7 + (V5 – V7) X 39.82 / 44.25	V10 + (V8 – V10) X 4.43 / 44.25
37H	V7 + (V5 – V7) X 38.93 / 44.25	V10 + (V8 – V10) X 5.33 / 44.25
38H	V7 + (V5 – V7) X 37.94 / 44.25	V10 + (V8 – V10) X 6.31 / 44.25
39H	V7 + (V5 – V7) X 36.86 / 44.25	V10 + (V8 – V10) X 7.39 / 44.25
3AH	V7 + (V5 – V7) X 35.66 / 44.25	V10 + (V8 – V10) X 8.6 / 44.25
3BH	V7 + (V5 – V7) X 34.29/ 44.25	V10 + (V8 – V10) X 9.96 / 44.25
3CH	V7 + (V5 – V7) X 32.7 / 44.25	V10 + (V8 – V10) X 11.5 / 44.25
3DH	V7 + (V5 – V7) X 30.73 / 44.25	V10 + (V8 – V10) X 13.5 / 44.25
3EH	V7 + (V5 – V7) X 27.28 / 44.25	V10 + (V8 – V10) X 16.9 / 44.25
3FH	V7	V8

6.5. Data Input Format
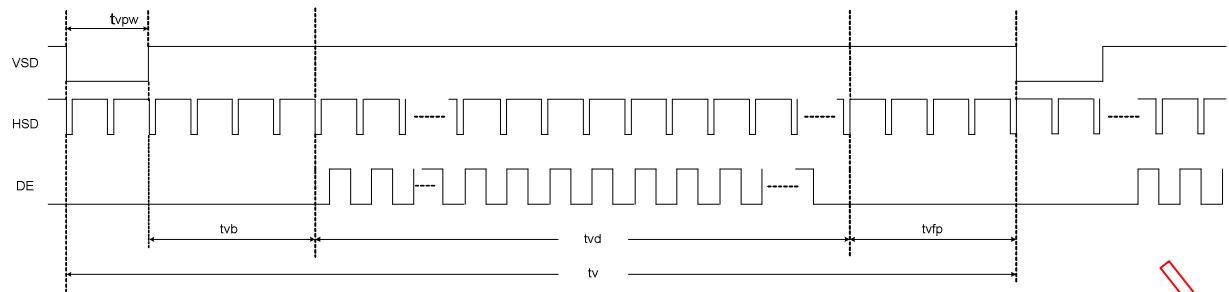
Figure 8. Vertical input timing
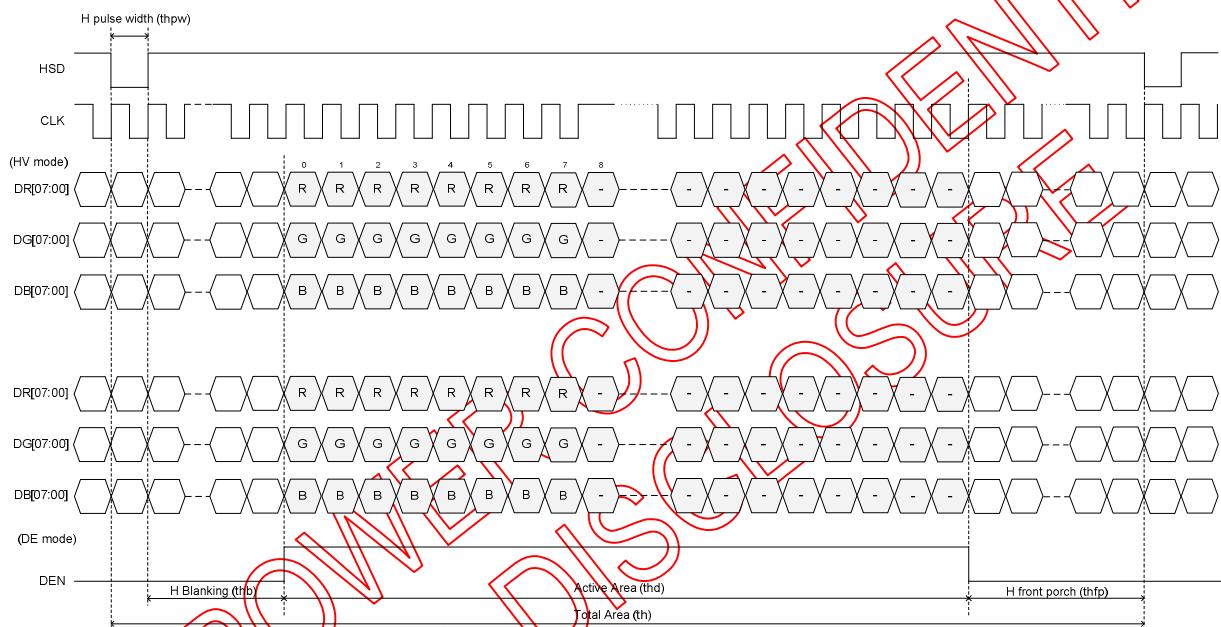
Figure 9. Horizontal input timing

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Preliminary **EK9716**

6.6. Timing Characteristic

6.6.1. For 800 × 480 panel

Table 20. Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		20	33.3	50	MHz	
1 Horizontal Line	th	908	928	1088	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	40	200		

Table 21. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd		480		H	
VSD period time	tv	517	525	712	H	tvpw+tvb=32H is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

6.6.2. For 800 × 600 panel

Table 22. Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		20	40	50	MHz	
1 Horizontal Line	th	908	1000	1088	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	112	200		

Table 23. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd		600		H	
VSD period time	tv	644	660	839	H	tvpw+tvb=39H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	38	38	36	H	
VSD Front Porch	tvfp	5	21	200	H	

6.6.3. For 400 × 480 panel

Table 24. Horizontal input timing

Parameter	Symbol	Value			Unit	
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		1	16.4	50	MHz	
1 Horizontal Line	th	508	520	688	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

Table 25. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Vertical display area	tvd		480		H	
VSD period time	tv	517	525	712	H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

6.6.4. For 400 × 240 panel

Table 26. Horizontal input timing

Parameter	Symbol	Value			Unit	
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		1	8.5	50	MHz	
1 Horizontal Line	th	508	520	688	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	47		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

Table 27. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Vertical display area	tvd		240		H	
VSD period time	tv	262	270	457	H	tvpw+tvb=17H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	16	16	14	H	
VSD Front Porch	tvfp	5	13	200	H	

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

Table 28. VOLTAGE (TA = 25℃, VSS = VSSA = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.5	+5.0	V
Analog Supply Voltage, VDDA, V1~V14	-0.5	+15.0	V

Table 29. TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	℃
Storage temperature	-55	+125	℃

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Range

Table 30. Recommended Operating Range (TA = -20 to 85℃, VSS = VSSA = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	2.7	3.3	3.6	V
Analog supply voltage	VDDA	6.5	-	13.5	V
Digital input voltage	VIN	0	-	VDD	V

7.3. DC Characteristics

Table 31. DC Characteristics

(TA = -20 to 85℃, VDD = 2.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	µA
High level output voltage	Voh	Ioh= -400 µA	VDD-0.4	-	-	V
Low level output voltage	Vol	Iol= +400 µA	-	-	VSS+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	200K	250K	300K	ohm
Digital Operation current	Idd	Fclk=50 MHz, FLD=48KHz, VDD=3.3V	-	14	18	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	µA
Analog Operating Current	Idda	No load, Fclk=50MHz, FLD=48KHz @ VDDA=10V,V1=8V, V14=0.4V	-	7	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are stopped	-	10	50	µA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input(Cascade Mode)	0.4*VDDA	-	VDDA-1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input(Cascade Mode)	VSSA+1	-	0.6*VDDA	V
Input level of V1 ~ V7	Vref3	Gamma correction voltage input(Dual Gate Mode)	0.4*VDDA	-	VDDA-0.1	V
Input level of V8 ~ V14	Vref4	Gamma correction voltage input(Dual Gate Mode)	VSSA+0.1	-	0.6*VDDA	V
Output Voltage deviation	Vod1	Vo = VSSA+0.1V ~ VSSA+0.5V and Vo = VDDA-0.5V ~ VDDA-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = VSSA+0.5V ~ VDDA-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = VSSA+0.5V ~ VDDA-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1200	0.1	-	VDDA-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1200; Vo=0.1V v.s 1.0V , VDDA=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1200; Vo=13.4V v.s 12.5V , VDDA=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

7.4. AC Characteristics

Table 32. AC Characteristics

(TA = -20 to 85℃, VDD = 2.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD Power On Slew rate	T_{POR}	From 0V to 90% VDD	-	-	20	ms
RSTB pulse width	T_{RST}	CLKIN = 50MHz	50	-	-	us
CLKIN cycle time	Tcph	-	20	-	-	ns
CLKIN pulse duty	Tcwh	-	40	50	60	%
VSD setup time	Tvst	-	8	-	-	ns
VSD hold time	Tvhd	-	8	-	-	ns
HSD setup time	Thst	-	8	-	-	ns
HSD hold time	Thhd	-	8	-	-	ns
Data set-up time	Tdsu	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
Data hold time	Tdhd	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
DEN setup time	Tesu	-	8	-	-	ns
DEN hold time	Tehd	-	8	-	-	ns
Output stable time	Tsst	10% to 90% target voltage. CL=120pF, R=10K ohm	-	-	6	us

7.5. Timing Table

Table 33. Parallel 24-bit RGB Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKIN Frequency	Fclk	VDD = 3.0V ~3.6V	-	40	50	MHz
CLKIN Cycle Time	Tclk	-	20	25	-	ns
CLKIN Pulse Duty	Tcwh	Tclk	40	50	60	%
Time from HSD to Source Output	Thso	-	-	64	-	CLKIN
Time from HSD to LD	Thld	-	-	64	-	CLKIN
Time from HSD to STV	Thstv	-	-	2	-	CLKIN
Time from HSD to CKV	Thckv	-	-	20	-	CLKIN
Time from HSD to OEV	Thoev	-	-	4	-	CLKIN
LD Pulse Width	Twld			10		CLKIN
CKV Pulse Width	Twckv	-	-	66	-	CLKIN
OEV Pulse Width	Twoev	-	-	74	-	CLKIN

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7.6. Timing Waveform
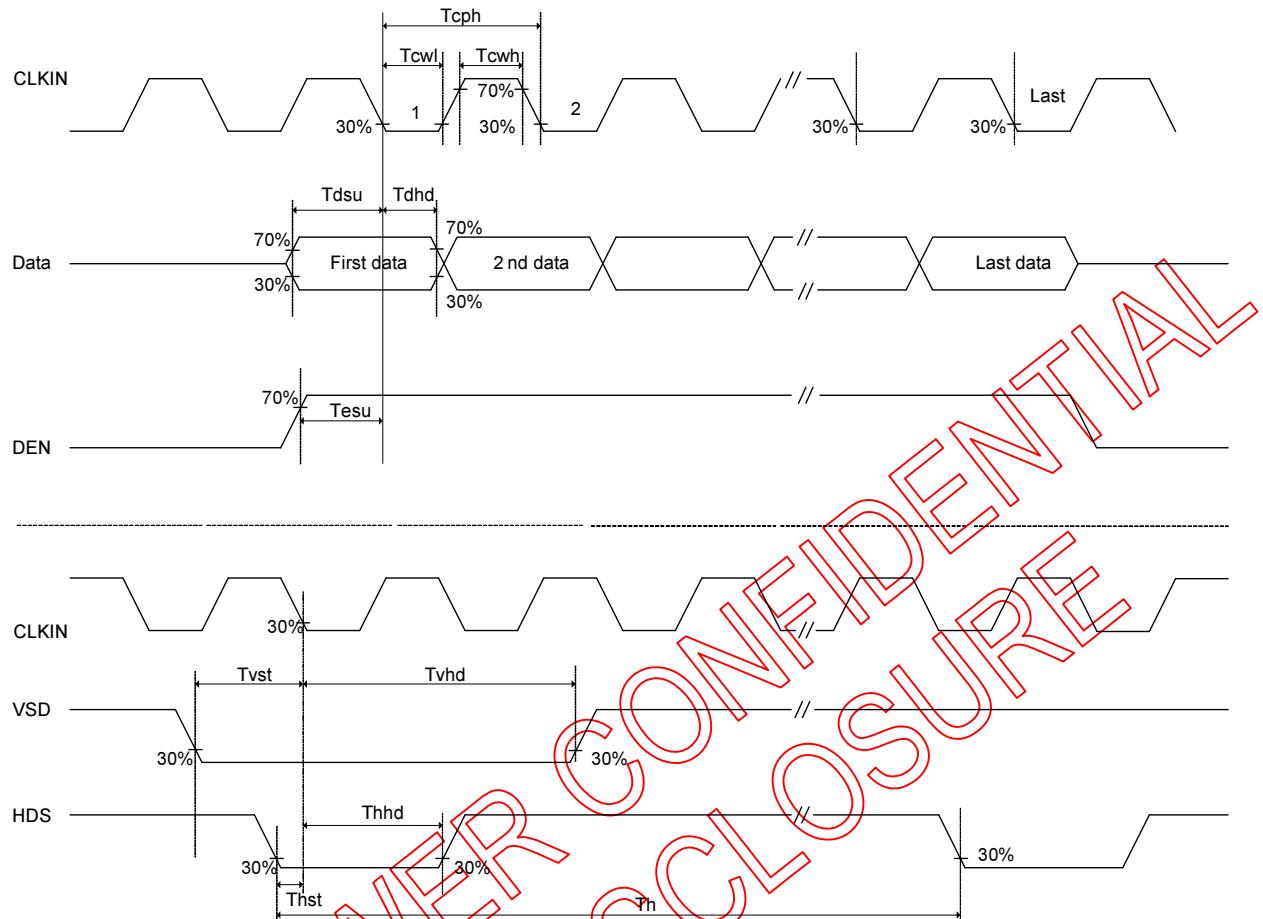
Figure 10. Input Clock and Data Timing Diagram
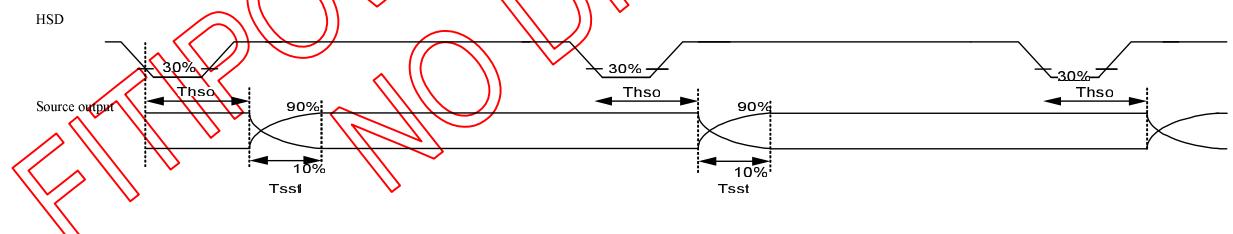
Figure 11. Source Output Timing Diagram(Cascade)
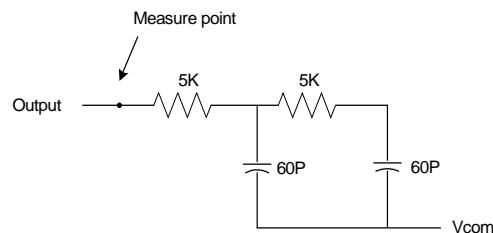
Figure 12. Output load condition
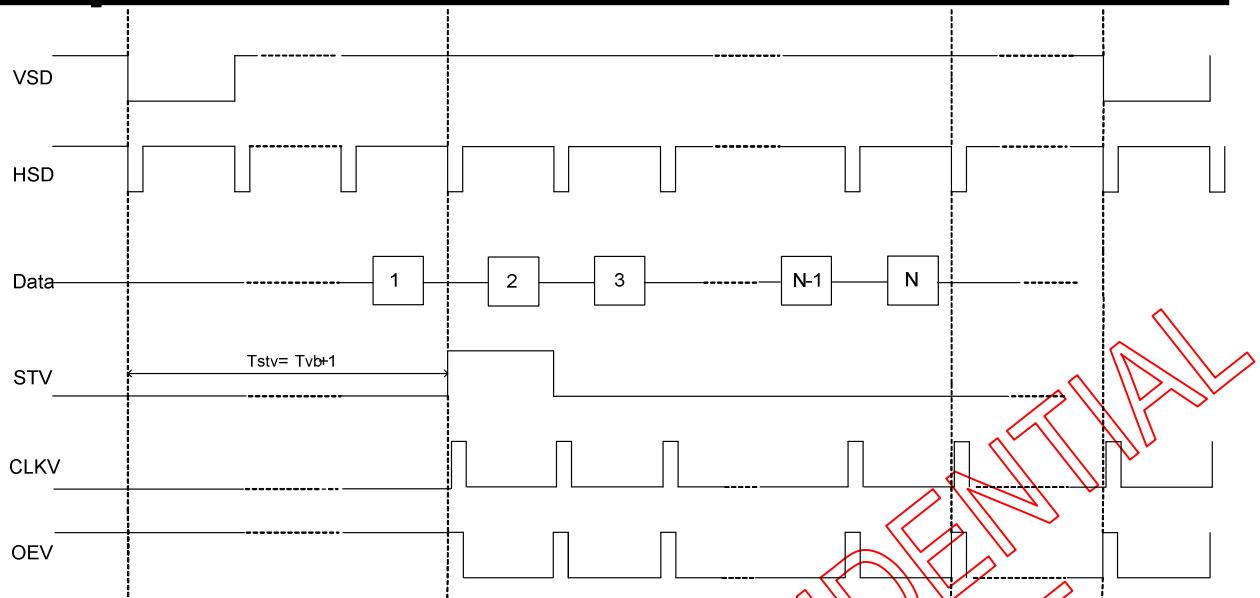
Figure 13. Vertical Timing Diagram HV (Cascade)
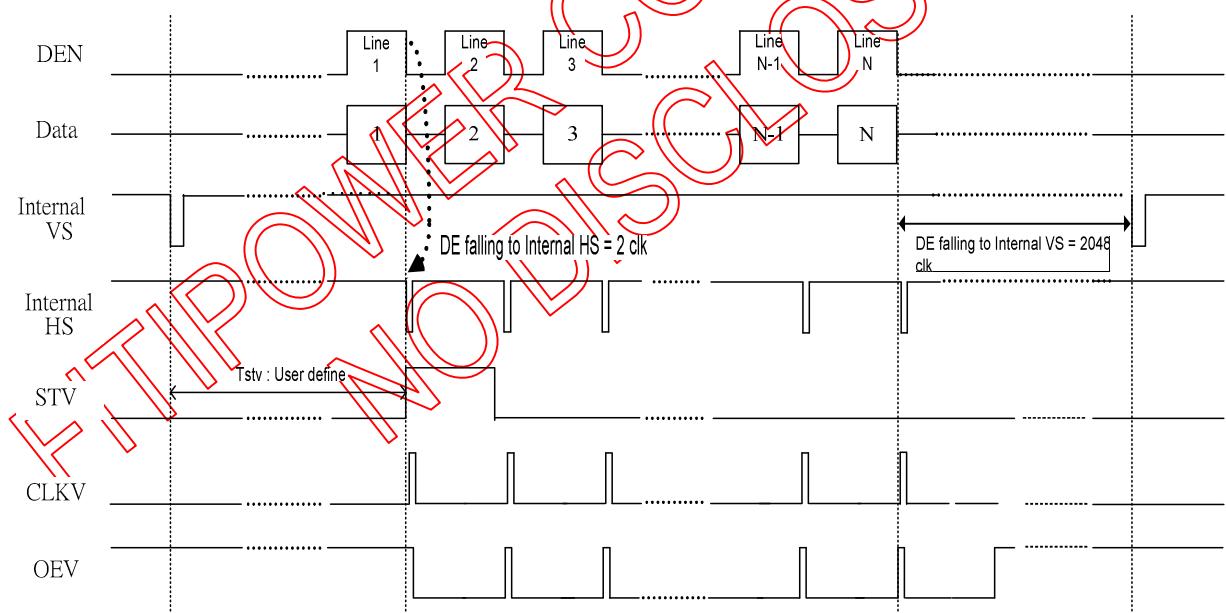
Figure 14. Vertical Timing Diagram DE (Cascade)
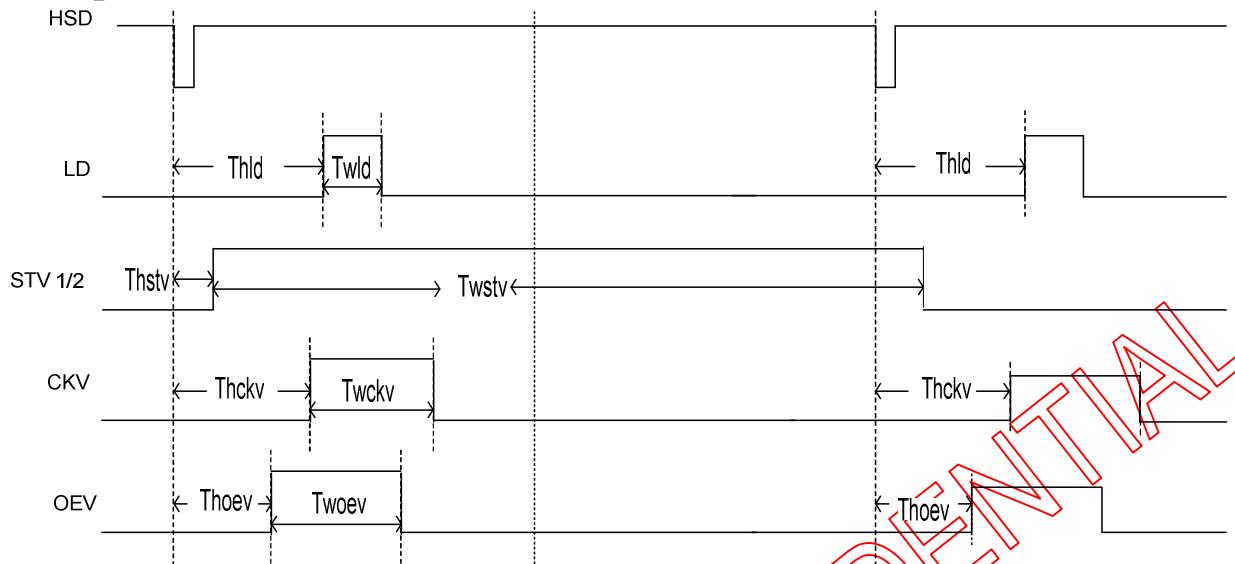
Figure 15. Gate Output Timing Diagram (Cascade)
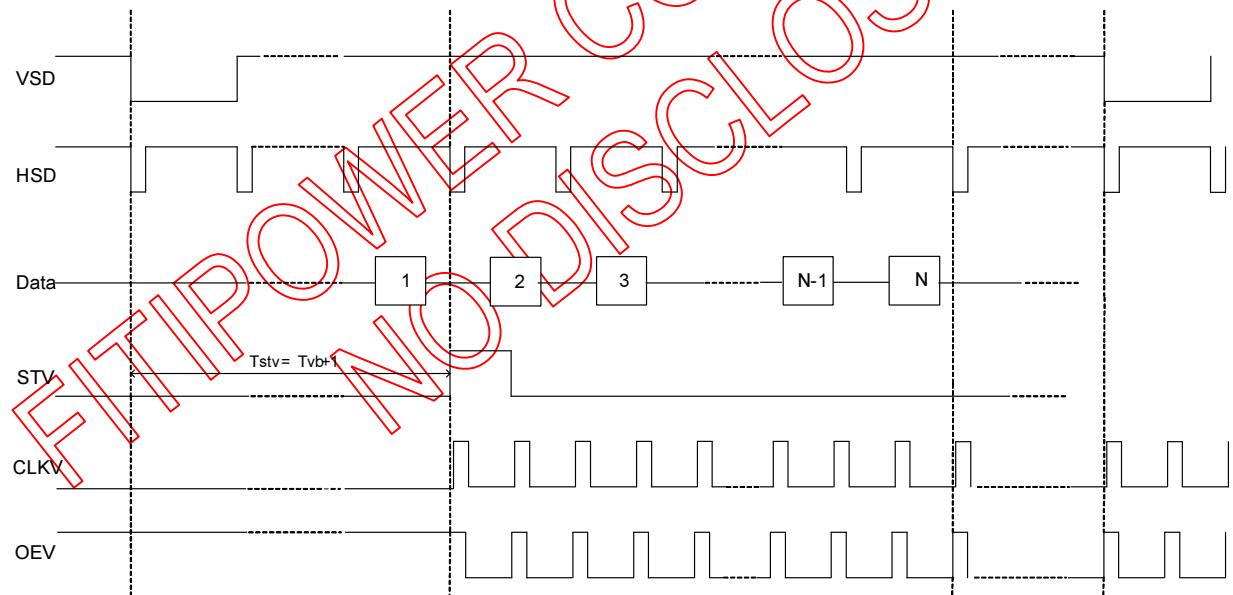
Figure 16. Vertical Timing Diagram HV (Dual Gate)
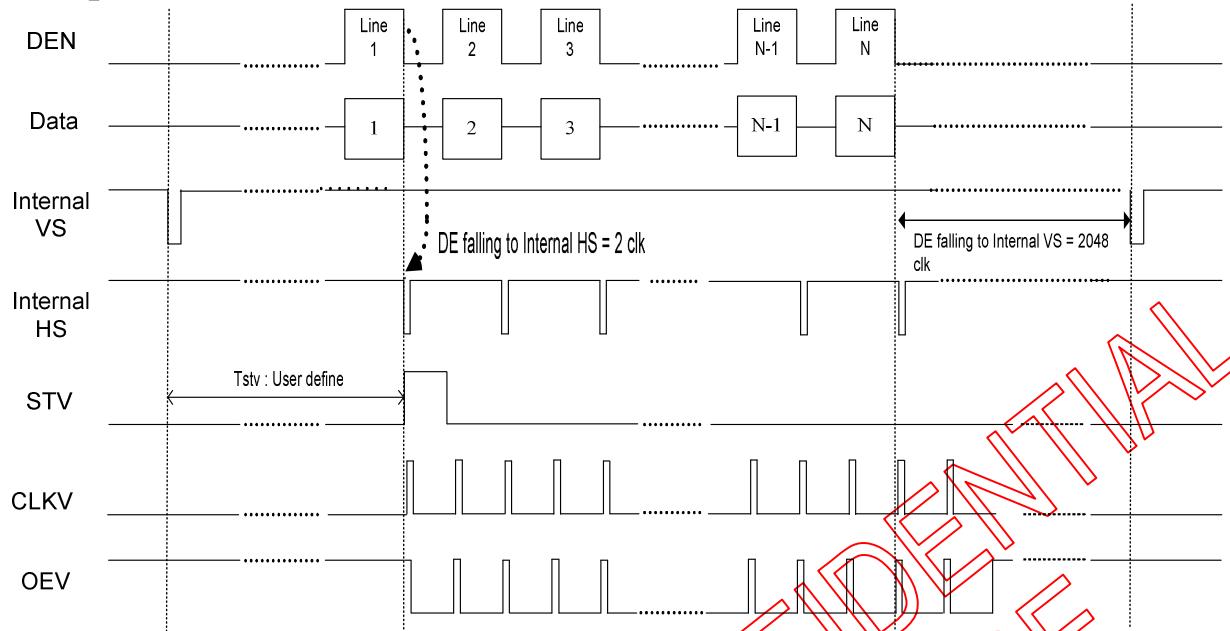
Figure 17. Vertical Timing Diagram DE (Dual Gate)
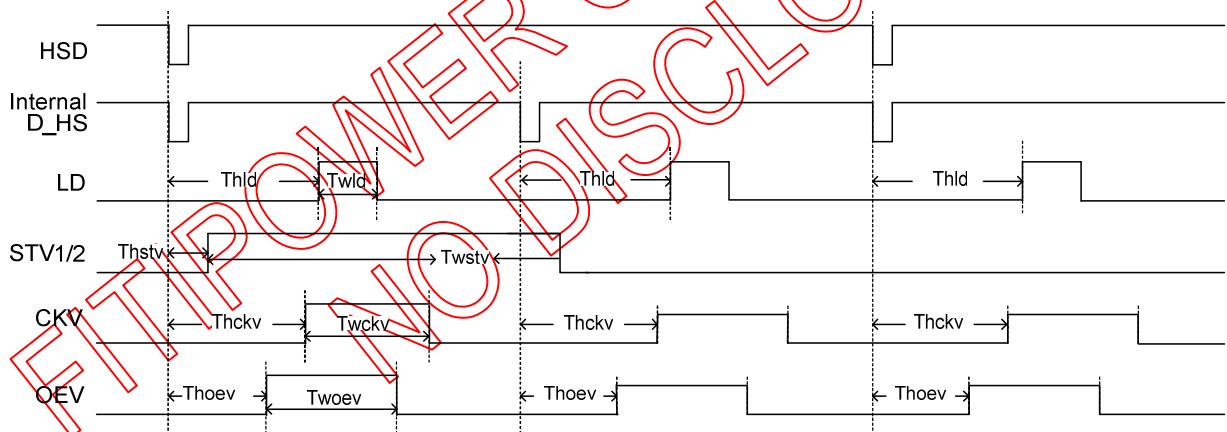
Figure 18. Gate Output Timing Diagram (Dual Gate)

8. PAD OUTLINE DIMENSION
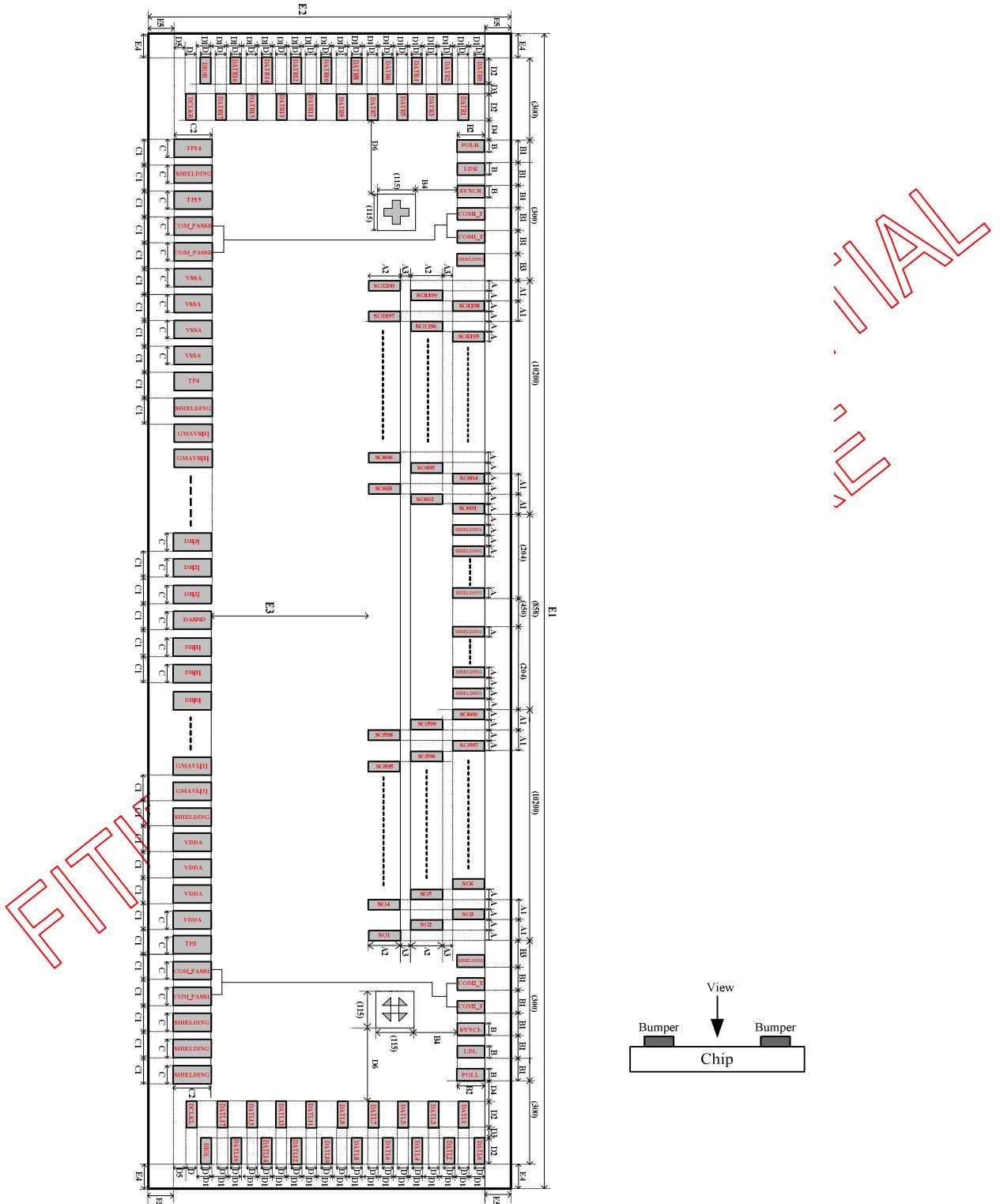
Figure 19. Pad Outline Dimension (Bump Side)

8.1. Alignment Mark

Alignment mark dimension (unit:um)

Left side   Right side
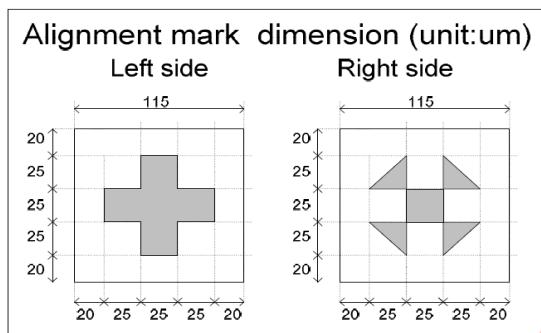
Figure 20. Alignment Mark

8.2. Pad Information

Symbol	Dimension(um)
A	17
A1	34
A2	110
A3	30
B	30
B1	50
B2	70
B3	50
B4	191.5
C	65
C1	85
C2	110

Symbol	Dimension(um)
D	30
D1	40
D2	100
D3	30
D4	70
D5	34
D6	168.5
E1	22572 (max) *
E2	938 (max) *
E3	324
E4	57 (max)
E5	57 (max)

*Note：Chip dimension includes scribe line

fitipower

Preliminary**EK9716**

8.3. Pad Coordinates

No	Name	CX	CY	No	Name	CX	CY	No	Name	CX	CY
1	TP14	-10922.5	-357	36	GMAVR[9]	-7947.5	-357	72	TP5	-4887.5	-357
2	SHIELDING[1]	-10837.5	-357	37	GMAVR[9]	-7862.5	-357	73	VSS	-4802.5	-357
3	TP15	-10752.5	-357	38	SHIELDING[11]	-7777.5	-357	74	VSS	-4717.5	-357
4	COM_PASSR	-10667.5	-357	39	GMAVR[10]	-7692.5	-357	75	VSS	-4632.5	-357
5	COM_PASSR	-10582.5	-357	40	GMAVR[10]	-7607.5	-357	76	VSS	-4547.5	-357
6	VSSA	-10497.5	-357	41	SHIELDING[12]	-7522.5	-357	77	TP6	-4462.5	-357
7	VSSA	-10412.5	-357	42	GMAVR[11]	-7437.5	-357	78	DIMO	-4377.5	-357
8	VSSA	-10327.5	-357	43	GMAVR[11]	-7352.5	-357	79	DIMO	-4292.5	-357
9	VSSA	-10242.5	-357	44	SHIELDING[13]	-7267.5	-357	80	TP7	-4207.5	-357
10	TP4	-10157.5	-357	45	GMAVR[12]	-7182.5	-357	81	VDD	-4122.5	-357
11	SHIELDING[2]	-10072.5	-357	46	GMAVR[12]	-7097.5	-357	82	VDD	-4037.5	-357
12	GMAVR[1]	-9987.5	-357	47	SHIELDING[14]	-7012.5	-357	83	VDD	-3952.5	-357
13	GMAVR[1]	-9902.5	-357	48	GMAVR[13]	-6927.5	-357	84	VDD	-3867.5	-357
14	SHIELDING[3]	-9817.5	-357	49	GMAVR[13]	-6842.5	-357	85	TP1	-3782.5	-357
15	GMAVR[2]	-9732.5	-357	50	SHIELDING[15]	-6757.5	-357	86	DBGATE	-3697.5	-357
16	GMAVR[2]	-9647.5	-357	51	GMAVR[14]	-6672.5	-357	87	DBGATE	-3612.5	-357
17	SHIELDING[4]	-9562.5	-357	52	GMAVR[14]	-6587.5	-357	88	CSB	-3527.5	-357
18	GMAVR[3]	-9477.5	-357	53	TP16	-6502.5	-357	89	MASL	-3442.5	-357
19	GMAVR[3]	-9392.5	-357	54	TP0	-6417.5	-357	90	MASL	-3357.5	-357
20	SHIELDING[5]	-9307.5	-357	55	SHIELDING[16]	-6332.5	-357	91	SCL	-3272.5	-357
21	GMAVR[4]	-9222.5	-357	56	SHIELDING[17]	-6247.5	-357	92	MASLOC	-3187.5	-357
22	GMAVR[4]	-9137.5	-357	57	SHIELDING[18]	-6162.5	-357	93	MASLOC	-3102.5	-357
23	SHIELDING[6]	-9052.5	-357	58	SHIELDING[19]	-6077.5	-357	94	SDA	-3017.5	-357
24	GMAVR[5]	-8967.5	-357	59	REV	-5992.5	-357	95	RES[0]	-2932.5	-357
25	GMAVR[5]	-8882.5	-357	60	BIST	-5907.5	-357	96	RES[0]	-2847.5	-357
26	SHIELDING[7]	-8797.5	-357	61	BIST	-5822.5	-357	97	CABC_EN[0]	-2762.5	-357
27	GMAVR[6]	-8712.5	-357	62	TP17	-5737.5	-357	98	CABC_EN[1]	-2677.5	-357
28	GMAVR[6]	-8627.5	-357	63	VDDA	-5652.5	-357	99	RES[1]	-2592.5	-357
29	SHIELDING[8]	-8542.5	-357	64	VDDA	-5567.5	-357	100	RES[1]	-2507.5	-357
30	GMAVR[7]	-8457.5	-357	65	VDDA	-5482.5	-357	101	CFSEL	-2422.5	-357
31	GMAVR[7]	-8372.5	-357	66	VDDA	-5397.5	-357	102	CFSEL	-2337.5	-357
32	SHIELDING[9]	-8287.5	-357	67	SHIELDING[20]	-5312.5	-357	103	DASHD[1]	-2252.5	-357
33	GMAVR[8]	-8202.5	-357	68	VSSA	-5227.5	-357	104	VSD	-2167.5	-357
34	GMAVR[8]	-8117.5	-357	69	VSSA	-5142.5	-357	105	VSD	-2082.5	-357
35	SHIELDING[10]	-8032.5	-357	70	VSSA	-5057.5	-357	106	DASHD[2]	-1997.5	-357
				71	VSSA	-4972.5	-357	107	HSD	-1912.5	-357

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No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
108	HSD	-1827.5	-357	147	DG[3]	1487.5	-357	186	SHLR	4802.5	-357
109	DASHD[3]	-1742.5	-357	148	DG[2]	1572.5	-357	187	SHIELDING[21]	4887.5	-357
110	DEN	-1657.5	-357	149	DG[2]	1657.5	-357	188	UPDN	4972.5	-357
111	DEN	-1572.5	-357	150	DASHD[12]	1742.5	-357	189	UPDN	5057.5	-357
112	DASHD[4]	-1487.5	-357	151	DG[1]	1827.5	-357	190	TP10	5142.5	-357
113	CLKIN	-1402.5	-357	152	DG[1]	1912.5	-357	191	STBYB	5227.5	-357
114	CLKIN	-1317.5	-357	153	DG[0]	1997.5	-357	192	STBYB	5312.5	-357
115	DASHD[5]	-1232.5	-357	154	DG[0]	2082.5	-357	193	TP11	5397.5	-357
116	DB[7]	-1147.5	-357	155	DASHD[13]	2167.5	-357	194	RSTB	5482.5	-357
117	DB[7]	-1062.5	-357	156	DR[7]	2252.5	-357	195	RSTB	5567.5	-357
118	DB[6]	-977.5	-357	157	DR[7]	2337.5	-357	196	TP12	5652.5	-357
119	DB[6]	-892.5	-357	158	DR[6]	2422.5	-357	197	VDD	5737.5	-357
120	DASHD[6]	-807.5	-357	159	DR[6]	2507.5	-357	198	VDD	5822.5	-357
121	DB[5]	-722.5	-357	160	DASHD[14]	2592.5	-357	199	VDD	5907.5	-357
122	DB[5]	-637.5	-357	161	DR[5]	2677.5	-357	200	VDD	5992.5	-357
123	DB[4]	-552.5	-357	162	DR[5]	2762.5	-357	201	CAS	6077.5	-357
124	DB[4]	-467.5	-357	163	DR[4]	2847.5	-357	202	VSS	6162.5	-357
125	DASHD[7]	-382.5	-357	164	DR[4]	2932.5	-357	203	VSS	6247.5	-357
126	DB[3]	-297.5	-357	165	DASHD[15]	3017.5	-357	204	VSS	6332.5	-357
127	DB[3]	-212.5	-357	166	DR[3]	3102.5	-357	205	VSS	6417.5	-357
128	DB[2]	-127.5	-357	167	DR[3]	3187.5	-357	206	TP2	6502.5	-357
129	DB[2]	-42.5	-357	168	DR[2]	3272.5	-357	207	GMAVL[14]	6587.5	-357
130	DASHD[8]	42.5	-357	169	DR[2]	3357.5	-357	208	GMAVL[14]	6672.5	-357
131	DB[1]	127.5	-357	170	DASHD[16]	3442.5	-357	209	SHIELDING[22]	6757.5	-357
132	DB[1]	212.5	-357	171	DR[1]	3527.5	-357	210	GMAVL[13]	6842.5	-357
133	DB[0]	297.5	-357	172	DR[1]	3612.5	-357	211	GMAVL[13]	6927.5	-357
134	DB[0]	382.5	-357	173	DR[0]	3697.5	-357	212	SHIELDING[23]	7012.5	-357
135	DASHD[9]	467.5	-357	174	DR[0]	3782.5	-357	213	GMAVL[12]	7097.5	-357
136	DG[7]	552.5	-357	175	DASHD[17]	3867.5	-357	214	GMAVL[12]	7182.5	-357
137	DG[7]	637.5	-357	176	TP13	3952.5	-357	215	SHIELDING[24]	7267.5	-357
138	DG[6]	722.5	-357	177	MODE	4037.5	-357	216	GMAVL[11]	7352.5	-357
139	DG[6]	807.5	-357	178	MODE	4122.5	-357	217	GMAVL[11]	7437.5	-357
140	DASHD[10]	892.5	-357	179	CLKPOL	4207.5	-357	218	SHIELDING[25]	7522.5	-357
141	DG[5]	977.5	-357	180	CLKPOL	4292.5	-357	219	GMAVL[10]	7607.5	-357
142	DG[5]	1062.5	-357	181	TP8	4377.5	-357	220	GMAVL[10]	7692.5	-357
143	DG[4]	1147.5	-357	182	DITHB	4462.5	-357	221	SHIELDING[26]	7777.5	-357
144	DG[4]	1232.5	-357	183	DITHB	4547.5	-357	222	GMAVL[9]	7862.5	-357
145	DASHD[11]	1317.5	-357	184	TP9	4632.5	-357	223	GMAVL[9]	7947.5	-357
146	DG[3]	1402.5	-357	185	SHLR	4717.5	-357	224	SHIELDING[27]	8032.5	-357

225	GMAVL[8]	8117.5	-357	263	DATL[15]	11049	-203	301	SO[17]	10348.5	217
226	GMAVL[8]	8202.5	-357	264	DATL[14]	11179	-163	302	SO[18]	10331.5	357
227	SHIELDING[28]	8287.5	-357	265	DATL[13]	11049	-123	303	SO[19]	10314.5	77
228	GMAVL[7]	8372.5	-357	266	DATL[12]	11179	-83	304	SO[20]	10297.5	217
229	GMAVL[7]	8457.5	-357	267	DATL[11]	11049	-43	305	SO[21]	10280.5	357
230	SHIELDING[29]	8542.5	-357	268	DATL[10]	11179	-3	306	SO[22]	10263.5	77
231	GMAVL[6]	8627.5	-357	269	DATL[9]	11049	37	307	SO[23]	10246.5	217
232	GMAVL[6]	8712.5	-357	270	DATL[8]	11179	77	308	SO[24]	10229.5	357
233	SHIELDING[30]	8797.5	-357	271	DATL[7]	11049	117	309	SO[25]	10212.5	77
234	GMAVL[5]	8882.5	-357	272	DATL[6]	11179	157	310	SO[26]	10195.5	217
235	GMAVL[5]	8967.5	-357	273	DATL[5]	11049	197	311	SO[27]	10178.5	357
236	SHIELDING[31]	9052.5	-357	274	DATL[4]	11179	237	312	SO[28]	10161.5	77
237	GMAVL[4]	9137.5	-357	275	DATL[3]	11049	277	313	SO[29]	10144.5	217
238	GMAVL[4]	9222.5	-357	276	DATL[2]	11179	317	314	SO[30]	10127.5	357
239	SHIELDING[32]	9307.5	-357	277	DATL[1]	11049	357	315	SO[31]	10110.5	77
240	GMAVL[3]	9392.5	-357	278	DATL[0]	11179	397	316	SO[32]	10093.5	217
241	GMAVL[3]	9477.5	-357	279	POLL	10914	377	317	SO[33]	10076.5	357
242	SHIELDING[33]	9562.5	-357	280	LDL	10864	377	318	SO[34]	10059.5	77
243	GMAVL[2]	9647.5	-357	281	SYNCL	10814	377	319	SO[35]	10042.5	217
244	GMAVL[2]	9732.5	-357	282	COM2_T	10764	377	320	SO[36]	10025.5	357
245	SHIELDING[34]	9817.5	-357	283	COM2_T	10714	377	321	SO[37]	10008.5	77
246	GMAVL[1]	9902.5	-357	284	SHIELDING[39]	10664	377	322	SO[38]	9991.5	217
247	GMAVL[1]	9987.5	-357	285	SO[1]	10620.5	77	323	SO[39]	9974.5	357
248	SHIELDING[35]	10072.5	-357	286	SO[2]	10603.5	217	324	SO[40]	9957.5	77
249	VDDA	10157.5	-357	287	SO[3]	10586.5	357	325	SO[41]	9940.5	217
250	VDDA	10242.5	-357	288	SO[4]	10569.5	77	326	SO[42]	9923.5	357
251	VDDA	10327.5	-357	289	SO[5]	10552.5	217	327	SO[43]	9906.5	77
252	VDDA	10412.5	-357	290	SO[6]	10535.5	357	328	SO[44]	9889.5	217
253	TP3	10497.5	-357	291	SO[7]	10518.5	77	329	SO[45]	9872.5	357
254	COM_PASSL	10582.5	-357	292	SO[8]	10501.5	217	330	SO[46]	9855.5	77
255	COM_PASSL	10667.5	-357	293	SO[9]	10484.5	357	331	SO[47]	9838.5	217
256	SHIELDING[36]	10752.5	-357	294	SO[10]	10467.5	77	332	SO[48]	9821.5	357
257	SHIELDING[37]	10837.5	-357	295	SO[11]	10450.5	217	333	SO[49]	9804.5	77
258	SHIELDING[38]	10922.5	-357	296	SO[12]	10433.5	357	334	SO[50]	9787.5	217
259	DCLKL	11049	-363	297	SO[13]	10416.5	77	335	SO[51]	9770.5	357
260	DIOL	11179	-323	298	SO[14]	10399.5	217	336	SO[52]	9753.5	77
261	DATL[17]	11049	-283	299	SO[15]	10382.5	357	337	SO[53]	9736.5	217
262	DATL[16]	11179	-243	300	SO[16]	10365.5	77	338	SO[54]	9719.5	357

339	SO[55]	9702.5	77	377	SO[93]	9056.5	357	415	SO[131]	8410.5	217
340	SO[56]	9685.5	217	378	SO[94]	9039.5	77	416	SO[132]	8393.5	357
341	SO[57]	9668.5	357	379	SO[95]	9022.5	217	417	SO[133]	8376.5	77
342	SO[58]	9651.5	77	380	SO[96]	9005.5	357	418	SO[134]	8359.5	217
343	SO[59]	9634.5	217	381	SO[97]	8988.5	77	419	SO[135]	8342.5	357
344	SO[60]	9617.5	357	382	SO[98]	8971.5	217	420	SO[136]	8325.5	77
345	SO[61]	9600.5	77	383	SO[99]	8954.5	357	421	SO[137]	8308.5	217
346	SO[62]	9583.5	217	384	SO[100]	8937.5	77	422	SO[138]	8291.5	357
347	SO[63]	9566.5	357	385	SO[101]	8920.5	217	423	SO[139]	8274.5	77
348	SO[64]	9549.5	77	386	SO[102]	8903.5	357	424	SO[140]	8257.5	217
349	SO[65]	9532.5	217	387	SO[103]	8886.5	77	425	SO[141]	8240.5	357
350	SO[66]	9515.5	357	388	SO[104]	8869.5	217	426	SO[142]	8223.5	77
351	SO[67]	9498.5	77	389	SO[105]	8852.5	357	427	SO[143]	8206.5	217
352	SO[68]	9481.5	217	390	SO[106]	8835.5	77	428	SO[144]	8189.5	357
353	SO[69]	9464.5	357	391	SO[107]	8818.5	217	429	SO[145]	8172.5	77
354	SO[70]	9447.5	77	392	SO[108]	8801.5	357	430	SO[146]	8155.5	217
355	SO[71]	9430.5	217	393	SO[109]	8784.5	77	431	SO[147]	8138.5	357
356	SO[72]	9413.5	357	394	SO[110]	8767.5	217	432	SO[148]	8121.5	77
357	SO[73]	9396.5	77	395	SO[111]	8750.5	357	433	SO[149]	8104.5	217
358	SO[74]	9379.5	217	396	SO[112]	8733.5	77	434	SO[150]	8087.5	357
359	SO[75]	9362.5	357	397	SO[113]	8716.5	217	435	SO[151]	8070.5	77
360	SO[76]	9345.5	77	398	SO[114]	8699.5	357	436	SO[152]	8053.5	217
361	SO[77]	9328.5	217	399	SO[115]	8682.5	77	437	SO[153]	8036.5	357
362	SO[78]	9311.5	357	400	SO[116]	8665.5	217	438	SO[154]	8019.5	77
363	SO[79]	9294.5	77	401	SO[117]	8648.5	357	439	SO[155]	8002.5	217
364	SO[80]	9277.5	217	402	SO[118]	8631.5	77	440	SO[156]	7985.5	357
365	SO[81]	9260.5	357	403	SO[119]	8614.5	217	441	SO[157]	7968.5	77
366	SO[82]	9243.5	77	404	SO[120]	8597.5	357	442	SO[158]	7951.5	217
367	SO[83]	9226.5	217	405	SO[121]	8580.5	77	443	SO[159]	7934.5	357
368	SO[84]	9209.5	357	406	SO[122]	8563.5	217	444	SO[160]	7917.5	77
369	SO[85]	9192.5	77	407	SO[123]	8546.5	357	445	SO[161]	7900.5	217
370	SO[86]	9175.5	217	408	SO[124]	8529.5	77	446	SO[162]	7883.5	357
371	SO[87]	9158.5	357	409	SO[125]	8512.5	217	447	SO[163]	7866.5	77
372	SO[88]	9141.5	77	410	SO[126]	8495.5	357	448	SO[164]	7849.5	217
373	SO[89]	9124.5	217	411	SO[127]	8478.5	77	449	SO[165]	7832.5	357
374	SO[90]	9107.5	357	412	SO[128]	8461.5	217	450	SO[166]	7815.5	77
375	SO[91]	9090.5	77	413	SO[129]	8444.5	357	451	SO[167]	7798.5	217
376	SO[92]	9073.5	217	414	SO[130]	8427.5	77	452	SO[168]	7781.5	357

453	SO[169]	7764.5	77		491	SO[207]	7118.5	357		529	SO[245]	6472.5	217
454	SO[170]	7747.5	217		492	SO[208]	7101.5	77		530	SO[246]	6455.5	357
455	SO[171]	7730.5	357		493	SO[209]	7084.5	217		531	SO[247]	6438.5	77
456	SO[172]	7713.5	77		494	SO[210]	7067.5	357		532	SO[248]	6421.5	217
457	SO[173]	7696.5	217		495	SO[211]	7050.5	77		533	SO[249]	6404.5	357
458	SO[174]	7679.5	357		496	SO[212]	7033.5	217		534	SO[250]	6387.5	77
459	SO[175]	7662.5	77		497	SO[213]	7016.5	357		535	SO[251]	6370.5	217
460	SO[176]	7645.5	217		498	SO[214]	6999.5	77		536	SO[252]	6353.5	357
461	SO[177]	7628.5	357		499	SO[215]	6982.5	217		537	SO[253]	6336.5	77
462	SO[178]	7611.5	77		500	SO[216]	6965.5	357		538	SO[254]	6319.5	217
463	SO[179]	7594.5	217		501	SO[217]	6948.5	77		539	SO[255]	6302.5	357
464	SO[180]	7577.5	357		502	SO[218]	6931.5	217		540	SO[256]	6285.5	77
465	SO[181]	7560.5	77		503	SO[219]	6914.5	357		541	SO[257]	6268.5	217
466	SO[182]	7543.5	217		504	SO[220]	6897.5	77		542	SO[258]	6251.5	357
467	SO[183]	7526.5	357		505	SO[221]	6880.5	217		543	SO[259]	6234.5	77
468	SO[184]	7509.5	77		506	SO[222]	6863.5	357		544	SO[260]	6217.5	217
469	SO[185]	7492.5	217		507	SO[223]	6846.5	77		545	SO[261]	6200.5	357
470	SO[186]	7475.5	357		508	SO[224]	6829.5	217		546	SO[262]	6183.5	77
471	SO[187]	7458.5	77		509	SO[225]	6812.5	357		547	SO[263]	6166.5	217
472	SO[188]	7441.5	217		510	SO[226]	6795.5	77		548	SO[264]	6149.5	357
473	SO[189]	7424.5	357		511	SO[227]	6778.5	217		549	SO[265]	6132.5	77
474	SO[190]	7407.5	77		512	SO[228]	6761.5	357		550	SO[266]	6115.5	217
475	SO[191]	7390.5	217		513	SO[229]	6744.5	77		551	SO[267]	6098.5	357
476	SO[192]	7373.5	357		514	SO[230]	6727.5	217		552	SO[268]	6081.5	77
477	SO[193]	7356.5	77		515	SO[231]	6710.5	357		553	SO[269]	6064.5	217
478	SO[194]	7339.5	217		516	SO[232]	6693.5	77		554	SO[270]	6047.5	357
479	SO[195]	7322.5	357		517	SO[233]	6676.5	217		555	SO[271]	6030.5	77
480	SO[196]	7305.5	77		518	SO[234]	6659.5	357		556	SO[272]	6013.5	217
481	SO[197]	7288.5	217		519	SO[235]	6642.5	77		557	SO[273]	5996.5	357
482	SO[198]	7271.5	357		520	SO[236]	6625.5	217		558	SO[274]	5979.5	77
483	SO[199]	7254.5	77		521	SO[237]	6608.5	357		559	SO[275]	5962.5	217
484	SO[200]	7237.5	217		522	SO[238]	6591.5	77		560	SO[276]	5945.5	357
485	SO[201]	7220.5	357		523	SO[239]	6574.5	217		561	SO[277]	5928.5	77
486	SO[202]	7203.5	77		524	SO[240]	6557.5	357		562	SO[278]	5911.5	217
487	SO[203]	7186.5	217		525	SO[241]	6540.5	77		563	SO[279]	5894.5	357
488	SO[204]	7169.5	357		526	SO[242]	6523.5	217		564	SO[280]	5877.5	77
489	SO[205]	7152.5	77		527	SO[243]	6506.5	357		565	SO[281]	5860.5	217
490	SO[206]	7135.5	217		528	SO[244]	6489.5	77		566	SO[282]	5843.5	357

567	SO[283]	5826.5	77	605	SO[321]	5180.5	357	643	SO[359]	4534.5	217
568	SO[284]	5809.5	217	606	SO[322]	5163.5	77	644	SO[360]	4517.5	357
569	SO[285]	5792.5	357	607	SO[323]	5146.5	217	645	SO[361]	4500.5	77
570	SO[286]	5775.5	77	608	SO[324]	5129.5	357	646	SO[362]	4483.5	217
571	SO[287]	5758.5	217	609	SO[325]	5112.5	77	647	SO[363]	4466.5	357
572	SO[288]	5741.5	357	610	SO[326]	5095.5	217	648	SO[364]	4449.5	77
573	SO[289]	5724.5	77	611	SO[327]	5078.5	357	649	SO[365]	4432.5	217
574	SO[290]	5707.5	217	612	SO[328]	5061.5	77	650	SO[366]	4415.5	357
575	SO[291]	5690.5	357	613	SO[329]	5044.5	217	651	SO[367]	4398.5	77
576	SO[292]	5673.5	77	614	SO[330]	5027.5	357	652	SO[368]	4381.5	217
577	SO[293]	5656.5	217	615	SO[331]	5010.5	77	653	SO[369]	4364.5	357
578	SO[294]	5639.5	357	616	SO[332]	4993.5	217	654	SO[370]	4347.5	77
579	SO[295]	5622.5	77	617	SO[333]	4976.5	357	655	SO[371]	4330.5	217
580	SO[296]	5605.5	217	618	SO[334]	4959.5	77	656	SO[372]	4313.5	357
581	SO[297]	5588.5	357	619	SO[335]	4942.5	217	657	SO[373]	4296.5	77
582	SO[298]	5571.5	77	620	SO[336]	4925.5	357	658	SO[374]	4279.5	217
583	SO[299]	5554.5	217	621	SO[337]	4908.5	77	659	SO[375]	4262.5	357
584	SO[300]	5537.5	357	622	SO[338]	4891.5	217	660	SO[376]	4245.5	77
585	SO[301]	5520.5	77	623	SO[339]	4874.5	357	661	SO[377]	4228.5	217
586	SO[302]	5503.5	217	624	SO[340]	4857.5	77	662	SO[378]	4211.5	357
587	SO[303]	5486.5	357	625	SO[341]	4840.5	217	663	SO[379]	4194.5	77
588	SO[304]	5469.5	77	626	SO[342]	4823.5	357	664	SO[380]	4177.5	217
589	SO[305]	5452.5	217	627	SO[343]	4806.5	77	665	SO[381]	4160.5	357
590	SO[306]	5435.5	357	628	SO[344]	4789.5	217	666	SO[382]	4143.5	77
591	SO[307]	5418.5	77	629	SO[345]	4772.5	357	667	SO[383]	4126.5	217
592	SO[308]	5401.5	217	630	SO[346]	4755.5	77	668	SO[384]	4109.5	357
593	SO[309]	5384.5	357	631	SO[347]	4738.5	217	669	SO[385]	4092.5	77
594	SO[310]	5367.5	77	632	SO[348]	4721.5	357	670	SO[386]	4075.5	217
595	SO[311]	5350.5	217	633	SO[349]	4704.5	77	671	SO[387]	4058.5	357
596	SO[312]	5333.5	357	634	SO[350]	4687.5	217	672	SO[388]	4041.5	77
597	SO[313]	5316.5	77	635	SO[351]	4670.5	357	673	SO[389]	4024.5	217
598	SO[314]	5299.5	217	636	SO[352]	4653.5	77	674	SO[390]	4007.5	357
599	SO[315]	5282.5	357	637	SO[353]	4636.5	217	675	SO[391]	3990.5	77
600	SO[316]	5265.5	77	638	SO[354]	4619.5	357	676	SO[392]	3973.5	217
601	SO[317]	5248.5	217	639	SO[355]	4602.5	77	677	SO[393]	3956.5	357
602	SO[318]	5231.5	357	640	SO[356]	4585.5	217	678	SO[394]	3939.5	77
603	SO[319]	5214.5	77	641	SO[357]	4568.5	357	679	SO[395]	3922.5	217
604	SO[320]	5197.5	217	642	SO[358]	4551.5	77	680	SO[396]	3905.5	357

681	SO[397]	3888.5	77	719	SO[435]	3242.5	357	757	SO[473]	2596.5	217
682	SO[398]	3871.5	217	720	SO[436]	3225.5	77	758	SO[474]	2579.5	357
683	SO[399]	3854.5	357	721	SO[437]	3208.5	217	759	SO[475]	2562.5	77
684	SO[400]	3837.5	77	722	SO[438]	3191.5	357	760	SO[476]	2545.5	217
685	SO[401]	3820.5	217	723	SO[439]	3174.5	77	761	SO[477]	2528.5	357
686	SO[402]	3803.5	357	724	SO[440]	3157.5	217	762	SO[478]	2511.5	77
687	SO[403]	3786.5	77	725	SO[441]	3140.5	357	763	SO[479]	2494.5	217
688	SO[404]	3769.5	217	726	SO[442]	3123.5	77	764	SO[480]	2477.5	357
689	SO[405]	3752.5	357	727	SO[443]	3106.5	217	765	SO[481]	2460.5	77
690	SO[406]	3735.5	77	728	SO[444]	3089.5	357	766	SO[482]	2443.5	217
691	SO[407]	3718.5	217	729	SO[445]	3072.5	77	767	SO[483]	2426.5	357
692	SO[408]	3701.5	357	730	SO[446]	3055.5	217	768	SO[484]	2409.5	77
693	SO[409]	3684.5	77	731	SO[447]	3038.5	357	769	SO[485]	2392.5	217
694	SO[410]	3667.5	217	732	SO[448]	3021.5	77	770	SO[486]	2375.5	357
695	SO[411]	3650.5	357	733	SO[449]	3004.5	217	771	SO[487]	2358.5	77
696	SO[412]	3633.5	77	734	SO[450]	2987.5	357	772	SO[488]	2341.5	217
697	SO[413]	3616.5	217	735	SO[451]	2970.5	77	773	SO[489]	2324.5	357
698	SO[414]	3599.5	357	736	SO[452]	2953.5	217	774	SO[490]	2307.5	77
699	SO[415]	3582.5	77	737	SO[453]	2936.5	357	775	SO[491]	2290.5	217
700	SO[416]	3565.5	217	738	SO[454]	2919.5	77	776	SO[492]	2273.5	357
701	SO[417]	3548.5	357	739	SO[455]	2902.5	217	777	SO[493]	2256.5	77
702	SO[418]	3531.5	77	740	SO[456]	2885.5	357	778	SO[494]	2239.5	217
703	SO[419]	3514.5	217	741	SO[457]	2868.5	77	779	SO[495]	2222.5	357
704	SO[420]	3497.5	357	742	SO[458]	2851.5	217	780	SO[496]	2205.5	77
705	SO[421]	3480.5	77	743	SO[459]	2834.5	357	781	SO[497]	2188.5	217
706	SO[422]	3463.5	217	744	SO[460]	2817.5	77	782	SO[498]	2171.5	357
707	SO[423]	3446.5	357	745	SO[461]	2800.5	217	783	SO[499]	2154.5	77
708	SO[424]	3429.5	77	746	SO[462]	2783.5	357	784	SO[500]	2137.5	217
709	SO[425]	3412.5	217	747	SO[463]	2766.5	77	785	SO[501]	2120.5	357
710	SO[426]	3395.5	357	748	SO[464]	2749.5	217	786	SO[502]	2103.5	77
711	SO[427]	3378.5	77	749	SO[465]	2732.5	357	787	SO[503]	2086.5	217
712	SO[428]	3361.5	217	750	SO[466]	2715.5	77	788	SO[504]	2069.5	357
713	SO[429]	3344.5	357	751	SO[467]	2698.5	217	789	SO[505]	2052.5	77
714	SO[430]	3327.5	77	752	SO[468]	2681.5	357	790	SO[506]	2035.5	217
715	SO[431]	3310.5	217	753	SO[469]	2664.5	77	791	SO[507]	2018.5	357
716	SO[432]	3293.5	357	754	SO[470]	2647.5	217	792	SO[508]	2001.5	77
717	SO[433]	3276.5	77	755	SO[471]	2630.5	357	793	SO[509]	1984.5	217
718	SO[434]	3259.5	217	756	SO[472]	2613.5	77	794	SO[510]	1967.5	357

795	SO[511]	1950.5	77	833	SO[549]	1304.5	357	871	SO[587]	658.5	217
796	SO[512]	1933.5	217	834	SO[550]	1287.5	77	872	SO[588]	641.5	357
797	SO[513]	1916.5	357	835	SO[551]	1270.5	217	873	SO[589]	624.5	77
798	SO[514]	1899.5	77	836	SO[552]	1253.5	357	874	SO[590]	607.5	217
799	SO[515]	1882.5	217	837	SO[553]	1236.5	77	875	SO[591]	590.5	357
800	SO[516]	1865.5	357	838	SO[554]	1219.5	217	876	SO[592]	573.5	77
801	SO[517]	1848.5	77	839	SO[555]	1202.5	357	877	SO[593]	556.5	217
802	SO[518]	1831.5	217	840	SO[556]	1185.5	77	878	SO[594]	539.5	357
803	SO[519]	1814.5	357	841	SO[557]	1168.5	217	879	SO[595]	522.5	77
804	SO[520]	1797.5	77	842	SO[558]	1151.5	357	880	SO[596]	505.5	217
805	SO[521]	1780.5	217	843	SO[559]	1134.5	77	881	SO[597]	488.5	357
806	SO[522]	1763.5	357	844	SO[560]	1117.5	217	882	SO[598]	471.5	77
807	SO[523]	1746.5	77	845	SO[561]	1100.5	357	883	SO[599]	454.5	217
808	SO[524]	1729.5	217	846	SO[562]	1083.5	77	884	SO[600]	437.5	357
809	SO[525]	1712.5	357	847	SO[563]	1066.5	217	885	SHIELDING[40]	403.5	357
810	SO[526]	1695.5	77	848	SO[564]	1049.5	357	886	SHIELDING[41]	369.5	357
811	SO[527]	1678.5	217	849	SO[565]	1032.5	77	887	SHIELDING[42]	335.5	357
812	SO[528]	1661.5	357	850	SO[566]	1015.5	217	888	SHIELDING[43]	301.5	357
813	SO[529]	1644.5	77	851	SO[567]	998.5	357	889	SHIELDING[44]	267.5	357
814	SO[530]	1627.5	217	852	SO[568]	981.5	77	890	SHIELDING[45]	233.5	357
815	SO[531]	1610.5	357	853	SO[569]	964.5	217	891	SHIELDING[46]	-233.5	357
816	SO[532]	1593.5	77	854	SO[570]	947.5	357	892	SHIELDING[47]	-267.5	357
817	SO[533]	1576.5	217	855	SO[571]	930.5	77	893	SHIELDING[48]	-301.5	357
818	SO[534]	1559.5	357	856	SO[572]	913.5	217	894	SHIELDING[49]	-335.5	357
819	SO[535]	1542.5	77	857	SO[573]	896.5	357	895	SHIELDING[50]	-369.5	357
820	SO[536]	1525.5	217	858	SO[574]	879.5	77	896	SHIELDING[51]	-403.5	357
821	SO[537]	1508.5	357	859	SO[575]	862.5	217	897	SO[601]	-437.5	357
822	SO[538]	1491.5	77	860	SO[576]	845.5	357	898	SO[602]	-454.5	217
823	SO[539]	1474.5	217	861	SO[577]	828.5	77	899	SO[603]	-471.5	77
824	SO[540]	1457.5	357	862	SO[578]	811.5	217	900	SO[604]	-488.5	357
825	SO[541]	1440.5	77	863	SO[579]	794.5	357	901	SO[605]	-505.5	217
826	SO[542]	1423.5	217	864	SO[580]	777.5	77	902	SO[606]	-522.5	77
827	SO[543]	1406.5	357	865	SO[581]	760.5	217	903	SO[607]	-539.5	357
828	SO[544]	1389.5	77	866	SO[582]	743.5	357	904	SO[608]	-556.5	217
829	SO[545]	1372.5	217	867	SO[583]	726.5	77	905	SO[609]	-573.5	77
830	SO[546]	1355.5	357	868	SO[584]	709.5	217	906	SO[610]	-590.5	357
831	SO[547]	1338.5	77	869	SO[585]	692.5	357	907	SO[611]	-607.5	217
832	SO[548]	1321.5	217	870	SO[586]	675.5	77	908	SO[612]	-624.5	77

909	SO[613]	-641.5	357	947	SO[651]	-1287.5	77	985	SO[689]	-1933.5	217
910	SO[614]	-658.5	217	948	SO[652]	-1304.5	357	986	SO[690]	-1950.5	77
911	SO[615]	-675.5	77	949	SO[653]	-1321.5	217	987	SO[691]	-1967.5	357
912	SO[616]	-692.5	357	950	SO[654]	-1338.5	77	988	SO[692]	-1984.5	217
913	SO[617]	-709.5	217	951	SO[655]	-1355.5	357	989	SO[693]	-2001.5	77
914	SO[618]	-726.5	77	952	SO[656]	-1372.5	217	990	SO[694]	-2018.5	357
915	SO[619]	-743.5	357	953	SO[657]	-1389.5	77	991	SO[695]	-2035.5	217
916	SO[620]	-760.5	217	954	SO[658]	-1406.5	357	992	SO[696]	-2052.5	77
917	SO[621]	-777.5	77	955	SO[659]	-1423.5	217	993	SO[697]	-2069.5	357
918	SO[622]	-794.5	357	956	SO[660]	-1440.5	77	994	SO[698]	-2086.5	217
919	SO[623]	-811.5	217	957	SO[661]	-1457.5	357	995	SO[699]	-2103.5	77
920	SO[624]	-828.5	77	958	SO[662]	-1474.5	217	996	SO[700]	-2120.5	357
921	SO[625]	-845.5	357	959	SO[663]	-1491.5	77	997	SO[701]	-2137.5	217
922	SO[626]	-862.5	217	960	SO[664]	-1508.5	357	998	SO[702]	-2154.5	77
923	SO[627]	-879.5	77	961	SO[665]	-1525.5	217	999	SO[703]	-2171.5	357
924	SO[628]	-896.5	357	962	SO[666]	-1542.5	77	1000	SO[704]	-2188.5	217
925	SO[629]	-913.5	217	963	SO[667]	-1559.5	357	1001	SO[705]	-2205.5	77
926	SO[630]	-930.5	77	964	SO[668]	-1576.5	217	1002	SO[706]	-2222.5	357
927	SO[631]	-947.5	357	965	SO[669]	-1593.5	77	1003	SO[707]	-2239.5	217
928	SO[632]	-964.5	217	966	SO[670]	-1610.5	357	1004	SO[708]	-2256.5	77
929	SO[633]	-981.5	77	967	SO[671]	-1627.5	217	1005	SO[709]	-2273.5	357
930	SO[634]	-998.5	357	968	SO[672]	-1644.5	77	1006	SO[710]	-2290.5	217
931	SO[635]	-1015.5	217	969	SO[673]	-1661.5	357	1007	SO[711]	-2307.5	77
932	SO[636]	-1032.5	77	970	SO[674]	-1678.5	217	1008	SO[712]	-2324.5	357
933	SO[637]	-1049.5	357	971	SO[675]	-1695.5	77	1009	SO[713]	-2341.5	217
934	SO[638]	-1066.5	217	972	SO[676]	-1712.5	357	1010	SO[714]	-2358.5	77
935	SO[639]	-1083.5	77	973	SO[677]	-1729.5	217	1011	SO[715]	-2375.5	357
936	SO[640]	-1100.5	357	974	SO[678]	-1746.5	77	1012	SO[716]	-2392.5	217
937	SO[641]	-1117.5	217	975	SO[679]	-1763.5	357	1013	SO[717]	-2409.5	77
938	SO[642]	-1134.5	77	976	SO[680]	-1780.5	217	1014	SO[718]	-2426.5	357
939	SO[643]	-1151.5	357	977	SO[681]	-1797.5	77	1015	SO[719]	-2443.5	217
940	SO[644]	-1168.5	217	978	SO[682]	-1814.5	357	1016	SO[720]	-2460.5	77
941	SO[645]	-1185.5	77	979	SO[683]	-1831.5	217	1017	SO[721]	-2477.5	357
942	SO[646]	-1202.5	357	980	SO[684]	-1848.5	77	1018	SO[722]	-2494.5	217
943	SO[647]	-1219.5	217	981	SO[685]	-1865.5	357	1019	SO[723]	-2511.5	77
944	SO[648]	-1236.5	77	982	SO[686]	-1882.5	217	1020	SO[724]	-2528.5	357
945	SO[649]	-1253.5	357	983	SO[687]	-1899.5	77	1021	SO[725]	-2545.5	217
946	SO[650]	-1270.5	217	984	SO[688]	-1916.5	357	1022	SO[726]	-2562.5	77

1023	SO[727]	-2579.5	357	1061	SO[765]	-3225.5	77	1099	SO[803]	-3871.5	217
1024	SO[728]	-2596.5	217	1062	SO[766]	-3242.5	357	1100	SO[804]	-3888.5	77
1025	SO[729]	-2613.5	77	1063	SO[767]	-3259.5	217	1101	SO[805]	-3905.5	357
1026	SO[730]	-2630.5	357	1064	SO[768]	-3276.5	77	1102	SO[806]	-3922.5	217
1027	SO[731]	-2647.5	217	1065	SO[769]	-3293.5	357	1103	SO[807]	-3939.5	77
1028	SO[732]	-2664.5	77	1066	SO[770]	-3310.5	217	1104	SO[808]	-3956.5	357
1029	SO[733]	-2681.5	357	1067	SO[771]	-3327.5	77	1105	SO[809]	-3973.5	217
1030	SO[734]	-2698.5	217	1068	SO[772]	-3344.5	357	1106	SO[810]	-3990.5	77
1031	SO[735]	-2715.5	77	1069	SO[773]	-3361.5	217	1107	SO[811]	-4007.5	357
1032	SO[736]	-2732.5	357	1070	SO[774]	-3378.5	77	1108	SO[812]	-4024.5	217
1033	SO[737]	-2749.5	217	1071	SO[775]	-3395.5	357	1109	SO[813]	-4041.5	77
1034	SO[738]	-2766.5	77	1072	SO[776]	-3412.5	217	1110	SO[814]	-4058.5	357
1035	SO[739]	-2783.5	357	1073	SO[777]	-3429.5	77	1111	SO[815]	-4075.5	217
1036	SO[740]	-2800.5	217	1074	SO[778]	-3446.5	357	1112	SO[816]	-4092.5	77
1037	SO[741]	-2817.5	77	1075	SO[779]	-3463.5	217	1113	SO[817]	-4109.5	357
1038	SO[742]	-2834.5	357	1076	SO[780]	-3480.5	77	1114	SO[818]	-4126.5	217
1039	SO[743]	-2851.5	217	1077	SO[781]	-3497.5	357	1115	SO[819]	-4143.5	77
1040	SO[744]	-2868.5	77	1078	SO[782]	-3514.5	217	1116	SO[820]	-4160.5	357
1041	SO[745]	-2885.5	357	1079	SO[783]	-3531.5	77	1117	SO[821]	-4177.5	217
1042	SO[746]	-2902.5	217	1080	SO[784]	-3548.5	357	1118	SO[822]	-4194.5	77
1043	SO[747]	-2919.5	77	1081	SO[785]	-3565.5	217	1119	SO[823]	-4211.5	357
1044	SO[748]	-2936.5	357	1082	SO[786]	-3582.5	77	1120	SO[824]	-4228.5	217
1045	SO[749]	-2953.5	217	1083	SO[787]	-3599.5	357	1121	SO[825]	-4245.5	77
1046	SO[750]	-2970.5	77	1084	SO[788]	-3616.5	217	1122	SO[826]	-4262.5	357
1047	SO[751]	-2987.5	357	1085	SO[789]	-3633.5	77	1123	SO[827]	-4279.5	217
1048	SO[752]	-3004.5	217	1086	SO[790]	-3650.5	357	1124	SO[828]	-4296.5	77
1049	SO[753]	-3021.5	77	1087	SO[791]	-3667.5	217	1125	SO[829]	-4313.5	357
1050	SO[754]	-3038.5	357	1088	SO[792]	-3684.5	77	1126	SO[830]	-4330.5	217
1051	SO[755]	-3055.5	217	1089	SO[793]	-3701.5	357	1127	SO[831]	-4347.5	77
1052	SO[756]	-3072.5	77	1090	SO[794]	-3718.5	217	1128	SO[832]	-4364.5	357
1053	SO[757]	-3089.5	357	1091	SO[795]	-3735.5	77	1129	SO[833]	-4381.5	217
1054	SO[758]	-3106.5	217	1092	SO[796]	-3752.5	357	1130	SO[834]	-4398.5	77
1055	SO[759]	-3123.5	77	1093	SO[797]	-3769.5	217	1131	SO[835]	-4415.5	357
1056	SO[760]	-3140.5	357	1094	SO[798]	-3786.5	77	1132	SO[836]	-4432.5	217
1057	SO[761]	-3157.5	217	1095	SO[799]	-3803.5	357	1133	SO[837]	-4449.5	77
1058	SO[762]	-3174.5	77	1096	SO[800]	-3820.5	217	1134	SO[838]	-4466.5	357
1059	SO[763]	-3191.5	357	1097	SO[801]	-3837.5	77	1135	SO[839]	-4483.5	217
1060	SO[764]	-3208.5	217	1098	SO[802]	-3854.5	357	1136	SO[840]	-4500.5	77

1137	SO[841]	-4517.5	357	1175	SO[879]	-5163.5	77	1213	SO[917]	-5809.5	217
1138	SO[842]	-4534.5	217	1176	SO[880]	-5180.5	357	1214	SO[918]	-5826.5	77
1139	SO[843]	-4551.5	77	1177	SO[881]	-5197.5	217	1215	SO[919]	-5843.5	357
1140	SO[844]	-4568.5	357	1178	SO[882]	-5214.5	77	1216	SO[920]	-5860.5	217
1141	SO[845]	-4585.5	217	1179	SO[883]	-5231.5	357	1217	SO[921]	-5877.5	77
1142	SO[846]	-4602.5	77	1180	SO[884]	-5248.5	217	1218	SO[922]	-5894.5	357
1143	SO[847]	-4619.5	357	1181	SO[885]	-5265.5	77	1219	SO[923]	-5911.5	217
1144	SO[848]	-4636.5	217	1182	SO[886]	-5282.5	357	1220	SO[924]	-5928.5	77
1145	SO[849]	-4653.5	77	1183	SO[887]	-5299.5	217	1221	SO[925]	-5945.5	357
1146	SO[850]	-4670.5	357	1184	SO[888]	-5316.5	77	1222	SO[926]	-5962.5	217
1147	SO[851]	-4687.5	217	1185	SO[889]	-5333.5	357	1223	SO[927]	-5979.5	77
1148	SO[852]	-4704.5	77	1186	SO[890]	-5350.5	217	1224	SO[928]	-5996.5	357
1149	SO[853]	-4721.5	357	1187	SO[891]	-5367.5	77	1225	SO[929]	-6013.5	217
1150	SO[854]	-4738.5	217	1188	SO[892]	-5384.5	357	1226	SO[930]	-6030.5	77
1151	SO[855]	-4755.5	77	1189	SO[893]	-5401.5	217	1227	SO[931]	-6047.5	357
1152	SO[856]	-4772.5	357	1190	SO[894]	-5418.5	77	1228	SO[932]	-6064.5	217
1153	SO[857]	-4789.5	217	1191	SO[895]	-5435.5	357	1229	SO[933]	-6081.5	77
1154	SO[858]	-4806.5	77	1192	SO[896]	-5452.5	217	1230	SO[934]	-6098.5	357
1155	SO[859]	-4823.5	357	1193	SO[897]	-5469.5	77	1231	SO[935]	-6115.5	217
1156	SO[860]	-4840.5	217	1194	SO[898]	-5486.5	357	1232	SO[936]	-6132.5	77
1157	SO[861]	-4857.5	77	1195	SO[899]	-5503.5	217	1233	SO[937]	-6149.5	357
1158	SO[862]	-4874.5	357	1196	SO[900]	-5520.5	77	1234	SO[938]	-6166.5	217
1159	SO[863]	-4891.5	217	1197	SO[901]	-5537.5	357	1235	SO[939]	-6183.5	77
1160	SO[864]	-4908.5	77	1198	SO[902]	-5554.5	217	1236	SO[940]	-6200.5	357
1161	SO[865]	-4925.5	357	1199	SO[903]	-5571.5	77	1237	SO[941]	-6217.5	217
1162	SO[866]	-4942.5	217	1200	SO[904]	-5588.5	357	1238	SO[942]	-6234.5	77
1163	SO[867]	-4959.5	77	1201	SO[905]	-5605.5	217	1239	SO[943]	-6251.5	357
1164	SO[868]	-4976.5	357	1202	SO[906]	-5622.5	77	1240	SO[944]	-6268.5	217
1165	SO[869]	-4993.5	217	1203	SO[907]	-5639.5	357	1241	SO[945]	-6285.5	77
1166	SO[870]	-5010.5	77	1204	SO[908]	-5656.5	217	1242	SO[946]	-6302.5	357
1167	SO[871]	-5027.5	357	1205	SO[909]	-5673.5	77	1243	SO[947]	-6319.5	217
1168	SO[872]	-5044.5	217	1206	SO[910]	-5690.5	357	1244	SO[948]	-6336.5	77
1169	SO[873]	-5061.5	77	1207	SO[911]	-5707.5	217	1245	SO[949]	-6353.5	357
1170	SO[874]	-5078.5	357	1208	SO[912]	-5724.5	77	1246	SO[950]	-6370.5	217
1171	SO[875]	-5095.5	217	1209	SO[913]	-5741.5	357	1247	SO[951]	-6387.5	77
1172	SO[876]	-5112.5	77	1210	SO[914]	-5758.5	217	1248	SO[952]	-6404.5	357
1173	SO[877]	-5129.5	357	1211	SO[915]	-5775.5	77	1249	SO[953]	-6421.5	217
1174	SO[878]	-5146.5	217	1212	SO[916]	-5792.5	357	1250	SO[954]	-6438.5	77

1251	SO[955]	-6455.5	357	1289	SO[993]	-7101.5	77	1327	SO[1031]	-7747.5	217
1252	SO[956]	-6472.5	217	1290	SO[994]	-7118.5	357	1328	SO[1032]	-7764.5	77
1253	SO[957]	-6489.5	77	1291	SO[995]	-7135.5	217	1329	SO[1033]	-7781.5	357
1254	SO[958]	-6506.5	357	1292	SO[996]	-7152.5	77	1330	SO[1034]	-7798.5	217
1255	SO[959]	-6523.5	217	1293	SO[997]	-7169.5	357	1331	SO[1035]	-7815.5	77
1256	SO[960]	-6540.5	77	1294	SO[998]	-7186.5	217	1332	SO[1036]	-7832.5	357
1257	SO[961]	-6557.5	357	1295	SO[999]	-7203.5	77	1333	SO[1037]	-7849.5	217
1258	SO[962]	-6574.5	217	1296	SO[1000]	-7220.5	357	1334	SO[1038]	-7866.5	77
1259	SO[963]	-6591.5	77	1297	SO[1001]	-7237.5	217	1335	SO[1039]	-7883.5	357
1260	SO[964]	-6608.5	357	1298	SO[1002]	-7254.5	77	1336	SO[1040]	-7900.5	217
1261	SO[965]	-6625.5	217	1299	SO[1003]	-7271.5	357	1337	SO[1041]	-7917.5	77
1262	SO[966]	-6642.5	77	1300	SO[1004]	-7288.5	217	1338	SO[1042]	-7934.5	357
1263	SO[967]	-6659.5	357	1301	SO[1005]	-7305.5	77	1339	SO[1043]	-7951.5	217
1264	SO[968]	-6676.5	217	1302	SO[1006]	-7322.5	357	1340	SO[1044]	-7968.5	77
1265	SO[969]	-6693.5	77	1303	SO[1007]	-7339.5	217	1341	SO[1045]	-7985.5	357
1266	SO[970]	-6710.5	357	1304	SO[1008]	-7356.5	77	1342	SO[1046]	-8002.5	217
1267	SO[971]	-6727.5	217	1305	SO[1009]	-7373.5	357	1343	SO[1047]	-8019.5	77
1268	SO[972]	-6744.5	77	1306	SO[1010]	-7390.5	217	1344	SO[1048]	-8036.5	357
1269	SO[973]	-6761.5	357	1307	SO[1011]	-7407.5	77	1345	SO[1049]	-8053.5	217
1270	SO[974]	-6778.5	217	1308	SO[1012]	-7424.5	357	1346	SO[1050]	-8070.5	77
1271	SO[975]	-6795.5	77	1309	SO[1013]	-7441.5	217	1347	SO[1051]	-8087.5	357
1272	SO[976]	-6812.5	357	1310	SO[1014]	-7458.5	77	1348	SO[1052]	-8104.5	217
1273	SO[977]	-6829.5	217	1311	SO[1015]	-7475.5	357	1349	SO[1053]	-8121.5	77
1274	SO[978]	-6846.5	77	1312	SO[1016]	-7492.5	217	1350	SO[1054]	-8138.5	357
1275	SO[979]	-6863.5	357	1313	SO[1017]	-7509.5	77	1351	SO[1055]	-8155.5	217
1276	SO[980]	-6880.5	217	1314	SO[1018]	-7526.5	357	1352	SO[1056]	-8172.5	77
1277	SO[981]	-6897.5	77	1315	SO[1019]	-7543.5	217	1353	SO[1057]	-8189.5	357
1278	SO[982]	-6914.5	357	1316	SO[1020]	-7560.5	77	1354	SO[1058]	-8206.5	217
1279	SO[983]	-6931.5	217	1317	SO[1021]	-7577.5	357	1355	SO[1059]	-8223.5	77
1280	SO[984]	-6948.5	77	1318	SO[1022]	-7594.5	217	1356	SO[1060]	-8240.5	357
1281	SO[985]	-6965.5	357	1319	SO[1023]	-7611.5	77	1357	SO[1061]	-8257.5	217
1282	SO[986]	-6982.5	217	1320	SO[1024]	-7628.5	357	1358	SO[1062]	-8274.5	77
1283	SO[987]	-6999.5	77	1321	SO[1025]	-7645.5	217	1359	SO[1063]	-8291.5	357
1284	SO[988]	-7016.5	357	1322	SO[1026]	-7662.5	77	1360	SO[1064]	-8308.5	217
1285	SO[989]	-7033.5	217	1323	SO[1027]	-7679.5	357	1361	SO[1065]	-8325.5	77
1286	SO[990]	-7050.5	77	1324	SO[1028]	-7696.5	217	1362	SO[1066]	-8342.5	357
1287	SO[991]	-7067.5	357	1325	SO[1029]	-7713.5	77	1363	SO[1067]	-8359.5	217
1288	SO[992]	-7084.5	217	1326	SO[1030]	-7730.5	357	1364	SO[1068]	-8376.5	77

1365	SO[1069]	-8393.5	357	1403	SO[1107]	-9039.5	77	1441	SO[1145]	-9685.5	217
1366	SO[1070]	-8410.5	217	1404	SO[1108]	-9056.5	357	1442	SO[1146]	-9702.5	77
1367	SO[1071]	-8427.5	77	1405	SO[1109]	-9073.5	217	1443	SO[1147]	-9719.5	357
1368	SO[1072]	-8444.5	357	1406	SO[1110]	-9090.5	77	1444	SO[1148]	-9736.5	217
1369	SO[1073]	-8461.5	217	1407	SO[1111]	-9107.5	357	1445	SO[1149]	-9753.5	77
1370	SO[1074]	-8478.5	77	1408	SO[1112]	-9124.5	217	1446	SO[1150]	-9770.5	357
1371	SO[1075]	-8495.5	357	1409	SO[1113]	-9141.5	77	1447	SO[1151]	-9787.5	217
1372	SO[1076]	-8512.5	217	1410	SO[1114]	-9158.5	357	1448	SO[1152]	-9804.5	77
1373	SO[1077]	-8529.5	77	1411	SO[1115]	-9175.5	217	1449	SO[1153]	-9821.5	357
1374	SO[1078]	-8546.5	357	1412	SO[1116]	-9192.5	77	1450	SO[1154]	-9838.5	217
1375	SO[1079]	-8563.5	217	1413	SO[1117]	-9209.5	357	1451	SO[1155]	-9855.5	77
1376	SO[1080]	-8580.5	77	1414	SO[1118]	-9226.5	217	1452	SO[1156]	-9872.5	357
1377	SO[1081]	-8597.5	357	1415	SO[1119]	-9243.5	77	1453	SO[1157]	-9889.5	217
1378	SO[1082]	-8614.5	217	1416	SO[1120]	-9260.5	357	1454	SO[1158]	-9906.5	77
1379	SO[1083]	-8631.5	77	1417	SO[1121]	-9277.5	217	1455	SO[1159]	-9923.5	357
1380	SO[1084]	-8648.5	357	1418	SO[1122]	-9294.5	77	1456	SO[1160]	-9940.5	217
1381	SO[1085]	-8665.5	217	1419	SO[1123]	-9311.5	357	1457	SO[1161]	-9957.5	77
1382	SO[1086]	-8682.5	77	1420	SO[1124]	-9328.5	217	1458	SO[1162]	-9974.5	357
1383	SO[1087]	-8699.5	357	1421	SO[1125]	-9345.5	77	1459	SO[1163]	-9991.5	217
1384	SO[1088]	-8716.5	217	1422	SO[1126]	-9362.5	357	1460	SO[1164]	-10008.5	77
1385	SO[1089]	-8733.5	77	1423	SO[1127]	-9379.5	217	1461	SO[1165]	-10025.5	357
1386	SO[1090]	-8750.5	357	1424	SO[1128]	-9396.5	77	1462	SO[1166]	-10042.5	217
1387	SO[1091]	-8767.5	217	1425	SO[1129]	-9413.5	357	1463	SO[1167]	-10059.5	77
1388	SO[1092]	-8784.5	77	1426	SO[1130]	-9430.5	217	1464	SO[1168]	-10076.5	357
1389	SO[1093]	-8801.5	357	1427	SO[1131]	-9447.5	77	1465	SO[1169]	-10093.5	217
1390	SO[1094]	-8818.5	217	1428	SO[1132]	-9464.5	357	1466	SO[1170]	-10110.5	77
1391	SO[1095]	-8835.5	77	1429	SO[1133]	-9481.5	217	1467	SO[1171]	-10127.5	357
1392	SO[1096]	-8852.5	357	1430	SO[1134]	-9498.5	77	1468	SO[1172]	-10144.5	217
1393	SO[1097]	-8869.5	217	1431	SO[1135]	-9515.5	357	1469	SO[1173]	-10161.5	77
1394	SO[1098]	-8886.5	77	1432	SO[1136]	-9532.5	217	1470	SO[1174]	-10178.5	357
1395	SO[1099]	-8903.5	357	1433	SO[1137]	-9549.5	77	1471	SO[1175]	-10195.5	217
1396	SO[1100]	-8920.5	217	1434	SO[1138]	-9566.5	357	1472	SO[1176]	-10212.5	77
1397	SO[1101]	-8937.5	77	1435	SO[1139]	-9583.5	217	1473	SO[1177]	-10229.5	357
1398	SO[1102]	-8954.5	357	1436	SO[1140]	-9600.5	77	1474	SO[1178]	-10246.5	217
1399	SO[1103]	-8971.5	217	1437	SO[1141]	-9617.5	357	1475	SO[1179]	-10263.5	77
1400	SO[1104]	-8988.5	77	1438	SO[1142]	-9634.5	217	1476	SO[1180]	-10280.5	357
1401	SO[1105]	-9005.5	357	1439	SO[1143]	-9651.5	77	1477	SO[1181]	-10297.5	217
1402	SO[1106]	-9022.5	217	1440	SO[1144]	-9668.5	357	1478	SO[1182]	-10314.5	77

1479	SO[1183]	-10331.5	357
1480	SO[1184]	-10348.5	217
1481	SO[1185]	-10365.5	77
1482	SO[1186]	-10382.5	357
1483	SO[1187]	-10399.5	217
1484	SO[1188]	-10416.5	77
1485	SO[1189]	-10433.5	357
1486	SO[1190]	-10450.5	217
1487	SO[1191]	-10467.5	77
1488	SO[1192]	-10484.5	357
1489	SO[1193]	-10501.5	217
1490	SO[1194]	-10518.5	77
1491	SO[1195]	-10535.5	357
1492	SO[1196]	-10552.5	217
1493	SO[1197]	-10569.5	77
1494	SO[1198]	-10586.5	357
1495	SO[1199]	-10603.5	217
1496	SO[1200]	-10620.5	77
1497	SHIELDING[52]	-10664	377
1498	COM1_T	-10714	377
1499	COM1_T	-10764	377
1500	SYNCR	-10814	377
1501	LDR	-10864	377
1502	POLR	-10914	377
1503	DATR[0]	-11179	397
1504	DATR[1]	-11049	357
1505	DATR[2]	-11179	317
1506	DATR[3]	-11049	277
1507	DATR[4]	-11179	237
1508	DATR[5]	-11049	197
1509	DATR[6]	-11179	157
1510	DATR[7]	-11049	117
1511	DATR[8]	-11179	77
1512	DATR[9]	-11049	37
1513	DATR[10]	-11179	-3
1514	DATR[11]	-11049	-43
1515	DATR[12]	-11179	-83
1516	DATR[13]	-11049	-123

1517	DATR[14]	-11179	-163
1518	DATR[15]	-11049	-203
1519	DATR[16]	-11179	-243
1520	DATR[17]	-11049	-283
1521	DIOR	-11179	-323
1522	DCLKR	-11049	-363

-	ALIGN_L	-10773	93
-	ALIGN_R	10773	93

9. DEFINITIONS

9.1. Data Sheet Status

Preliminary Data Sheet	This data sheet contains preliminary data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

9.2. Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

10. REVISION HISTORY

Revision	Content	Page	Date
0.1	New Issue.	--	2011/02/11
0.2	Modify HFRC function default value	17	2012/01/31

APPENDIX A : BIST PATTERN

R→G→B→Black→White→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame