GC9703C

a-Si TFT LCD Single-Chip Driver
800(RGB)x1800 Resolution,
16.7M-color Without internal GRAM

Datasheet

V1.2

2023-12-20

Ordering Information

◆ **GC9703C**

(a-Si TFT LCD Single Chip Driver)

(800(RGB)x1800 Resolution, 16.7M-color Without internal GRAM)

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2023-10-14	Document Release	Aaron
V1.1	2023-12-06	AE Review	Lucy
V1.2	2023-12-20	AE Review	Lucy

Table of Content

1. DESCRIPTION

The GC9703C device is a 16.7M single-chip (SOC) driver. It is comprised of a 2400-channel source driver (S1 ~ S2400 and S_RA,S_LB), a gate-IC-less level shifter and a power supply circuit to drive a dot-matrix TFT LCD with 800 (RGB) x 1800 dots at maximum.

The GC9703C can configure functions via the MIPI[1] DSI[2] Interface; transmit video data via MIPI DSI Interface.

The GC9703C can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The GC9703C supports Idle Mode (8-color low power mode) display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

2. FEATURES

Display resolution option
• 800 x RGB x (1280, others), (Source output from S1 to S1200, S1201 to S2400)
• 768 x RGB x (1280, others), (Source output from S1 to S1152, S1249 to S2400)
• 750 x RGB x (1334, others), (Source output from S55 to S1152, S1249 to S2400)
• 750 x RGB x (1334, others), (Source output from S1 to S1152, S1249 to S2346)
• 750 x RGB x (1334, others), (Source output from S1 to S1125, S1276 to S2400)
• 720 x RGB x (1280, others), (Source output from S1 to S1080, S1321 to S2400)
• 640 x RGB x (1280, others), (Source output from S1 to S960, S1441 to S2400)
• 600 x RGB x (1280,1024, others), (Source output from S1 to S900, S1501 to S2400)
• 540 x RGB x (1280,960, others), (Source output from S1 to S810, S1591 to S2400)
• 480 x RGB x (1280,960, others), (Source output from S1 to S720, S1681 to S2400)
• 480 x RGB x (1280,960, others), (Source output from S961 to S1200, S1201 to S2400)
• 480 x RGB x (1280,960, others), (Source output from S1 to S900, S1501 to S2040)
• 400 x RGB x (1280,960, others), (Source output from S1201 to S2400)
• 400 x RGB x (1280,960, others), (Source output from S1 to S600, S1801 to S2400)
• 320 x RGB x (1280,960, others), (Source output from S1441 to S2400)

Display mode (Color mode)
- Full color mode: 16.7M-colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Idle mode: 8 colors

Interface
-MIPI DSI (3/4 data lane): MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01)

Display features
- Supports 2400 source channel outputs (S1 ~ S2400 and S_R and S_LB)
- Supports gate control signals to gate driver in the panel
- Supports column inversion
- Gamma correction (4 preset Gamma curve)
- On module VCOM control

Power saving modes:
- Sleep mode
- Idle mode

Other on-chip functions/Miscellaneous
- Software programmable color depth mode
- Oscillator for display clock generation
- DC VCOM voltage generator and adjustment
- DGC (Digital Gamma Correction) function
- VGH/VGL voltage generator for gate control signal in panel

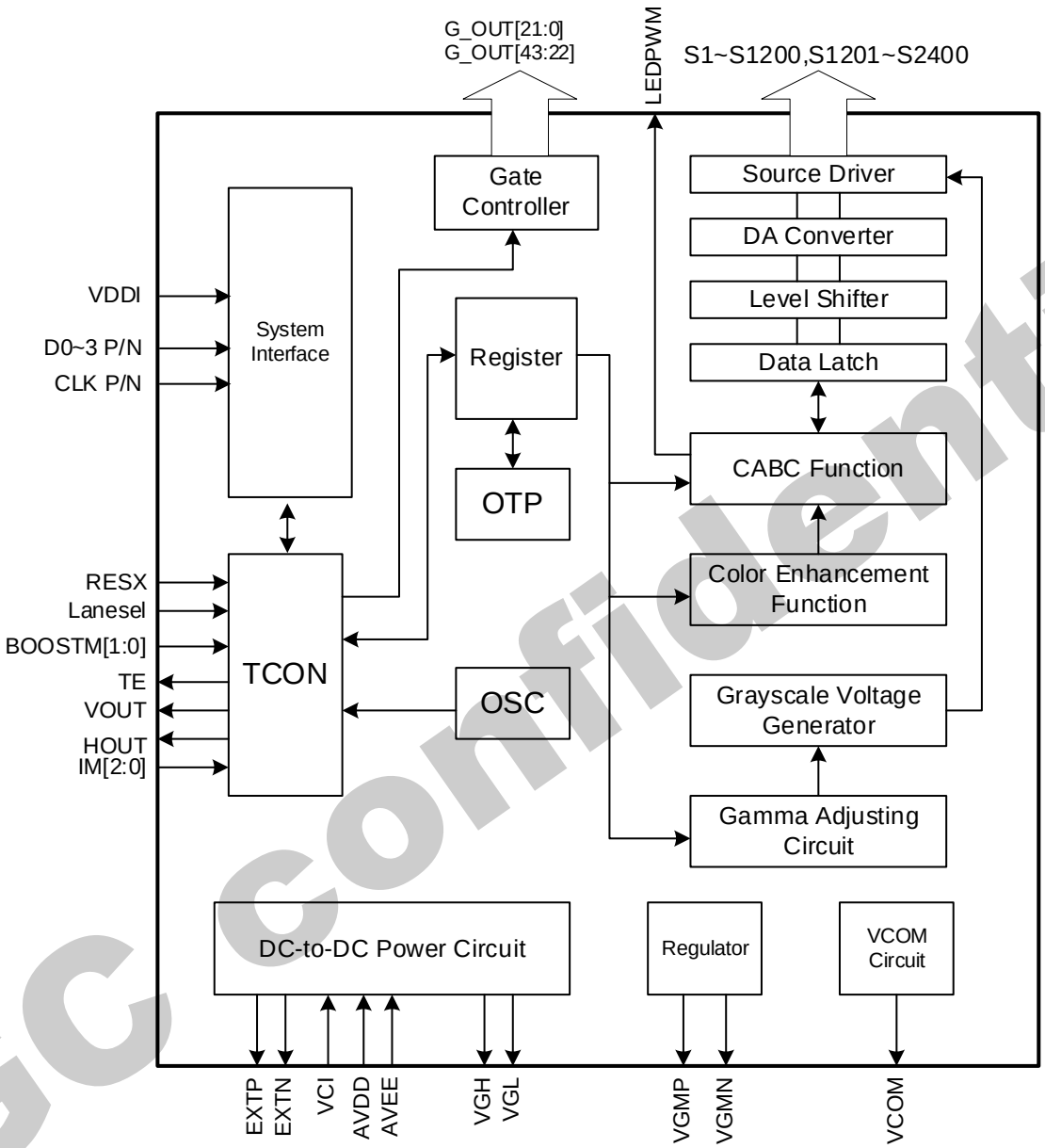
- Gate control signals to gate driver in panel (GIP)
- OTP (One-Time Programming) memory store initialization register settings
- Provide 3 times to store DC VCOM value setting and ID1 ~ ID3

Input power：

- External power IC：
  I/O and interface power supply (VDDI)：1.65V to 3.3V
  Analog power supply (VCI)：2.5V to 3.3V
- Three-Power Mode：
  I/O and interface power supply (VDDI)：1.65V to 3.3V
  Analog power supply (AVDD)：4.5V to 6.0V
  Analog power supply (AVEE)：-4.5V to -6.0V
- Output voltage：
  Positive source output voltage level: VGMP=3.3V to 5.6V
  Negative source output voltage level: VGMN=-5.6V to -3.3V
  Positive gate driver output voltage level: VGH=+10V to +16V
  Negative gate driver output voltage level: VGL=-8.0V to -12V
  VCOM=-3.5V to 0V

Operate temperature range: −20℃ to +85℃

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1. PIN DESCRIPTION

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
Fix to VDDI level when not in use.</td></tr>
<tr><td>BOOSTM[1:0]</td><td>I</td><td>- Power type selection pins
<table>
<tr><th>BOOSTM[1]</th><th>BOOSTM[0]</th><th>Power mode</th></tr>
<tr><td>1</td><td>0</td><td>2 power
External VDDI and VCI</td></tr>
<tr><td>0</td><td>0</td><td rowspan="3">3 power
Extenal VDDI,AVDD and AVEE (VCI=AVDD)
Note 1</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td colspan="2">prohibited</td><td>-</td></tr>
</table>
Note 1: VCI and AVDD pads must be connected by external metal path.</td></tr>
<tr><td>IM[2:0], Lanesel</td><td>I</td><td>-MIPI Lane Config Pin, Pin and register co-configuration MIPI mode, as follows
Table 2: DSI Interface Lane Mode Selection
<table>
<tr><th colspan="4">External Pad Set</th><th>Register</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><th>LANSEL</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Page0_RAEh
MIPI_LANE_SEL</th><th>D0P/N Pin</th><th>D1P/N Pin</th><th>CLKP/N Pin</th><th>D2P/N Pin</th><th>D3P/N Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>D3P/N</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>D3P/N</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>D3N/P</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-</td><td>-</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>-</td><td>-</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>-</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>-</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>-</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>-</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>-</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>-</td></tr>
<tr><td colspan="5">Others</td><td colspan="5">Reserved</td></tr>
</table>
If MIPI are not used, they should be connected to GND.</td></tr>
</table>

CLKP **CLKN**	I	MIPI DSI differential clock pair (DSI-CLK+/-). If MIPI are not used, they should be connected to GND.
HS_D0P **HS_D0N**	I/O	MIPI DSI differential data pair (DSI-D0+/-). If MIPI are not used, they should be connected to GND
HS_D1P **HS_D1N**	I	MIPI DSI differential data pair (DSI-D1+/-). If MIPI are not used, they should be connected to GND
HS_D2P **HS_D2N**	I	MIPI DSI differential data pair (DSI-D2+/-). If MIPI are not used, they should be connected to GND
HS_D3P **HS_D3N**	I	MIPI DSI differential data pair (DSI-D3+/-). If MIPI are not used, they should be connected to GND
TE	O	- Tearing effect output pin. ***Leave the pin open when not in use.***
TE1	O	- Tearing effect output pin. ***Leave the pin open when not in use.***
VOUT	I/O	- Touch synchronization signal (VOUT). ***Leave the pin open when not in use.***
HOUT	I/O	- Touch synchronization signal (HOUT). ***Leave the pin open when not in use.***
LEDPWM	O	- The PWM frequency output for LED driver control. ***Leave the pin open when not in use.***
Driver Output		
Pin Name	**I/O**	**Description**
G_OUT [43:22]	O	- Gate control signals for panel in left side of IC. ***Leave the pin open when not in use.***
G_OUT [21:0]	O	- Gate control signals for panel in right side of IC. ***Leave the pin open when not in use.***

<table>
<tr><td>S[2400:1201]
S[1200:1]</td><td>O</td><td>- Source output voltage signals applied to a LCD panel.
Source output mapping with different resolution
<table><tr><th>Disaply resulation</th><th>Source channels</th></tr><tr><td>800(RGB)</td><td>S1 ~ S1200, S1201 ~ S2400</td></tr><tr><td>768(RGB)</td><td>S1 ~ S1152,S1249 ~ S2400</td></tr><tr><td>750(RGB)</td><td>S55 ~ S1152,S1249 ~ S2346</td></tr><tr><td>750(RGB)</td><td>S1 ~ S1152, S1249 ~ S2346</td></tr><tr><td>750(RGB)</td><td>S1 ~ S1125, S1276 ~ S2400</td></tr><tr><td>720(RGB)</td><td>S1 ~ S1080, S1321 ~ S2400</td></tr><tr><td>640(RGB)</td><td>S1 ~ S960, S1441 ~ S2400</td></tr><tr><td>600(RGB)</td><td>S1 ~ S900, S1501 ~ S2400</td></tr><tr><td>540(RGB)</td><td>S1 ~ S810, S1591 ~ S2400</td></tr><tr><td>480(RGB)</td><td>S1 ~ S720, S1681 ~S2400</td></tr><tr><td>480(RGB)</td><td>S961 ~ S1200, S1201 ~S2400</td></tr><tr><td>480(RGB)</td><td>S1 ~ S900, S1501 ~S2040</td></tr><tr><td>400(RGB)</td><td>S1201 ~S2400</td></tr><tr><td>400(RGB)</td><td>S1 ~ S600, S1801 ~ S2400</td></tr><tr><td>320(RGB)</td><td>S1441 ~ S2400</td></tr></table></td></tr>
<tr><td>VCOM</td><td>O</td><td>-Regulator output for common voltage of panel
Note: Vcom pad must connect to another side of the Vcom padvia the FPC. You can connect a 2.2uF capacitor to keep stable.</td></tr>
<tr><td colspan="3">Input Power Pin</td></tr>
<tr><td>Pin Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>AVDDR
AVDD</td><td>I</td><td>- Power supply to Analog circuits. You can connect a 2.2uF capacitor to keep stable.</td></tr>
<tr><td>AVEER
AVEE</td><td>I</td><td>- Power supply to Analog circuits. You can connect a 2.2uF capacitor to keep stable.</td></tr>
<tr><td>VCI</td><td>I</td><td>- Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.3V. You can connect a 2.2uF capacitor to keep stable.</td></tr>
<tr><td>VDDI</td><td>I</td><td>- Power supply to digital circuits. Connect to an external power supply of 1.65V to 3.3V. You can connect a 2.2uF capacitor to keep stable.</td></tr>
</table>

AVSS	I	- Ground of analog circuit of whole chip.
VSSAM	I	- Ground of High Speed Interface circuit.
VSSR	I	- Ground of regulator circuits.
CVSS	I	- Ground of charge pump circuit.
VSS	I	- Ground of digital circuit of whole chip.
Power Pin		
Pin Name	**I/O**	**Description**
DVDD	O	- Internal logic voltage output.
VDDMA	O	- Internal logic regulated power output for MIPI.
VDDML	O	- Internal logic regulated power for MIPI High Speed mode /Low Power mode
VGMP	O	- Output voltage generated from AVDD. LDO output for positive gamma voltage generator.
VGMN	O	- Output voltage generated from AVEE. LDO output for negative gamma voltage generator.
VGH	O	- High voltage level for GIP control signals and gate circuit of panel. You can connect a 1.0uF capacitor to keep stable.
VGL	O	- Low voltage level for GIP control signals and gate circuit of panel. You can connect a 1.0uF capacitor to keep stable.
MTP_PWR	I	- OTP programming power.
EXTP	O	-Control signal output to generate AVDD/AVEE
EXTN	O	-Control signal output to generate AVDD/AVEE
Test Pin		
Pin Name	**I/O**	**Description**
TESTP_L **TESTP_R** **TESTN_L** **TESTN_R** **TESTO**	O	- Internal Test pins. ***Leave the pin open when not in use.***

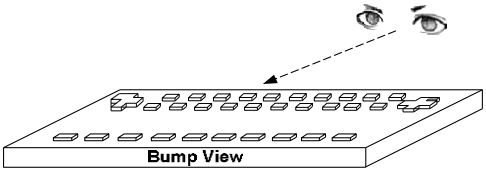
4.2. Output Bump Dimension

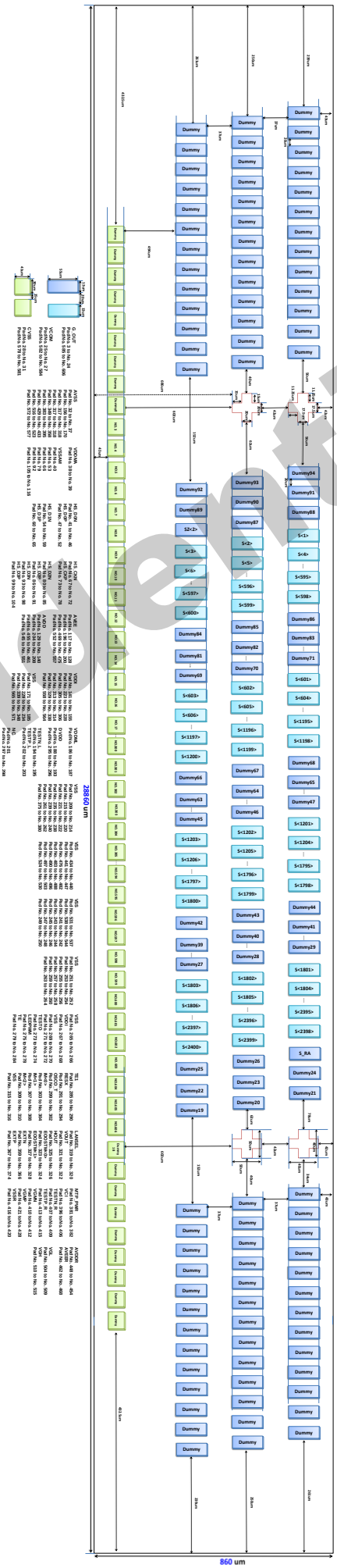
Au bump height： 9μm

Au bump size:

13μm x 55μm
Pad 623 to pad 3182

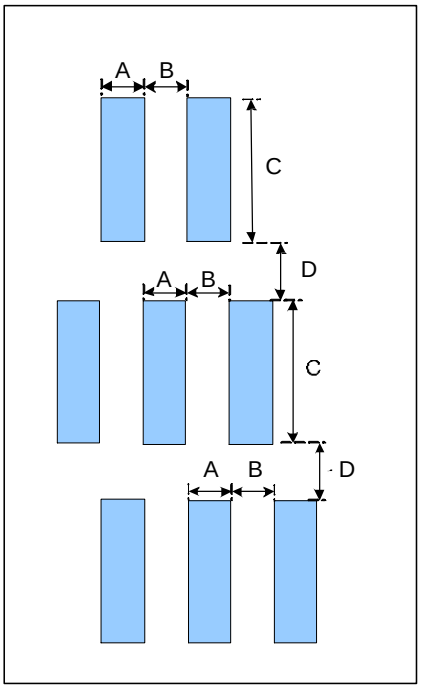
30μm x 41μm
Pad 1 to Pad 622





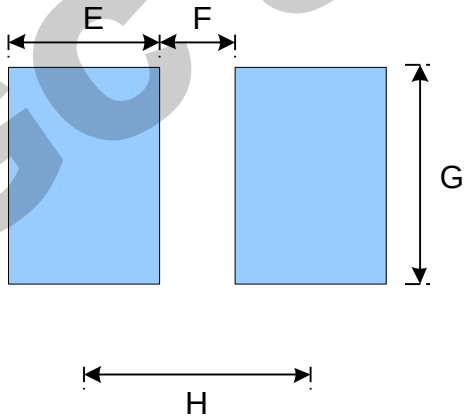
4.3. Input Bump Dimension

- **Output Pads**



Symbol	Item	Size
A	Bump Width	13 um
B	Bump Gap 1 (Horizontal)	20 um
C	Bump Height	55 um
D	Bump Gap 2 (Vertical)	37 um

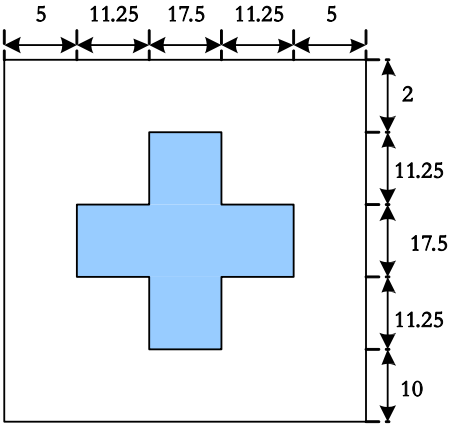
- **Input Pads**



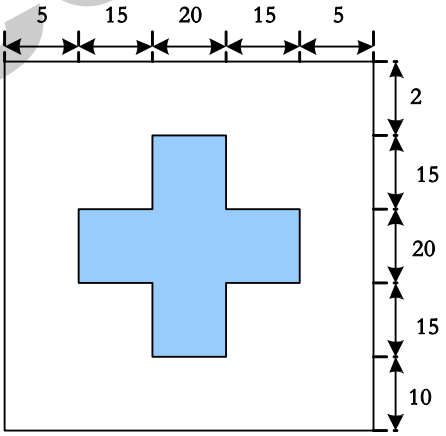
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15um
G	Bump Height	41 um
H	Bump Pitch	45 um
	Bump thickness	9 um

4.4. Alignment Mark Dimension

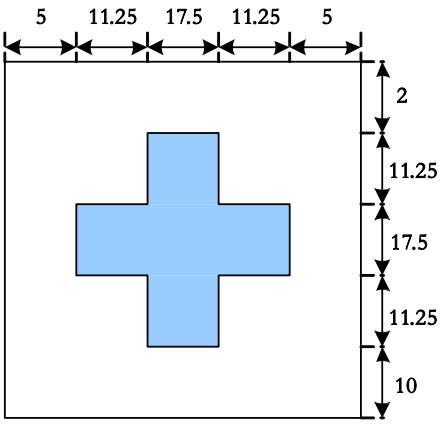
- **Alignment Mark ALIGN_L1 : (X,Y)=(-13706,368)**



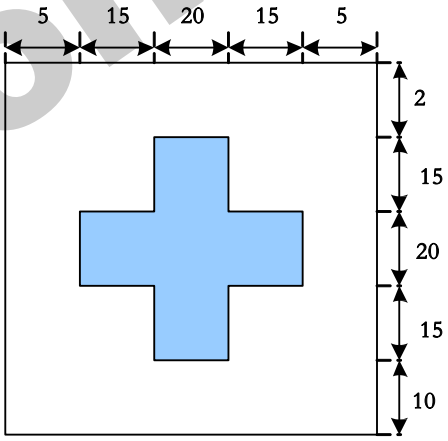
- **Alignment Mark ALIGN_L2 : (X,Y)=(-13706,281)**



- **Alignment Mark ALIGN_R1 : (X,Y)=(+13706,368)**



- **Alignment Mark ALIGN_R2 : (X,Y)=(+13706,281)**



4.5. Chip Information

Chip size	28860μm x860μm(include scribe line)
Chip thickness	200μm
Pad Location	Pad center
Coordinate Origin	Chip center

4.6. Pad Coordination

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
1	DUMMY	-13982.5	-366.5	71	HS_D1P	-10822.5	-366.5	141	AVDD	-7672.5	-366.5	211	AVDD	-4522.5	-366.5
2	DUMMY	-13937.5	-366.5	72	HS_D1P	-10777.5	-366.5	142	AVDD	-7627.5	-366.5	212	AVDD	-4477.5	-366.5
3	DUMMY	-13892.5	-366.5	73	VSSAM	-10732.5	-366.5	143	AVDD	-7582.5	-366.5	213	AVDD	-4432.5	-366.5
4	DUMMY	-13847.5	-366.5	74	HS_CKN	-10687.5	-366.5	144	AVDD	-7537.5	-366.5	214	AVDD	-4387.5	-366.5
5	DUMMY	-13802.5	-366.5	75	HS_CKN	-10642.5	-366.5	145	AVDD	-7492.5	-366.5	215	AVDD	-4342.5	-366.5
6	DUMMY	-13757.5	-366.5	76	HS_CKN	-10597.5	-366.5	146	AVDD	-7447.5	-366.5	216	VSS	-4297.5	-366.5
7	DUMMY	-13712.5	-366.5	77	HS_CKN	-10552.5	-366.5	147	AVDD	-7402.5	-366.5	217	VSS	-4252.5	-366.5
8	DUMMY	-13667.5	-366.5	78	HS_CKN	-10507.5	-366.5	148	VDDI	-7357.5	-366.5	218	VSS	-4207.5	-366.5
9	DUMMY0	-13622.5	-366.5	79	HS_CKN	-10462.5	-366.5	149	VDDI	-7312.5	-366.5	219	VSS	-4162.5	-366.5
10	G_OUT<22>	-13577.5	-366.5	80	HS_CKP	-10417.5	-366.5	150	VDDI	-7267.5	-366.5	220	VSS	-4117.5	-366.5
11	G_OUT<23>	-13532.5	-366.5	81	HS_CKP	-10372.5	-366.5	151	VDDI	-7222.5	-366.5	221	VSS	-4072.5	-366.5
12	G_OUT<24>	-13487.5	-366.5	82	HS_CKP	-10327.5	-366.5	152	VDDI	-7177.5	-366.5	222	VSS	-4027.5	-366.5
13	G_OUT<25>	-13442.5	-366.5	83	HS_CKP	-10282.5	-366.5	153	VDDI	-7132.5	-366.5	223	VSS	-3982.5	-366.5
14	G_OUT<26>	-13397.5	-366.5	84	HS_CKP	-10237.5	-366.5	154	VDDI	-7087.5	-366.5	224	VSS	-3937.5	-366.5
15	G_OUT<27>	-13352.5	-366.5	85	HS_CKP	-10192.5	-366.5	155	VDDI	-7042.5	-366.5	225	VSS	-3892.5	-366.5
16	G_OUT<28>	-13307.5	-366.5	86	VSSAM	-10147.5	-366.5	156	VDDI	-6997.5	-366.5	226	VSS	-3847.5	-366.5
17	G_OUT<29>	-13262.5	-366.5	87	HS_D2N	-10102.5	-366.5	157	VDDI	-6952.5	-366.5	227	VSS	-3802.5	-366.5
18	G_OUT<30>	-13217.5	-366.5	88	HS_D2N	-10057.5	-366.5	158	VDDI	-6907.5	-366.5	228	VSS	-3757.5	-366.5
19	G_OUT<31>	-13172.5	-366.5	89	HS_D2N	-10012.5	-366.5	159	VDDI	-6862.5	-366.5	229	VSS	-3712.5	-366.5
20	G_OUT<32>	-13127.5	-366.5	90	HS_D2N	-9967.5	-366.5	160	VDDI	-6817.5	-366.5	230	VDDI	-3667.5	-366.5
21	G_OUT<33>	-13082.5	-366.5	91	HS_D2N	-9922.5	-366.5	161	VDDI	-6772.5	-366.5	231	VDDI	-3622.5	-366.5
22	G_OUT<34>	-13037.5	-366.5	92	HS_D2N	-9877.5	-366.5	162	VDDI	-6727.5	-366.5	232	VDDI	-3577.5	-366.5
23	G_OUT<35>	-12992.5	-366.5	93	HS_D2P	-9832.5	-366.5	163	AVSS	-6682.5	-366.5	233	VDDI	-3532.5	-366.5
24	G_OUT<36>	-12947.5	-366.5	94	HS_D2P	-9787.5	-366.5	164	AVSS	-6637.5	-366.5	234	VDDI	-3487.5	-366.5
25	G_OUT<37>	-12902.5	-366.5	95	HS_D2P	-9742.5	-366.5	165	AVSS	-6592.5	-366.5	235	VDDI	-3442.5	-366.5
26	G_OUT<38>	-12857.5	-366.5	96	HS_D2P	-9697.5	-366.5	166	AVSS	-6547.5	-366.5	236	VSS	-3397.5	-366.5
27	G_OUT<39>	-12812.5	-366.5	97	HS_D2P	-9652.5	-366.5	167	AVSS	-6502.5	-366.5	237	VSS	-3352.5	-366.5
28	G_OUT<40>	-12767.5	-366.5	98	HS_D2P	-9607.5	-366.5	168	AVSS	-6457.5	-366.5	238	VSS	-3307.5	-366.5
29	G_OUT<41>	-12722.5	-366.5	99	VSSAM	-9562.5	-366.5	169	AVSS	-6412.5	-366.5	239	VSS	-3262.5	-366.5
30	G_OUT<42>	-12677.5	-366.5	100	HS_D3N	-9517.5	-366.5	170	AVSS	-6367.5	-366.5	240	VSS	-3217.5	-366.5
31	G_OUT<43>	-12632.5	-366.5	101	HS_D3N	-9472.5	-366.5	171	AVSS	-6322.5	-366.5	241	VSS	-3172.5	-366.5
32	VCOM	-12587.5	-366.5	102	HS_D3N	-9427.5	-366.5	172	AVSS	-6277.5	-366.5	242	VSS	-3127.5	-366.5
33	VCOM	-12542.5	-366.5	103	HS_D3N	-9382.5	-366.5	173	AVSS	-6232.5	-366.5	243	VSS	-3082.5	-366.5
34	VCOM	-12497.5	-366.5	104	HS_D3N	-9337.5	-366.5	174	AVSS	-6187.5	-366.5	244	VSS	-3037.5	-366.5
35	CVSS	-12442.5	-366.5	105	HS_D3N	-9292.5	-366.5	175	AVSS	-6142.5	-366.5	245	VSS	-2992.5	-366.5
36	CVSS	-12397.5	-366.5	106	HS_D3P	-9247.5	-366.5	176	AVSS	-6097.5	-366.5	246	VSS	-2947.5	-366.5
37	CVSS	-12352.5	-366.5	107	HS_D3P	-9202.5	-366.5	177	AVSS	-6052.5	-366.5	247	VSS	-2902.5	-366.5
38	CVSS	-12307.5	-366.5	108	HS_D3P	-9157.5	-366.5	178	VSS	-6007.5	-366.5	248	VSS	-2857.5	-366.5
39	AVSS	-12262.5	-366.5	109	HS_D3P	-9112.5	-366.5	179	VSS	-5962.5	-366.5	249	VSS	-2812.5	-366.5
40	AVSS	-12217.5	-366.5	110	HS_D3P	-9067.5	-366.5	180	VSS	-5917.5	-366.5	250	VSS	-2767.5	-366.5
41	AVSS	-12172.5	-366.5	111	HS_D3P	-9022.5	-366.5	181	VSS	-5872.5	-366.5	251	VSS	-2722.5	-366.5
42	AVSS	-12127.5	-366.5	112	VSSAM	-8977.5	-366.5	182	VSS	-5827.5	-366.5	252	VSS	-2677.5	-366.5
43	AVSS	-12082.5	-366.5	113	VSSAM	-8932.5	-366.5	183	VSS	-5782.5	-366.5	253	VSS	-2632.5	-366.5
44	AVSS	-12037.5	-366.5	114	VSSAM	-8887.5	-366.5	184	VSS	-5737.5	-366.5	254	VSS	-2587.5	-366.5
45	VDDMA	-11992.5	-366.5	115	VSSAM	-8842.5	-366.5	185	VSS	-5692.5	-366.5	255	VSS	-2542.5	-366.5
46	VDDMA	-11947.5	-366.5	116	VSSAM	-8797.5	-366.5	186	VSS	-5647.5	-366.5	256	VSS	-2497.5	-366.5
47	VSSAM	-11902.5	-366.5	117	VSSAM	-8752.5	-366.5	187	VSS	-5602.5	-366.5	257	VSS	-2452.5	-366.5
48	HS_D0N	-11857.5	-366.5	118	VSSAM	-8707.5	-366.5	188	VSS	-5557.5	-366.5	258	VSS	-2407.5	-366.5
49	HS_D0N	-11812.5	-366.5	119	VSSAM	-8662.5	-366.5	189	VSS	-5512.5	-366.5	259	VSS	-2362.5	-366.5
50	HS_D0N	-11767.5	-366.5	120	VSSAM	-8617.5	-366.5	190	VSS	-5467.5	-366.5	260	VSS	-2317.5	-366.5
51	HS_D0N	-11722.5	-366.5	121	VSSAM	-8572.5	-366.5	191	VSS	-5422.5	-366.5	261	VSS	-2272.5	-366.5
52	HS_D0N	-11677.5	-366.5	122	VSSAM	-8527.5	-366.5	192	VSS	-5377.5	-366.5	262	VSS	-2227.5	-366.5
53	HS_D0N	-11632.5	-366.5	123	VSSAM	-8482.5	-366.5	193	VDDML	-5332.5	-366.5	263	VSS	-2182.5	-366.5
54	HS_D0P	-11587.5	-366.5	124	AVEE	-8437.5	-366.5	194	VDDML	-5287.5	-366.5	264	VSS	-2137.5	-366.5
55	HS_D0P	-11542.5	-366.5	125	AVEE	-8392.5	-366.5	195	DVDD	-5242.5	-366.5	265	VSS	-2092.5	-366.5
56	HS_D0P	-11497.5	-366.5	126	AVEE	-8347.5	-366.5	196	DVDD	-5197.5	-366.5	266	VSS	-2047.5	-366.5
57	HS_D0P	-11452.5	-366.5	127	AVEE	-8302.5	-366.5	197	DVDD	-5152.5	-366.5	267	VSS	-2002.5	-366.5
58	HS_D0P	-11407.5	-366.5	128	AVEE	-8257.5	-366.5	198	DVDD	-5107.5	-366.5	268	VSS	-1957.5	-366.5
59	HS_D0P	-11362.5	-366.5	129	AVEE	-8212.5	-366.5	199	DVDD	-5062.5	-366.5	269	VSS	-1912.5	-366.5
60	VSSAM	-11317.5	-366.5	130	AVEE	-8167.5	-366.5	200	DVDD	-5017.5	-366.5	270	VSS	-1867.5	-366.5
61	HS_D1N	-11272.5	-366.5	131	AVEE	-8122.5	-366.5	201	TESTN_L	-4972.5	-366.5	271	VSS	-1822.5	-366.5
62	HS_D1N	-11227.5	-366.5	132	AVEE	-8077.5	-366.5	202	TESTN_L	-4927.5	-366.5	272	VSS	-1777.5	-366.5
63	HS_D1N	-11182.5	-366.5	133	AVEE	-8032.5	-366.5	203	AVEE	-4882.5	-366.5	273	VSS	-1732.5	-366.5
64	HS_D1N	-11137.5	-366.5	134	AVEE	-7987.5	-366.5	204	AVEE	-4837.5	-366.5	274	VDDI	-1687.5	-366.5
65	HS_D1N	-11092.5	-366.5	135	AVEE	-7942.5	-366.5	205	AVEE	-4792.5	-366.5	275	VDDI	-1642.5	-366.5
66	HS_D1N	-11047.5	-366.5	136	AVDD	-7897.5	-366.5	206	AVEE	-4747.5	-366.5	276	VSS	-1597.5	-366.5
67	HS_D1P	-11002.5	-366.5	137	AVDD	-7852.5	-366.5	207	AVEE	-4702.5	-366.5	277	VSS	-1552.5	-366.5
68	HS_D1P	-10957.5	-366.5	138	AVDD	-7807.5	-366.5	208	NC	-4657.5	-366.5	278	VSS	-1507.5	-366.5
69	HS_D1P	-10912.5	-366.5	139	AVDD	-7762.5	-366.5	209	TESTP_L	-4612.5	-366.5	279	VSS	-1462.5	-366.5
70	HS_D1P	-10867.5	-366.5	140	AVDD	-7717.5	-366.5	210	TESTP_L	-4567.5	-366.5	280	TESTO	-1417.5	-366.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
281	TESTO	-1372.5	-366.5	351	VSS	1777.5	-366.5	421	TESTP_R	4927.5	-366.5	491	VSS	8077.5	-366.5
282	LEDPWM	-1327.5	-366.5	352	VSS	1822.5	-366.5	422	TESTP_R	4972.5	-366.5	492	VSS	8122.5	-366.5
283	LEDPWM	-1282.5	-366.5	353	VSS	1867.5	-366.5	423	VSSR	5017.5	-366.5	493	VSS	8167.5	-366.5
284	LEDPWM	-1237.5	-366.5	354	VSS	1912.5	-366.5	424	VSSR	5062.5	-366.5	494	VSS	8212.5	-366.5
285	LEDPWM	-1192.5	-366.5	355	VSS	1957.5	-366.5	425	VSSR	5107.5	-366.5	495	VSS	8257.5	-366.5
286	TE	-1147.5	-366.5	356	AVSS	2002.5	-366.5	426	VSSR	5152.5	-366.5	496	VSS	8302.5	-366.5
287	TE	-1102.5	-366.5	357	AVSS	2047.5	-366.5	427	VSSR	5197.5	-366.5	497	VSS	8347.5	-366.5
288	TE	-1057.5	-366.5	358	AVSS	2092.5	-366.5	428	VGMP	5242.5	-366.5	498	VSS	8392.5	-366.5
289	TE	-1012.5	-366.5	359	AVSS	2137.5	-366.5	429	VGMP	5287.5	-366.5	499	VSS	8437.5	-366.5
290	TE	-967.5	-366.5	360	AVSS	2182.5	-366.5	430	VGMP	5332.5	-366.5	500	VSS	8482.5	-366.5
291	TE	-922.5	-366.5	361	AVSS	2227.5	-366.5	431	VGMP	5377.5	-366.5	501	VSS	8527.5	-366.5
292	TE1	-877.5	-366.5	362	AVSS	2272.5	-366.5	432	VGMP	5422.5	-366.5	502	VSS	8572.5	-366.5
293	TE1	-832.5	-366.5	363	AVSS	2317.5	-366.5	433	VGMP	5467.5	-366.5	503	VSS	8617.5	-366.5
294	TE1	-787.5	-366.5	364	AVSS	2362.5	-366.5	434	VGMP	5512.5	-366.5	504	VSS	8662.5	-366.5
295	TE1	-742.5	-366.5	365	AVSS	2407.5	-366.5	435	VGMP	5557.5	-366.5	505	VSS	8707.5	-366.5
296	TE1	-697.5	-366.5	366	EXTN	2452.5	-366.5	436	AVSS	5602.5	-366.5	506	VSS	8752.5	-366.5
297	TE1	-652.5	-366.5	367	EXTN	2497.5	-366.5	437	AVSS	5647.5	-366.5	507	VSS	8797.5	-366.5
298	RESX	-607.5	-366.5	368	EXTN	2542.5	-366.5	438	AVSS	5692.5	-366.5	508	VSS	8842.5	-366.5
299	RESX	-562.5	-366.5	369	EXTN	2587.5	-366.5	439	AVSS	5737.5	-366.5	509	VSS	8887.5	-366.5
300	RESX	-517.5	-366.5	370	EXTN	2632.5	-366.5	440	AVSS	5782.5	-366.5	510	VSS	8932.5	-366.5
301	RESX	-472.5	-366.5	371	EXTN	2677.5	-366.5	441	VSS	5827.5	-366.5	511	VGL	8977.5	-366.5
302	DVDD	-427.5	-366.5	372	EXTN	2722.5	-366.5	442	VSS	5872.5	-366.5	512	VGL	9022.5	-366.5
303	DVDD	-382.5	-366.5	373	EXTN	2767.5	-366.5	443	VSS	5917.5	-366.5	513	VGL	9067.5	-366.5
304	NC	-337.5	-366.5	374	EXTP	2812.5	-366.5	444	VSS	5962.5	-366.5	514	VGL	9112.5	-366.5
305	NC	-292.5	-366.5	375	EXTP	2857.5	-366.5	445	VSS	6007.5	-366.5	515	VGL	9157.5	-366.5
306	OSC0_T	-247.5	-366.5	376	EXTP	2902.5	-366.5	446	VSS	6052.5	-366.5	516	VGL	9202.5	-366.5
307	OSC0_T	-202.5	-366.5	377	EXTP	2947.5	-366.5	447	VSS	6097.5	-366.5	517	VGH	9247.5	-366.5
308	OSC1_T	-157.5	-366.5	378	EXTP	2992.5	-366.5	448	VSS	6142.5	-366.5	518	VGH	9292.5	-366.5
309	OSC1_T	-112.5	-366.5	379	EXTP	3037.5	-366.5	449	VSS	6187.5	-366.5	519	VGH	9337.5	-366.5
310	IM<0>	-67.5	-366.5	380	EXTP	3082.5	-366.5	450	VSS	6232.5	-366.5	520	VGH	9382.5	-366.5
311	IM<0>	-22.5	-366.5	381	EXTP	3127.5	-366.5	451	VSS	6277.5	-366.5	521	VGH	9427.5	-366.5
312	VDDI	22.5	-366.5	382	VSS	3172.5	-366.5	452	VSS	6322.5	-366.5	522	VGH	9472.5	-366.5
313	VDDI	67.5	-366.5	383	VSS	3217.5	-366.5	453	VSS	6367.5	-366.5	523	AVSS	9517.5	-366.5
314	IM<1>	112.5	-366.5	384	VSS	3262.5	-366.5	454	VSS	6412.5	-366.5	524	AVSS	9562.5	-366.5
315	IM<1>	157.5	-366.5	385	VSS	3307.5	-366.5	455	AVDDR	6457.5	-366.5	525	AVSS	9607.5	-366.5
316	IM<2>	202.5	-366.5	386	VSS	3352.5	-366.5	456	AVDDR	6502.5	-366.5	526	AVSS	9652.5	-366.5
317	IM<2>	247.5	-366.5	387	VSS	3397.5	-366.5	457	AVDDR	6547.5	-366.5	527	AVSS	9697.5	-366.5
318	NC	292.5	-366.5	388	MTP_PWR	3442.5	-366.5	458	AVDDR	6592.5	-366.5	528	AVSS	9742.5	-366.5
319	NC	337.5	-366.5	389	MTP_PWR	3487.5	-366.5	459	AVDDR	6637.5	-366.5	529	AVSS	9787.5	-366.5
320	VDDI	382.5	-366.5	390	AVSS	3532.5	-366.5	460	AVDDR	6682.5	-366.5	530	AVSS	9832.5	-366.5
321	VDDI	427.5	-366.5	391	AVSS	3577.5	-366.5	461	AVDDR	6727.5	-366.5	531	VSS	9877.5	-366.5
322	VSS	472.5	-366.5	392	AVSS	3622.5	-366.5	462	AVDD	6772.5	-366.5	532	VSS	9922.5	-366.5
323	VSS	517.5	-366.5	393	AVSS	3667.5	-366.5	463	AVDD	6817.5	-366.5	533	VSS	9967.5	-366.5
324	AVSS	562.5	-366.5	394	AVSS	3712.5	-366.5	464	AVDD	6862.5	-366.5	534	VSS	10012.5	-366.5
325	AVSS	607.5	-366.5	395	AVSS	3757.5	-366.5	465	AVDD	6907.5	-366.5	535	VSS	10057.5	-366.5
326	LANSEL	652.5	-366.5	396	AVSS	3802.5	-366.5	466	AVDD	6952.5	-366.5	536	VSS	10102.5	-366.5
327	LANSEL	697.5	-366.5	397	AVSS	3847.5	-366.5	467	AVDD	6997.5	-366.5	537	VSS	10147.5	-366.5
328	VOUT	742.5	-366.5	398	AVSS	3892.5	-366.5	468	AVDD	7042.5	-366.5	538	VSS	10192.5	-366.5
329	VOUT	787.5	-366.5	399	AVSS	3937.5	-366.5	469	AVEER	7087.5	-366.5	539	VSS	10237.5	-366.5
330	BOOSTM<0>	832.5	-366.5	400	AVSS	3982.5	-366.5	470	AVEER	7132.5	-366.5	540	VSS	10282.5	-366.5
331	BOOSTM<0>	877.5	-366.5	401	AVSS	4027.5	-366.5	471	AVEER	7177.5	-366.5	541	VSS	10327.5	-366.5
332	HOUT	922.5	-366.5	402	AVSS	4072.5	-366.5	472	AVEER	7222.5	-366.5	542	VSS	10372.5	-366.5
333	HOUT	967.5	-366.5	403	VCI	4117.5	-366.5	473	AVEER	7267.5	-366.5	543	VSS	10417.5	-366.5
334	BOOSTM<1>	1012.5	-366.5	404	VCI	4162.5	-366.5	474	AVEER	7312.5	-366.5	544	VSS	10462.5	-366.5
335	BOOSTM<1>	1057.5	-366.5	405	VCI	4207.5	-366.5	475	AVEER	7357.5	-366.5	545	VSS	10507.5	-366.5
336	VDDI	1102.5	-366.5	406	VCI	4252.5	-366.5	476	AVEE	7402.5	-366.5	546	VSS	10552.5	-366.5
337	VDDI	1147.5	-366.5	407	VCI	4297.5	-366.5	477	AVEE	7447.5	-366.5	547	VSS	10597.5	-366.5
338	VDDI	1192.5	-366.5	408	VCI	4342.5	-366.5	478	AVEE	7492.5	-366.5	548	VSS	10642.5	-366.5
339	VDDI	1237.5	-366.5	409	VCI	4387.5	-366.5	479	AVEE	7537.5	-366.5	549	VSS	10687.5	-366.5
340	VDDI	1282.5	-366.5	410	VCI	4432.5	-366.5	480	AVEE	7582.5	-366.5	550	VSS	10732.5	-366.5
341	VDDI	1327.5	-366.5	411	VCI	4477.5	-366.5	481	AVEE	7627.5	-366.5	551	VSS	10777.5	-366.5
342	VDDI	1372.5	-366.5	412	VCI	4522.5	-366.5	482	AVEE	7672.5	-366.5	552	AVDD	10822.5	-366.5
343	VDDI	1417.5	-366.5	413	VCI	4567.5	-366.5	483	VSS	7717.5	-366.5	553	AVDD	10867.5	-366.5
344	VDDI	1462.5	-366.5	414	TESTN_R	4612.5	-366.5	484	VSS	7762.5	-366.5	554	AVDD	10912.5	-366.5
345	VDDI	1507.5	-366.5	415	TESTN_R	4657.5	-366.5	485	VSS	7807.5	-366.5	555	AVDD	10957.5	-366.5
346	VSS	1552.5	-366.5	416	TESTN_R	4702.5	-366.5	486	VSS	7852.5	-366.5	556	AVDD	11002.5	-366.5
347	VSS	1597.5	-366.5	417	VGMN	4747.5	-366.5	487	VSS	7897.5	-366.5	557	AVDD	11047.5	-366.5
348	VSS	1642.5	-366.5	418	VGMN	4792.5	-366.5	488	VSS	7942.5	-366.5	558	AVDD	11092.5	-366.5
349	VSS	1687.5	-366.5	419	VGMN	4837.5	-366.5	489	VSS	7987.5	-366.5	559	AVEE	11137.5	-366.5
350	VSS	1732.5	-366.5	420	TESTP_R	4882.5	-366.5	490	VSS	8032.5	-366.5	560	AVEE	11182.5	-366.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
561	AVEE	11227.5	-366.5	631	DUMMY	14107.5	267.5	701	S<2372>	13216.5	267.5	771	S<2302>	12446.5	359.5
562	AVEE	11272.5	-366.5	632	DUMMY	14140.5	267.5	702	S<2371>	13205.5	359.5	772	S<2301>	12435.5	175.5
563	AVEE	11317.5	-366.5	633	DUMMY	14173.5	267.5	703	S<2370>	13194.5	175.5	773	S<2300>	12424.5	267.5
564	AVEE	11362.5	-366.5	634	DUMMY	14162.5	359.5	704	S<2369>	13183.5	267.5	774	S<2299>	12413.5	359.5
565	VDDI	11407.5	-366.5	635	DUMMY	14129.5	359.5	705	S<2368>	13172.5	359.5	775	S<2298>	12402.5	175.5
566	VDDI	11452.5	-366.5	636	DUMMY	14096.5	359.5	706	S<2367>	13161.5	175.5	776	S<2297>	12391.5	267.5
567	VDDI	11497.5	-366.5	637	DUMMY	14063.5	359.5	707	S<2366>	13150.5	267.5	777	S<2296>	12380.5	359.5
568	VDDI	11542.5	-366.5	638	DUMMY	14041.5	267.5	708	S<2365>	13139.5	359.5	778	S<2295>	12369.5	175.5
569	VDDI	11587.5	-366.5	639	DUMMY	14030.5	359.5	709	S<2364>	13128.5	175.5	779	S<2294>	12358.5	267.5
570	VDDI	11632.5	-366.5	640	DUMMY	14008.5	267.5	710	S<2363>	13117.5	267.5	780	S<2293>	12347.5	359.5
571	VDDI	11677.5	-366.5	641	DUMMY	13997.5	359.5	711	S<2362>	13106.5	359.5	781	S<2292>	12336.5	175.5
572	VSS	11722.5	-366.5	642	DUMMY	13975.5	267.5	712	S<2361>	13095.5	175.5	782	S<2291>	12325.5	267.5
573	VSS	11767.5	-366.5	643	DUMMY	13964.5	359.5	713	S<2360>	13084.5	267.5	783	S<2290>	12314.5	359.5
574	VSS	11812.5	-366.5	644	DUMMY	13953.5	175.5	714	S<2359>	13073.5	359.5	784	S<2289>	12303.5	175.5
575	VSS	11857.5	-366.5	645	DUMMY	13942.5	267.5	715	S<2358>	13062.5	175.5	785	S<2288>	12292.5	267.5
576	VSS	11902.5	-366.5	646	DUMMY	13931.5	359.5	716	S<2357>	13051.5	267.5	786	S<2287>	12281.5	359.5
577	VSS	11947.5	-366.5	647	DUMMY	13920.5	175.5	717	S<2356>	13040.5	359.5	787	S<2286>	12270.5	175.5
578	VSS	11992.5	-366.5	648	DUMMY	13909.5	267.5	718	S<2355>	13029.5	175.5	788	S<2285>	12259.5	267.5
579	AVSS	12037.5	-366.5	649	DUMMY	13898.5	359.5	719	S<2354>	13018.5	267.5	789	S<2284>	12248.5	359.5
580	AVSS	12082.5	-366.5	650	DUMMY	13887.5	175.5	720	S<2353>	13007.5	359.5	790	S<2283>	12237.5	175.5
581	AVSS	12127.5	-366.5	651	DUMMY	13876.5	267.5	721	S<2352>	12996.5	175.5	791	S<2282>	12226.5	267.5
582	AVSS	12172.5	-366.5	652	DUMMY	13865.5	359.5	722	S<2351>	12985.5	267.5	792	S<2281>	12215.5	359.5
583	AVSS	12217.5	-366.5	653	DUMMY	13854.5	175.5	723	S<2350>	12974.5	359.5	793	S<2280>	12204.5	175.5
584	AVSS	12262.5	-366.5	654	DUMMY	13843.5	267.5	724	S<2349>	12963.5	175.5	794	S<2279>	12193.5	267.5
585	CVSS	12307.5	-366.5	655	DUMMY	13832.5	359.5	725	S<2348>	12952.5	267.5	795	S<2278>	12182.5	359.5
586	CVSS	12352.5	-366.5	656	DUMMY	13821.5	175.5	726	S<2347>	12941.5	359.5	796	S<2277>	12171.5	175.5
587	CVSS	12397.5	-366.5	657	DUMMY	13810.5	267.5	727	S<2346>	12930.5	175.5	797	S<2276>	12160.5	267.5
588	CVSS	12442.5	-366.5	658	DUMMY	13799.5	359.5	728	S<2345>	12919.5	267.5	798	S<2275>	12149.5	359.5
589	VCOM	12497.5	-366.5	659	DUMMY	13788.5	175.5	729	S<2344>	12908.5	359.5	799	S<2274>	12138.5	175.5
590	VCOM	12542.5	-366.5	660	DUMMY	13777.5	267.5	730	S<2343>	12897.5	175.5	800	S<2273>	12127.5	267.5
591	VCOM	12587.5	-366.5	661	DUMMY	13766.5	359.5	731	S<2342>	12886.5	267.5	801	S<2272>	12116.5	359.5
592	G_OUT<21>	12632.5	-366.5	662	Unput Label	13706	281	732	S<2341>	12875.5	359.5	802	S<2271>	12105.5	175.5
593	G_OUT<20>	12677.5	-366.5	663	Unput Label	13706	368	733	S<2340>	12864.5	175.5	803	S<2270>	12094.5	267.5
594	G_OUT<19>	12722.5	-366.5	664	DUMMY19	13623.5	175.5	734	S<2339>	12853.5	267.5	804	S<2269>	12083.5	359.5
595	G_OUT<18>	12767.5	-366.5	665	DUMMY20	13612.5	267.5	735	S<2338>	12842.5	359.5	805	S<2268>	12072.5	175.5
596	G_OUT<17>	12812.5	-366.5	666	DUMMY21	13601.5	359.5	736	S<2337>	12831.5	175.5	806	S<2267>	12061.5	267.5
597	G_OUT<16>	12857.5	-366.5	667	DUMMY22	13590.5	175.5	737	S<2336>	12820.5	267.5	807	S<2266>	12050.5	359.5
598	G_OUT<15>	12902.5	-366.5	668	DUMMY23	13579.5	267.5	738	S<2335>	12809.5	359.5	808	S<2265>	12039.5	175.5
599	G_OUT<14>	12947.5	-366.5	669	DUMMY24	13568.5	359.5	739	S<2334>	12798.5	175.5	809	S<2264>	12028.5	267.5
600	G_OUT<13>	12992.5	-366.5	670	DUMMY25	13557.5	175.5	740	S<2333>	12787.5	267.5	810	S<2263>	12017.5	359.5
601	G_OUT<12>	13037.5	-366.5	671	DUMMY26	13546.5	267.5	741	S<2332>	12776.5	359.5	811	S<2262>	12006.5	175.5
602	G_OUT<11>	13082.5	-366.5	672	SZ<3>	13535.5	359.5	742	S<2331>	12765.5	175.5	812	S<2261>	11995.5	267.5
603	G_OUT<10>	13127.5	-366.5	673	S<2400>	13524.5	175.5	743	S<2330>	12754.5	267.5	813	S<2260>	11984.5	359.5
604	G_OUT<9>	13172.5	-366.5	674	S<2399>	13513.5	267.5	744	S<2329>	12743.5	359.5	814	S<2259>	11973.5	175.5
605	G_OUT<8>	13217.5	-366.5	675	S<2398>	13502.5	359.5	745	S<2328>	12732.5	175.5	815	S<2258>	11962.5	267.5
606	G_OUT<7>	13262.5	-366.5	676	S<2397>	13491.5	175.5	746	S<2327>	12721.5	267.5	816	S<2257>	11951.5	359.5
607	G_OUT<6>	13307.5	-366.5	677	S<2396>	13480.5	267.5	747	S<2326>	12710.5	359.5	817	S<2256>	11940.5	175.5
608	G_OUT<5>	13352.5	-366.5	678	S<2395>	13469.5	359.5	748	S<2325>	12699.5	175.5	818	S<2255>	11929.5	267.5
609	G_OUT<4>	13397.5	-366.5	679	S<2394>	13458.5	175.5	749	S<2324>	12688.5	267.5	819	S<2254>	11918.5	359.5
610	G_OUT<3>	13442.5	-366.5	680	S<2393>	13447.5	267.5	750	S<2323>	12677.5	359.5	820	S<2253>	11907.5	175.5
611	G_OUT<2>	13487.5	-366.5	681	S<2392>	13436.5	359.5	751	S<2322>	12666.5	175.5	821	S<2252>	11896.5	267.5
612	G_OUT<1>	13532.5	-366.5	682	S<2391>	13425.5	175.5	752	S<2321>	12655.5	267.5	822	S<2251>	11885.5	359.5
613	G_OUT<0>	13577.5	-366.5	683	S<2390>	13414.5	267.5	753	S<2320>	12644.5	359.5	823	S<2250>	11874.5	175.5
614	DUMMY18	13622.5	-366.5	684	S<2389>	13403.5	359.5	754	S<2319>	12633.5	175.5	824	S<2249>	11863.5	267.5
615	DUMMY	13667.5	-366.5	685	S<2388>	13392.5	175.5	755	S<2318>	12622.5	267.5	825	S<2248>	11852.5	359.5
616	DUMMY	13712.5	-366.5	686	S<2387>	13381.5	267.5	756	S<2317>	12611.5	359.5	826	S<2247>	11841.5	175.5
617	DUMMY	13757.5	-366.5	687	S<2386>	13370.5	359.5	757	S<2316>	12600.5	175.5	827	S<2246>	11830.5	267.5
618	DUMMY	13802.5	-366.5	688	S<2385>	13359.5	175.5	758	S<2315>	12589.5	267.5	828	S<2245>	11819.5	359.5
619	DUMMY	13847.5	-366.5	689	S<2384>	13348.5	267.5	759	S<2314>	12578.5	359.5	829	S<2244>	11808.5	175.5
620	DUMMY	13892.5	-366.5	690	S<2383>	13337.5	359.5	760	S<2313>	12567.5	175.5	830	S<2243>	11797.5	267.5
621	DUMMY	13937.5	-366.5	691	S<2382>	13326.5	175.5	761	S<2312>	12556.5	267.5	831	S<2242>	11786.5	359.5
622	DUMMY	13982.5	-366.5	692	S<2381>	13315.5	267.5	762	S<2311>	12545.5	359.5	832	S<2241>	11775.5	175.5
623	DUMMY	13986.5	175.5	693	S<2380>	13304.5	359.5	763	S<2310>	12534.5	175.5	833	S<2240>	11764.5	267.5
624	DUMMY	14019.5	175.5	694	S<2379>	13293.5	175.5	764	S<2309>	12523.5	267.5	834	S<2239>	11753.5	359.5
625	DUMMY	14052.5	175.5	695	S<2378>	13282.5	267.5	765	S<2308>	12512.5	359.5	835	S<2238>	11742.5	175.5
626	DUMMY	14085.5	175.5	696	S<2377>	13271.5	359.5	766	S<2307>	12501.5	175.5	836	S<2237>	11731.5	267.5
627	DUMMY	14118.5	175.5	697	S<2376>	13260.5	175.5	767	S<2306>	12490.5	267.5	837	S<2236>	11720.5	359.5
628	DUMMY	14151.5	175.5	698	S<2375>	13249.5	267.5	768	S<2305>	12479.5	359.5	838	S<2235>	11709.5	175.5
629	DUMMY	14184.5	175.5	699	S<2374>	13238.5	359.5	769	S<2304>	12468.5	175.5	839	S<2234>	11698.5	267.5
630	DUMMY	14074.5	267.5	700	S<2373>	13227.5	175.5	770	S<2303>	12457.5	267.5	840	S<2233>	11687.5	359.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
841	S<2232>	11676.5	175.5	911	S<2162>	10906.5	267.5	981	S<2092>	10136.5	359.5	1051	S<2022>	9366.5	175.5
842	S<2231>	11665.5	267.5	912	S<2161>	10895.5	359.5	982	S<2091>	10125.5	175.5	1052	S<2021>	9355.5	267.5
843	S<2230>	11654.5	359.5	913	S<2160>	10884.5	175.5	983	S<2090>	10114.5	267.5	1053	S<2020>	9344.5	359.5
844	S<2229>	11643.5	175.5	914	S<2159>	10873.5	267.5	984	S<2089>	10103.5	359.5	1054	S<2019>	9333.5	175.5
845	S<2228>	11632.5	267.5	915	S<2158>	10862.5	359.5	985	S<2088>	10092.5	175.5	1055	S<2018>	9322.5	267.5
846	S<2227>	11621.5	359.5	916	S<2157>	10851.5	175.5	986	S<2087>	10081.5	267.5	1056	S<2017>	9311.5	359.5
847	S<2226>	11610.5	175.5	917	S<2156>	10840.5	267.5	987	S<2086>	10070.5	359.5	1057	S<2016>	9300.5	175.5
848	S<2225>	11599.5	267.5	918	S<2155>	10829.5	359.5	988	S<2085>	10059.5	175.5	1058	S<2015>	9289.5	267.5
849	S<2224>	11588.5	359.5	919	S<2154>	10818.5	175.5	989	S<2084>	10048.5	267.5	1059	S<2014>	9278.5	359.5
850	S<2223>	11577.5	175.5	920	S<2153>	10807.5	267.5	990	S<2083>	10037.5	359.5	1060	S<2013>	9267.5	175.5
851	S<2222>	11566.5	267.5	921	S<2152>	10796.5	359.5	991	S<2082>	10026.5	175.5	1061	S<2012>	9256.5	267.5
852	S<2221>	11555.5	359.5	922	S<2151>	10785.5	175.5	992	S<2081>	10015.5	267.5	1062	S<2011>	9245.5	359.5
853	S<2220>	11544.5	175.5	923	S<2150>	10774.5	267.5	993	S<2080>	10004.5	359.5	1063	S<2010>	9234.5	175.5
854	S<2219>	11533.5	267.5	924	S<2149>	10763.5	359.5	994	S<2079>	9993.5	175.5	1064	S<2009>	9223.5	267.5
855	S<2218>	11522.5	359.5	925	S<2148>	10752.5	175.5	995	S<2078>	9982.5	267.5	1065	S<2008>	9212.5	359.5
856	S<2217>	11511.5	175.5	926	S<2147>	10741.5	267.5	996	S<2077>	9971.5	359.5	1066	S<2007>	9201.5	175.5
857	S<2216>	11500.5	267.5	927	S<2146>	10730.5	359.5	997	S<2076>	9960.5	175.5	1067	S<2006>	9190.5	267.5
858	S<2215>	11489.5	359.5	928	S<2145>	10719.5	175.5	998	S<2075>	9949.5	267.5	1068	S<2005>	9179.5	359.5
859	S<2214>	11478.5	175.5	929	S<2144>	10708.5	267.5	999	S<2074>	9938.5	359.5	1069	S<2004>	9168.5	175.5
860	S<2213>	11467.5	267.5	930	S<2143>	10697.5	359.5	1000	S<2073>	9927.5	175.5	1070	S<2003>	9157.5	267.5
861	S<2212>	11456.5	359.5	931	S<2142>	10686.5	175.5	1001	S<2072>	9916.5	267.5	1071	S<2002>	9146.5	359.5
862	S<2211>	11445.5	175.5	932	S<2141>	10675.5	267.5	1002	S<2071>	9905.5	359.5	1072	S<2001>	9135.5	175.5
863	S<2210>	11434.5	267.5	933	S<2140>	10664.5	359.5	1003	S<2070>	9894.5	175.5	1073	S<2000>	9124.5	267.5
864	S<2209>	11423.5	359.5	934	S<2139>	10653.5	175.5	1004	S<2069>	9883.5	267.5	1074	S<1999>	9113.5	359.5
865	S<2208>	11412.5	175.5	935	S<2138>	10642.5	267.5	1005	S<2068>	9872.5	359.5	1075	S<1998>	9102.5	175.5
866	S<2207>	11401.5	267.5	936	S<2137>	10631.5	359.5	1006	S<2067>	9861.5	175.5	1076	S<1997>	9091.5	267.5
867	S<2206>	11390.5	359.5	937	S<2136>	10620.5	175.5	1007	S<2066>	9850.5	267.5	1077	S<1996>	9080.5	359.5
868	S<2205>	11379.5	175.5	938	S<2135>	10609.5	267.5	1008	S<2065>	9839.5	359.5	1078	S<1995>	9069.5	175.5
869	S<2204>	11368.5	267.5	939	S<2134>	10598.5	359.5	1009	S<2064>	9828.5	175.5	1079	S<1994>	9058.5	267.5
870	S<2203>	11357.5	359.5	940	S<2133>	10587.5	175.5	1010	S<2063>	9817.5	267.5	1080	S<1993>	9047.5	359.5
871	S<2202>	11346.5	175.5	941	S<2132>	10576.5	267.5	1011	S<2062>	9806.5	359.5	1081	S<1992>	9036.5	175.5
872	S<2201>	11335.5	267.5	942	S<2131>	10565.5	359.5	1012	S<2061>	9795.5	175.5	1082	S<1991>	9025.5	267.5
873	S<2200>	11324.5	359.5	943	S<2130>	10554.5	175.5	1013	S<2060>	9784.5	267.5	1083	S<1990>	9014.5	359.5
874	S<2199>	11313.5	175.5	944	S<2129>	10543.5	267.5	1014	S<2059>	9773.5	359.5	1084	S<1989>	9003.5	175.5
875	S<2198>	11302.5	267.5	945	S<2128>	10532.5	359.5	1015	S<2058>	9762.5	175.5	1085	S<1988>	8992.5	267.5
876	S<2197>	11291.5	359.5	946	S<2127>	10521.5	175.5	1016	S<2057>	9751.5	267.5	1086	S<1987>	8981.5	359.5
877	S<2196>	11280.5	175.5	947	S<2126>	10510.5	267.5	1017	S<2056>	9740.5	359.5	1087	S<1986>	8970.5	175.5
878	S<2195>	11269.5	267.5	948	S<2125>	10499.5	359.5	1018	S<2055>	9729.5	175.5	1088	S<1985>	8959.5	267.5
879	S<2194>	11258.5	359.5	949	S<2124>	10488.5	175.5	1019	S<2054>	9718.5	267.5	1089	S<1984>	8948.5	359.5
880	S<2193>	11247.5	175.5	950	S<2123>	10477.5	267.5	1020	S<2053>	9707.5	359.5	1090	S<1983>	8937.5	175.5
881	S<2192>	11236.5	267.5	951	S<2122>	10466.5	359.5	1021	S<2052>	9696.5	175.5	1091	S<1982>	8926.5	267.5
882	S<2191>	11225.5	359.5	952	S<2121>	10455.5	175.5	1022	S<2051>	9685.5	267.5	1092	S<1981>	8915.5	359.5
883	S<2190>	11214.5	175.5	953	S<2120>	10444.5	267.5	1023	S<2050>	9674.5	359.5	1093	S<1980>	8904.5	175.5
884	S<2189>	11203.5	267.5	954	S<2119>	10433.5	359.5	1024	S<2049>	9663.5	175.5	1094	S<1979>	8893.5	267.5
885	S<2188>	11192.5	359.5	955	S<2118>	10422.5	175.5	1025	S<2048>	9652.5	267.5	1095	S<1978>	8882.5	359.5
886	S<2187>	11181.5	175.5	956	S<2117>	10411.5	267.5	1026	S<2047>	9641.5	359.5	1096	S<1977>	8871.5	175.5
887	S<2186>	11170.5	267.5	957	S<2116>	10400.5	359.5	1027	S<2046>	9630.5	175.5	1097	S<1976>	8860.5	267.5
888	S<2185>	11159.5	359.5	958	S<2115>	10389.5	175.5	1028	S<2045>	9619.5	267.5	1098	S<1975>	8849.5	359.5
889	S<2184>	11148.5	175.5	959	S<2114>	10378.5	267.5	1029	S<2044>	9608.5	359.5	1099	S<1974>	8838.5	175.5
890	S<2183>	11137.5	267.5	960	S<2113>	10367.5	359.5	1030	S<2043>	9597.5	175.5	1100	S<1973>	8827.5	267.5
891	S<2182>	11126.5	359.5	961	S<2112>	10356.5	175.5	1031	S<2042>	9586.5	267.5	1101	S<1972>	8816.5	359.5
892	S<2181>	11115.5	175.5	962	S<2111>	10345.5	267.5	1032	S<2041>	9575.5	359.5	1102	S<1971>	8805.5	175.5
893	S<2180>	11104.5	267.5	963	S<2110>	10334.5	359.5	1033	S<2040>	9564.5	175.5	1103	S<1970>	8794.5	267.5
894	S<2179>	11093.5	359.5	964	S<2109>	10323.5	175.5	1034	S<2039>	9553.5	267.5	1104	S<1969>	8783.5	359.5
895	S<2178>	11082.5	175.5	965	S<2108>	10312.5	267.5	1035	S<2038>	9542.5	359.5	1105	S<1968>	8772.5	175.5
896	S<2177>	11071.5	267.5	966	S<2107>	10301.5	359.5	1036	S<2037>	9531.5	175.5	1106	S<1967>	8761.5	267.5
897	S<2176>	11060.5	359.5	967	S<2106>	10290.5	175.5	1037	S<2036>	9520.5	267.5	1107	S<1966>	8750.5	359.5
898	S<2175>	11049.5	175.5	968	S<2105>	10279.5	267.5	1038	S<2035>	9509.5	359.5	1108	S<1965>	8739.5	175.5
899	S<2174>	11038.5	267.5	969	S<2104>	10268.5	359.5	1039	S<2034>	9498.5	175.5	1109	S<1964>	8728.5	267.5
900	S<2173>	11027.5	359.5	970	S<2103>	10257.5	175.5	1040	S<2033>	9487.5	267.5	1110	S<1963>	8717.5	359.5
901	S<2172>	11016.5	175.5	971	S<2102>	10246.5	267.5	1041	S<2032>	9476.5	359.5	1111	S<1962>	8706.5	175.5
902	S<2171>	11005.5	267.5	972	S<2101>	10235.5	359.5	1042	S<2031>	9465.5	175.5	1112	S<1961>	8695.5	267.5
903	S<2170>	10994.5	359.5	973	S<2100>	10224.5	175.5	1043	S<2030>	9454.5	267.5	1113	S<1960>	8684.5	359.5
904	S<2169>	10983.5	175.5	974	S<2099>	10213.5	267.5	1044	S<2029>	9443.5	359.5	1114	S<1959>	8673.5	175.5
905	S<2168>	10972.5	267.5	975	S<2098>	10202.5	359.5	1045	S<2028>	9432.5	175.5	1115	S<1958>	8662.5	267.5
906	S<2167>	10961.5	359.5	976	S<2097>	10191.5	175.5	1046	S<2027>	9421.5	267.5	1116	S<1957>	8651.5	359.5
907	S<2166>	10950.5	175.5	977	S<2096>	10180.5	267.5	1047	S<2026>	9410.5	359.5	1117	S<1956>	8640.5	175.5
908	S<2165>	10939.5	267.5	978	S<2095>	10169.5	359.5	1048	S<2025>	9399.5	175.5	1118	S<1955>	8629.5	267.5
909	S<2164>	10928.5	359.5	979	S<2094>	10158.5	175.5	1049	S<2024>	9388.5	267.5	1119	S<1954>	8618.5	359.5
910	S<2163>	10917.5	175.5	980	S<2093>	10147.5	267.5	1050	S<2023>	9377.5	359.5	1120	S<1953>	8607.5	175.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
1121	S<1952>	8596.5	267.5	1191	S<1882>	7826.5	359.5	1261	S<1812>	7056.5	175.5	1331	S<1760>	6286.5	267.5
1122	S<1951>	8585.5	359.5	1192	S<1881>	7815.5	175.5	1262	S<1811>	7045.5	267.5	1332	S<1759>	6275.5	359.5
1123	S<1950>	8574.5	175.5	1193	S<1880>	7804.5	267.5	1263	S<1810>	7034.5	359.5	1333	S<1758>	6264.5	175.5
1124	S<1949>	8563.5	267.5	1194	S<1879>	7793.5	359.5	1264	S<1809>	7023.5	175.5	1334	S<1757>	6253.5	267.5
1125	S<1948>	8552.5	359.5	1195	S<1878>	7782.5	175.5	1265	S<1808>	7012.5	267.5	1335	S<1756>	6242.5	359.5
1126	S<1947>	8541.5	175.5	1196	S<1877>	7771.5	267.5	1266	S<1807>	7001.5	359.5	1336	S<1755>	6231.5	175.5
1127	S<1946>	8530.5	267.5	1197	S<1876>	7760.5	359.5	1267	S<1806>	6990.5	175.5	1337	S<1754>	6220.5	267.5
1128	S<1945>	8519.5	359.5	1198	S<1875>	7749.5	175.5	1268	S<1805>	6979.5	267.5	1338	S<1753>	6209.5	359.5
1129	S<1944>	8508.5	175.5	1199	S<1874>	7738.5	267.5	1269	S<1804>	6968.5	359.5	1339	S<1752>	6198.5	175.5
1130	S<1943>	8497.5	267.5	1200	S<1873>	7727.5	359.5	1270	S<1803>	6957.5	175.5	1340	S<1751>	6187.5	267.5
1131	S<1942>	8486.5	359.5	1201	S<1872>	7716.5	175.5	1271	S<1802>	6946.5	267.5	1341	S<1750>	6176.5	359.5
1132	S<1941>	8475.5	175.5	1202	S<1871>	7705.5	267.5	1272	S<1801>	6935.5	359.5	1342	S<1749>	6165.5	175.5
1133	S<1940>	8464.5	267.5	1203	S<1870>	7694.5	359.5	1273	DUMMY27	6924.5	175.5	1343	S<1748>	6154.5	267.5
1134	S<1939>	8453.5	359.5	1204	S<1869>	7683.5	175.5	1274	DUMMY28	6913.5	267.5	1344	S<1747>	6143.5	359.5
1135	S<1938>	8442.5	175.5	1205	S<1868>	7672.5	267.5	1275	DUMMY29	6902.5	359.5	1345	S<1746>	6132.5	175.5
1136	S<1937>	8431.5	267.5	1206	S<1867>	7661.5	359.5	1276	DUMMY30	6891.5	175.5	1346	S<1745>	6121.5	267.5
1137	S<1936>	8420.5	359.5	1207	S<1866>	7650.5	175.5	1277	DUMMY31	6880.5	267.5	1347	S<1744>	6110.5	359.5
1138	S<1935>	8409.5	175.5	1208	S<1865>	7639.5	267.5	1278	DUMMY32	6869.5	359.5	1348	S<1743>	6099.5	175.5
1139	S<1934>	8398.5	267.5	1209	S<1864>	7628.5	359.5	1279	DUMMY33	6858.5	175.5	1349	S<1742>	6088.5	267.5
1140	S<1933>	8387.5	359.5	1210	S<1863>	7617.5	175.5	1280	DUMMY34	6847.5	267.5	1350	S<1741>	6077.5	359.5
1141	S<1932>	8376.5	175.5	1211	S<1862>	7606.5	267.5	1281	DUMMY35	6836.5	359.5	1351	S<1740>	6066.5	175.5
1142	S<1931>	8365.5	267.5	1212	S<1861>	7595.5	359.5	1282	DUMMY36	6825.5	175.5	1352	S<1739>	6055.5	267.5
1143	S<1930>	8354.5	359.5	1213	S<1860>	7584.5	175.5	1283	DUMMY37	6814.5	267.5	1353	S<1738>	6044.5	359.5
1144	S<1929>	8343.5	175.5	1214	S<1859>	7573.5	267.5	1284	DUMMY38	6803.5	359.5	1354	S<1737>	6033.5	175.5
1145	S<1928>	8332.5	267.5	1215	S<1858>	7562.5	359.5	1285	DUMMY39	6792.5	175.5	1355	S<1736>	6022.5	267.5
1146	S<1927>	8321.5	359.5	1216	S<1857>	7551.5	175.5	1286	DUMMY40	6781.5	267.5	1356	S<1735>	6011.5	359.5
1147	S<1926>	8310.5	175.5	1217	S<1856>	7540.5	267.5	1287	DUMMY41	6770.5	359.5	1357	S<1734>	6000.5	175.5
1148	S<1925>	8299.5	267.5	1218	S<1855>	7529.5	359.5	1288	DUMMY42	6759.5	175.5	1358	S<1733>	5989.5	267.5
1149	S<1924>	8288.5	359.5	1219	S<1854>	7518.5	175.5	1289	DUMMY43	6748.5	267.5	1359	S<1732>	5978.5	359.5
1150	S<1923>	8277.5	175.5	1220	S<1853>	7507.5	267.5	1290	DUMMY44	6737.5	359.5	1360	S<1731>	5967.5	175.5
1151	S<1922>	8266.5	267.5	1221	S<1852>	7496.5	359.5	1291	S<1800>	6726.5	175.5	1361	S<1730>	5956.5	267.5
1152	S<1921>	8255.5	359.5	1222	S<1851>	7485.5	175.5	1292	S<1799>	6715.5	267.5	1362	S<1729>	5945.5	359.5
1153	S<1920>	8244.5	175.5	1223	S<1850>	7474.5	267.5	1293	S<1798>	6704.5	359.5	1363	S<1728>	5934.5	175.5
1154	S<1919>	8233.5	267.5	1224	S<1849>	7463.5	359.5	1294	S<1797>	6693.5	175.5	1364	S<1727>	5923.5	267.5
1155	S<1918>	8222.5	359.5	1225	S<1848>	7452.5	175.5	1295	S<1796>	6682.5	267.5	1365	S<1726>	5912.5	359.5
1156	S<1917>	8211.5	175.5	1226	S<1847>	7441.5	267.5	1296	S<1795>	6671.5	359.5	1366	S<1725>	5901.5	175.5
1157	S<1916>	8200.5	267.5	1227	S<1846>	7430.5	359.5	1297	S<1794>	6660.5	175.5	1367	S<1724>	5890.5	267.5
1158	S<1915>	8189.5	359.5	1228	S<1845>	7419.5	175.5	1298	S<1793>	6649.5	267.5	1368	S<1723>	5879.5	359.5
1159	S<1914>	8178.5	175.5	1229	S<1844>	7408.5	267.5	1299	S<1792>	6638.5	359.5	1369	S<1722>	5868.5	175.5
1160	S<1913>	8167.5	267.5	1230	S<1843>	7397.5	359.5	1300	S<1791>	6627.5	175.5	1370	S<1721>	5857.5	267.5
1161	S<1912>	8156.5	359.5	1231	S<1842>	7386.5	175.5	1301	S<1790>	6616.5	267.5	1371	S<1720>	5846.5	359.5
1162	S<1911>	8145.5	175.5	1232	S<1841>	7375.5	267.5	1302	S<1789>	6605.5	359.5	1372	S<1719>	5835.5	175.5
1163	S<1910>	8134.5	267.5	1233	S<1840>	7364.5	359.5	1303	S<1788>	6594.5	175.5	1373	S<1718>	5824.5	267.5
1164	S<1909>	8123.5	359.5	1234	S<1839>	7353.5	175.5	1304	S<1787>	6583.5	267.5	1374	S<1717>	5813.5	359.5
1165	S<1908>	8112.5	175.5	1235	S<1838>	7342.5	267.5	1305	S<1786>	6572.5	359.5	1375	S<1716>	5802.5	175.5
1166	S<1907>	8101.5	267.5	1236	S<1837>	7331.5	359.5	1306	S<1785>	6561.5	175.5	1376	S<1715>	5791.5	267.5
1167	S<1906>	8090.5	359.5	1237	S<1836>	7320.5	175.5	1307	S<1784>	6550.5	267.5	1377	S<1714>	5780.5	359.5
1168	S<1905>	8079.5	175.5	1238	S<1835>	7309.5	267.5	1308	S<1783>	6539.5	359.5	1378	S<1713>	5769.5	175.5
1169	S<1904>	8068.5	267.5	1239	S<1834>	7298.5	359.5	1309	S<1782>	6528.5	175.5	1379	S<1712>	5758.5	267.5
1170	S<1903>	8057.5	359.5	1240	S<1833>	7287.5	175.5	1310	S<1781>	6517.5	267.5	1380	S<1711>	5747.5	359.5
1171	S<1902>	8046.5	175.5	1241	S<1832>	7276.5	267.5	1311	S<1780>	6506.5	359.5	1381	S<1710>	5736.5	175.5
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1173	S<1900>	8024.5	359.5	1243	S<1830>	7254.5	175.5	1313	S<1778>	6484.5	267.5	1383	S<1708>	5714.5	359.5
1174	S<1899>	8013.5	175.5	1244	S<1829>	7243.5	267.5	1314	S<1777>	6473.5	359.5	1384	S<1707>	5703.5	175.5
1175	S<1898>	8002.5	267.5	1245	S<1828>	7232.5	359.5	1315	S<1776>	6462.5	175.5	1385	S<1706>	5692.5	267.5
1176	S<1897>	7991.5	359.5	1246	S<1827>	7221.5	175.5	1316	S<1775>	6451.5	267.5	1386	S<1705>	5681.5	359.5
1177	S<1896>	7980.5	175.5	1247	S<1826>	7210.5	267.5	1317	S<1774>	6440.5	359.5	1387	S<1704>	5670.5	175.5
1178	S<1895>	7969.5	267.5	1248	S<1825>	7199.5	359.5	1318	S<1773>	6429.5	175.5	1388	S<1703>	5659.5	267.5
1179	S<1894>	7958.5	359.5	1249	S<1824>	7188.5	175.5	1319	S<1772>	6418.5	267.5	1389	S<1702>	5648.5	359.5
1180	S<1893>	7947.5	175.5	1250	S<1823>	7177.5	267.5	1320	S<1771>	6407.5	359.5	1390	S<1701>	5637.5	175.5
1181	S<1892>	7936.5	267.5	1251	S<1822>	7166.5	359.5	1321	S<1770>	6396.5	175.5	1391	S<1700>	5626.5	267.5
1182	S<1891>	7925.5	359.5	1252	S<1821>	7155.5	175.5	1322	S<1769>	6385.5	267.5	1392	S<1699>	5615.5	359.5
1183	S<1890>	7914.5	175.5	1253	S<1820>	7144.5	267.5	1323	S<1768>	6374.5	359.5	1393	S<1698>	5604.5	175.5
1184	S<1889>	7903.5	267.5	1254	S<1819>	7133.5	359.5	1324	S<1767>	6363.5	175.5	1394	S<1697>	5593.5	267.5
1185	S<1888>	7892.5	359.5	1255	S<1818>	7122.5	175.5	1325	S<1766>	6352.5	267.5	1395	S<1696>	5582.5	359.5
1186	S<1887>	7881.5	175.5	1256	S<1817>	7111.5	267.5	1326	S<1765>	6341.5	359.5	1396	S<1695>	5571.5	175.5
1187	S<1886>	7870.5	267.5	1257	S<1816>	7100.5	359.5	1327	S<1764>	6330.5	175.5	1397	S<1694>	5560.5	267.5
1188	S<1885>	7859.5	359.5	1258	S<1815>	7089.5	175.5	1328	S<1763>	6319.5	267.5	1398	S<1693>	5549.5	359.5
1189	S<1884>	7848.5	175.5	1259	S<1814>	7078.5	267.5	1329	S<1762>	6308.5	359.5	1399	S<1692>	5538.5	175.5
1190	S<1883>	7837.5	267.5	1260	S<1813>	7067.5	359.5	1330	S<1761>	6297.5	175.5	1400	S<1691>	5527.5	267.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
1401	S<1690>	5516.5	359.5	1471	S<1620>	4746.5	175.5	1541	S<1550>	3976.5	267.5	1611	S<1480>	3206.5	359.5
1402	S<1689>	5505.5	175.5	1472	S<1619>	4735.5	267.5	1542	S<1549>	3965.5	359.5	1612	S<1479>	3195.5	175.5
1403	S<1688>	5494.5	267.5	1473	S<1618>	4724.5	359.5	1543	S<1548>	3954.5	175.5	1613	S<1478>	3184.5	267.5
1404	S<1687>	5483.5	359.5	1474	S<1617>	4713.5	175.5	1544	S<1547>	3943.5	267.5	1614	S<1477>	3173.5	359.5
1405	S<1686>	5472.5	175.5	1475	S<1616>	4702.5	267.5	1545	S<1546>	3932.5	359.5	1615	S<1476>	3162.5	175.5
1406	S<1685>	5461.5	267.5	1476	S<1615>	4691.5	359.5	1546	S<1545>	3921.5	175.5	1616	S<1475>	3151.5	267.5
1407	S<1684>	5450.5	359.5	1477	S<1614>	4680.5	175.5	1547	S<1544>	3910.5	267.5	1617	S<1474>	3140.5	359.5
1408	S<1683>	5439.5	175.5	1478	S<1613>	4669.5	267.5	1548	S<1543>	3899.5	359.5	1618	S<1473>	3129.5	175.5
1409	S<1682>	5428.5	267.5	1479	S<1612>	4658.5	359.5	1549	S<1542>	3888.5	175.5	1619	S<1472>	3118.5	267.5
1410	S<1681>	5417.5	359.5	1480	S<1611>	4647.5	175.5	1550	S<1541>	3877.5	267.5	1620	S<1471>	3107.5	359.5
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1416	S<1675>	5351.5	359.5	1486	S<1605>	4581.5	175.5	1556	S<1535>	3811.5	267.5	1626	S<1465>	3041.5	359.5
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1418	S<1673>	5329.5	267.5	1488	S<1603>	4559.5	359.5	1558	S<1533>	3789.5	175.5	1628	S<1463>	3019.5	267.5
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Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
1681	S<1410>	2436.5	175.5	1751	S<1340>	1666.5	267.5	1821	S<1270>	896.5	359.5	1891	DUMMY45	126.5	175.5
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1683	S<1408>	2414.5	359.5	1753	S<1338>	1644.5	175.5	1823	S<1268>	874.5	267.5	1893	DUMMY47	104.5	359.5
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1691	S<1400>	2326.5	267.5	1761	S<1330>	1556.5	359.5	1831	S<1260>	786.5	175.5	1901	DUMMY55	16.5	267.5
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1694	S<1397>	2293.5	267.5	1764	S<1327>	1523.5	359.5	1834	S<1257>	753.5	175.5	1904	DUMMY58	-16.5	267.5
1695	S<1396>	2282.5	359.5	1765	S<1326>	1512.5	175.5	1835	S<1256>	742.5	267.5	1905	DUMMY59	-27.5	359.5
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1711	S<1380>	2106.5	175.5	1781	S<1310>	1336.5	267.5	1851	S<1240>	566.5	359.5	1921	S<1194>	-203.5	175.5
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1718	S<1373>	2029.5	267.5	1788	S<1303>	1259.5	359.5	1858	S<1233>	489.5	175.5	1928	S<1187>	-280.5	267.5
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1730	S<1361>	1897.5	267.5	1800	S<1291>	1127.5	359.5	1870	S<1221>	357.5	175.5	1940	S<1175>	-412.5	267.5
1731	S<1360>	1886.5	359.5	1801	S<1290>	1116.5	175.5	1871	S<1220>	346.5	267.5	1941	S<1174>	-423.5	359.5
1732	S<1359>	1875.5	175.5	1802	S<1289>	1105.5	267.5	1872	S<1219>	335.5	359.5	1942	S<1173>	-434.5	175.5
1733	S<1358>	1864.5	267.5	1803	S<1288>	1094.5	359.5	1873	S<1218>	324.5	175.5	1943	S<1172>	-445.5	267.5
1734	S<1357>	1853.5	359.5	1804	S<1287>	1083.5	175.5	1874	S<1217>	313.5	267.5	1944	S<1171>	-456.5	359.5
1735	S<1356>	1842.5	175.5	1805	S<1286>	1072.5	267.5	1875	S<1216>	302.5	359.5	1945	S<1170>	-467.5	175.5
1736	S<1355>	1831.5	267.5	1806	S<1285>	1061.5	359.5	1876	S<1215>	291.5	175.5	1946	S<1169>	-478.5	267.5
1737	S<1354>	1820.5	359.5	1807	S<1284>	1050.5	175.5	1877	S<1214>	280.5	267.5	1947	S<1168>	-489.5	359.5
1738	S<1353>	1809.5	175.5	1808	S<1283>	1039.5	267.5	1878	S<1213>	269.5	359.5	1948	S<1167>	-500.5	175.5
1739	S<1352>	1798.5	267.5	1809	S<1282>	1028.5	359.5	1879	S<1212>	258.5	175.5	1949	S<1166>	-511.5	267.5
1740	S<1351>	1787.5	359.5	1810	S<1281>	1017.5	175.5	1880	S<1211>	247.5	267.5	1950	S<1165>	-522.5	359.5
1741	S<1350>	1776.5	175.5	1811	S<1280>	1006.5	267.5	1881	S<1210>	236.5	359.5	1951	S<1164>	-533.5	175.5
1742	S<1349>	1765.5	267.5	1812	S<1279>	995.5	359.5	1882	S<1209>	225.5	175.5	1952	S<1163>	-544.5	267.5
1743	S<1348>	1754.5	359.5	1813	S<1278>	984.5	175.5	1883	S<1208>	214.5	267.5	1953	S<1162>	-555.5	359.5
1744	S<1347>	1743.5	175.5	1814	S<1277>	973.5	267.5	1884	S<1207>	203.5	359.5	1954	S<1161>	-566.5	175.5
1745	S<1346>	1732.5	267.5	1815	S<1276>	962.5	359.5	1885	S<1206>	192.5	175.5	1955	S<1160>	-577.5	267.5
1746	S<1345>	1721.5	359.5	1816	S<1275>	951.5	175.5	1886	S<1205>	181.5	267.5	1956	S<1159>	-588.5	359.5
1747	S<1344>	1710.5	175.5	1817	S<1274>	940.5	267.5	1887	S<1204>	170.5	359.5	1957	S<1158>	-599.5	175.5
1748	S<1343>	1699.5	267.5	1818	S<1273>	929.5	359.5	1888	S<1203>	159.5	175.5	1958	S<1157>	-610.5	267.5
1749	S<1342>	1688.5	359.5	1819	S<1272>	918.5	175.5	1889	S<1202>	148.5	267.5	1959	S<1156>	-621.5	359.5
1750	S<1341>	1677.5	175.5	1820	S<1271>	907.5	267.5	1890	S<1201>	137.5	359.5	1960	S<1155>	-632.5	175.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
1961	S<1154>	-643.5	267.5	2031	S<1084>	-1413.5	359.5	2101	S<1014>	-2183.5	175.5	2171	S<944>	-2953.5	267.5
1962	S<1153>	-654.5	359.5	2032	S<1083>	-1424.5	175.5	2102	S<1013>	-2194.5	267.5	2172	S<943>	-2964.5	359.5
1963	S<1152>	-665.5	175.5	2033	S<1082>	-1435.5	267.5	2103	S<1012>	-2205.5	359.5	2173	S<942>	-2975.5	175.5
1964	S<1151>	-676.5	267.5	2034	S<1081>	-1446.5	359.5	2104	S<1011>	-2216.5	175.5	2174	S<941>	-2986.5	267.5
1965	S<1150>	-687.5	359.5	2035	S<1080>	-1457.5	175.5	2105	S<1010>	-2227.5	267.5	2175	S<940>	-2997.5	359.5
1966	S<1149>	-698.5	175.5	2036	S<1079>	-1468.5	267.5	2106	S<1009>	-2238.5	359.5	2176	S<939>	-3008.5	175.5
1967	S<1148>	-709.5	267.5	2037	S<1078>	-1479.5	359.5	2107	S<1008>	-2249.5	175.5	2177	S<938>	-3019.5	267.5
1968	S<1147>	-720.5	359.5	2038	S<1077>	-1490.5	175.5	2108	S<1007>	-2260.5	267.5	2178	S<937>	-3030.5	359.5
1969	S<1146>	-731.5	175.5	2039	S<1076>	-1501.5	267.5	2109	S<1006>	-2271.5	359.5	2179	S<936>	-3041.5	175.5
1970	S<1145>	-742.5	267.5	2040	S<1075>	-1512.5	359.5	2110	S<1005>	-2282.5	175.5	2180	S<935>	-3052.5	267.5
1971	S<1144>	-753.5	359.5	2041	S<1074>	-1523.5	175.5	2111	S<1004>	-2293.5	267.5	2181	S<934>	-3063.5	359.5
1972	S<1143>	-764.5	175.5	2042	S<1073>	-1534.5	267.5	2112	S<1003>	-2304.5	359.5	2182	S<933>	-3074.5	175.5
1973	S<1142>	-775.5	267.5	2043	S<1072>	-1545.5	359.5	2113	S<1002>	-2315.5	175.5	2183	S<932>	-3085.5	267.5
1974	S<1141>	-786.5	359.5	2044	S<1071>	-1556.5	175.5	2114	S<1001>	-2326.5	267.5	2184	S<931>	-3096.5	359.5
1975	S<1140>	-797.5	175.5	2045	S<1070>	-1567.5	267.5	2115	S<1000>	-2337.5	359.5	2185	S<930>	-3107.5	175.5
1976	S<1139>	-808.5	267.5	2046	S<1069>	-1578.5	359.5	2116	S<999>	-2348.5	175.5	2186	S<929>	-3118.5	267.5
1977	S<1138>	-819.5	359.5	2047	S<1068>	-1589.5	175.5	2117	S<998>	-2359.5	267.5	2187	S<928>	-3129.5	359.5
1978	S<1137>	-830.5	175.5	2048	S<1067>	-1600.5	267.5	2118	S<997>	-2370.5	359.5	2188	S<927>	-3140.5	175.5
1979	S<1136>	-841.5	267.5	2049	S<1066>	-1611.5	359.5	2119	S<996>	-2381.5	175.5	2189	S<926>	-3151.5	267.5
1980	S<1135>	-852.5	359.5	2050	S<1065>	-1622.5	175.5	2120	S<995>	-2392.5	267.5	2190	S<925>	-3162.5	359.5
1981	S<1134>	-863.5	175.5	2051	S<1064>	-1633.5	267.5	2121	S<994>	-2403.5	359.5	2191	S<924>	-3173.5	175.5
1982	S<1133>	-874.5	267.5	2052	S<1063>	-1644.5	359.5	2122	S<993>	-2414.5	175.5	2192	S<923>	-3184.5	267.5
1983	S<1132>	-885.5	359.5	2053	S<1062>	-1655.5	175.5	2123	S<992>	-2425.5	267.5	2193	S<922>	-3195.5	359.5
1984	S<1131>	-896.5	175.5	2054	S<1061>	-1666.5	267.5	2124	S<991>	-2436.5	359.5	2194	S<921>	-3206.5	175.5
1985	S<1130>	-907.5	267.5	2055	S<1060>	-1677.5	359.5	2125	S<990>	-2447.5	175.5	2195	S<920>	-3217.5	267.5
1986	S<1129>	-918.5	359.5	2056	S<1059>	-1688.5	175.5	2126	S<989>	-2458.5	267.5	2196	S<919>	-3228.5	359.5
1987	S<1128>	-929.5	175.5	2057	S<1058>	-1699.5	267.5	2127	S<988>	-2469.5	359.5	2197	S<918>	-3239.5	175.5
1988	S<1127>	-940.5	267.5	2058	S<1057>	-1710.5	359.5	2128	S<987>	-2480.5	175.5	2198	S<917>	-3250.5	267.5
1989	S<1126>	-951.5	359.5	2059	S<1056>	-1721.5	175.5	2129	S<986>	-2491.5	267.5	2199	S<916>	-3261.5	359.5
1990	S<1125>	-962.5	175.5	2060	S<1055>	-1732.5	267.5	2130	S<985>	-2502.5	359.5	2200	S<915>	-3272.5	175.5
1991	S<1124>	-973.5	267.5	2061	S<1054>	-1743.5	359.5	2131	S<984>	-2513.5	175.5	2201	S<914>	-3283.5	267.5
1992	S<1123>	-984.5	359.5	2062	S<1053>	-1754.5	175.5	2132	S<983>	-2524.5	267.5	2202	S<913>	-3294.5	359.5
1993	S<1122>	-995.5	175.5	2063	S<1052>	-1765.5	267.5	2133	S<982>	-2535.5	359.5	2203	S<912>	-3305.5	175.5
1994	S<1121>	-1006.5	267.5	2064	S<1051>	-1776.5	359.5	2134	S<981>	-2546.5	175.5	2204	S<911>	-3316.5	267.5
1995	S<1120>	-1017.5	359.5	2065	S<1050>	-1787.5	175.5	2135	S<980>	-2557.5	267.5	2205	S<910>	-3327.5	359.5
1996	S<1119>	-1028.5	175.5	2066	S<1049>	-1798.5	267.5	2136	S<979>	-2568.5	359.5	2206	S<909>	-3338.5	175.5
1997	S<1118>	-1039.5	267.5	2067	S<1048>	-1809.5	359.5	2137	S<978>	-2579.5	175.5	2207	S<908>	-3349.5	267.5
1998	S<1117>	-1050.5	359.5	2068	S<1047>	-1820.5	175.5	2138	S<977>	-2590.5	267.5	2208	S<907>	-3360.5	359.5
1999	S<1116>	-1061.5	175.5	2069	S<1046>	-1831.5	267.5	2139	S<976>	-2601.5	359.5	2209	S<906>	-3371.5	175.5
2000	S<1115>	-1072.5	267.5	2070	S<1045>	-1842.5	359.5	2140	S<975>	-2612.5	175.5	2210	S<905>	-3382.5	267.5
2001	S<1114>	-1083.5	359.5	2071	S<1044>	-1853.5	175.5	2141	S<974>	-2623.5	267.5	2211	S<904>	-3393.5	359.5
2002	S<1113>	-1094.5	175.5	2072	S<1043>	-1864.5	267.5	2142	S<973>	-2634.5	359.5	2212	S<903>	-3404.5	175.5
2003	S<1112>	-1105.5	267.5	2073	S<1042>	-1875.5	359.5	2143	S<972>	-2645.5	175.5	2213	S<902>	-3415.5	267.5
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2006	S<1109>	-1138.5	267.5	2076	S<1039>	-1908.5	359.5	2146	S<969>	-2678.5	175.5	2216	S<899>	-3448.5	267.5
2007	S<1108>	-1149.5	359.5	2077	S<1038>	-1919.5	175.5	2147	S<968>	-2689.5	267.5	2217	S<898>	-3459.5	359.5
2008	S<1107>	-1160.5	175.5	2078	S<1037>	-1930.5	267.5	2148	S<967>	-2700.5	359.5	2218	S<897>	-3470.5	175.5
2009	S<1106>	-1171.5	267.5	2079	S<1036>	-1941.5	359.5	2149	S<966>	-2711.5	175.5	2219	S<896>	-3481.5	267.5
2010	S<1105>	-1182.5	359.5	2080	S<1035>	-1952.5	175.5	2150	S<965>	-2722.5	267.5	2220	S<895>	-3492.5	359.5
2011	S<1104>	-1193.5	175.5	2081	S<1034>	-1963.5	267.5	2151	S<964>	-2733.5	359.5	2221	S<894>	-3503.5	175.5
2012	S<1103>	-1204.5	267.5	2082	S<1033>	-1974.5	359.5	2152	S<963>	-2744.5	175.5	2222	S<893>	-3514.5	267.5
2013	S<1102>	-1215.5	359.5	2083	S<1032>	-1985.5	175.5	2153	S<962>	-2755.5	267.5	2223	S<892>	-3525.5	359.5
2014	S<1101>	-1226.5	175.5	2084	S<1031>	-1996.5	267.5	2154	S<961>	-2766.5	359.5	2224	S<891>	-3536.5	175.5
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2016	S<1099>	-1248.5	359.5	2086	S<1029>	-2018.5	175.5	2156	S<959>	-2788.5	267.5	2226	S<889>	-3558.5	359.5
2017	S<1098>	-1259.5	175.5	2087	S<1028>	-2029.5	267.5	2157	S<958>	-2799.5	359.5	2227	S<888>	-3569.5	175.5
2018	S<1097>	-1270.5	267.5	2088	S<1027>	-2040.5	359.5	2158	S<957>	-2810.5	175.5	2228	S<887>	-3580.5	267.5
2019	S<1096>	-1281.5	359.5	2089	S<1026>	-2051.5	175.5	2159	S<956>	-2821.5	267.5	2229	S<886>	-3591.5	359.5
2020	S<1095>	-1292.5	175.5	2090	S<1025>	-2062.5	267.5	2160	S<955>	-2832.5	359.5	2230	S<885>	-3602.5	175.5
2021	S<1094>	-1303.5	267.5	2091	S<1024>	-2073.5	359.5	2161	S<954>	-2843.5	175.5	2231	S<884>	-3613.5	267.5
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2023	S<1092>	-1325.5	175.5	2093	S<1022>	-2095.5	267.5	2163	S<952>	-2865.5	359.5	2233	S<882>	-3635.5	175.5
2024	S<1091>	-1336.5	267.5	2094	S<1021>	-2106.5	359.5	2164	S<951>	-2876.5	175.5	2234	S<881>	-3646.5	267.5
2025	S<1090>	-1347.5	359.5	2095	S<1020>	-2117.5	175.5	2165	S<950>	-2887.5	267.5	2235	S<880>	-3657.5	359.5
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2027	S<1088>	-1369.5	267.5	2097	S<1018>	-2139.5	359.5	2167	S<948>	-2909.5	175.5	2237	S<878>	-3679.5	267.5
2028	S<1087>	-1380.5	359.5	2098	S<1017>	-2150.5	175.5	2168	S<947>	-2920.5	267.5	2238	S<877>	-3690.5	359.5
2029	S<1086>	-1391.5	175.5	2099	S<1016>	-2161.5	267.5	2169	S<946>	-2931.5	359.5	2239	S<876>	-3701.5	175.5
2030	S<1085>	-1402.5	267.5	2100	S<1015>	-2172.5	359.5	2170	S<945>	-2942.5	175.5	2240	S<875>	-3712.5	267.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
2241	S<874>	-3723.5	359.5	2311	S<804>	-4493.5	175.5	2381	S<734>	-5263.5	267.5	2451	S<664>	-6033.5	359.5
2242	S<873>	-3734.5	175.5	2312	S<803>	-4504.5	267.5	2382	S<733>	-5274.5	359.5	2452	S<663>	-6044.5	175.5
2243	S<872>	-3745.5	267.5	2313	S<802>	-4515.5	359.5	2383	S<732>	-5285.5	175.5	2453	S<662>	-6055.5	267.5
2244	S<871>	-3756.5	359.5	2314	S<801>	-4526.5	175.5	2384	S<731>	-5296.5	267.5	2454	S<661>	-6066.5	359.5
2245	S<870>	-3767.5	175.5	2315	S<800>	-4537.5	267.5	2385	S<730>	-5307.5	359.5	2455	S<660>	-6077.5	175.5
2246	S<869>	-3778.5	267.5	2316	S<799>	-4548.5	359.5	2386	S<729>	-5318.5	175.5	2456	S<659>	-6088.5	267.5
2247	S<868>	-3789.5	359.5	2317	S<798>	-4559.5	175.5	2387	S<728>	-5329.5	267.5	2457	S<658>	-6099.5	359.5
2248	S<867>	-3800.5	175.5	2318	S<797>	-4570.5	267.5	2388	S<727>	-5340.5	359.5	2458	S<657>	-6110.5	175.5
2249	S<866>	-3811.5	267.5	2319	S<796>	-4581.5	359.5	2389	S<726>	-5351.5	175.5	2459	S<656>	-6121.5	267.5
2250	S<865>	-3822.5	359.5	2320	S<795>	-4592.5	175.5	2390	S<725>	-5362.5	267.5	2460	S<655>	-6132.5	359.5
2251	S<864>	-3833.5	175.5	2321	S<794>	-4603.5	267.5	2391	S<724>	-5373.5	359.5	2461	S<654>	-6143.5	175.5
2252	S<863>	-3844.5	267.5	2322	S<793>	-4614.5	359.5	2392	S<723>	-5384.5	175.5	2462	S<653>	-6154.5	267.5
2253	S<862>	-3855.5	359.5	2323	S<792>	-4625.5	175.5	2393	S<722>	-5395.5	267.5	2463	S<652>	-6165.5	359.5
2254	S<861>	-3866.5	175.5	2324	S<791>	-4636.5	267.5	2394	S<721>	-5406.5	359.5	2464	S<651>	-6176.5	175.5
2255	S<860>	-3877.5	267.5	2325	S<790>	-4647.5	359.5	2395	S<720>	-5417.5	175.5	2465	S<650>	-6187.5	267.5
2256	S<859>	-3888.5	359.5	2326	S<789>	-4658.5	175.5	2396	S<719>	-5428.5	267.5	2466	S<649>	-6198.5	359.5
2257	S<858>	-3899.5	175.5	2327	S<788>	-4669.5	267.5	2397	S<718>	-5439.5	359.5	2467	S<648>	-6209.5	175.5
2258	S<857>	-3910.5	267.5	2328	S<787>	-4680.5	359.5	2398	S<717>	-5450.5	175.5	2468	S<647>	-6220.5	267.5
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2309	S<806>	-4471.5	267.5	2379	S<736>	-5241.5	359.5	2449	S<666>	-6011.5	175.5	2519	DUMMY73	-6781.5	267.5
2310	S<805>	-4482.5	359.5	2380	S<735>	-5252.5	175.5	2450	S<665>	-6022.5	267.5	2520	DUMMY74	-6792.5	359.5

Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
2521	DUMMY75	-6803.5	175.5	2591	S<542>	-7573.5	267.5	2661	S<472>	-8343.5	359.5	2731	S<402>	-9113.5	175.5
2522	DUMMY76	-6814.5	267.5	2592	S<541>	-7584.5	359.5	2662	S<471>	-8354.5	175.5	2732	S<401>	-9124.5	267.5
2523	DUMMY77	-6825.5	359.5	2593	S<540>	-7595.5	175.5	2663	S<470>	-8365.5	267.5	2733	S<400>	-9135.5	359.5
2524	DUMMY78	-6836.5	175.5	2594	S<539>	-7606.5	267.5	2664	S<469>	-8376.5	359.5	2734	S<399>	-9146.5	175.5
2525	DUMMY79	-6847.5	267.5	2595	S<538>	-7617.5	359.5	2665	S<468>	-8387.5	175.5	2735	S<398>	-9157.5	267.5
2526	DUMMY80	-6858.5	359.5	2596	S<537>	-7628.5	175.5	2666	S<467>	-8398.5	267.5	2736	S<397>	-9168.5	359.5
2527	DUMMY81	-6869.5	175.5	2597	S<536>	-7639.5	267.5	2667	S<466>	-8409.5	359.5	2737	S<396>	-9179.5	175.5
2528	DUMMY82	-6880.5	267.5	2598	S<535>	-7650.5	359.5	2668	S<465>	-8420.5	175.5	2738	S<395>	-9190.5	267.5
2529	DUMMY83	-6891.5	359.5	2599	S<534>	-7661.5	175.5	2669	S<464>	-8431.5	267.5	2739	S<394>	-9201.5	359.5
2530	DUMMY84	-6902.5	175.5	2600	S<533>	-7672.5	267.5	2670	S<463>	-8442.5	359.5	2740	S<393>	-9212.5	175.5
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2801	S<332>	-9883.5	267.5	2871	S<262>	-10653.5	359.5	2941	S<192>	-11423.5	175.5	3011	S<122>	-12193.5	267.5
2802	S<331>	-9894.5	359.5	2872	S<261>	-10664.5	175.5	2942	S<191>	-11434.5	267.5	3012	S<121>	-12204.5	359.5
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Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis	Number	Name	X-axis	Y-axis
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3086	S<47>	-13018.5	267.5	3156	DUMMY	-13898.5	175.5								
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3088	S<45>	-13040.5	175.5	3158	DUMMY	-13920.5	359.5								
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3141	DUMMY94	-13623.5	359.5												
3142	Unput Label	-13706	281												
3143	Unput Label	-13706	368												
3144	DUMMY	-13766.5	175.5												
3145	DUMMY	-13777.5	267.5												
3146	DUMMY	-13788.5	359.5												
3147	DUMMY	-13799.5	175.5												
3148	DUMMY	-13810.5	267.5												
3149	DUMMY	-13821.5	359.5												
3150	DUMMY	-13832.5	175.5												

5. Interface

5.1. MIPI Interface

The selection of a given interfaces are done by setting LANSEL, IM2, IM1 ,IM0 pins and Page0_AE_bit0 as show in **Table 2**

Table 2: DSI Interface Lane Mode Selection

External Pad Set				Register	Configuration of MIPI Lane				
LANSEL	IM2	IM1	IM0	Page0_RAEh MIPI_LANE_SEL	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	0	1	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	1	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	1	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
0	1	0	0	1	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	1	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
0	1	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
1	0	0	0	1	-	-	CLKP/N	D1P/N	D0P/N
1	0	0	1	1	-	-	CLKN/P	D1N/P	D0N/P
1	0	1	0	1	D0P/N	D1P/N	CLKP/N	-	-
1	0	1	1	1	D0N/P	D1N/P	CLKN/P	-	-
1	1	0	0	1	-	D0P/N	CLKP/N	D1P/N	-
1	1	0	1	1	-	D0N/P	CLKN/P	D1N/P	-
1	1	1	0	1	-	D1P/N	CLKP/N	D0P/N	-
1	1	1	1	1	-	D1N/P	CLKN/P	D0N/P	-
0	0	0	0	0	-	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	0	-	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	0	D0P/N	D1P/N	CLKP/N	D2P/N	-
0	0	1	1	0	D0N/P	D1N/P	CLKN/P	D2N/P	-
0	1	0	0	0	-	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	0	-	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	0	D2P/N	D1P/N	CLKP/N	D0P/N	-
0	1	1	1	0	D2N/P	D1N/P	CLKN/P	D0N/P	-
Others					Reserved				

5.1.1.General Description

The MIPI DSI is enabled or disabled by external IM[2:0] and LANSEL pin.

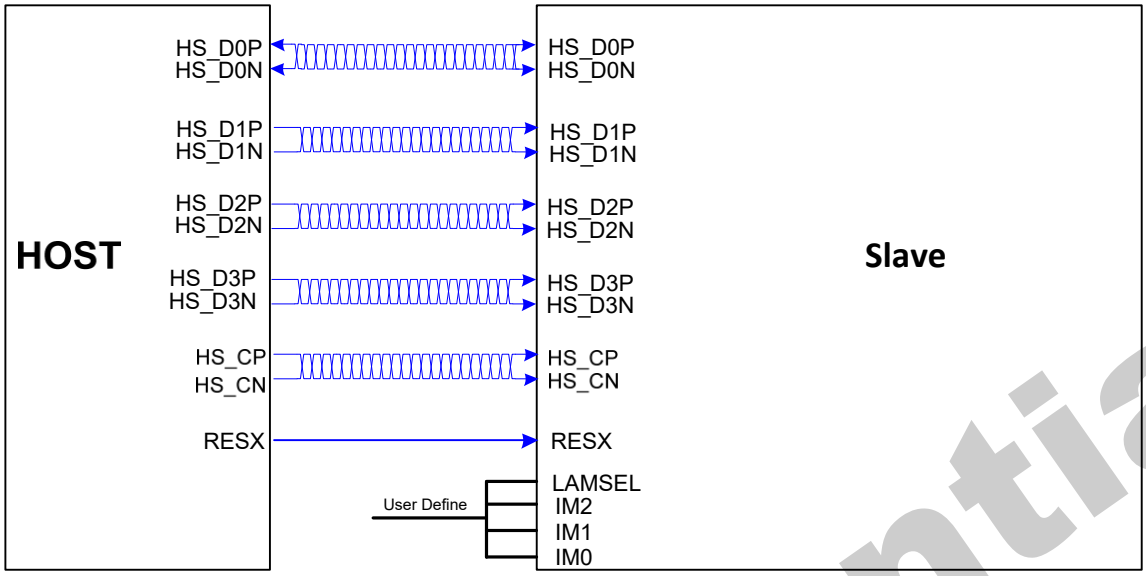


Figure 13 DSI system interface diagram

5.1.2.Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 10 High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage		High Speed	Low Power	
	DATA_P	DATA_N	Burst Mode	Control	Escape
HS-0	Low	High	Differential – 0	Note 1	Note 1
HS-1	High	Low	Differential – 1	Note 1	Note 1
LP-00	Low	Low	Not Defined	Bridge	Space
LP-01	Low	High	Not Defined	HS – Request	Mark - 0
LP-10	High	Low	Not Defined	LP - Request	Mark - 1
LP-11	High	High	Not Defined	Stop	Note 2

Note 1 *Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.*

Note 2 *If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.*

Note 3 *n = 0 and 1 (D1+/- lanes only for HS-0 and HS-1)*

5.1.3.DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

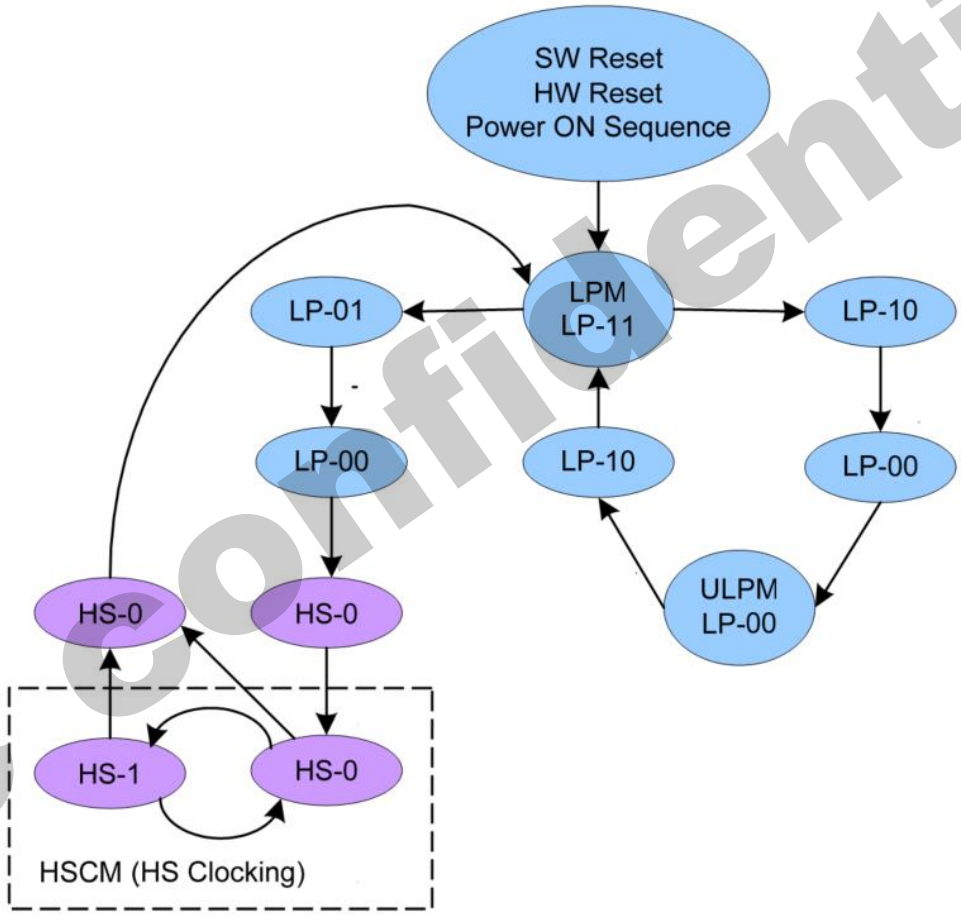


Figure 14 Clock Lanes Power Modes

5.1.4.Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset, HW Reset or Power On Sequence =>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

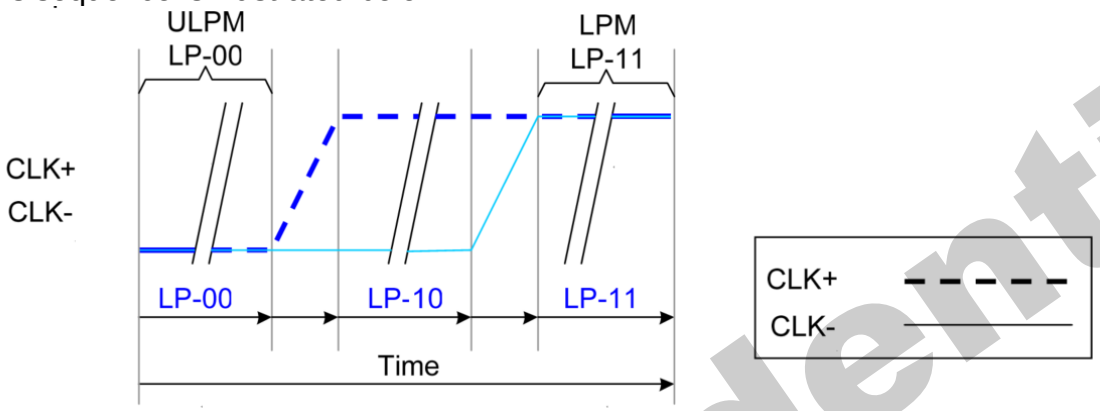


Figure 15 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

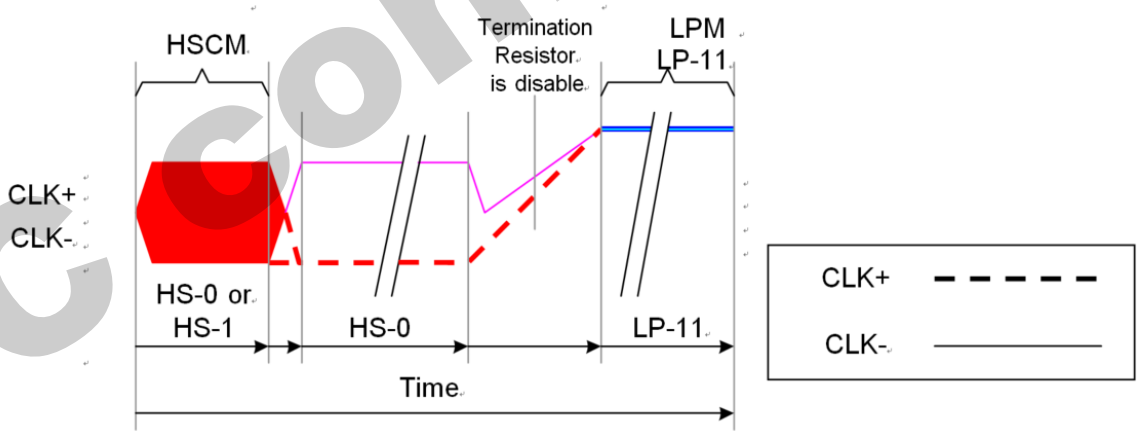


Figure 16 From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below

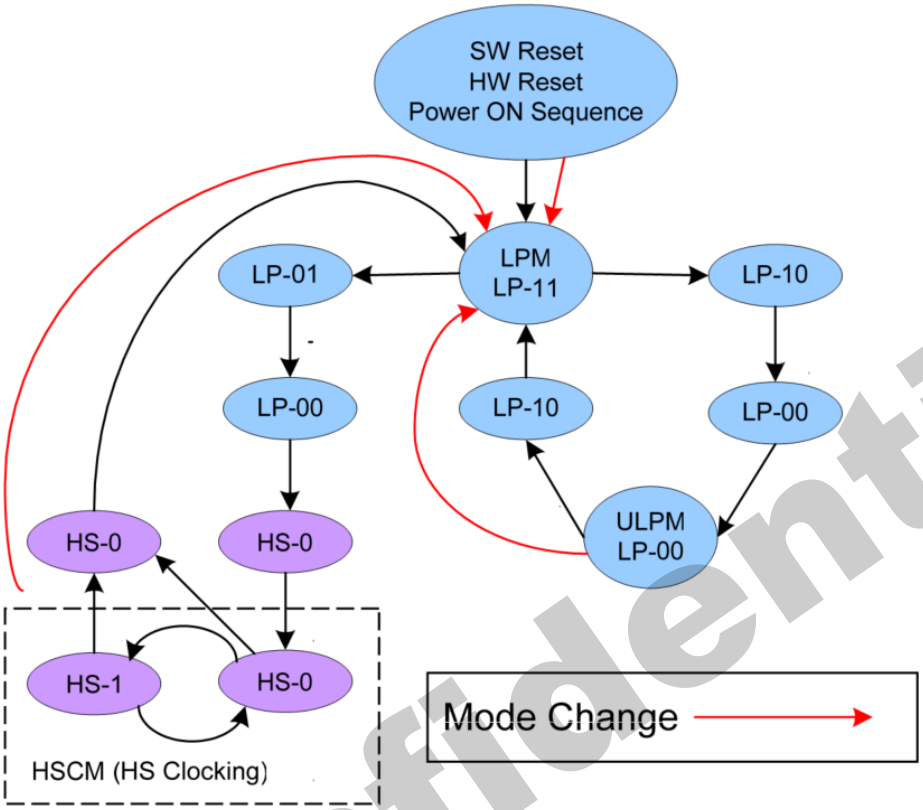


Figure 17 All Three Mode Changes to LPM on the Flow Chart

5.1.5.Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM).

This sequence is illustrated below.

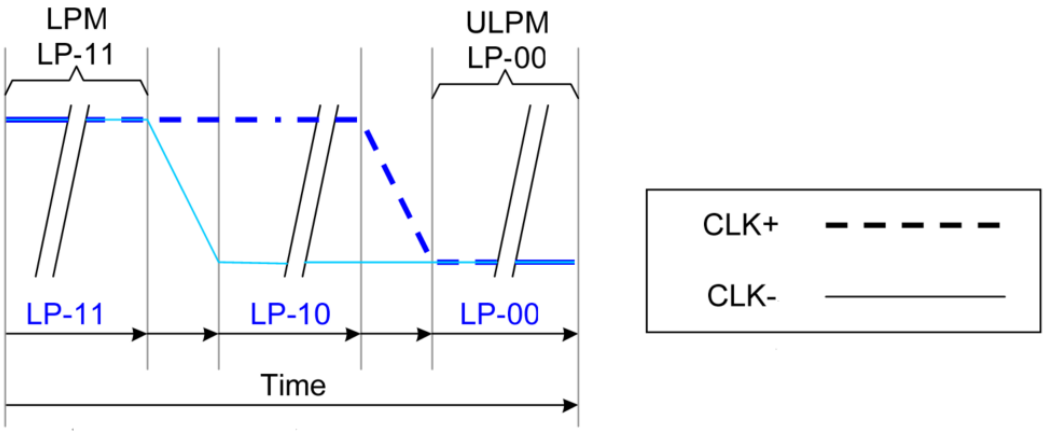


Figure 18 From LPM to ULPM

The mode change is also illustrated below.

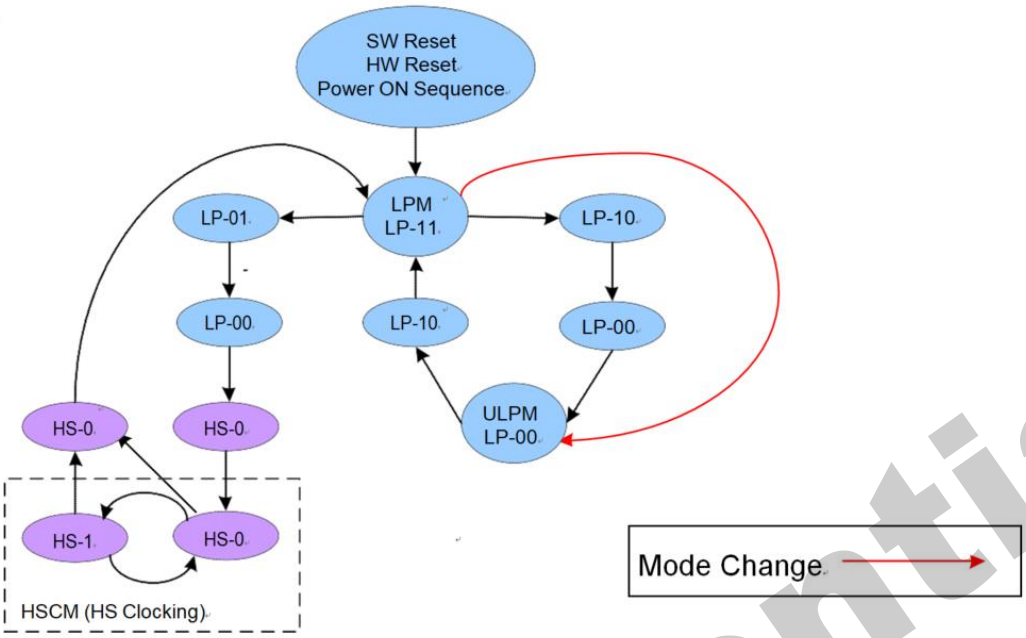


Figure 19 Mode Change from LPM to ULPM on the Flow Chart

5.1.6.High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

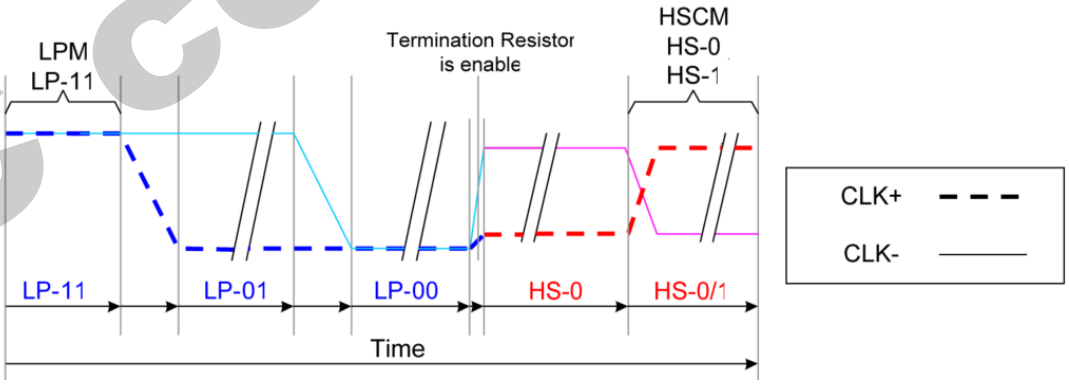


Figure 20 From LPM to HSCM

The mode change is also illustrated below.

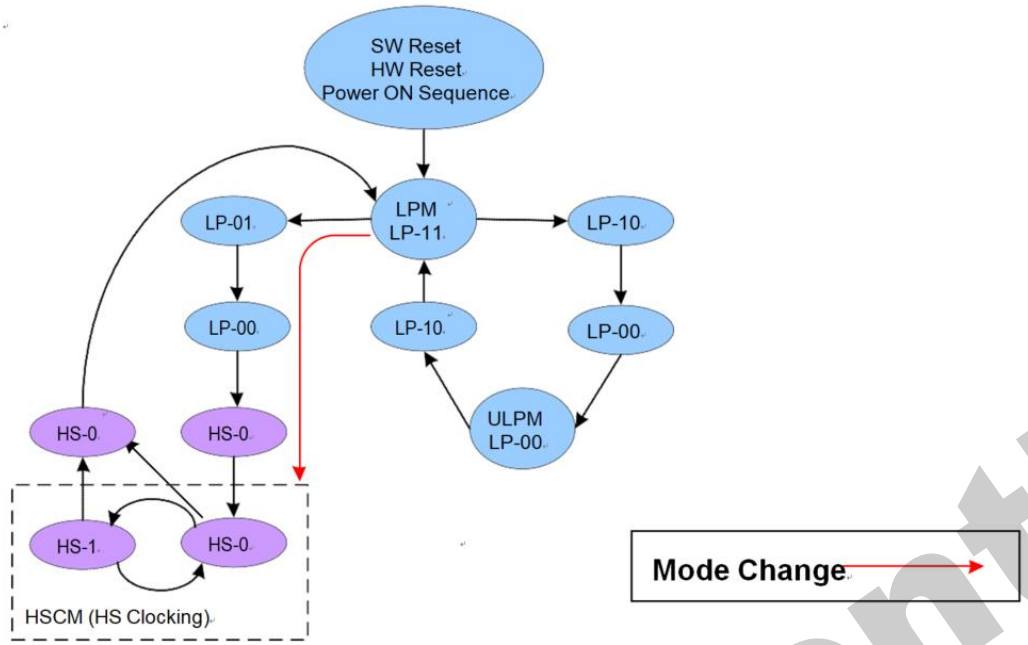


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

Even number of transitions

Start state is HS-0

End state is HS-0

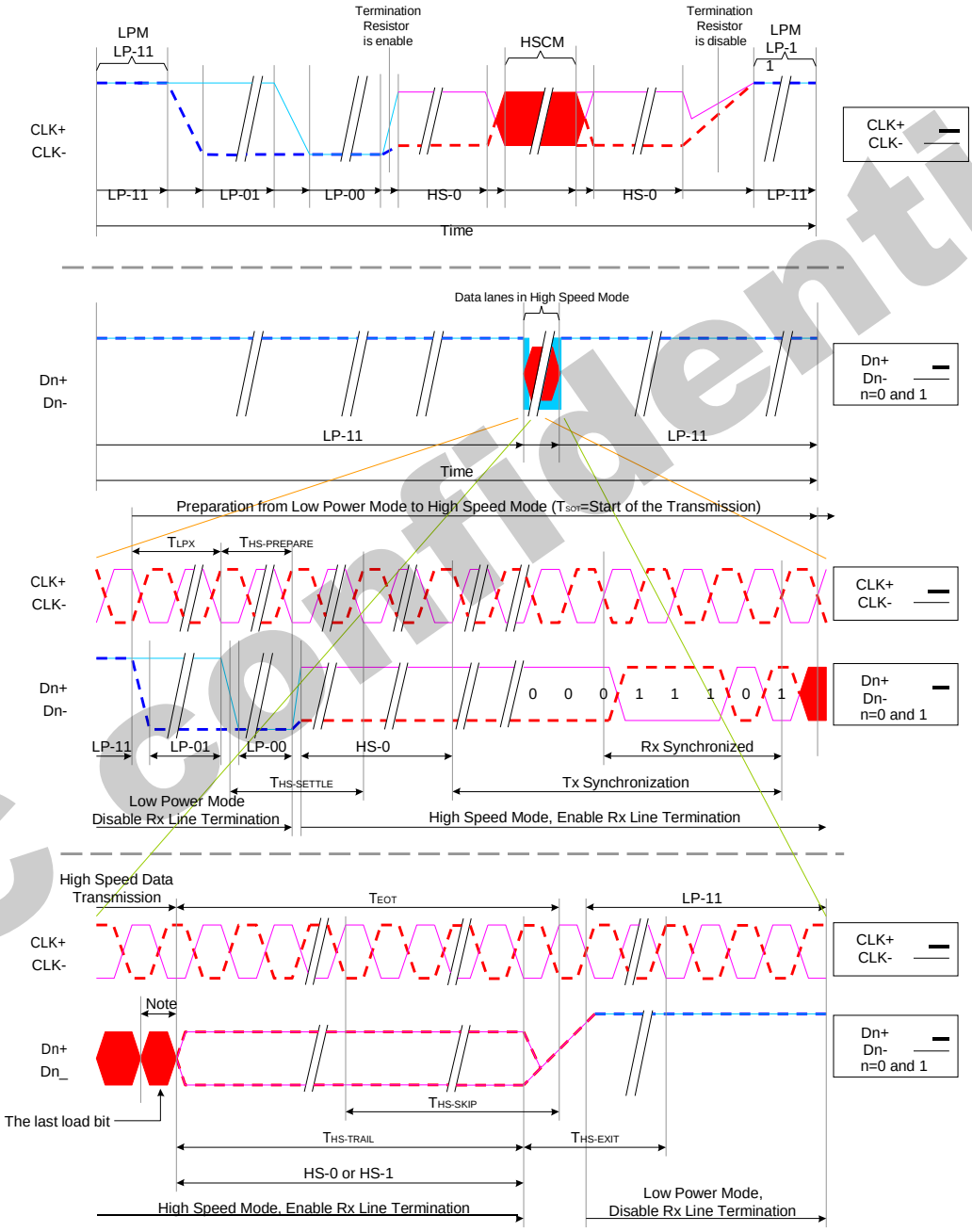


Figure 22 High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.1.7.DSI-D1 and DSI-D0 Data Lanes

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven in different modes which are:

Escape Mode (Only DSI-D0+/- data lanes are used)

High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 11 Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 -+ LP-10 -+ LP-00 -+ LP-01 -+ LP-00	LP-00 -+ LP-10 -+ LP-11
High-Speed Data	LP-11 -+ LP-01 -+ LP-00 -+ HS-0	(HS-0 or HS-1) -+ LP-11
Bus Turnaround Request	LP-11 -+ LP-10 -+ LP-00 -+ LP-10 -+ LP-00	Hi-Z

Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. More information on chapter "Bus Turnaround ".

5.1.8. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

Send “Low-Power Data Transmission” (LPDT) e.g. from the MPU to the display module,

Drive data lanes to “Ultra-Low Power State” (ULPS),

Indicate “Remote Application Reset” (RAR), which is resetting the display module,

Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follow

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

A load if it is needed

Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

End: LP-11

This basic construction is illustrated below:

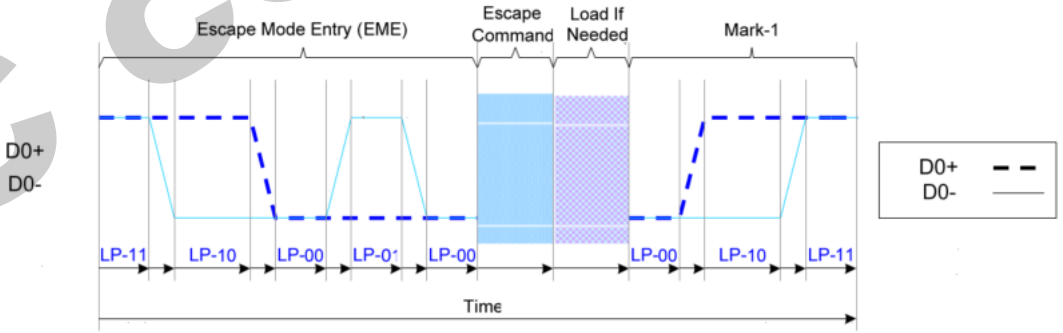


Figure 23 General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, see Table 12: Escape Commands.

An example of a Mode type Escape Command is ‘Ultra-Low Power Mode’ where the MPU instructs the display module to enter it’s Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 12 Escape Commands[Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit -+ Last Bit Transmitted)	Dn	
Low-Power Data	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, [Note 1]	Mo	1001 1111 b	-	-
Undefined-2, [Note 1]	Mo	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, [Note 1]	Trigger	1010 0000 b	-	-

Note 1. This Escape command support has not been implemented on the display module.
n = 1
x = Supported
- = Not Supported

5.1.9.Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MPU.

The Low Power Data Transmission (LPDT) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

Load (Data):

One or more bytes (8 bit)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

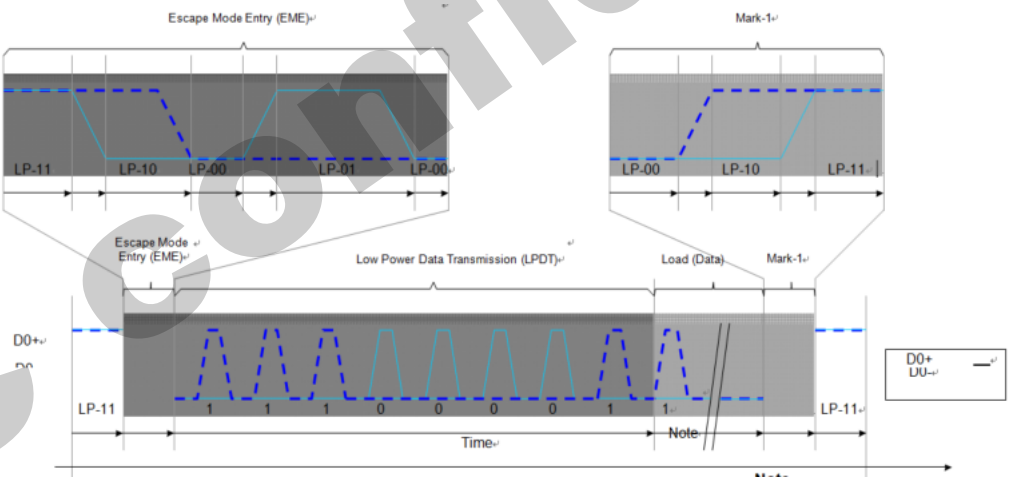


Figure 24 Low-Power Data Transmission (LPDT)[Note]

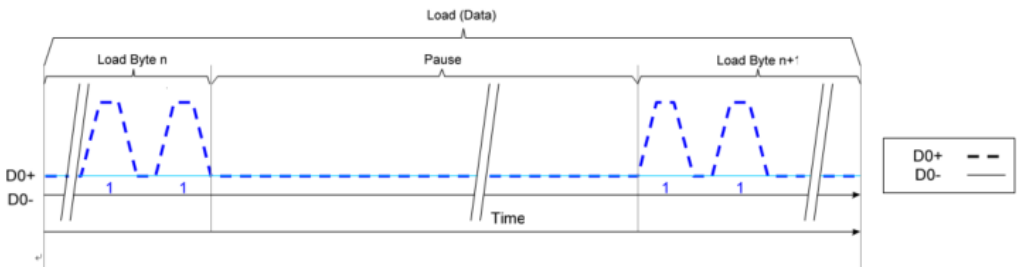


Figure 25 Pause (Example)

Note Load (Data) is presenting that the first bit is logical '1' in this example.

5.1.10. Ultra-Low Power State (ULPS)

The MPU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

Ultra-Low Power State (ULPS) when the MPU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

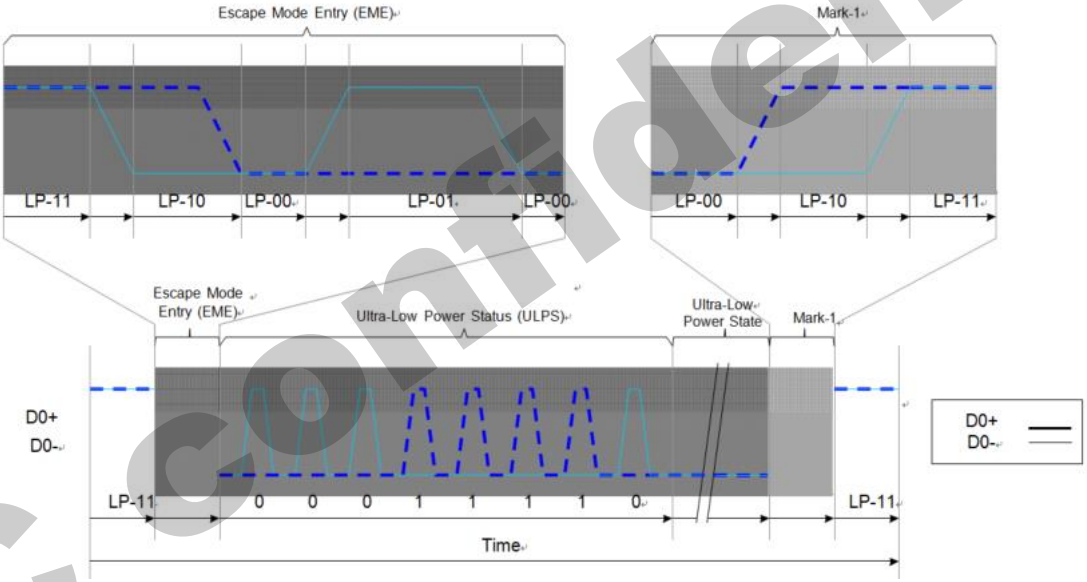


Figure 26 Ultra-Low Power State (ULPS)

5.1.11. Acknowledge (ACK)

The display module can inform to the MPU when an error has not recognized on it by Acknowledge (ACK). The display module is sending the Acknowledge (ACK) what is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

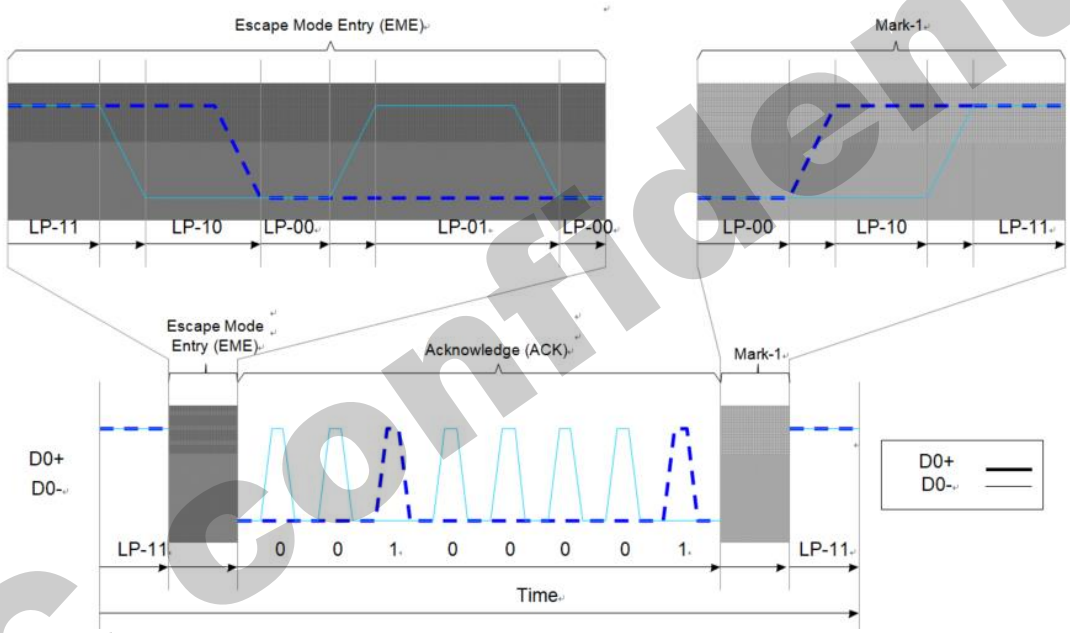


Figure 28 Acknowledge (ACK)

5.1.12. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MPU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

Start: LP-11

HS-Request: LP-01

HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)

End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

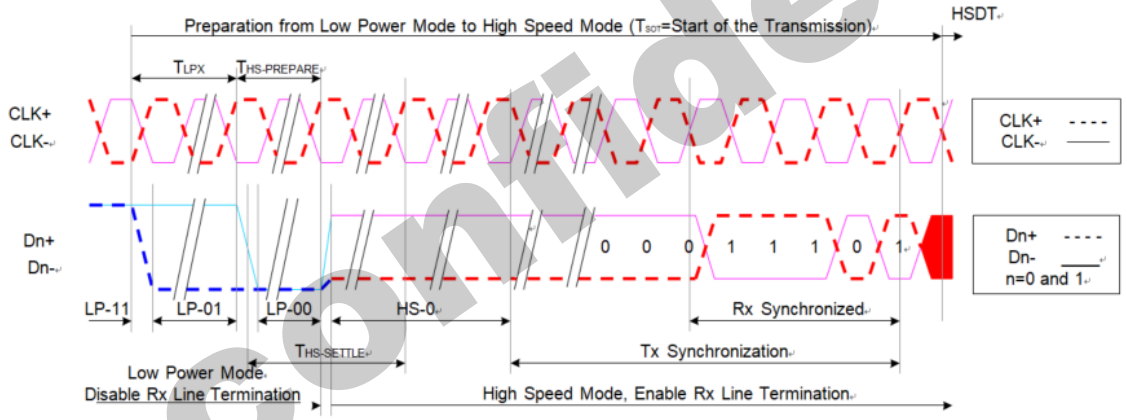


Figure 29 Entering High-Speed Data Transmission (T_{SOT} of HSDT)

5.1.13. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MPU and this HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

Start: High-Speed Data Transmission (HSDT)

Stops High-Speed Data Transmission

MPU changes to HS-1, if the last load bit is HS-0 MPU changes to HS-0, if the last load bit is HS-1

End: LP-11 (Rx: Lane Termination Disable)

his same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

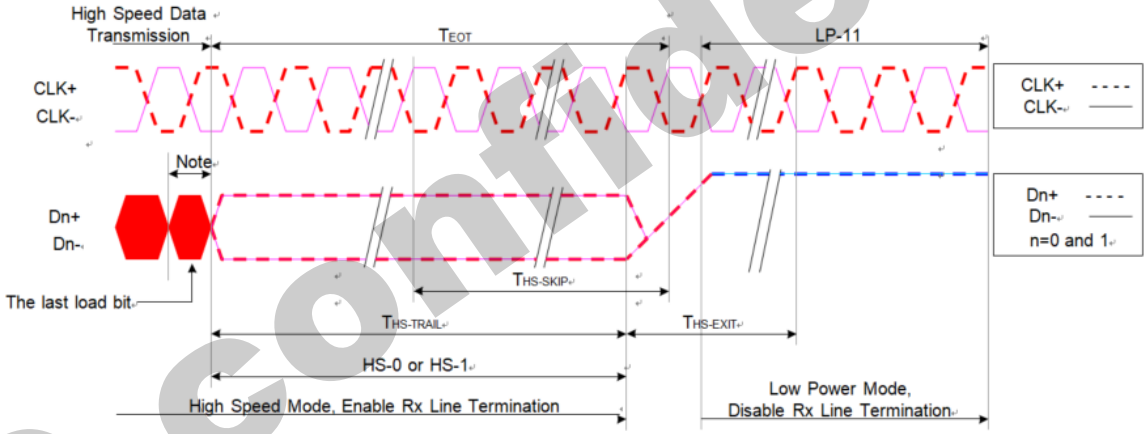


Figure 30 Leaving High-Speed Data Transmission (T_{EOT} of HSDT)[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.1.14. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

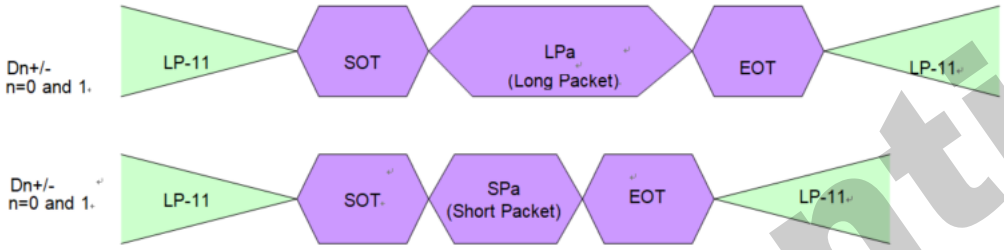


Figure 31 Single Packet in Low-Speed Data Transmissio

The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:

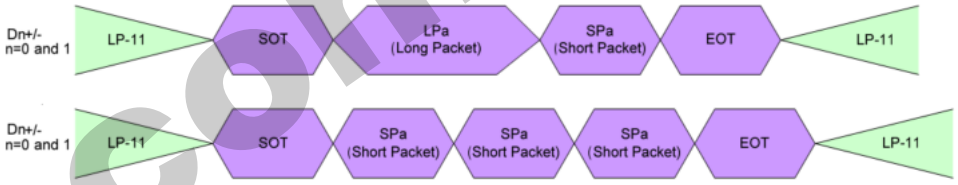


Figure 32 Multiple Packets in High-Speed Data Transmission – Examples

Table 13 Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

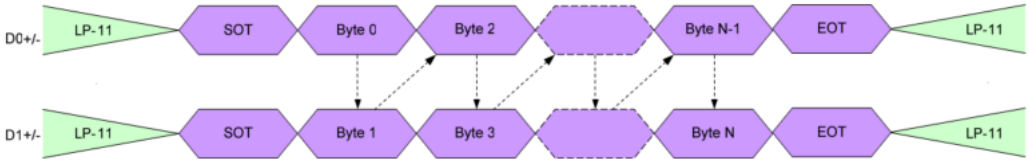


Figure 33 Single Packet in HSDT – Even Number of Bytes

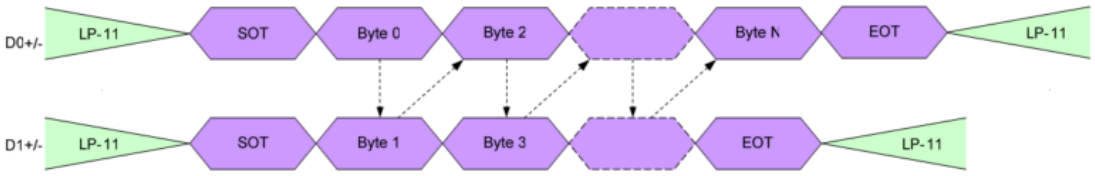


Figure 34 Single Packet in HSDT – Odd Number of Byte

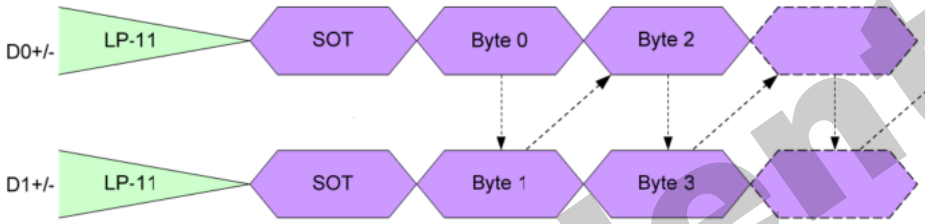


Figure 35 Start of Transmission (SoT) in HSDT for Multiple Packets

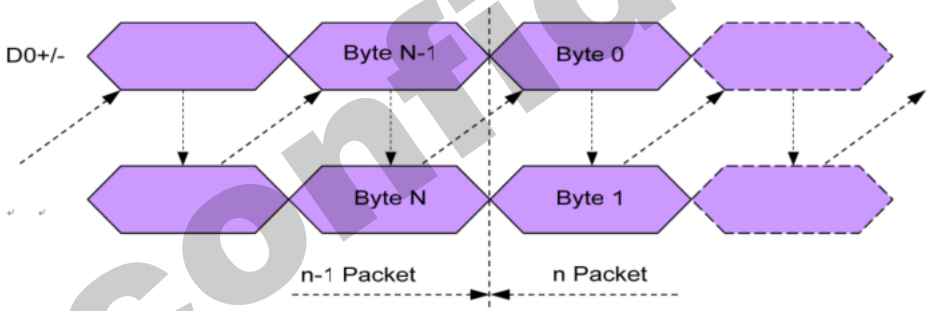


Figure 36 Continue Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

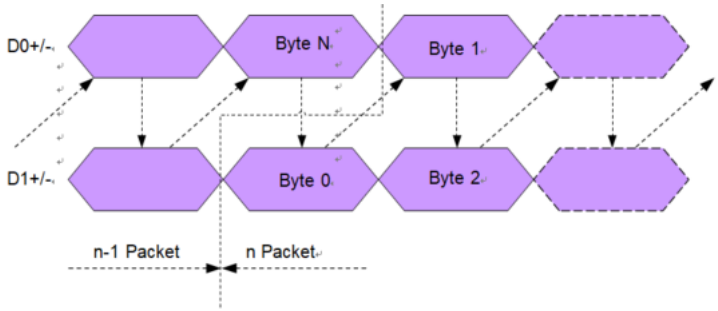


Figure 37 Continue Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

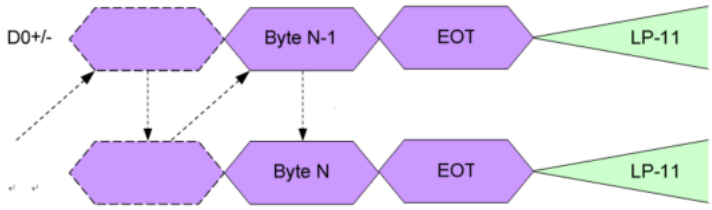


Figure 38 End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

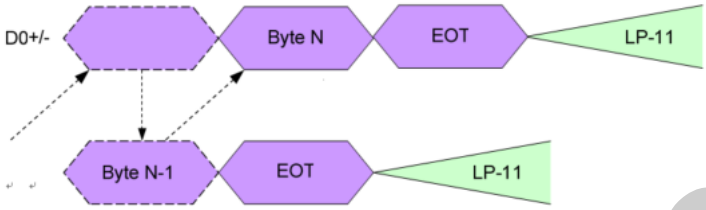


Figure 39 End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at cthe End of the Packet

5.1.15. Bus Turnaround (BTA)

The MPU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MPU or display module.

The MPU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MPU wants to do the bus turnaround procedure to the display module, as follows.

Start (MPU): LP-11

Turnaround Request (MPU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00

The MPU waits until the display module is starting to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)

The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MPU to the display module) is illustrated below

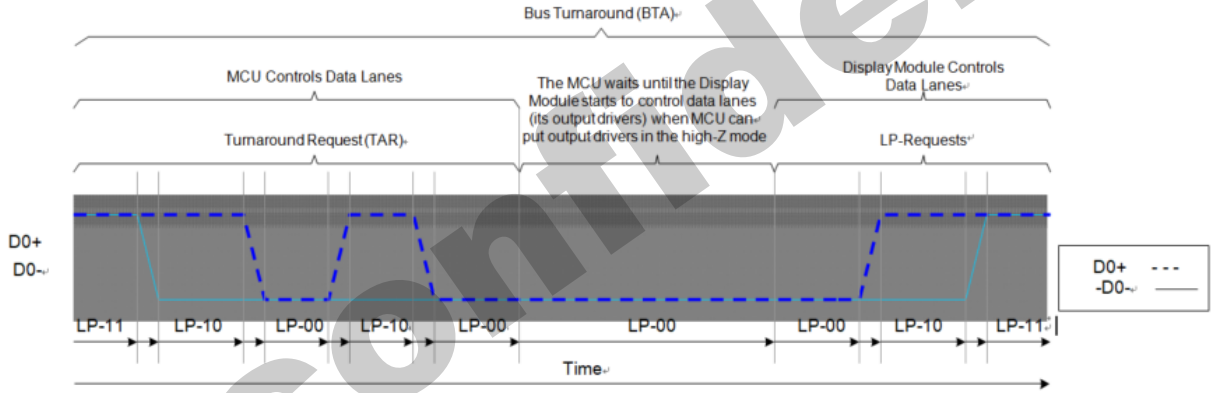


Figure 40 Bus Turnaround Procedure

MPU and display module terms are switched on the Figure 40, if the Bus Turnaround (BTA) is from the display module to the MPU.

6. Command

6.1. User Command Set

Table 6.1.1 User Command Set

R/W	Address	Parameter								Function
	MIPI	D7	D6	D5	D4	D3	D2	D1	D0	
R	04h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
		ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
R	0Ah	Booster	idle		sleep_out	normal_on	disp_on			Read Display Power Mode
R	0Bh				gs	bgr	ss			Read Display MADCTR
R	0Dh			inv_on	pixel_on	pixel_off		gamma_curve_sel[1:0]		Read Display Image Mode
R	0Eh	TE_ON	TE_MODE							Read TE Mode
W	10h	No Argument								Sleep in & booster off
W	11h	No Argument								Sleep out & booster on
W	13h	No Argument								Normal display mode on
W	20h	No Argument								INVOFF
W	21h	No Argument								INVON
W	22h	No Argument								ALLPOFF
W	23h	No Argument								ALLPON
W	28h	No Argument								Display off
W	29h	No Argument								Display on
W	34h	No Argument								TE OFF
W	35h								M	TE ON
W	36h					BGR		SS	GS	MADCTR
\W	38h	No Argument								Idle mode off
W	39h	No Argument								Idle mode on
W	44h						SCANLINE[10:8]			SETSCANLINE
		SCANLINE[7:0]								
R	45h						SCANLINE[10:8]			GETSCANLINE
		SCANLINE[7:0]								
W	51h					DBV[11:8]				Write display brightness
		DBV[7:0]								
R	52h					DBV[11:8]				Read display brightness
		DBV[7:0]								
W	53h			BCTL		DIM EN	BL			Write Control Display
R	54h			BCTL		DIM EN	BL			Read Control Display
R	DAh	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
R	DBh	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
R	DCh	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3
W	D7h	0X61								Manufacture command enable
		0X74								
		0X97								
W	D0h	0	0	0	MAUNC	0	0	PAGE[1:0]		Page set

Read Display ID (04h)

User Command Set		04h : RDNUMED (Read Display ID)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Read	ID1[7:0]								00h
2st Parameter	Read	ID2[7:0]								97h
3st Parameter	Read	ID3[7:0]								03h
Description	This read byte returns 24-bit display identification information. (the module's manufacture ID). And it is equal to returns value of DAh,DBh,DCh command.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009703
S/W Reset	24'h009703
H/W Reset	24'h009703

Read Display Power Mode (0Ah)

User Command Set		0Ah : RDDPM (Read Display Power Mode)								
	Write /	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	Booster	idle	0	sleep_out	normal_on	disp_on	0	0	8'h08

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault.
		1	Booster On and working well
D6	IDEL MODE	0	IDEL MODE ON
		1	IDEL MODE OFF
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off.
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off.
		1	Display is On

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h08
H/W Reset	8'h08

Read Display MADCTL (0Bh)

User Command Set		0Bh : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	0	GS	BGR	0	SS	8'h00

Description

This command indicates the current status of the display as described in the table below.

Description	Value	Status
BGR	0	RGB
	1	BGR
GS	0	Gate output Top to Bottom
	1	Gate output Bottom to Top
SS	0	Source output Left to Right
	1	Source output Right to Left

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Read Display Image Mode (0Dh)

User Command Set		0Dh : RDDPM (Read Display Image Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	0	1	0Dh
1st Parameter	Read	0	0	INVO	allpon	allpoff	0	0	0	8'h00

Description

This command indicates the current display image mode as described in the table below.

Bit	Description	Value	Status
D5	Inversion On/Off	0	Inversion is Off.
		1	Inversion is On.
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Read TE Mode (0Eh)

User Command Set		0Eh : Read TE Mode								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	1	0	0Eh
1st Parameter	Read	TE_ON	TE_MODE	0	0	0	0	0	0	8'h00
Description	This command indicates the TE status of the display as described in the table below.									
Restriction										
Register Availability										
Default										

Bit	Description	Value	Status
D7	TE_ON	0	TE hiz
		1	TE output
D6	TE_Mode	0	Te mode on
		1	Te mode off

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00

Sleep In (10h)

User Command Set		10h : Sleep In								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	xx								XXh
Description	This command causes the GC9703C to enter the minimum power consumption mode.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep outmode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Sleep Out (11h)

User Command Set		11h : Sleep Out								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	xx								XXh
Description	This command causes the GC9703C to enter the Sleep Out mode									
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The GC9703C loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the GC9703C is already Sleep Out mode.									
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep out mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Normal Display Mode On (13h)

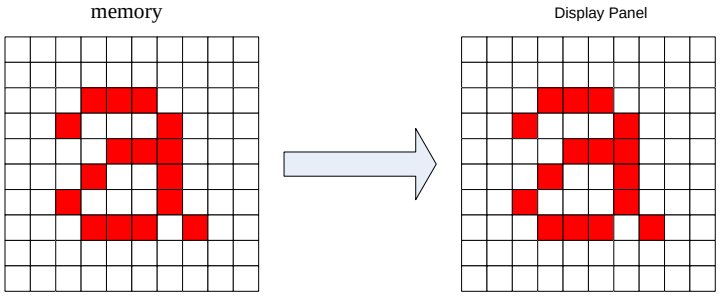
User Command Set		13h :CLOMD(Normal Display Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	1	1	13h
1st Parameter	Read	xx								XXh
Description	This command returns the display to Normal Display									
Restriction	This command has no effect when Normal Display Mode is active.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

Display Inversion OFF (20h)

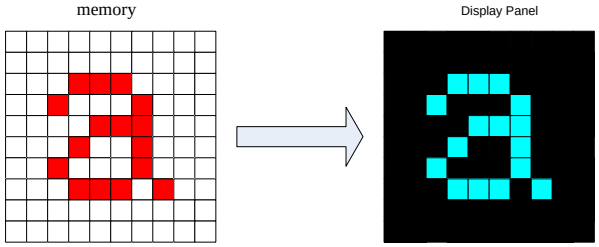
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h
1st Parameter	-	xx								XXh
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. 									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Display inversion off
H/W Reset	Display inversion off

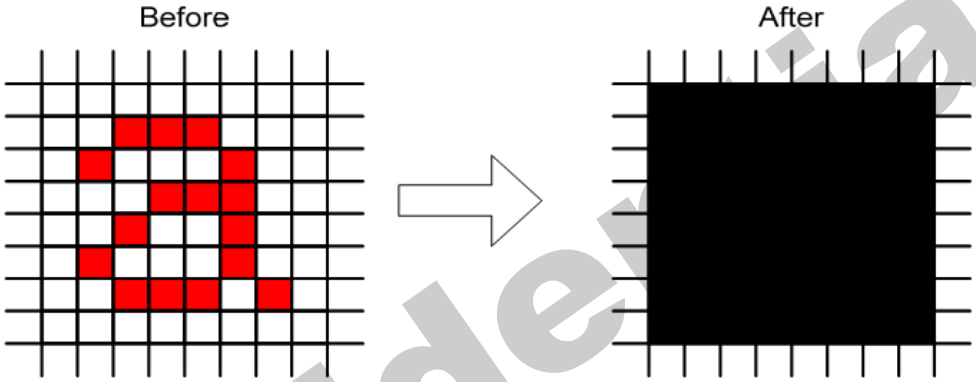
Display Inversion ON (21h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h
1st Parameter	-	xx								XXh
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.. 									
Restriction										
Register Availability										
Default										

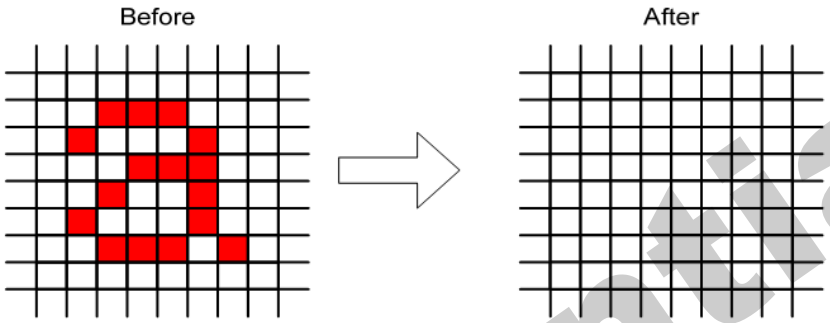
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Display inversion off
H/W Reset	Display inversion off

All Pixel Off (22h)

User Command Set		22h : CLOMD(all pixel Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	-	xx								XXh
Description	This command turns the display panel black in 'Sleep Out' mode and a status of the' Display On/Off' register can be 'on' or 'off'. This command does not change any other status 'All Pixels On', 'Normal Display Mode On' commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

All Pixel On (23h)

User Command Set		23h : CLOMD(all pixel On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	Read	xx								XXh
Description	This command turns the display panel white in 'Sleep Out ' mode and a status of the 'Display On/Off' register can be 'on' or'off'. This command does not change any other status. 'All Pixels Off', 'Normal Display Mode On'– commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

Display Off (28h)

User Command Set		28h : CLOMD(Display Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28h
1st Parameter	-	XX								XXh
Description	This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted. This command makes no change any other status.									
Restriction	This command has no effect when module is already in Display Off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

Display ON (29h)

User Command Set		29h : CLOMD(Display On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	1	29h
1st Parameter	-	XX								XXh
Description	This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status.									
Restriction	This command has no effect when IC is already in Display on mode.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

TE Off (34h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	-	XX								XXh
Description	This command is used to turn off (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already off.									
Register Availability										

Status	Availability
Power On Sequence	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	TE off
H/W Reset	TE off

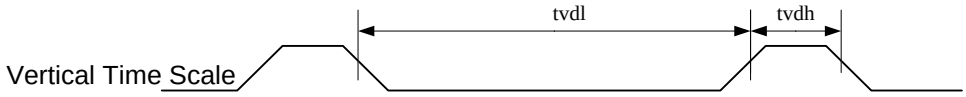
TE on(35h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h
1st Parameter	-								M	XXh

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already on.

Register Availability

Status	Availability
Power On Sequence	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	TE off
H/W Reset	TE off

MADCTR (36h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	1	0	36h
1st Parameter	Write					BGR		SS	GS	00

Description

This command defines read/write scanning direction of frame memory.

GS	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
SS	Horizontal Refresh Order	LCD horizontal refreshing direction control.

Restriction

This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 16.7M colors.
X = Don't care.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Idle Mode Off (38h)

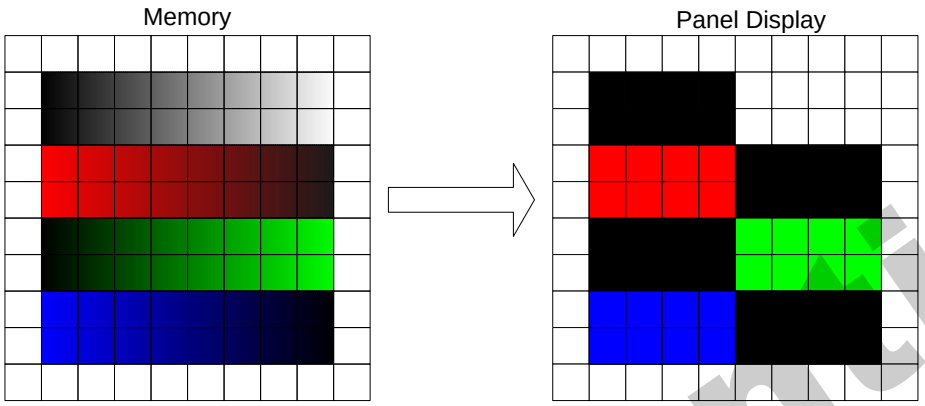
User Command Set		38h : CLOMD(Idle Mode Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	0	0	38h
1st Parameter	-	xx								xxh
Description	This command returns the display to Normal Display									
Restriction	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors. X = Don't care.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Idle Mode On (39h)

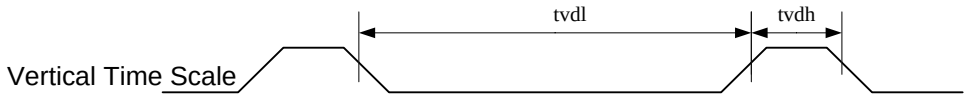
User Command Set		39h : CLOMD(Idle Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	0	1	39h
1st Parameter	Write	xx								xxh
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Scan Line (44h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	0	44h
1st Parameter	Write						SCANLINE[10:8]			00h
2nd Parameter	Write	SCANLINE[7:0]								00h
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of SCANLINE [10:0]  eg: when the SCANLINE [10:0]=1,the TE will output at the position of Gate1. when the SCANLINE [10:0]=2,the TE will output at the position of Gate2. when the SCANLINE [10:0]=3,the TE will output at the position of Gate3. …									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	11'h000
Sleep Out	11'h000
Sleep In	11'h000

Default

Status	Default Value
Power On Sequence	11'h000
S/W Reset	11'h000
H/W Reset	11'h000

Write Display Brightness Value (51h)

	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write					DBV[11:8]				00h
2nd Parameter	Write	DBV[7:0]								00h
Description	The command is used to adjust the brightness value of the display. DBV[11:0]: 12 bit, for display brightness of manual brightness setting. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.									
Restriction										
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read Display Brightness Value (52h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	1	0	1	0	52h
1st Parameter	Read					DBV[11:8]				00h
2nd Parameter	Read	DBV[7:0]								00h
Description	The command is used to read the brightness value of the display. DBV[11:0]: 12 bit, for display brightness of manual brightness setting in the 51h.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Write CTL Display(53h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write	0	0	BCTRL	0	Dim en	BL	0	0	00h

Description

This command is used to control brightness.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to Dim en bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)
1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

BL: Backlight Control On/Off without Dimming Effect
When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (Dim en="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": output low (for high active) LEDONPOL="1": output high (for low active)
1	on	LEDONPOL="0": output high (for high active) LEDONPOL="1": output low (for low active)

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at Dim en ="1"。

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read CTL Display(54h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Read	0	0	BCTRL	0	Dim en	BL	0	0	00
Description	This command returns brightness control.									
Restriction										
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Read ID1 (DAh)

User Command Set		DAh : RDDPM (Read ID1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								8h'00
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 1rst parameter of 04h command. The ID1 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0h'00
S/W Reset	0h'00
H/W Reset	0h'00

Read ID2 (DBh)

User Command Set		DBh : RDDPM (Read ID2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								8'h97
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 2th parameter of 04h command. The ID2 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0'h97
S/W Reset	0'h97
H/W Reset	0'h97

Read ID3 (DCh)

User Command Set		DCh : RDDPM (Read ID3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	1	0	0	DCh
1st Parameter	Read	ID3[7:0]								8'h03
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 3th parameter of 04h command. The ID3 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h03
S/W Reset	8'h03
H/W Reset	8'h03

EXTC Command Set enable register (D7h)

	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	0	1	1	1	D7h
1st Parameter	Write	0	1	1	0	0	0	0	1	61h
2st Parameter	Write	0	1	1	1	0	1	0	0	74h
3st Parameter	Write	1	0	0	1	0	1	1	1	97h

Description

‘D7h” is used to enable page select of page register.Three parameters must be wriitern continusly.

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24h’ 000000
S/W Reset	24h’ 000000
H/W Reset	24h’ 000000

Page Sel (D0h)

User Command Set		D0h : Page Select								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	0	0	0	0	D0h
1st Parameter	Write	0	0	0	MAUC	0	0	PAGE[1:0]		00h

Description

Bit	Description	Value
MAUC	Manufacture Command Set enable/disable	"0": Manufacture Command Set disable "1": Manufacture Command Set enable
PAGE[1:0]	Manufacture Command Set selection	00:page0 01:page1 10:page2 11:page3

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8h' 00
S/W Reset	8h' 00
H/W Reset	8h' 00

6.2 Page 0 Command Set

Table 6.1.2 Page 0 Command Set

R/W	Address	Parameter								Function
	MIPI	D7	D6	D5	D4	D3	D2	D1	D0	
W	61h			Vcom_fix_en						VCOM_CTL_EN
W	69h		Lanesel_en							LANSEL_EN
W	AEh	0	1	1	1	0	0	0	D2D_LANSEL	INTER_LANSEL
W	FDh	D2D_VCOM_RES_FIX[7:0]								VCOM_CTL

VCOM_CTL(FDh)

Page0 Command Set										
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default(Hex)
Command	Write	1	1	1	1	1	1	0	1	FDh
1st Parameter	Write	D2D_VCOM_RES_FIX<7:0>								8'h7f

Description

D2D_VCOM_RES_FIX<7:0> is the adjustment register of VCOM in normal-temperature environment.

D2D_VCOM_RES_FIX<7:0>HEX	VCOM(V)
0	0
…	STEP -0.025
C	-0.3
D	-0.315
…	STEP -0.015
16	-0.45
17	-0.46
..	STEP -0.01
7F	-1.5
…	STEP -0.01
9D	-1.8
9E	-1.815
…	STEP -0.015
D0	-2.565
D1	-2.58
…	STEP -0.02
FF	-3.5

Restriction

To enable this command, "Page 0 Command Set enable register (D0h) " must set first.
Andenable register (61h)" b5" must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h7f
S/W Reset	8'h7f
H/W Reset	8'h7f

INTER_LANESEL(AEh)

Page0 Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	1	1	1	0	AEh
1st Parameter	Write	0	1	1	1	0	0	0	D2D_LANSEL	8'h70

Description

D2D_LANSEL with IC PAD LANSEL IM[2:0] configure MIPI Lane SWAP

Table 2: DSI Interface Lane Mode Selection

External Pad Set				Register	Configuration of MIPI Lane				
LANSEL	IM2	IM1	IM0	Page0_RAEh MIPI_LANE_SEL	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	0	1	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	1	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	1	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
0	1	0	0	1	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	1	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
0	1	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
1	0	0	0	1	-	-	CLKP/N	D1P/N	D0P/N
1	0	0	1	1	-	-	CLKN/P	D1N/P	D0N/P
1	0	1	0	1	D0P/N	D1P/N	CLKP/N	-	-
1	0	1	1	1	D0N/P	D1N/P	CLKN/P	-	-
1	1	0	0	1	-	D0P/N	CLKP/N	D1P/N	-
1	1	0	1	1	-	D0N/P	CLKN/P	D1N/P	-
1	1	1	0	1	-	D1P/N	CLKP/N	D0P/N	-
1	1	1	1	1	-	D1N/P	CLKN/P	D0N/P	-
0	0	0	0	0	-	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	0	-	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	0	D0P/N	D1P/N	CLKP/N	D2P/N	-
0	0	1	1	0	D0N/P	D1N/P	CLKN/P	D2N/P	-
0	1	0	0	0	-	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	0	-	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	0	D2P/N	D1P/N	CLKP/N	D0P/N	-
0	1	1	1	0	D2N/P	D1N/P	CLKN/P	D0N/P	-
Others					Reserved				

Restriction

To enable this command, "Page 0 Command Set enable register (D0h) " must set first.
Andenable register (69h)" b6" must set 1

Register Availability

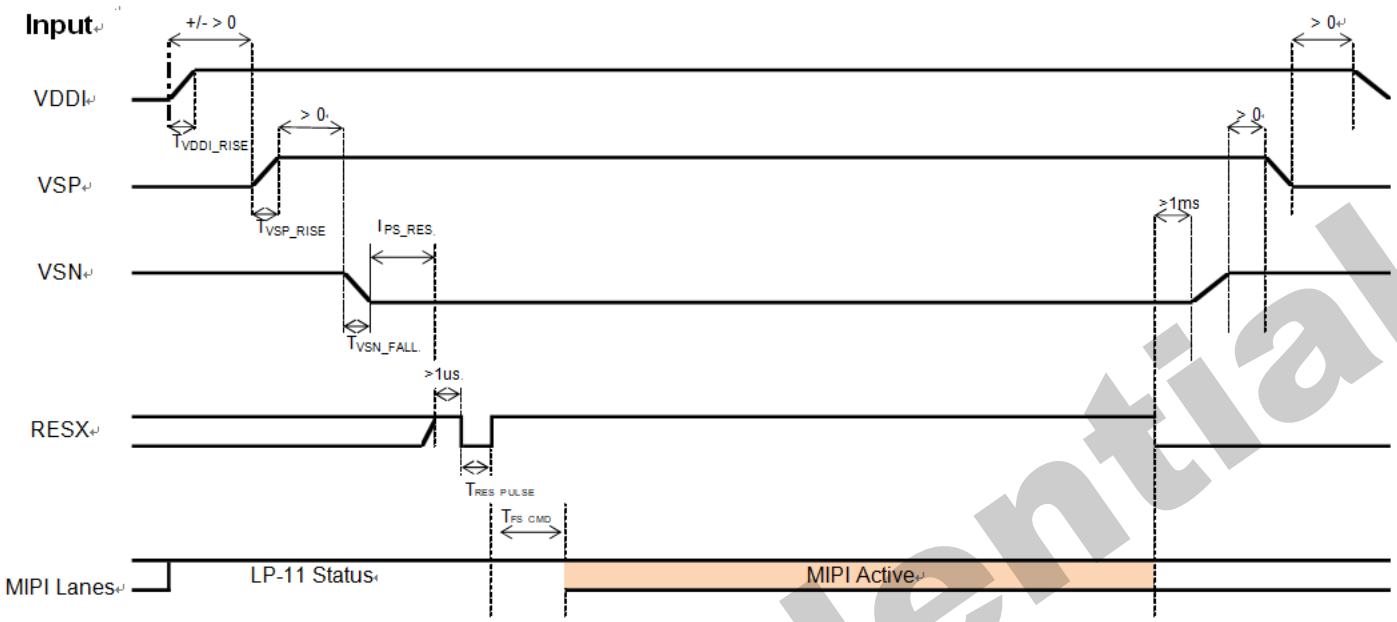
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

7. Power ON/OFF Sequence

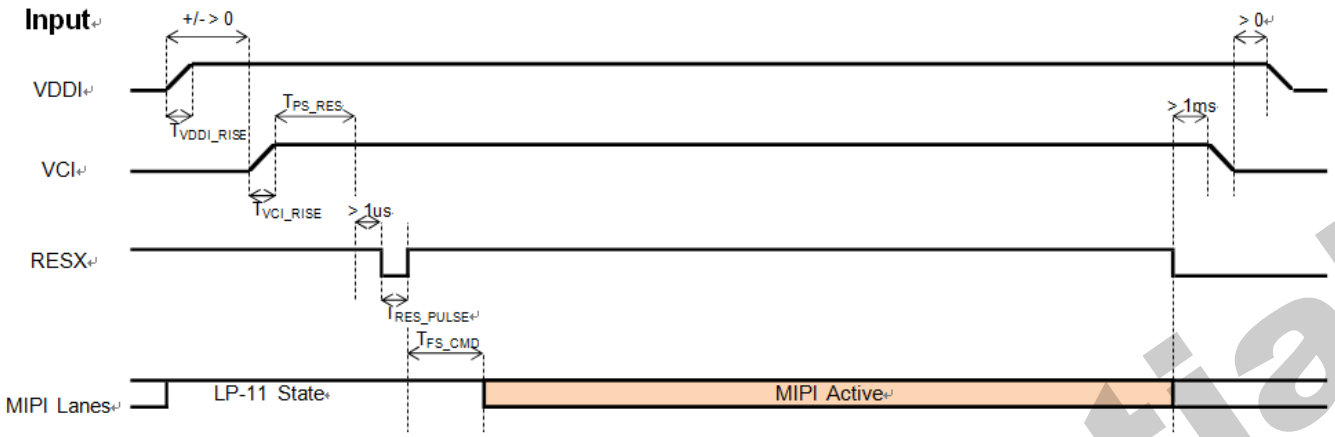
7.1. 3 Power Mode



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{AVDD_RISE}	AVDD Rise time	10	-	-	us
T_{AVEE_FALL}	AVEE Fall time	10	-	-	us
T_{PS_RES}	VDDI/AVDD on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	50	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Power on/off sequence with 3 Power Mode

7.2. 2 Power Mode



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	VCI Rise time	10	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	50	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Power on/off sequence with 2 Power Mode

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on Table 42. When the GC9703C is used out of the absolute maximum ratings, it may be permanently damaged. To use the GC9703C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9703C will malfunction and cause poor reliability.

Table 43 Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VDD ~ AVSS	V	-0.3 ~ +4.6
Supply voltage (I/O)	VDDI ~ VSS	V	-0.3 ~ +1.68
OTP Supply voltage	VPP ~ AGND	V	-0.3 ~ +10
Supply voltage	AVDD ~ AGND	V	-0.3 ~ +8
Supply voltage	AVEE ~ AGND	V	0.3 ~ -8
Supply voltage	VGH ~ AGND	V	-0.3 ~ +20
Supply voltage	VGL ~ AGND	V	0.3 ~ -16
Driver supply voltage	AVDD – AVEE	V	≦14V
Driver supply voltage	VGH – VGL	V	≦30V
Input voltage	V_{IN}	V	-0.3 ~ VDDI + 0.3
HS Input voltage	V_{HSIN}	V	-0.3 ~ + 2
Operating temperature	Topr	℃	-20 ~ +85
Storage temperature	Tstg	℃	-55 ~ +110

Note:

Even if the one of the above parameters is exceeded momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the exceeding values which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VCI	-	2.5	2.8	3.3	V
Operating voltage	VDDI	-	1.65	1.8	3.3	V
OTP Supply voltage	VPP	-		8.0		V
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V
Logic High level output voltage	VOH	-	0.8*VDDI		VDDI	V
Logic Low level output voltage	VOL	-	0		0.2*VDDI	V
Gate Driver High Voltage	VGH	-	10	-	16	V
Gate Driver Low Voltage	VGL	-	-12	-	-8.0	V
Driver Supply Voltage	-	|VGH-VGL|	18	-	28	V
DC VCOM Amplitude Voltage	VCOM		-3.5	-1.5	0	V
Source Output Range	VSOUT	-	VGMN +0.1	-	VGMP -0.1	V
Positive Gamma Reference Voltage	VGMP	-	3.3	4.5	5.6	V
Negative Gamma Reference Voltage	VGMN	-	-5.6	-4.5	-3.3	V

.

8.3. DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

8.4. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	VCI	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	V_{VDD_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{VDDI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are VDDI or VDD. See examples as reference purposes, when V_{VDD_NOISE} and V_{VDDI_NOISE} are maximums, below.

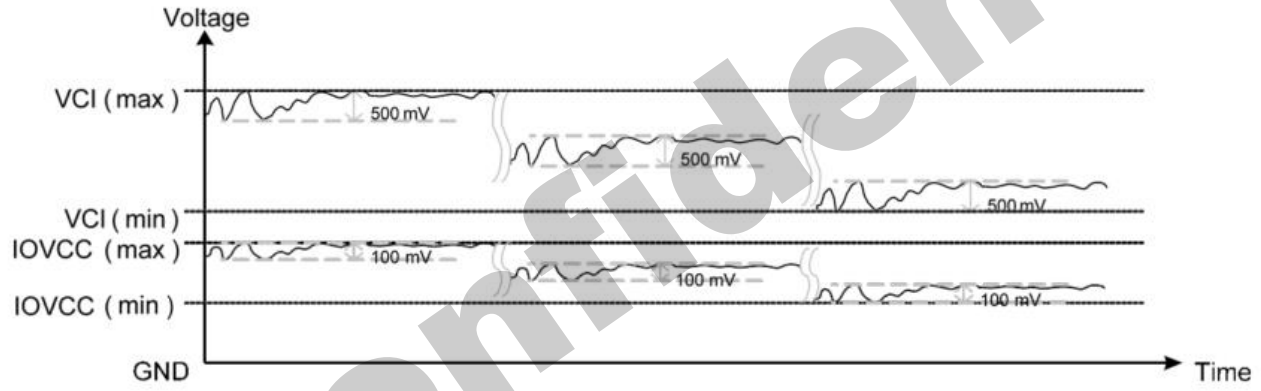


Figure 109 Noise on Power Supply Lines

8.5. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA, Note 2	0.8 V_{VDD}	-	V_{VDD}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=1mA, Note 2	0.0	-	0.2V_{VDD}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD, Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD, Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM
3. DSI High Speed mode is off

8.6. Spike / Glitch Rejection

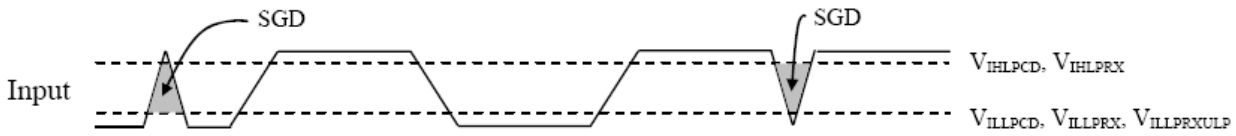


Figure 110 Spike / Glitch Rejection

Note:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1.

Table 44 Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

8.7. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	00	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-		-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), VDDI = 1.65 to 1.95V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0 and 1.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

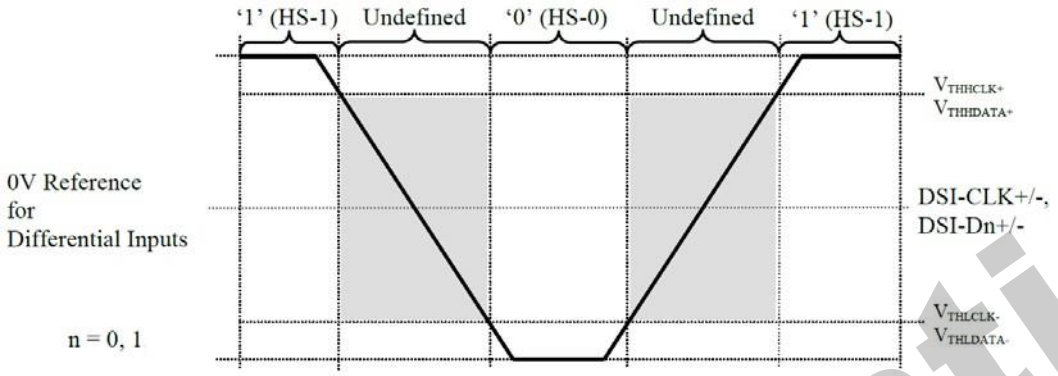
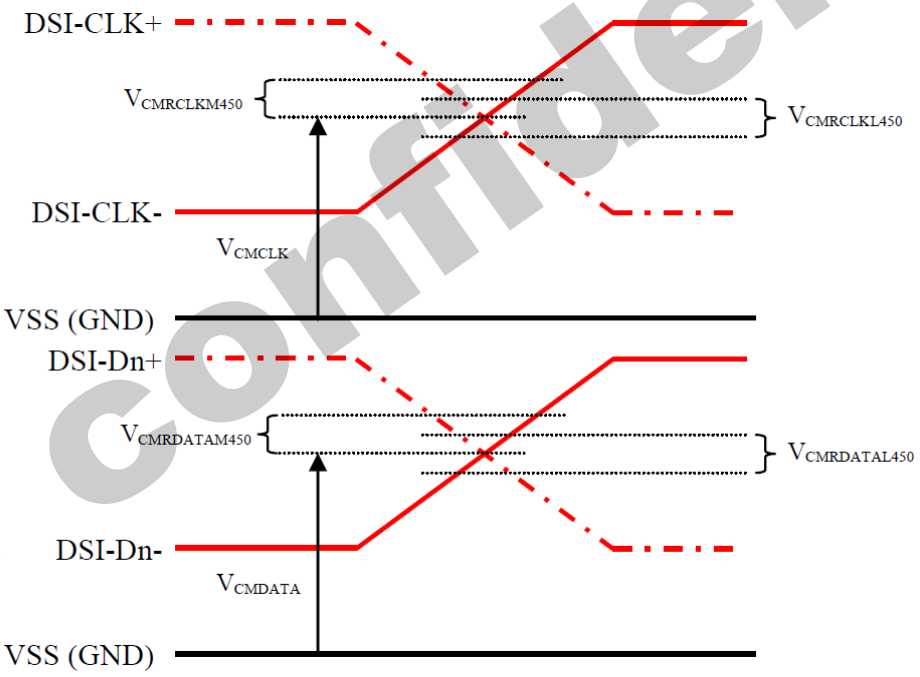


Figure 111 Differential Inputs Logical '0's and '1's, Threshold High/Low, Differential Voltage Range



Note: n = 0 and 1

Figure 112 Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

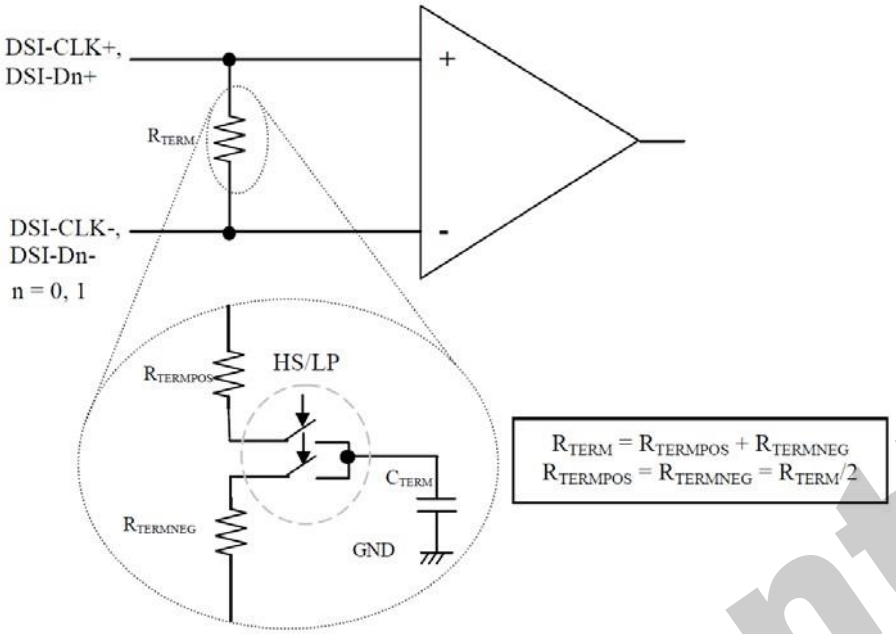


Figure 113 Differential Pair Termination Resistor on the Receiver Side

8.8. AC Characteristic

8.8.1.DSI Timing Characteristics

8.8.1.1. High Speed Mode – Clock Channel Timing

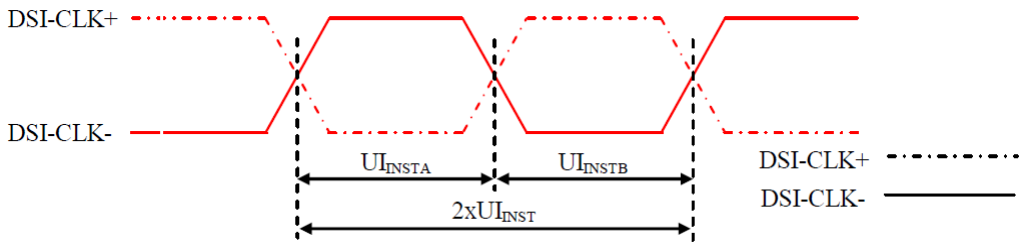


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

8.8.1.2. High Speed Mode – Data Clock Channel Timing

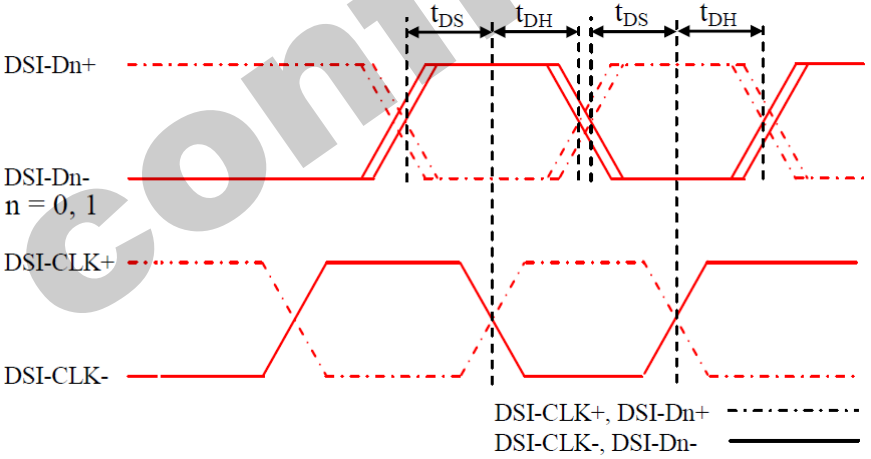


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

8.8.1.3. High Speed Mode – Rise and Fall Timings

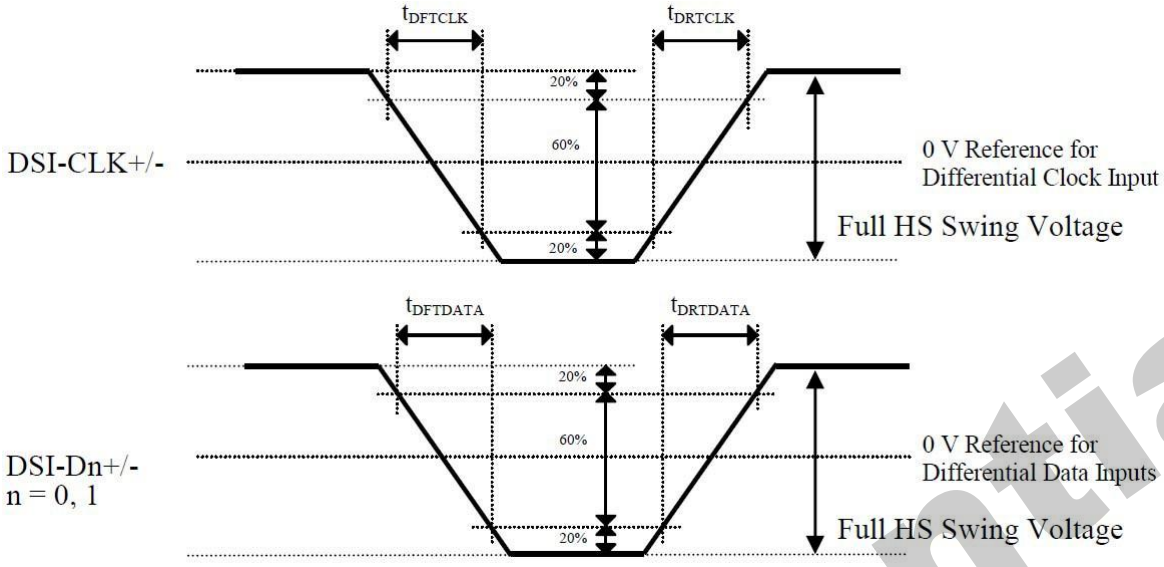


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

8.8.1.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9703C) sequence below.

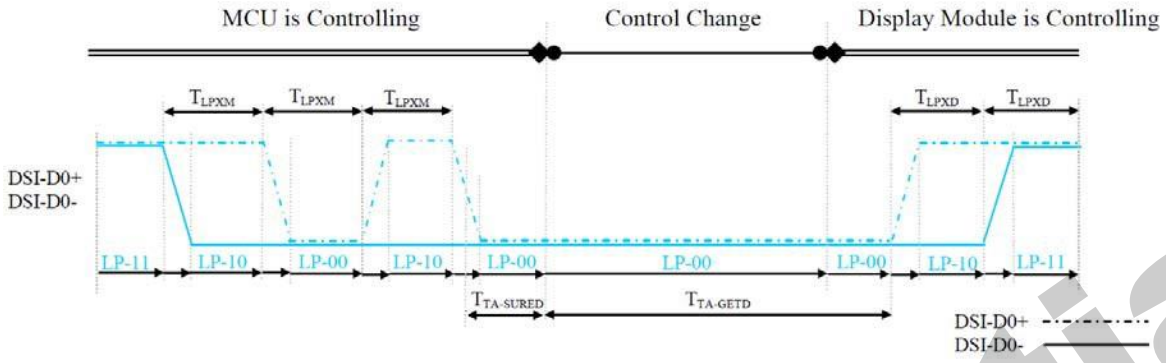


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9703C) to the MPU sequence below.

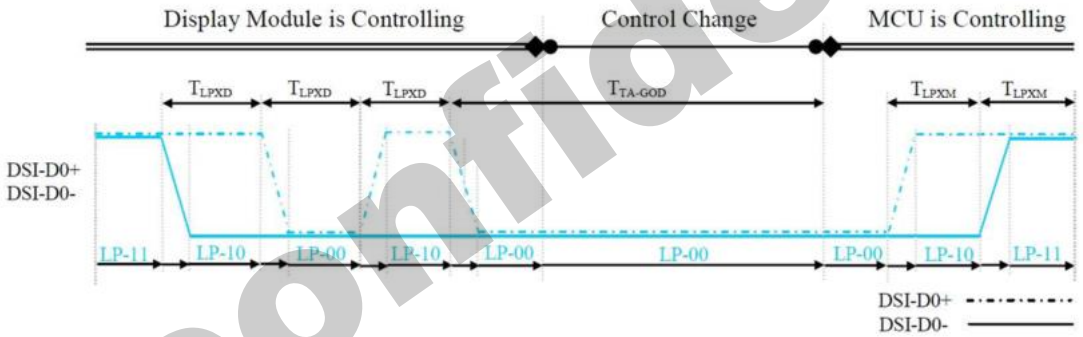


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ⇑ Display Module (GC C)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9703C) ⇑ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (GC9703C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DS-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9703C)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns

8.8.1.5. Data Lanes from Low Power Mode to High Speed Mode

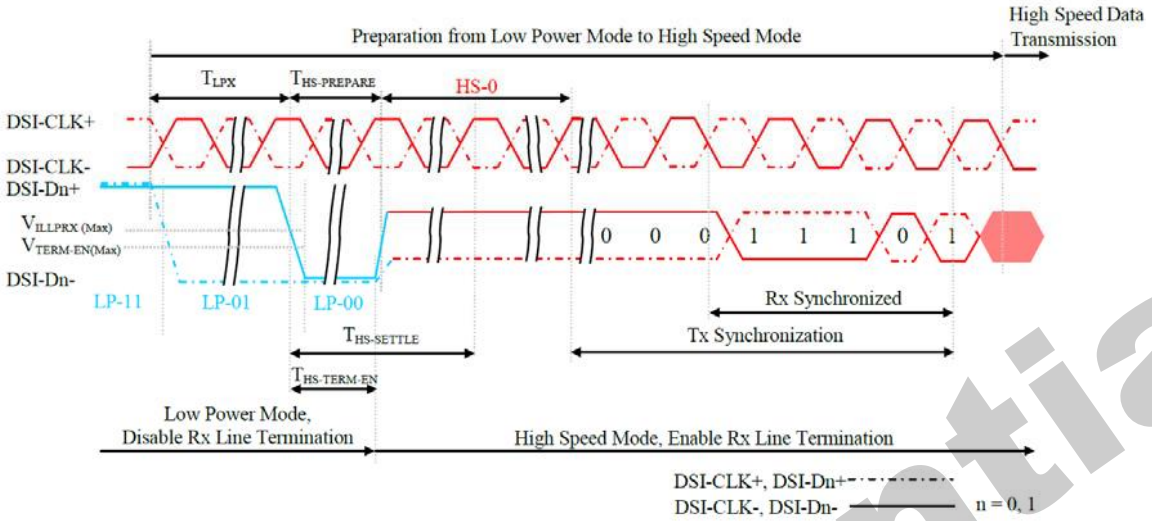


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

8.8.1.6. Data Lanes from High Speed Mode to Low Power Mode

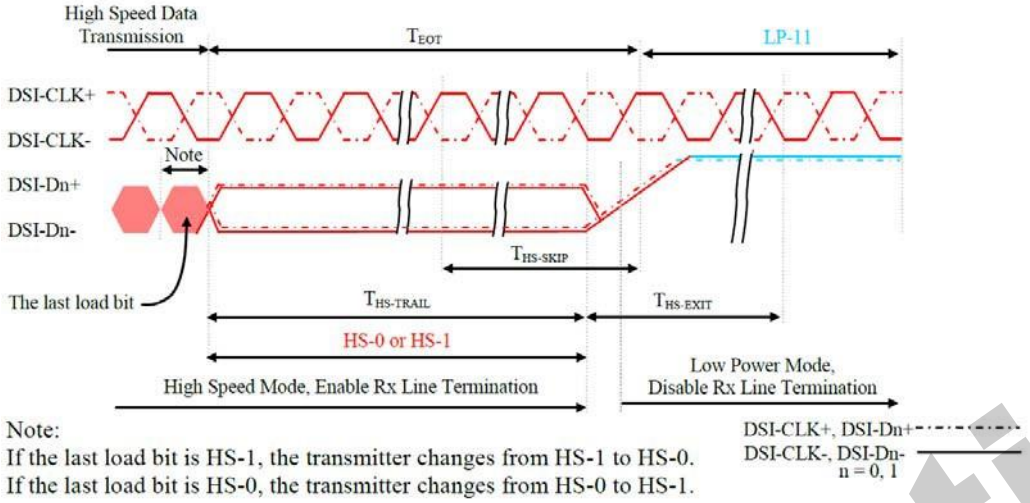


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9703C) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

8.8.2. DSI Clock Burst – High Speed Mode to/from Low Power Mode

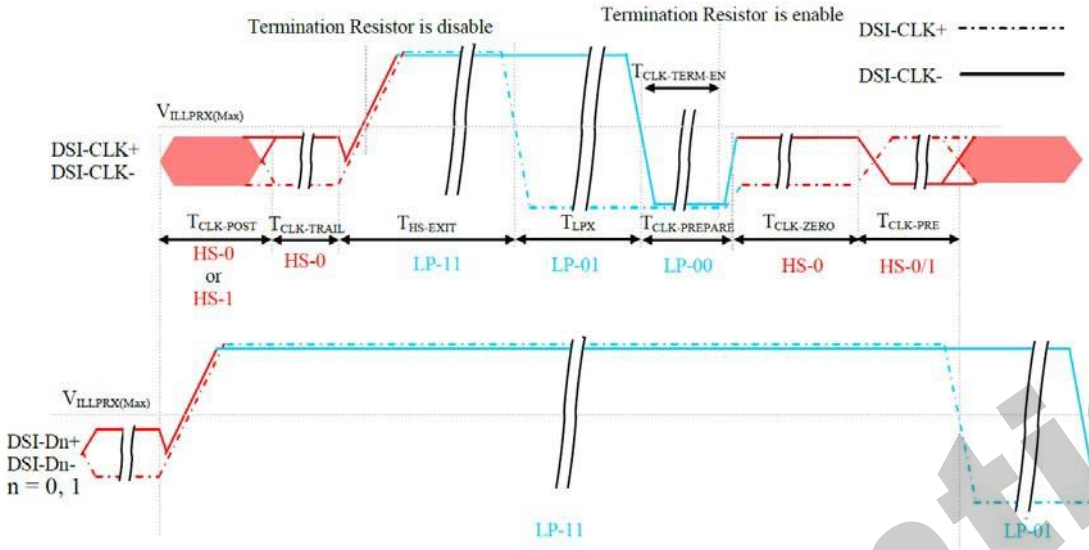


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
SI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns