HD61830/HD61830B

LCDC (LCD Timing Controller)

HITACHI

Description

The HD61830/HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals.

It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830/HD61830B is produced by the CMOS process. Thus, combined with a CMOS microcontroller it can complete a liquid crystal display device with lower power dissipation.

Features

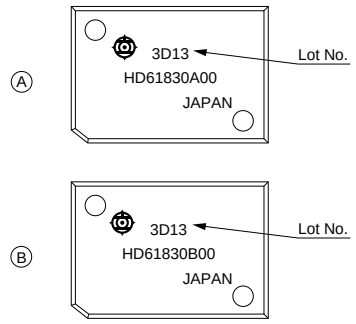
- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - Graphic mode: 512k dots (2^{16} bytes)
  - Character mode: 4096 characters (2^{12} characters)
- Internal character generator ROM: 7360 bits
  - 160 types of 5×7 dot characters
  - 32 types of 5×11 dot characters
    Total 192 characters
  - Can be extended to 256 characters (4 kbytes max.) with external ROM

- Interfaces to 8-bit MPU
- Display duty cycle (can be selected by a program)
  Static to 1/128 duty cycle
- Various instruction functions
  — Scroll, cursor on/off/blink, character blink, bit manipulation
- Display method: Selectable A or B types
- Internal oscillator (with external resistor and capacitor) HD61830
- Operating frequency
  — 1.1 MHz HD61830
  — 2.4 MHz HD61830B
- Low power dissipation
- Power supply: Single +5 V ±10%
- CMOS process

Differences between Products HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal or external	External only
Operating frequency	1.1 MHz	2.4 MHz
Pin arrangement and signal name	Pin 6: C Pin 7: R Pin 9: CPO	Pin 6: $\overline{CE}$ Pin 7: $\overline{OE}$ Pin 9: NC
Package marking to see figure	Ⓐ	Ⓑ

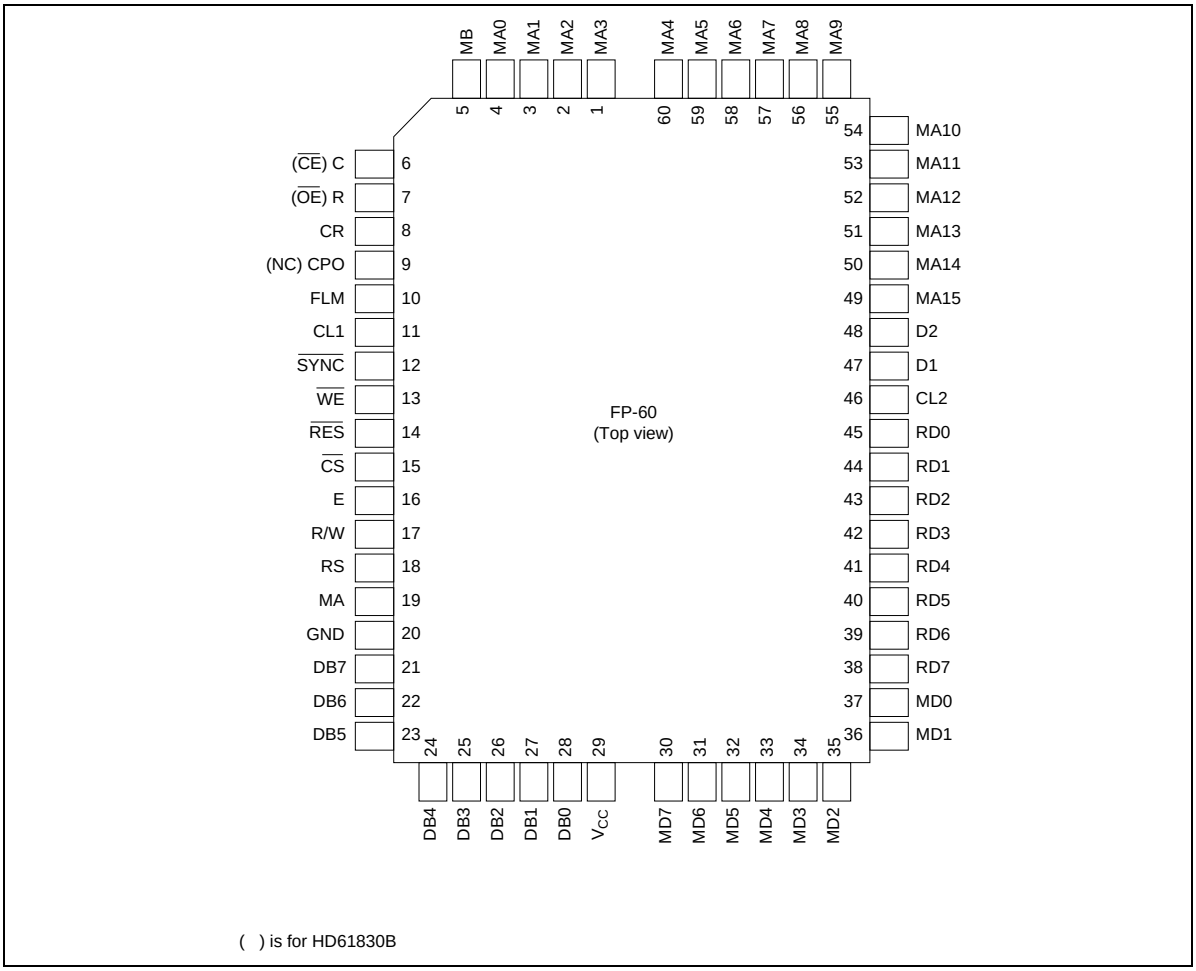
Package Marking



Ordering Information

Type No.	Package
HD61830A00H	60-pin plastic QFP (FP-60)
HD61830B00H	

Pin Arrangement

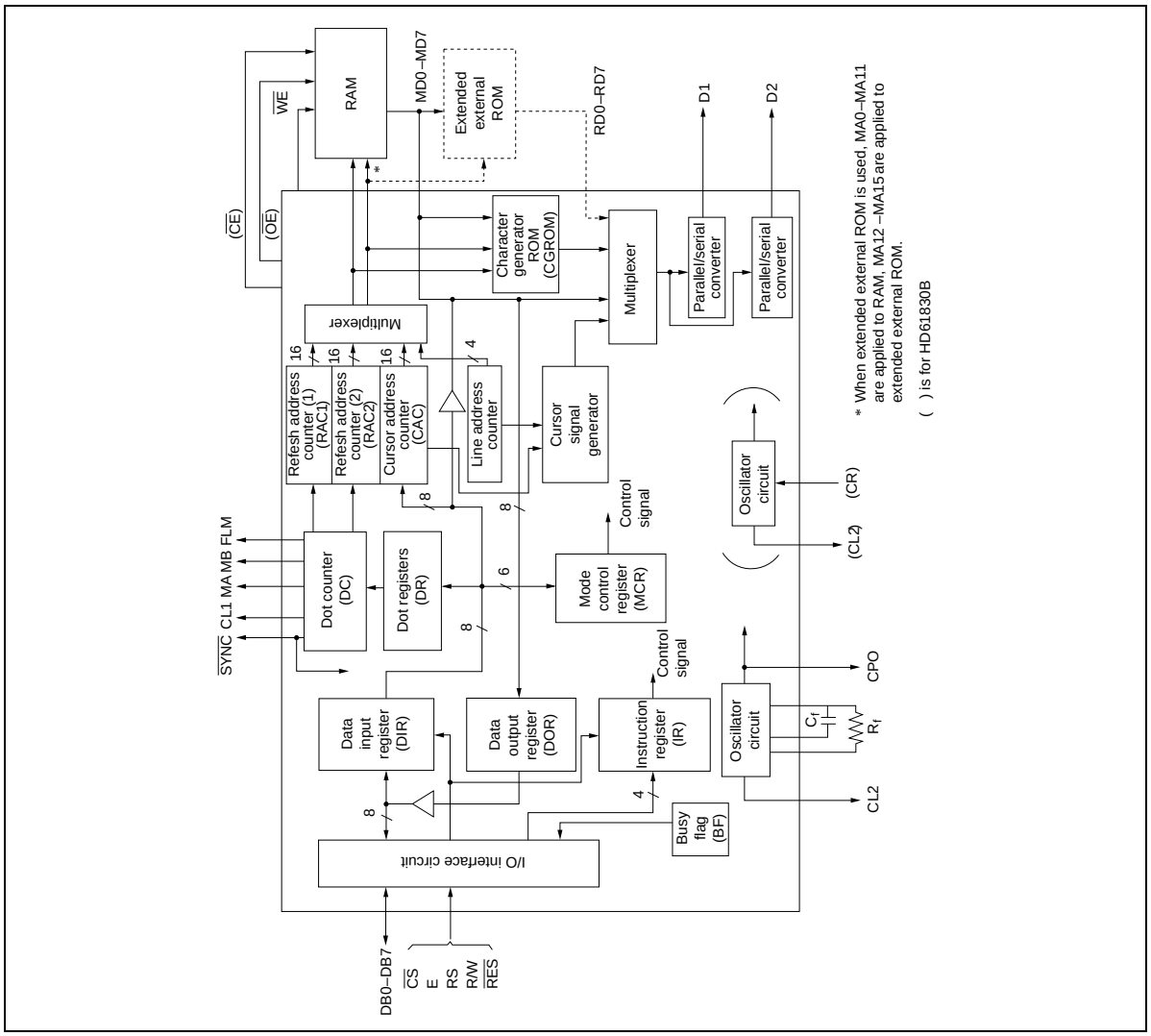


( ) is for HD61830B

Terminal Functions

Symbol	Pin Number	I/O	Function
DB0–DB7	28–21	I/O	Data bus: Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{CS}$	15	I	Chip select: Selected state with $\overline{CS}$ = 0
R/W	17	I	Read/Write:R/W = 1: MPU ← HD61830 R/W = 0: MPU → HD61830
RS	18	I	Register select: RS = 1: Instruction register RS = 0: Data register
E	16	I	Enable: Data is written at the fall of E Data can be read while E is 1
CR	8	I	CR oscillator (HD61830), External clock input (HD61830B)
C	6	—	CR oscillator to capacitor (HD61830 only)
R	7	—	CR oscillator to resistor (HD61830 only)
CPO	9	O	Clock signal for HD61830 in slave mode (HD61830 only)
$\overline{CE}$	6	O	Chip enable (HD61830B only) $\overline{CE}$ = 0: Chip enables make external RAM in active
$\overline{OE}$	7	O	Output enable (HD61830B only) $\overline{OE}$ = 1: Output enable informs external RAM that HD61830B requires data bus
NC	9	Open	Unused terminal. Don't connect any wires to this terminal (HD61830B only)
MA0–MA15	4–1, 60–49	O	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 (0: Character 1st line, F: Character 16th line)
MD0–MD7	37–30	I/O	Display data bus: Three-state I/O common terminal
RD0–RD7	45–38	I	ROM data input: Dot data from external character generator is input
$\overline{WE}$	13	O	Write enable: Write signal for external RAM
CL2	46	O	Display data shift clock for LCD drivers
CL1	11	O	Display data latch signal for LCD drivers
FLM	10	O	Frame signal for display synchronization
MA	19	O	Signal for converting liquid crystal driving signal into AC, A type
MB	5	O	Signal for converting liquid crystal driving signal into AC, B type
D1	47	O	Display data serial output D1: For upper half of screen D2: For lower half of screen
D2	48		
$\overline{SYNC}$	12	I/O	Synchronous signal for parallel operation Three-state I/O common terminal (with pull-up MOS) Master: Synchronous signal is output Slave: Synchronous signal is input
$\overline{RES}$	14	I	Reset: Reset = 0 results in display off, slave mode and H_p = 6

Block Diagram



Block Functions

Registers

The HD61830/HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR), and mode control register (MCR).

The IR is a 4-bit register that stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register, and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR, and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at the high level).

The DR are registers used to store dot information such as character pitches and the number of vertical dots, and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display on/off and cursor on/off/blink. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

The busy flag = 1 indicates the HD61830 is performing an internal operation. Instructions cannot be accepted. As shown in Control Instruction, read busy flag, the busy flag is output on DB7 under the conditions of RS = 1, R/W = 1, and E = 1. Make sure the busy flag is 0 before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

Refresh Address Counters (RAC1/RAC2)

The refresh address counters, RAC1 and RAC2, control the addresses of external RAM, character generator ROM (CGROM), and extended external ROM. The RAC1 is used for the upper half of the screen and the RAC2 for the lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12–MA15) are ignored. The 4 bits of line address counter are output instead and used as the address of extended ROM.

Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 characters) or 5×11 (32 characters). The use of extended ROM allows 8×16 (256 characters max.) to be used.

Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by instruction. It holds an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of the cursor address counter is automatically increased by 1 after the display data is read or written and after the set/clear bit instruction is executed.

Cursor Signal Generator

The cursor can be displayed by instruction in character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM, or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS = 1, and the data register code is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS = 0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. **Mode Control:** Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor off	Internal CG	Character display (Character mode)
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int. CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

2. Set Character Pitch: Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is included in the determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

H_p indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the H_p indicates the number of bits of 1-byte display data to be displayed.

There are three H_p values (Table 1).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(Vp – 1) binary				0	(H_p – 1) binary		

Table 1 H_p Values

Hp	DB2	DB1	DB0	Horizontal Character Pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set Number of Characters: H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$n = H_p \times H_N$

H_N can be set to an even number from 2 to 128 (decimal).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N – 1) binary						

4. Set Number of Time Divisions (Inverse of Display Duty Ratio): N_X indicates the number of time divisions in multiplex display.

$1/N_X$ is the display duty ratio.

A value of 1 to 128 (decimal) can be set to N_X.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time-divisions reg.	0	0	0	(N_X – 1) binary						

5. Set Cursor Position: C_p indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying $C_p = 8$ (decimal). The cursor horizontal length is equal to the horizontal character pitch H_p. A value of 1 to 16 (decimal) can be set to C_p. If a smaller value than the vertical character pitch Vp is set ($C_p \leq$ Vp), and a character overlaps with the cursor, the cursor has higher priority of display (at cursor display on). If C_p is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to H_p.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(C_p – 1) binary			

6. Set Display Start Low Order Address: Cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB3–DB0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

Set Display Start High Order Address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

7. Set Cursor Address (Low Order) (RAM Write Low Order Address): Cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM.

That is, data at the address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the character specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements setting the cursor address (Table 2).

The cursor address counter is a 16-bit up-counter with set and reset functions. When bit N changes from 1 to 0, bit N + 1 is incremented by 1. When setting the low order address, the LSB (bit 1) of the high order address is incremented by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in the Table 2.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

Set Cursor Address (High Order) (RAM Write High Order Address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

Table 2 Cursor Address Setting

Condition	Requirement
When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
When you want to rewrite only the low order address.	Do not fail to set the high order address again after setting the low order address.
When you want to rewrite only the high order address.	Set the high order address. You do not have to set the low order address again.

8. Write Display Data: After the code $"0C" is written into the instruction register with RS = 1, 8-bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

9. Read Display Data: Data can be read from the RAM with RS = 0 after writing code $"0D" into the instruction register. Figure 1 shows the read procedure.

This instruction outputs the contents of data output register on the data bus (DB0 to DB7) and then transfers RAM data specified by the cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second one. Thus, make one dummy read when reading data after setting the cursor address.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

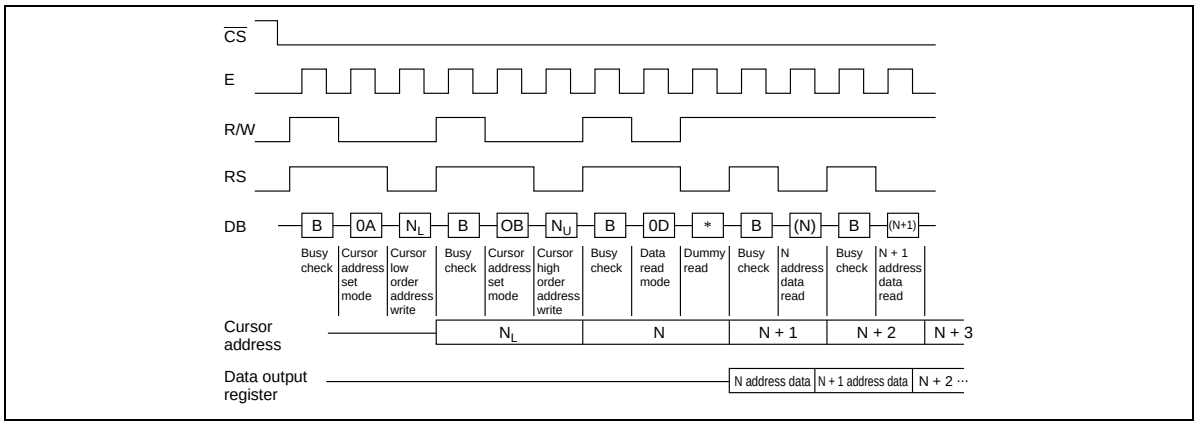


Figure 1 Read Procedure

10. Clear Bit: The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value from 1 to 8. N_B = 1 and N_B = 8 indicates LSB and MSB, respectively.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

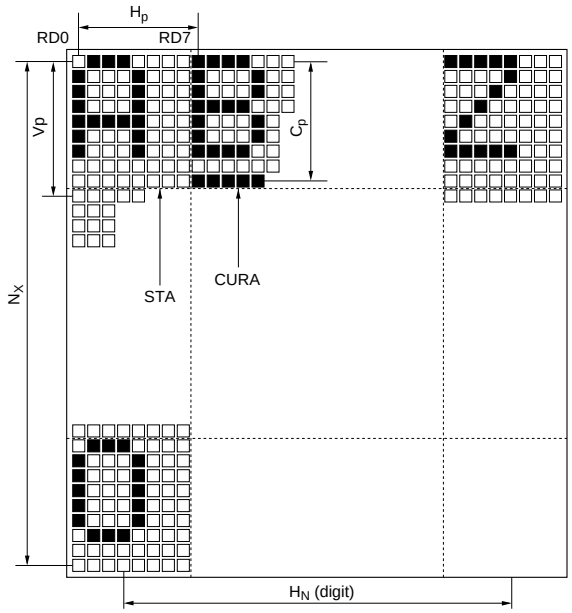
Set Bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

11. Read Busy Flag: When the read mode is set with RS = 1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of the other instructions. After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag = 1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS = 1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS = 1.

The busy flag can be read without specifying any instruction register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0				*			

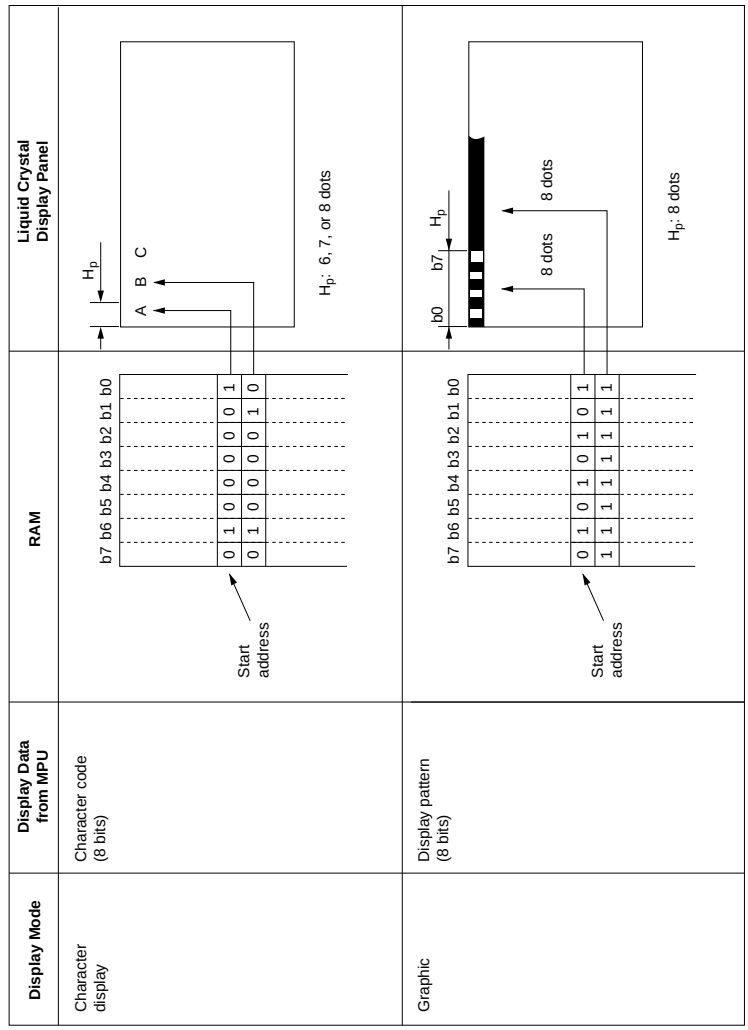


Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizontal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode	2 to 128 digits (an even number)
Vp	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time divisions	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on the screen is m, and the number of horizontal dots is n,
$1/m = 1/N_X$ = display duty ratio
$n = H_p \times H_N$,
m/Vp = Number of display lines
$C_p \leq Vp$

Figure 2 Display Variables

Display Mode



Internal Character Generator Patterns and Character Codes



Example of Correspondence between External CGROM Address Data and Character Pattern

8 × 8 Dot Font

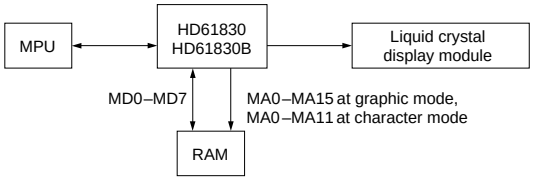
	A10	0								0								0	1
	A 9	0								0								0	1
	A 8	0								0								1	1
	A 7	0								1								0	1
A6 A5 A4 A3	A2 A1 A0	00	01	02	03	04	05	06	07	00	01	02	03	04	05	06	07		
0 0 0 0	0 0 0	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0		
	0 0 1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0 1 0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0 1 1	1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0		
	1 0 0	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0		
	1 0 1	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0		
	1 1 0	1	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0		
	1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0 0 0 1	0 0 0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0		
	0 0 1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0		
	0 1 0	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	1		
	0 1 1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0		
	1 0 0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0		
	1 0 1	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0		
	1 1 0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0		
	1 1 1	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0		
0 0 1 0	0 0 0																		

8 × 16 Dot Font

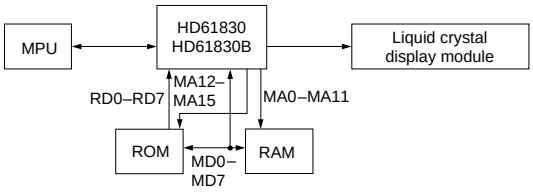
	A11	0								0								0	
	A10	0								0								0	
	A 9	0								0								1	
	A 8	0								1								0	
A7 A6 A5 A4	A3 A2 A1 A0	00	01	02	03	04	05	06	07	00	01	02	03	04	05	06	07		
0 0 0 0	0 0 0 0					0	0	0	0	0	0	0	0	0	0	0	0		
	0 0 0 1		0	0	0		0	0	0	0	0	0	0	0	0	0	0		
	0 0 1 0		0	0	0		0	0	0	0	0	0	0	0	0	0	0		
	0 0 1 1					0	0	0	0		0	0	0	0		0			
	0 1 0 0		0		0	0	0	0	0		0	0	0	0		0	0		
	0 1 0 1		0	0		0	0	0	0	0		0		0	0	0	0		
	0 1 1 0		0	0	0		0	0	0	0	0		0	0	0	0	0		
	0 1 1 1	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0		
	1 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0		
	1 0 0 1	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0		
	1 0 1 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	1 0 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	1 1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	1 1 0 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	1 1 1 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	1 1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Example of Configuration

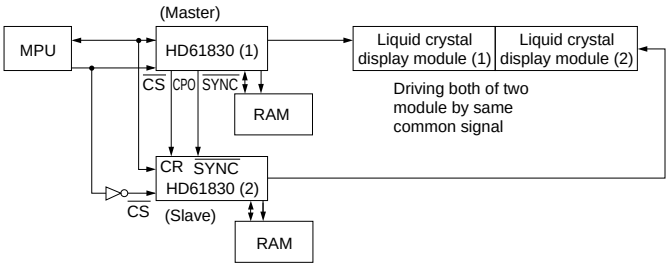
Graphic Mode or Character Mode (1) (Internal Character Generator)



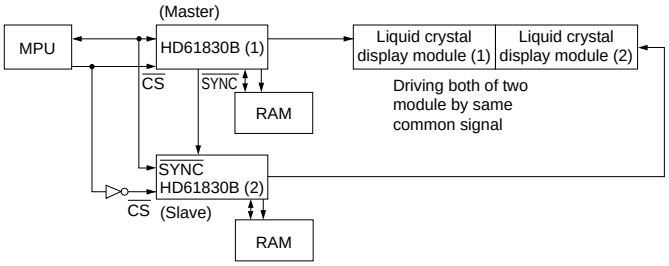
Character Mode (2) (External Character Generator)



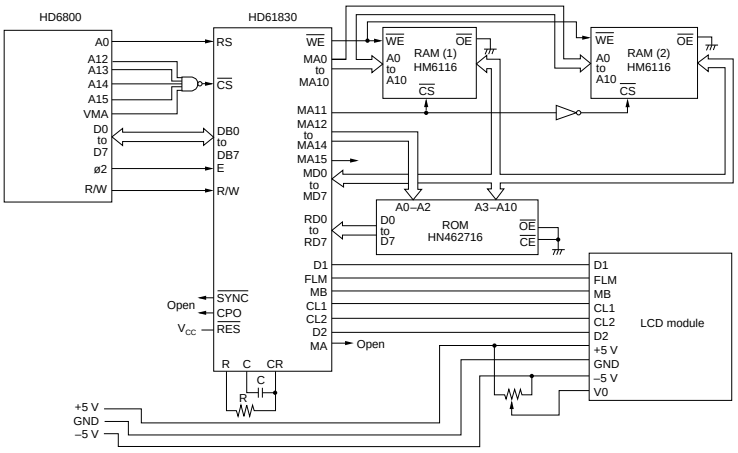
Parallel Operation (HD61830)



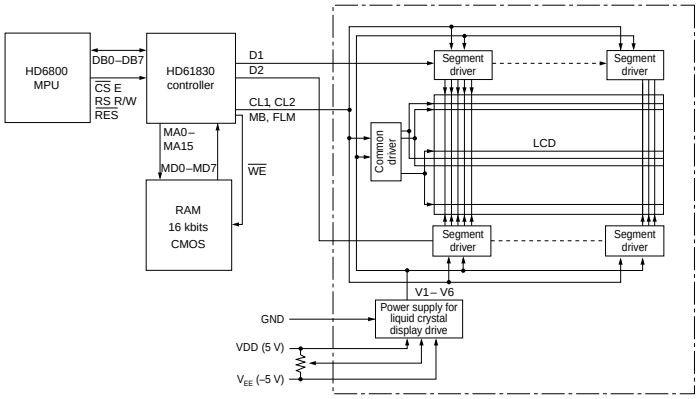
Parallel Operation (HD61830B)



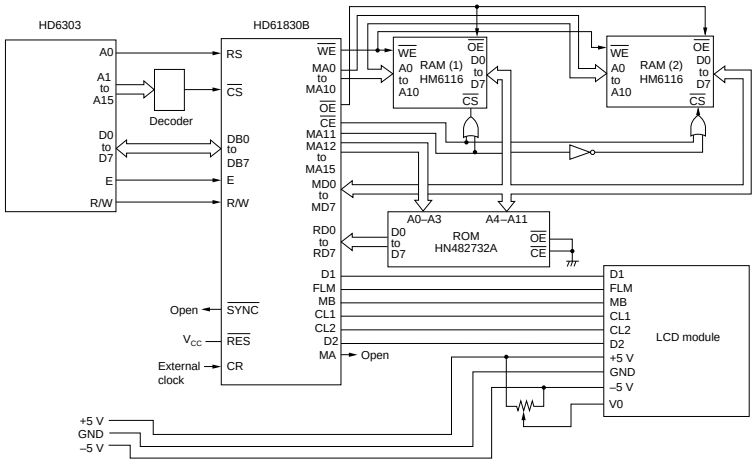
HD61830 Application (Character Mode, External CG, Character Font 8 × 8)



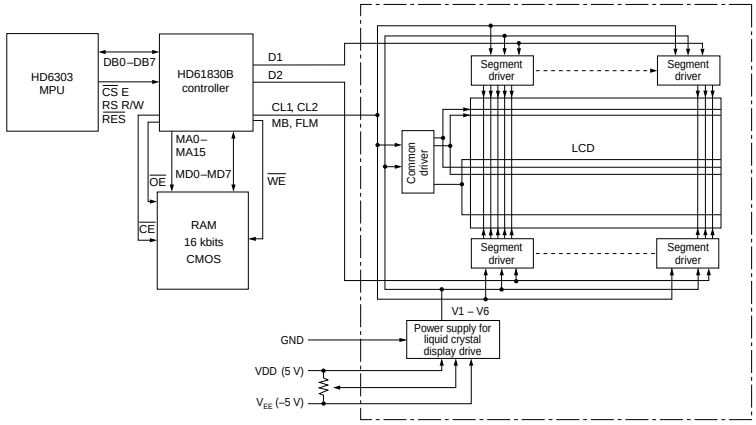
HD61830 Application (Graphic Mode)



HD61830B Application (Character Mode, External CG, Character Font 8 × 8)



HD61830B Application (Graphic Mode)



HD61830 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	VT	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltages are referenced to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

HD61830 Electrical Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

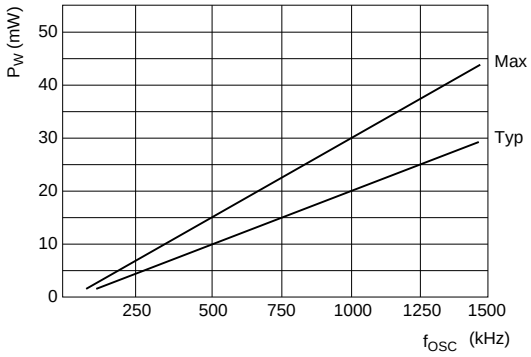
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (TTL)	VIH	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	VIL	0	—	0.8	V		2
Input high voltage	VIHR	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	VIHC	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	VILC	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	VOH	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	VOL	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	VOHC	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	VOLC	0	—	0.4	V	I_{OL} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	VIN = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	VOUT = 0 – V_{CC}	8
Power dissipation (1)	P_W1	—	10	15	mW	CR oscillation f_{osc} = 500 kHz	9
Power dissipation (2)	P_W2	—	20	30	mW	External clock f_{cp} = 1 MHz	9
Internal clock operation (Clock oscillation frequency)	f_{osc}	400	500	600	kHz	C_f = 15 pF ±5% R_f = 39 kΩ ±2%	10
External clock operation (External clock operating frequency)	f_{cp}	100	500	1100	kHz		11
External clock duty	Duty	47.5	50	52.5	%		11
External clock rise time	t_{rcp}	—	—	0.05	µs		11
External clock fall time	t_{fcp}	—	—	0.05	µs		11
Pull-up current	I_{PL}	2	10	20	µA	VIN = GND	12

Notes: The I/O terminals have the following configuration:

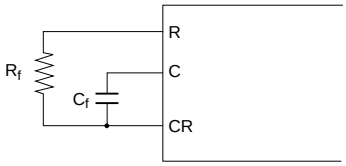
1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB0–DB7, $\overline{WE}$, MA0–MA15, and MD0–MD7.
6. Applied to terminals $\overline{SYNC}$, CP0, FLM, CL1, CL2, D1, D2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

9. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

   The relationship between the operating frequency and the power dissipation is given below.

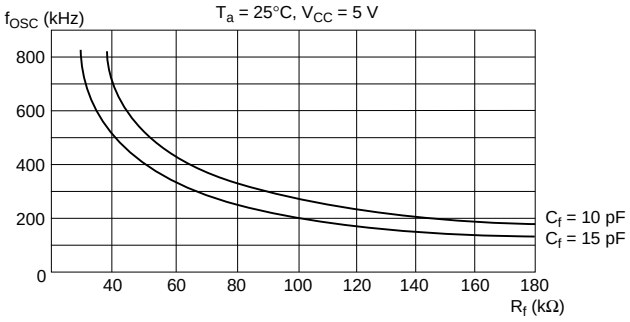


10. Applied to the operation of the internal oscillator when oscillation resistor R_f and oscillation capacity C_f are used.

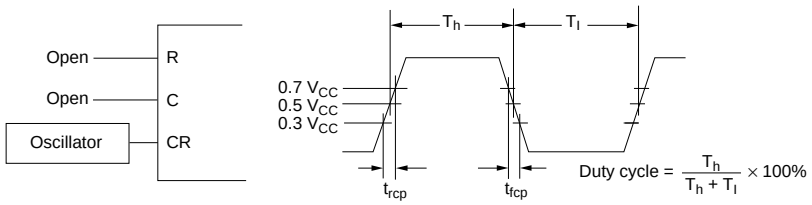


C_f = 15 pF ±5%
R_f = 39 kΩ ±2%
(when f_{OSC} = 500 kHz typ)

The relationship among oscillation frequency, R_f and C_f is given below.



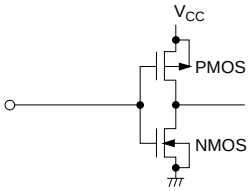
11. Applied to external clock operation.



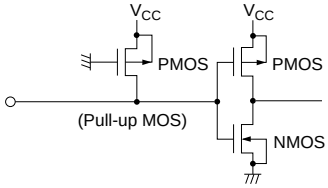
12. Applied to $\overline{\text{SYNC}}$, DB0–DB7, and RD0–RD7.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

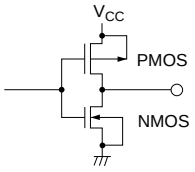


Applicable terminal: RD0–RD7 (with pull-up MOS)



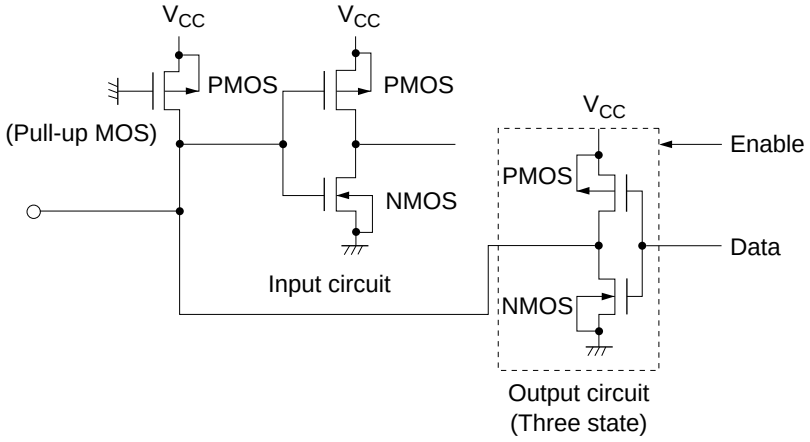
Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, D1, D2, $\overline{WE}$, CPO, MA0–MA15



I/O Common Terminal

Applicable terminal: DB0–DB7, $\overline{SYNC}$, MD0–MD7 (MD0–MD7 have no pull-up MOS)

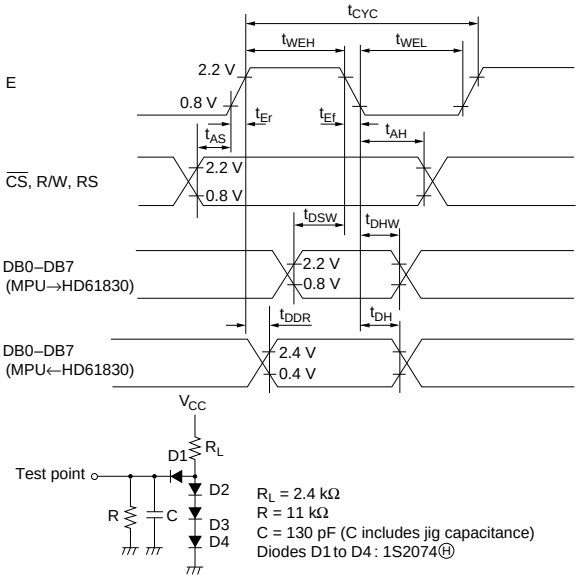


Timing Characteristics

HD61830 MPU Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

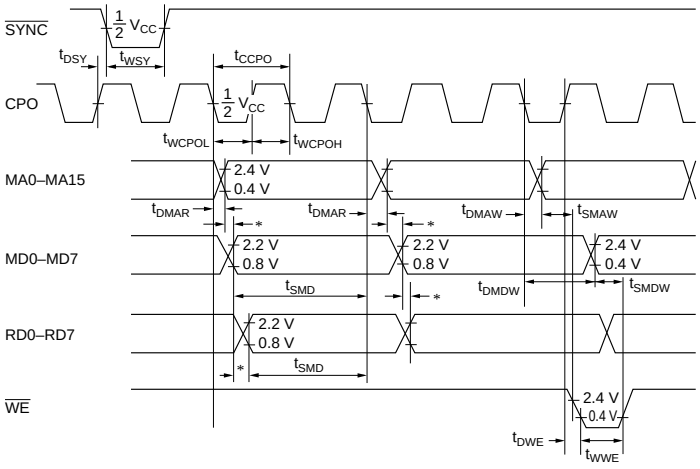
Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Output data hold time		t_{DH}	20	—	—	ns

Note: * The following load circuit is connected for specification:



HD61830 External RAM and ROM Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
$\overline{SYNC}$ delay time		t_{DSY}	—	—	200	ns
$\overline{SYNC}$ pulse width	Low level	t_{WSY}	900	—	—	ns
CPO cycle time		t_{CCPO}	900	—	—	ns
CPO pulse width	High level	t_{WCPOH}	450	—	—	ns
	Low level	t_{WCPOL}	450	—	—	ns
MA0 to MA15 refresh delay time		t_{DMAR}	—	—	200	ns
MA0 to MA15 write address delay time		t_{DMAW}	—	—	200	ns
MD0 to MD7 write data delay time		t_{DMDW}	—	—	200	ns
MD0 to MD7, RD0 to RD7 setup time		t_{SMD}	900	—	—	ns
Memory address setup time		t_{SMAW}	250	—	—	ns
Memory data setup time		t_{SMDW}	250	—	—	ns
$\overline{WE}$ delay time		t_{DWE}	—	—	200	ns
$\overline{WE}$ pulse width (low level)		t_{WWE}	450	—	—	ns

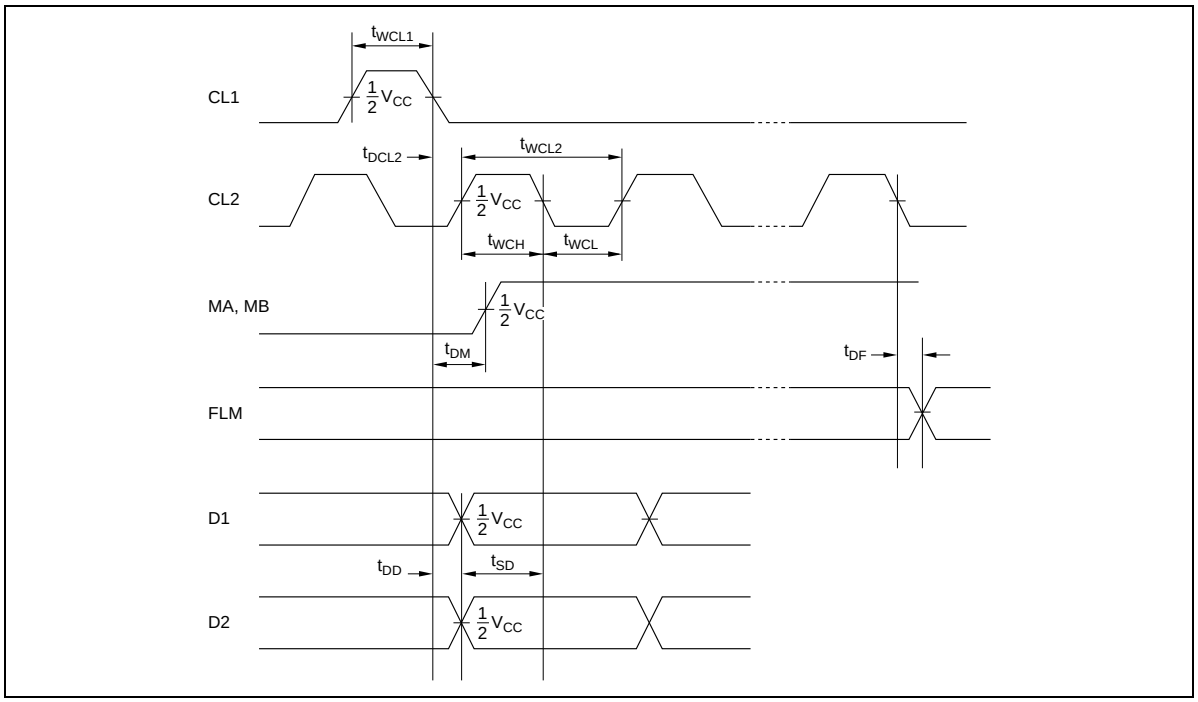


Notes: 1. No load is applied to all the output terminals.
2. "*" indicates the delay time of RAM and ROM.

HD61830 LCD Driver Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Clock pulse width (high level)		t_{WCL1}	450	—	—	ns
Clock delay time		t_{DCL2}	—	—	200	ns
Clock cycle time		t_{WCL2}	900	—	—	ns
Clock pulse width	High level	t_{WCH}	450	—	—	ns
	Low level	t_{WCL}	450	—	—	ns
MA, MB delay time		t_{DM}	—	—	300	ns
FLM delay time		t_{DF}	—	—	300	ns
Data delay time		t_{DD}	—	—	200	ns
Data setup time		t_{SD}	250	—	—	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D1, and D2).



HD61830B Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	VT	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltage is referred to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

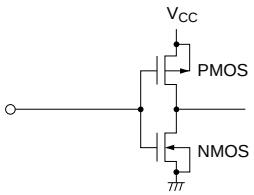
HD61830B Electrical Characteristics (V_{CC} = 5V ±10%, GND = 0V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (TTL)	VIH	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	VIL	0	—	0.8	V		2
Input high voltage	VIHR	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	VIHC	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	VILC	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	VOH	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	VOL	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	VOHC	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	VOLC	0	—	0.4	V	I_{OI} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	VIN = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	VOUT = 0 – V_{CC}	8
Pull-up current	I_{PL}	2	10	20	µA	Vin = GND	9
Power dissipation	P_W	—	—	50	mW	External clock f_{cp} = 2.4 MHz	10

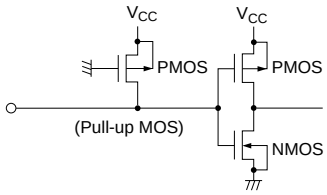
Notes:
1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB0–DB7, $\overline{WE}$, MA0–MA15, $\overline{OE}$, $\overline{CE}$, and MD0–MD7.
6. Applied to terminals $\overline{SYNC}$, FLM, CL1, CL2, D1, D2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.
9. Applied to $\overline{SYNC}$, DB0–DB7, and RD0–RD7.
10. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

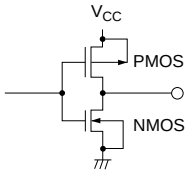


Applicable terminal: RD0–RD7 (with pull-up MOS)



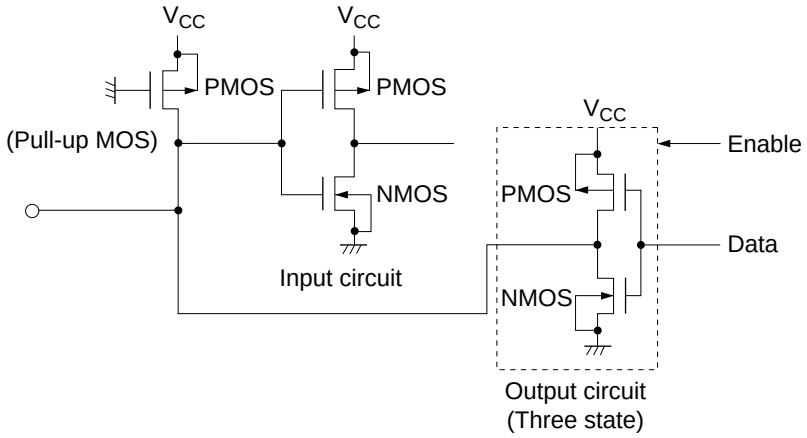
Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0–MA15



I/O Common Terminal

Applicable terminal: DB0–DB7, $\overline{SYNC}$, MD0–MD7 (MD0–MD7 have no pull-up MOS)

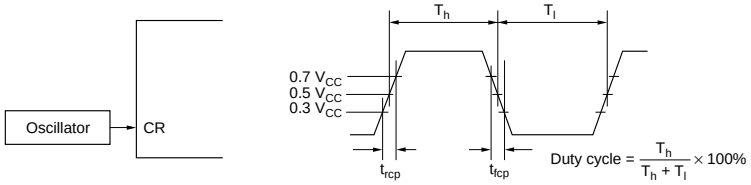


Timing Characteristics

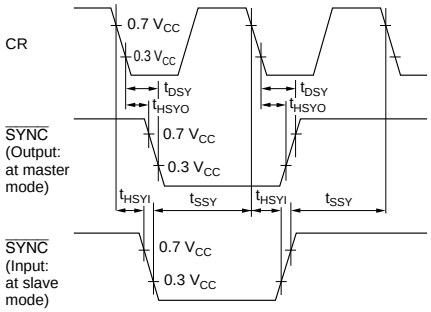
HD61830B Clock Operation (V_{CC} = 5 V ±10%, GND = 0V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
External clock operating frequency	f_{cp}	100	—	2400	kHz	1
External clock duty	Duty	47.5	50	52.5	%	1
External clock rise time	t_{rcp}	—	—	25.0	ns	1
External clock fall time	t_{fcp}	—	—	25.0	ns	1
$\overline{SYNC}$ output hold time	t_{HSYO}	30	—	—	ns	2, 3
$\overline{SYNC}$ output delay time	t_{DSY}	—	—	210	ns	2, 3
$\overline{SYNC}$ input hold time	t_{HSYI}	10	—	—	ns	2
$\overline{SYNC}$ input set-up time	t_{SSY}	—	—	180	ns	2

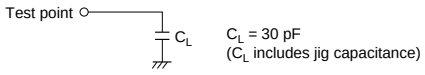
Notes: 1. Applied to external clock input terminal.



2. Applied to $\overline{SYNC}$ terminal.



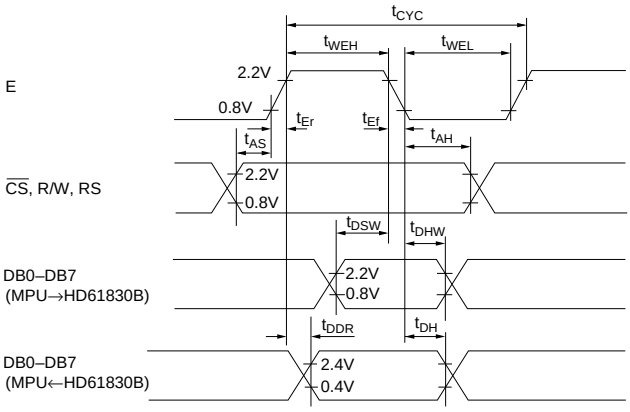
3. Testing load circuit.

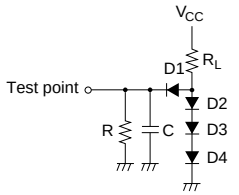


HD61830B MPU Interface (V_{CC} = 5V ±10%, GND = 0V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Output data hold time		t_{DH}	20	—	—	ns

Note: * The following load circuit is connected for specification:



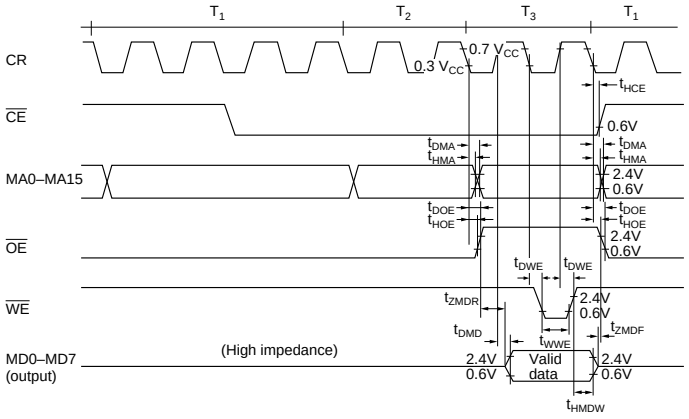


R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (C includes jig capacitance)
Diodes D1 to D4 : 1S2074Ⓗ

HD61830B External RAM and ROM Interface (V_{CC} = 5V ±10%, GND = 0V, T_a = –20 to +75°C)

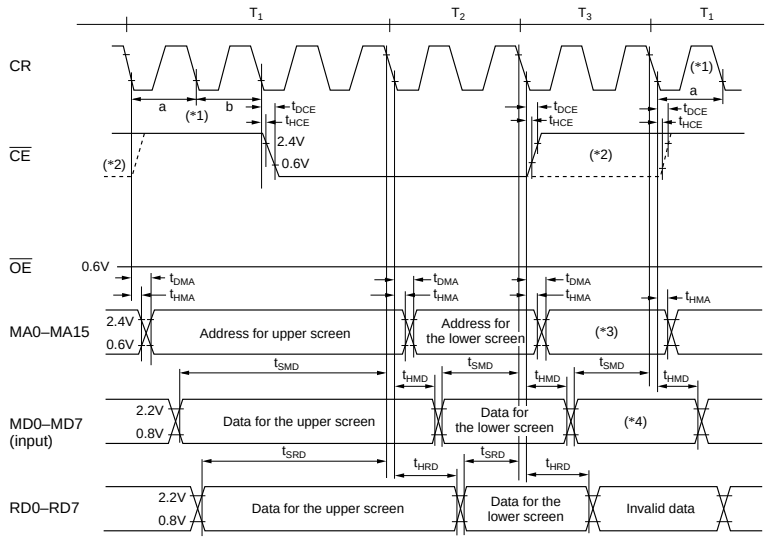
Item	Symbol	Min	Typ	Max	Unit	Notes
MA0–MA15 delay time	t_{DMA}	—	—	300	ns	1, 2, 3
MA0–MA15 hold time	t_{HMA}	40	—	—	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}	—	—	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}	40	—	—	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}	—	—	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}	40	—	—	ns	1, 3
MD output delay time	t_{DMD}	—	—	150	ns	1, 3
MD output hold time	t_{HMDW}	10	—	—	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}	—	—	150	ns	1, 3
$\overline{WE}$ clock pulse width	t_{WWE}	150	—	—	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}	10	—	—	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}	50	—	—	ns	1, 3
RD data set-up time	t_{SRD}	50	—	—	ns	2
RD data hold time	t_{HRD}	40	—	—	ns	2
MD data set-up time	t_{SMD}	50	—	—	ns	2
MD data hold time	t_{HMD}	40	—	—	ns	2

Notes: 1. RAM write timing



T1: Memory data refresh timing for upper screen
T2: Memory data refresh timing for lower screen
T3: Memory read/write timing

2. ROM/RAM read timing



*1 This figures shows the timing for H_p = 8.

For H_p = 7, time shown by “b” becomes zero. For H_p = 6, time shown by “a” and “b” become zero.

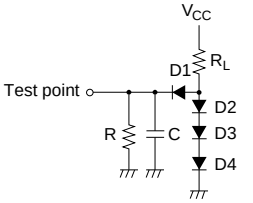
Therefore, the number of clock pulses during T1 become 4, 3, or 2 in the case of H_p = 8, H_p = 7, or H_p = 6 respectively.

*2 The waveform for instructions with memory read is shown with a dash line. In other cases, the waveform shown with a solid line is generated.

*3 When an instruction with RAM read/write is executed, the value of cursor address is output. In other cases, invalid data is output.

*4 When an instruction with RAM read is executed, HD61830B latches the data at this timing. In other cases, this data is invalid.

3. Test load circuit

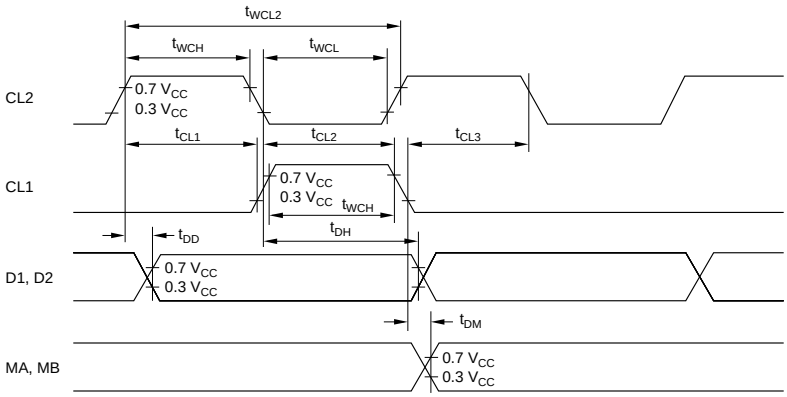


R_L = 2.4 kΩ
R = 11 kΩ
C = 50 pF (C includes jig capacitance)
Diodes D1 to D4 : 1S2074Ⓗ

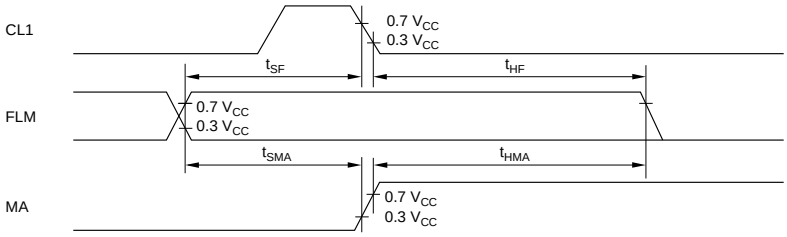
HD61830B LCD Driver Interface (V_{CC} = 5V ±10%, GND = 0V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{WCL2}	416	—	—	ns	1, 3
Clock pulse width(high level)	t_{WCH}	150	—	—	ns	1, 3
Clock pulse width(low level)	t_{WCL}	150	—	—	ns	1, 3
Data delay time	t_{DD}	—	—	50	ns	1, 3
Data hold time	t_{DH}	100	—	—	ns	1, 3
Clock phase difference (1)	t_{CL1}	100	—	—	ns	1, 3
Clock phase difference (2)	t_{CL2}	100	—	—	ns	1, 3
Clock phase difference (3)	t_{CL3}	100	—	—	ns	1, 3
MA, MB delay time	t_{DM}	–200	—	200	ns	1, 3
FLM set-up time	t_{SF}	400	—	—	ns	2, 3
FLM hold time	t_{HF}	1000	—	—	ns	2, 3
MA set-up time	t_{SMA}	400	—	—	ns	2, 3
MA hold time	t_{HMA}	1000	—	—	ns	2, 3

Notes: 1.



2.



3. Test load circuit

