DATA SHEET

(DOC No. HX8346-A(T)-DS)

HX8346-A(T)

240RGB x 320 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Version 01 July, 2007

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1. General Description

This manual describes the Himax's HX8346-A 240RGBx320 dots resolution driving controller. The HX8346-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8346-A can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8346-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8346-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

HX8346-A supports four-type interface mode: Command-Parameter interface mode, Register-Content interface mode, RGB interface mode and Hardware-Control interface mode. Command-Parameter interface mode, Register-Content interface mode and Hardware-Control interface mode are selected by the external pins IFSEL setting, and RGB interface mode is selected by internal bit RGB_EN setting. The description of this manual focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8346-A(N) datasheet for detail.

2. Features

2.1 Display

- Resolution: 240(H)xRGB(H) x320(V)
- Display Color modes
  - A. Normal Display Mode On
    - a. 65,536(R(5),G(6),B(5)) colors
    - b. 262,144(R(6),G(6),B(6)) colors
    - c. 4,096(R(4),G(4),B(4)) colors
  - B. Idle Mode On
    - a. 8 (R(1),G(1),B(1)) colors.

2.2 Display module

- AM-LCD glass 240xRGBx320
- Gamma correction (4 preset gamma curves)
- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - A. VLCD = 3.0 to 6.0V (Source output voltage range)
  - B. VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - C. VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240 (H) x 320 (V) x 18 bit

2.3 Display/Control interface

- Display Interface types supported
  - A. 8/16/18 MPU parallel interface
  - B. Serial data transfer interface.
  - C. 16/18 data lines parallel video (RGB) interface.

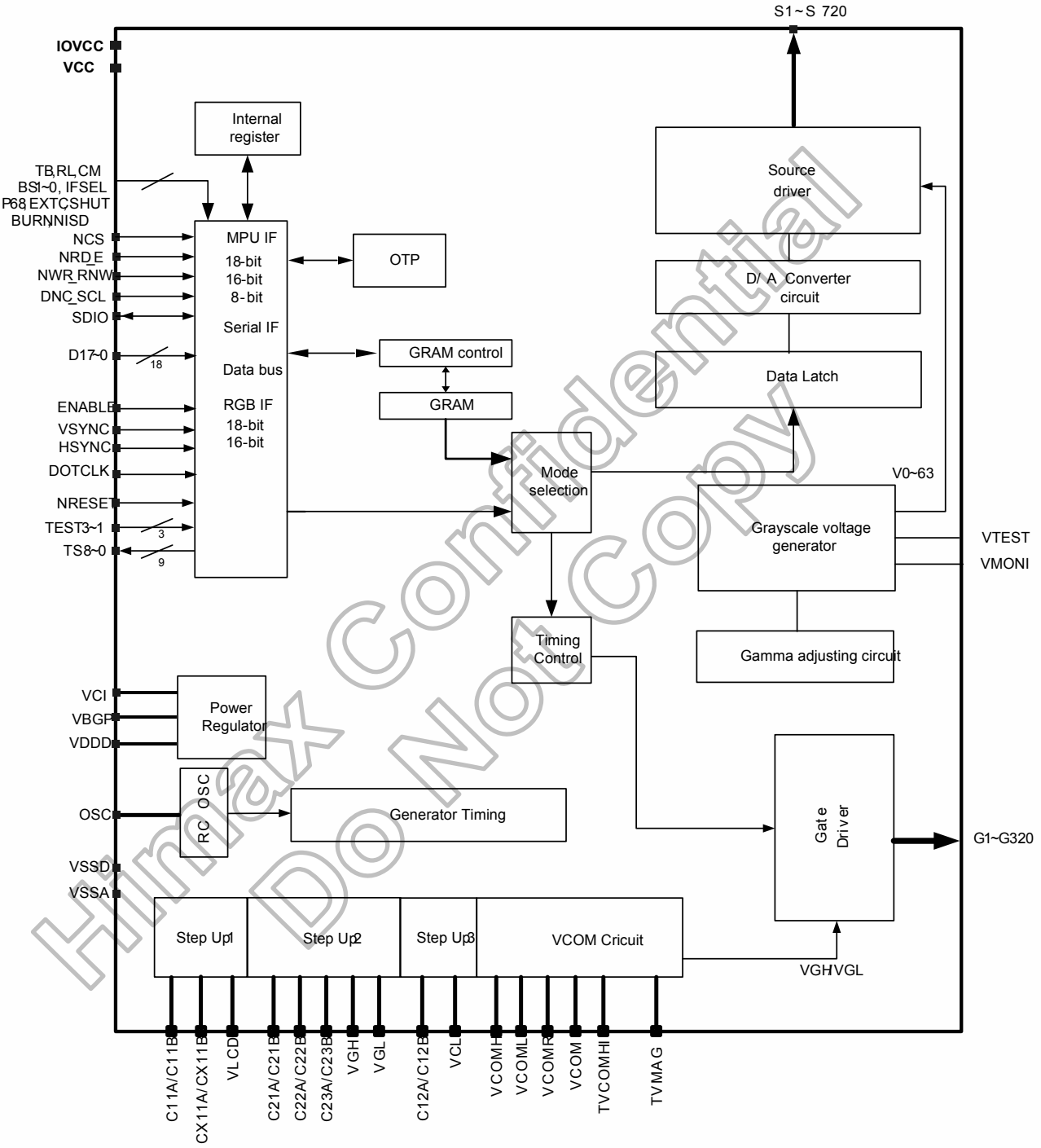
- Control Interface types supported
  - A. Register-Content interface mode. (IFSEL[1:0] = 2'b 01)
  - B. Hardware-Control interface mode. (IFSEL[1:0] = 2'b1X)

- Logic voltage (IOVCC): 1.65 ~ 3.3V
- Logic voltage (VCC): 2.3 ~ 3.3V
- Driver power supply (VCI): 2.3 ~ 3.3V
- Color modes
  - A. 16 bit/pixel: R(5), G(6), B(5)
  - B. 18 bit/pixel: R(6), G(6), B(6)
  - C. 12 bit/pixel: R(4), G(4), B(4)

2.4 Others

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -30 ~ +85 °C
- Suitable for all brand LCM module
  - Command set :**DMIF-S50AP-K12**
  - Hardware control pin
  - Himax defined command set
- Proprietary multi phase driving for lower power consumption
- Support external VDD for lower power consumption (such as 1.8 volts input)
- Support RGB through mode with lower power consumption
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (one-time-programming) non-volatile memory
- Shorter chip width (1.2mm)

3. Block Diagram



4. Pin Description

4.1 Pin Description

<table>
<tr><th colspan="6">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="2">Description</th></tr>
<tr><td rowspan="10">P68,BS2,
BS1,BS0</td><td rowspan="10">I</td><td rowspan="10">4</td><td rowspan="10">VSSD/
IOVCC</td><td colspan="2">Select the MPU interface mode as listed below
Use with IFSEL=2'b01 Register-content interface mode</td></tr>
<tr><td colspan="2"><table>
<tr><th>P68</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>Data pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 65K-Color</td><td>D24-D16:Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system, 262K-Color</td><td>D24-D16:Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface , 80-system, 262K-Color</td><td>D24-D18:Unused, D17-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 80-system, 262-Color</td><td>D24-D8:Unused, D7-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 65K-Color</td><td>D24-D16:Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system, 262K-Color</td><td>D24-D16:Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface , 68-system, 262K-Color</td><td>D24-D18:Unused, D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 68-system, 262K-Color</td><td>D24-D8:Unused, D7-D0: Data</td></tr>
<tr><td>x</td><td>1</td><td>1</td><td>ID</td><td>Serial bus IF</td><td>DNC_SCL, SDO,SDI</td></tr>
</table></td></tr>
<tr><td>IFSEL1,
IFSEL0</td><td>I</td><td>2</td><td>MPU</td><td colspan="2">Interface format select pin<table>
<tr><th>IFSEL1</th><th>IFSEL0</th><th>Interface Format Selection</th></tr>
<tr><td>0</td><td>1</td><td>Register-content interface mode</td></tr>
</table></td></tr>
<tr><td>EXTC
(IFSEL[1:0]=00)</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">I80 system: Serves as a write signal and writes data at the rising edge.
M68 system: 0: Write, 1: Read.
Fix it to IOVCC or VSSD level when using serial bus interface.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td colspan="2">I80 system: Serves as a read signal and read data at the low level.
M68 system: 0: Read/Write disable, 1: Read/Write enable.
Fix it to IOVCC or VSSD level when using serial bus interface.</td></tr>
</table>

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td>The signal for command or parameter select under parallel mode(i.e. Not serial bus interface):
Low: command.
High: parameter.
When under serial bus interface, it servers as SCL.
Under Index-content operates as RS.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level if unused (High active, if EPL=0).</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal. Has to be fixed to VSSD level if is not used.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>CM
(IFSEL[1:0]=1X)</td><td>I</td><td>1</td><td>MPU</td><td>Normal color mode and idle mode select pin only for Hardware control type. “Low” = Normal color
“High” = idle
When operate in other type, must be connected to VSSD or IOVCC.</td></tr>
<tr><td>SHUT
(IFSEL[1:0]=1X)</td><td>I</td><td>1</td><td>MPU</td><td>Power on/off select pin only for Hardware control type.
When operate in other type, must be connected to VSSD or IOVCC.</td></tr>
<tr><td>RL
(IFSEL[1:0]=1X)</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the source driver output data shift direction only for Hardware control type.
When operate in other type, must be connected to VSSD or IOVCC.
<table>
<tr><th>RL</th><th>Module source output direction</th></tr>
<tr><td>0</td><td>S1 -> S720</td></tr>
<tr><td>1</td><td>S720 -> S1</td></tr>
</table></td></tr>
<tr><td>TB
(IFSEL[1:0]=1X)</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the Gate driver scan direction only for Hardware control type.
When operate in other type, must be connected to VSSD or IOVCC.
<table>
<tr><th>TB</th><th>Module Gate output direction</th></tr>
<tr><td>0</td><td>G1 -> G320</td></tr>
<tr><td>1</td><td>G320 -> G1</td></tr>
</table></td></tr>
<tr><td>BGR_Panel</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the color mapping.
<table>
<tr><th>BGR_panel</th><th>Color mapping</th></tr>
<tr><td>0</td><td>R->G->B</td></tr>
<tr><td>1</td><td>B->G->R</td></tr>
</table></td></tr>
<tr><td>REV_Panel</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the display reversion.
<table>
<tr><th>REV_Panel</th><th>Mapping data</th></tr>
<tr><td>0</td><td>“0” to minimum pixel voltage for normal black pane</td></tr>
<tr><td>1</td><td>“0” to maximum pixel voltage for normal white pane</td></tr>
</table></td></tr>
<tr><td>GS_Panel</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the Gate driver scan direction on panel module. If not use, it must be connected to VSSD or IOVCC.
<table>
<tr><th>GS_Panel</th><th>Module Gate output direction</th></tr>
<tr><td>0</td><td>G1 -> G320</td></tr>
<tr><td>1</td><td>G320 -> G1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th colspan="4">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>SS_Panel</td><td>I</td><td>1</td><td>MPU</td><td>Input pin to select the Source driver scan direction on panel module.
<table><tr><th>SS_Panel</th><th>Module source output direction</th></tr><tr><td>0</td><td>S1 -> S720</td></tr><tr><td>1</td><td>S720 -> S1</td></tr></table></td></tr>
<tr><td>SM_Panel</td><td>I</td><td>1</td><td>MPU</td><td>Specify the scan order of gate driver.
<table><tr><th>SM_Panel</th><th>Scan direction</th></tr><tr><td>0</td><td>G1,G2,G3…G320
OR
G320, G319,G18,…G1</td></tr><tr><td>1</td><td>G1,G3, G5…G319, G2,G4,...,G320
OR
G320, G318,G316,…G2, G319, G317,…G1</td></tr></table></td></tr>
<tr><td>OSC</td><td>I</td><td>1</td><td>Oscillation Resistor</td><td>Oscillator input for test purpose.
If not used, please let it open or connected to VSSD.</td></tr>
<tr><td>VCOMR</td><td>I</td><td>1</td><td>Resistor or open</td><td>A VCOMH reference voltage. When adjusting VCOMH externally, set registers to halt the VCOMH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VCOMH by setting the internal register of the HX8346-A.</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td>Serial data input. If not used, please let it connected to IOVCC.</td></tr>
<tr><td>HSSP_EN</td><td>I</td><td>1</td><td>VSSD</td><td>Dummy pin, It must be connected to VSSD.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td>This pin can select the free running mode for burn in test.
The display data alternates between full black and full white independent of input data in free running mode.
Burn=L: Normal operation mode, Burn=H: Free running mode (Using internal oscillator)
If it is not used, let it open or connected to VSSD.(internal pull low)</td></tr>
<tr><td>HS_CLK_P</td><td>I</td><td>1</td><td>VSSD</td><td>Dummy pin, It must be connected to VSSD.</td></tr>
<tr><td>HS_CLK_N</td><td>I</td><td>1</td><td>VSSD</td><td>Dummy pin, It must be connected to VSSD.</td></tr>
<tr><td>HS_DA_P</td><td>I</td><td>1</td><td>VSSD</td><td>Dummy pin, It must be connected to VSSD.</td></tr>
<tr><td>HS_DA_N</td><td>I</td><td>1</td><td>VSSD</td><td>Dummy pin, It must be connected to VSSD.</td></tr>
<tr><td>REGVDD</td><td>I</td><td>1</td><td>MPU</td><td>If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. Must be connected to IOVCC or VSSD.</td></tr>
<tr><td>LED_FB</td><td>I</td><td>1</td><td>LED circuit</td><td>Backlight control feedback. If not used, please let it open or connected to VSSD.</td></tr>
</table>

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not use, let it to open.
SDO	O	1	MPU	Serial data output. If not use, let it to open.
FLM	O	1	Open	Frame pulse
PWM_OUT	O	1	LED circuit	Backlight On/Off control pin. Voltage rage = 0~ VCC. If not use, let it to open.
LED_SW	O	1	LED circuit	Backlight control output. If not use, let it to open.

<table>
<tr><th colspan="5">Input/Output Part</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>C11A,C11B
C12A,C12B</td><td>I/O</td><td>4</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.</td></tr>
<tr><td>CX11A, CX11B</td><td>I/O</td><td>2</td><td>Step-up Capacitor</td><td>Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.</td></tr>
<tr><td>C21A,C21B
C22A,C22B
C23A,C23B</td><td>I/O</td><td>6</td><td>Step-up Capacitor</td><td>Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.</td></tr>
<tr><td>D23~0</td><td>I/O</td><td>24</td><td>MPU</td><td>1. System interface
<table>
<tr><th>Data bus</th><th>Used</th><th>Unused</th></tr>
<tr><td>8-bit bus</td><td>D7-D0</td><td>D23-D8</td></tr>
<tr><td>16-bit bus</td><td>D15-D0</td><td>D23-D16</td></tr>
<tr><td>18-bit bus</td><td>D17-D0</td><td>D23-D18</td></tr>
</table>
2. RGB interface
<table>
<tr><th>Data bus</th><th>Used</th><th>Unused</th></tr>
<tr><td>16-bit bus</td><td>D21~17,
D13~8, D5~1</td><td>D23-22, D16
D15-14, D7-6, D0</td></tr>
<tr><td>18-bit bus</td><td>D21~16,
D13~8, D5~0</td><td>D23-22,
D15-14, D7-6</td></tr>
</table>
Connected unused pins to VSSD level.</td></tr>
</table>

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	1	Power Supply	Digital IO Pad power supply
VCI	P	1	Power Supply	Analog power supply
VCC	P	1	Power Supply	Digital circuit power supply
VCI2	O	1	Stabilizing Capacitor	Internal voltage for the step-up circuit 2.
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
VBGP	-	1	Open	Band Gap Voltage. Let it to be open.
VREG1	P	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREG3	P	1	Stabilizing Capacitor	A reference voltage for VGH&VGL.
VCOMH	P	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
VLCD	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and VLCD. Place a schotkey barrier diode (see “configuration of the power supply”).
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGH. Place a schottkey barrier diode between VCI and VGH. Place a schottkey barrier diode (see “configuration of the power supply”).
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”).
NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL, Source and VCOM would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.

Test pin and others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
PADA0, PADB0	I	2	MPU	Test pin for display glass break detection. If not used, please open these pins.
PADA1~ PADA4, PADB1~ PADB4	I	8	MPU	Test pin for chip attachment detection. If not used, please open these pins.
TEST3-1	I	3	GND	Test pin input (Internal pull low).
TS8~0	O	9	Open	A test pin. Disconnect it.
SO_TEST1~3	O	3	Open	A test pin.
VMONI	O	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must be left open.
TVCOMHI	O	1	Open	A test pin output. Must be left open.
TVMAG	O	1	Open	A test pin output. Must be left open.
DUMMYR1-10	-	10	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR10 are short-circuited within the chip. DUMMYR2 and DUMMYR9 are short-circuited within the chip. DUMMYR3 and DUMMYR4 are short-circuited within the chip. DUMMYR5 and DUMMYR6 are short-circuited within the chip. DUMMYR7 and DUMMYR8 are short-circuited within the chip.
DUMMY	-	16	Open	Dummy pads.

4.2 Pin assignment

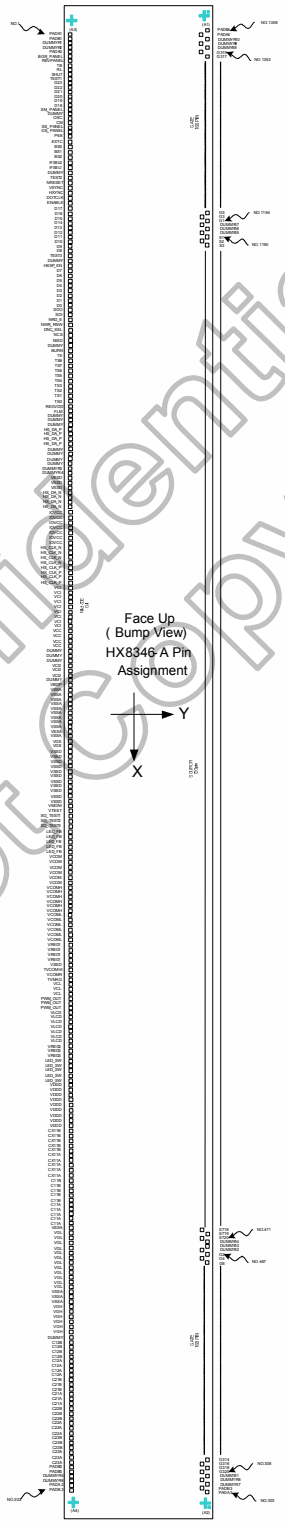
- Chip Size: 23020 x 1267 um
  Include seal ring 20 x 2 um
  Include scribe line 40 x 2 um
- Chip thickness300um
- Pad Location PAD Center
- Coordinate Origin Chip Center
- Au Bump Size

1. 28 um x120um
   Input:
   No. 1 to No.2 No. 301 to No.302

2. 50 um x120um
   Input:
   No. 3 to No.300

3. 20 um x96um
   Staggered LCD output side
   No. 303 to No. 1358

- The chip size includes the core size seal ring size and scribe line size
- Au bump pitch Refer to Pad Coordinate
- Au bump height 15um
- Numbers in the figure corresponds to pad coordinate numbers



4.3 PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	PADA1	-10498	-508.5	61	NRD_E	-6335	-508.5	121	VCI	-2135	-508.5	181	VCOMH	2065	-508.5
2	PADB1	-10454	-508.5	62	NWR_RNW	-6265	-508.5	122	VCI	-2065	-508.5	182	VCOMH	2135	-508.5
3	DUMMYR1	-10395	-508.5	63	DNC_SCL	-6195	-508.5	123	VCI	-1995	-508.5	183	VCOMH	2205	-508.5
4	DUMMYR2	-10325	-508.5	64	NCS	-6125	-508.5	124	VCC	-1925	-508.5	184	VCOMH	2275	-508.5
5	PADA0	-10255	-508.5	65	NISD	-6055	-508.5	125	VCC	-1855	-508.5	185	VCOML	2345	-508.5
6	BGR_PANEL	-10185	-508.5	66	DUMMY	-5985	-508.5	126	VCC	-1785	-508.5	186	VCOML	2415	-508.5
7	REV_PANEL	-10115	-508.5	67	BURN	-5915	-508.5	127	VCC	-1715	-508.5	187	VCOML	2485	-508.5
8	TB	-10045	-508.5	68	TE	-5845	-508.5	128	DUMMY	-1645	-508.5	188	VCOML	2555	-508.5
9	RL	-9975	-508.5	69	TS8	-5775	-508.5	129	DUMMY	-1575	-508.5	189	VCOML	2625	-508.5
10	SHUT	-9905	-508.5	70	TS7	-5705	-508.5	130	DUMMY	-1505	-508.5	190	VCOML	2695	-508.5
11	TEST1	-9835	-508.5	71	TS6	-5635	-508.5	131	VCI2	-1435	-508.5	191	VREG1	2765	-508.5
12	D23	-9765	-508.5	72	TS5	-5565	-508.5	132	VCI2	-1365	-508.5	192	VREG1	2835	-508.5
13	D22	-9695	-508.5	73	TS4	-5495	-508.5	133	VCI2	-1295	-508.5	193	VREG1	2905	-508.5
14	D21	-9625	-508.5	74	TS3	-5425	-508.5	134	DUMMY	-1225	-508.5	194	VREG1	2975	-508.5
15	D20	-9555	-508.5	75	TS2	-5355	-508.5	135	VBGP	-1155	-508.5	195	VSSD	3045	-508.5
16	D19	-9485	-508.5	76	TS1	-5285	-508.5	136	VSSA	-1085	-508.5	196	TVCOMHI	3115	-508.5
17	D18	-9415	-508.5	77	TS0	-5215	-508.5	137	VSSA	-1015	-508.5	197	VCOMR	3185	-508.5
18	SM_PANEL	-9345	-508.5	78	REGVDD	-5145	-508.5	138	VSSA	-945	-508.5	198	TVMAG	3255	-508.5
19	DUMMY	-9275	-508.5	79	FLM	-5075	-508.5	139	VSSA	-875	-508.5	199	VCL	3325	-508.5
20	OSC	-9205	-508.5	80	DUMMY	-5005	-508.5	140	VSSA	-805	-508.5	200	VCL	3395	-508.5
21	CM	-9135	-508.5	81	DUMMY	-4935	-508.5	141	VSSA	-735	-508.5	201	VCL	3465	-508.5
22	SS_PANEL	-9065	-508.5	82	DUMMY	-4865	-508.5	142	VSSA	-665	-508.5	202	PWM_OUT	3535	-508.5
23	GS_PANEL	-8995	-508.5	83	HS_DA_P	-4795	-508.5	143	VSSA	-595	-508.5	203	PWM_OUT	3605	-508.5
24	P68	-8925	-508.5	84	HS_DA_P	-4725	-508.5	144	VSSA	-525	-508.5	204	PWM_OUT	3675	-508.5
25	EXTC	-8855	-508.5	85	HS_DA_P	-4655	-508.5	145	VSSA	-455	-508.5	205	VLCD	3745	-508.5
26	BS0	-8785	-508.5	86	HS_DA_P	-4585	-508.5	146	VSSA	-385	-508.5	206	VLCD	3815	-508.5
27	BS1	-8715	-508.5	87	DUMMY	-4515	-508.5	147	VGS	-315	-508.5	207	VLCD	3885	-508.5
28	BS2	-8645	-508.5	88	DUMMY	-4445	-508.5	148	VGS	-245	-508.5	208	VLCD	3955	-508.5
29	IFSEL0	-8575	-508.5	89	DUMMY	-4375	-508.5	149	VSSD	-175	-508.5	209	VLCD	4025	-508.5
30	IFSEL1	-8505	-508.5	90	DUMMY	-4305	-508.5	150	VSSD	-105	-508.5	210	VLCD	4095	-508.5
31	DUMMY	-8435	-508.5	91	DUMMYR3	-4235	-508.5	151	VSSD	-35	-508.5	211	VLCD	4165	-508.5
32	TEST2	-8365	-508.5	92	DUMMYR4	-4165	-508.5	152	VSSD	35	-508.5	212	VREG3	4235	-508.5
33	NRESET	-8295	-508.5	93	VSSD	-4095	-508.5	153	VSSD	105	-508.5	213	VREG3	4305	-508.5
34	VSYNC	-8225	-508.5	94	VSSD	-4025	-508.5	154	VSSD	175	-508.5	214	VREG3	4375	-508.5
35	HSYNC	-8155	-508.5	95	VSSD	-3955	-508.5	155	VSSD	245	-508.5	215	LED_SW	4445	-508.5
36	DOTCLK	-8085	-508.5	96	HS_DA_N	-3885	-508.5	156	VSSD	315	-508.5	216	LED_SW	4515	-508.5
37	ENABLE	-8015	-508.5	97	HS_DA_N	-3815	-508.5	157	VSSD	385	-508.5	217	LED_SW	4585	-508.5
38	D17	-7945	-508.5	98	HS_DA_N	-3745	-508.5	158	VSSD	455	-508.5	218	LED_SW	4655	-508.5
39	D16	-7875	-508.5	99	HS_DA_N	-3675	-508.5	159	VSSD	525	-508.5	219	LED_SW	4725	-508.5
40	D15	-7805	-508.5	100	IOVCC	-3605	-508.5	160	VSSD	595	-508.5	220	VDDD	4795	-508.5
41	D14	-7735	-508.5	101	IOVCC	-3535	-508.5	161	VSSD	665	-508.5	221	VDDD	4865	-508.5
42	D13	-7665	-508.5	102	IOVCC	-3465	-508.5	162	VSSD	735	-508.5	222	VDDD	4935	-508.5
43	D12	-7595	-508.5	103	IOVCC	-3395	-508.5	163	VMONI	805	-508.5	223	VDDD	5005	-508.5
44	D11	-7525	-508.5	104	IOVCC	-3325	-508.5	164	VTEST	875	-508.5	224	VDDD	5075	-508.5
45	D10	-7455	-508.5	105	IOVCC	-3255	-508.5	165	SO_TEST1	945	-508.5	225	VDDD	5145	-508.5
46	D9	-7385	-508.5	106	IOVCC	-3185	-508.5	166	SO_TEST2	1015	-508.5	226	VDDD	5215	-508.5
47	D8	-7315	-508.5	107	HS_CLK_N	-3115	-508.5	167	SO_TEST3	1085	-508.5	227	VDDD	5285	-508.5
48	TEST3	-7245	-508.5	108	HS_CLK_N	-3045	-508.5	168	LED_FB	1155	-508.5	228	VDDD	5355	-508.5
49	DUMMY	-7175	-508.5	109	HS_CLK_N	-2975	-508.5	169	LED_FB	1225	-508.5	229	C11BX	5425	-508.5
50	HSSP_EN	-7105	-508.5	110	HS_CLK_N	-2905	-508.5	170	LED_FB	1295	-508.5	230	C11BX	5495	-508.5
51	D7	-7035	-508.5	111	HS_CLK_P	-2835	-508.5	171	LED_FB	1365	-508.5	231	C11BX	5565	-508.5
52	D6	-6965	-508.5	112	HS_CLK_P	-2765	-508.5	172	LED_FB	1435	-508.5	232	C11BX	5635	-508.5
53	D5	-6895	-508.5	113	HS_CLK_P	-2695	-508.5	173	VCOM	1505	-508.5	233	C11BX	5705	-508.5
54	D4	-6825	-508.5	114	HS_CLK_P	-2625	-508.5	174	VCOM	1575	-508.5	234	C11AX	5775	-508.5
55	D3	-6755	-508.5	115	VCI	-2555	-508.5	175	VCOM	1645	-508.5	235	C11AX	5845	-508.5
56	D2	-6685	-508.5	116	VCI	-2485	-508.5	176	VCOM	1715	-508.5	236	C11AX	5915	-508.5
57	D1	-6615	-508.5	117	VCI	-2415	-508.5	177	VCOM	1785	-508.5	237	C11AX	5985	-508.5
58	D0	-6545	-508.5	118	VCI	-2345	-508.5	178	VCOM	1855	-508.5	238	C11AX	6055	-508.5
59	SDO	-6475	-508.5	119	VCI	-2275	-508.5	179	VCOMH	1925	-508.5	239	C11B	6125	-508.5
60	SDI	-6405	-508.5	120	VCI	-2205	-508.5	180	VCOMH	1995	-508.5	240	C11B	6195	-508.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
241	C11B	6265	-508.5	301	PADA2	10454	-508.5	361	G214	9510	520.5	421	G94	8310	520.5
242	C11B	6335	-508.5	302	PADB2	10498	-508.5	362	G212	9490	395.5	422	G92	8290	395.5
243	C11B	6405	-508.5	303	PADA3	10670	520.5	363	G210	9470	520.5	423	G90	8270	520.5
244	C11A	6475	-508.5	304	PADB3	10650	395.5	364	G208	9450	395.5	424	G88	8250	395.5
245	C11A	6545	-508.5	305	DUMMYR7	10630	520.5	365	G206	9430	520.5	425	G86	8230	520.5
246	C11A	6615	-508.5	306	DUMMYR8	10610	395.5	366	G204	9410	395.5	426	G84	8210	395.5
247	C11A	6685	-508.5	307	DUMMY51	10590	520.5	367	G202	9390	520.5	427	G82	8190	520.5
248	C11A	6755	-508.5	308	G320	10570	395.5	368	G200	9370	395.5	428	G80	8170	395.5
249	VSSA	6825	-508.5	309	G318	10550	520.5	369	G198	9350	520.5	429	G78	8150	520.5
250	VGL	6895	-508.5	310	G316	10530	395.5	370	G196	9330	395.5	430	G76	8130	395.5
251	VGL	6965	-508.5	311	G314	10510	520.5	371	G194	9310	520.5	431	G74	8110	520.5
252	VGL	7035	-508.5	312	G312	10490	395.5	372	G192	9290	395.5	432	G72	8090	395.5
253	VGL	7105	-508.5	313	G310	10470	520.5	373	G190	9270	520.5	433	G70	8070	520.5
254	VGL	7175	-508.5	314	G308	10450	395.5	374	G188	9250	395.5	434	G68	8050	395.5
255	VGL	7245	-508.5	315	G306	10430	520.5	375	G186	9230	520.5	435	G66	8030	520.5
256	VGL	7315	-508.5	316	G304	10410	395.5	376	G184	9210	395.5	436	G64	8010	395.5
257	VGL	7385	-508.5	317	G302	10390	520.5	377	G182	9190	520.5	437	G62	7990	520.5
258	VGL	7455	-508.5	318	G300	10370	395.5	378	G180	9170	395.5	438	G60	7970	395.5
259	VGL	7525	-508.5	319	G298	10350	520.5	379	G178	9150	520.5	439	G58	7950	520.5
260	VGL	7595	-508.5	320	G296	10330	395.5	380	G176	9130	395.5	440	G56	7930	395.5
261	VGL	7665	-508.5	321	G294	10310	520.5	381	G174	9110	520.5	441	G54	7910	520.5
262	VSSA	7735	-508.5	322	G292	10290	395.5	382	G172	9090	395.5	442	G52	7890	395.5
263	VSSA	7805	-508.5	323	G290	10270	520.5	383	G170	9070	520.5	443	G50	7870	520.5
264	VSSA	7875	-508.5	324	G288	10250	395.5	384	G168	9050	395.5	444	G48	7850	395.5
265	VGH	7945	-508.5	325	G286	10230	520.5	385	G166	9030	520.5	445	G46	7830	520.5
266	VGH	8015	-508.5	326	G284	10210	395.5	386	G164	9010	395.5	446	G44	7810	395.5
267	VGH	8085	-508.5	327	G282	10190	520.5	387	G162	8990	520.5	447	G42	7790	520.5
268	VGH	8155	-508.5	328	G280	10170	395.5	388	G160	8970	395.5	448	G40	7770	395.5
269	VGH	8225	-508.5	329	G278	10150	520.5	389	G158	8950	520.5	449	G38	7750	520.5
270	VGH	8295	-508.5	330	G276	10130	395.5	390	G156	8930	395.5	450	G36	7730	395.5
271	DUMMY	8365	-508.5	331	G274	10110	520.5	391	G154	8910	520.5	451	G34	7710	520.5
272	C12B	8435	-508.5	332	G272	10090	395.5	392	G152	8890	395.5	452	G32	7690	395.5
273	C12B	8505	-508.5	333	G270	10070	520.5	393	G150	8870	520.5	453	G30	7670	520.5
274	C12B	8575	-508.5	334	G268	10050	395.5	394	G148	8850	395.5	454	G28	7650	395.5
275	C12B	8645	-508.5	335	G266	10030	520.5	395	G146	8830	520.5	455	G26	7630	520.5
276	C12A	8715	-508.5	336	G264	10010	395.5	396	G144	8810	395.5	456	G24	7610	395.5
277	C12A	8785	-508.5	337	G262	9990	520.5	397	G142	8790	520.5	457	G22	7590	520.5
278	C12A	8855	-508.5	338	G260	9970	395.5	398	G140	8770	395.5	458	G20	7570	395.5
279	C12A	8925	-508.5	339	G258	9950	520.5	399	G138	8750	520.5	459	G18	7550	520.5
280	C21B	8995	-508.5	340	G256	9930	395.5	400	G136	8730	395.5	460	G16	7530	395.5
281	C21B	9065	-508.5	341	G254	9910	520.5	401	G134	8710	520.5	461	G14	7510	520.5
282	C21B	9135	-508.5	342	G252	9890	395.5	402	G132	8690	395.5	462	G12	7490	395.5
283	C21A	9205	-508.5	343	G250	9870	520.5	403	G130	8670	520.5	463	G10	7470	520.5
284	C21A	9275	-508.5	344	G248	9850	395.5	404	G128	8650	395.5	464	G8	7450	395.5
285	C21A	9345	-508.5	345	G246	9830	520.5	405	G126	8630	520.5	465	G6	7430	520.5
286	C22B	9415	-508.5	346	G244	9810	395.5	406	G124	8610	395.5	466	G4	7410	395.5
287	C22B	9485	-508.5	347	G242	9790	520.5	407	G122	8590	520.5	467	G2	7390	520.5
288	C22B	9555	-508.5	348	G240	9770	395.5	408	G120	8570	395.5	468	DUMMY52	7370	395.5
289	C22A	9625	-508.5	349	G238	9750	520.5	409	G118	8550	520.5	469	DUMMY53	7350	520.5
290	C22A	9695	-508.5	350	G236	9730	395.5	410	G116	8530	395.5	470	DUMMY54	7130	520.5
291	C22A	9765	-508.5	351	G234	9710	520.5	411	G114	8510	520.5	471	S720	7110	395.5
292	C23B	9835	-508.5	352	G232	9690	395.5	412	G112	8490	395.5	472	S719	7090	520.5
293	C23B	9905	-508.5	353	G230	9670	520.5	413	G110	8470	520.5	473	S718	7070	395.5
294	C23B	9975	-508.5	354	G228	9650	395.5	414	G108	8450	395.5	474	S717	7050	520.5
295	C23A	10045	-508.5	355	G226	9630	520.5	415	G106	8430	520.5	475	S716	7030	395.5
296	C23A	10115	-508.5	356	G224	9610	395.5	416	G104	8410	395.5	476	S715	7010	520.5
297	C23A	10185	-508.5	357	G222	9590	520.5	417	G102	8390	520.5	477	S714	6990	395.5
298	PADB0	10255	-508.5	358	G220	9570	395.5	418	G100	8370	395.5	478	S713	6970	520.5
299	DUMMYR5	10325	-508.5	359	G218	9550	520.5	419	G98	8350	520.5	479	S712	6950	395.5
300	DUMMYR6	10395	-508.5	360	G216	9530	395.5	420	G96	8330	395.5	480	S711	6930	520.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
481	S710	6910	395.5	541	S650	5710	395.5	601	S590	4510	395.5	661	S530	3310	395.5
482	S709	6890	520.5	542	S649	5690	520.5	602	S589	4490	520.5	662	S529	3290	520.5
483	S708	6870	395.5	543	S648	5670	395.5	603	S588	4470	395.5	663	S528	3270	395.5
484	S707	6850	520.5	544	S647	5650	520.5	604	S587	4450	520.5	664	S527	3250	520.5
485	S706	6830	395.5	545	S646	5630	395.5	605	S586	4430	395.5	665	S526	3230	395.5
486	S705	6810	520.5	546	S645	5610	520.5	606	S585	4410	520.5	666	S525	3210	520.5
487	S704	6790	395.5	547	S644	5590	395.5	607	S584	4390	395.5	667	S524	3190	395.5
488	S703	6770	520.5	548	S643	5570	520.5	608	S583	4370	520.5	668	S523	3170	520.5
489	S702	6750	395.5	549	S642	5550	395.5	609	S582	4350	395.5	669	S522	3150	395.5
490	S701	6730	520.5	550	S641	5530	520.5	610	S581	4330	520.5	670	S521	3130	520.5
491	S700	6710	395.5	551	S640	5510	395.5	611	S580	4310	395.5	671	S520	3110	395.5
492	S699	6690	520.5	552	S639	5490	520.5	612	S579	4290	520.5	672	S519	3090	520.5
493	S698	6670	395.5	553	S638	5470	395.5	613	S578	4270	395.5	673	S518	3070	395.5
494	S697	6650	520.5	554	S637	5450	520.5	614	S577	4250	520.5	674	S517	3050	520.5
495	S696	6630	395.5	555	S636	5430	395.5	615	S576	4230	395.5	675	S516	3030	395.5
496	S695	6610	520.5	556	S635	5410	520.5	616	S575	4210	520.5	676	S515	3010	520.5
497	S694	6590	395.5	557	S634	5390	395.5	617	S574	4190	395.5	677	S514	2990	395.5
498	S693	6570	520.5	558	S633	5370	520.5	618	S573	4170	520.5	678	S513	2970	520.5
499	S692	6550	395.5	559	S632	5350	395.5	619	S572	4150	395.5	679	S512	2950	395.5
500	S691	6530	520.5	560	S631	5330	520.5	620	S571	4130	520.5	680	S511	2930	520.5
501	S690	6510	395.5	561	S630	5310	395.5	621	S570	4110	395.5	681	S510	2910	395.5
502	S689	6490	520.5	562	S629	5290	520.5	622	S569	4090	520.5	682	S509	2890	520.5
503	S688	6470	395.5	563	S628	5270	395.5	623	S568	4070	395.5	683	S508	2870	395.5
504	S687	6450	520.5	564	S627	5250	520.5	624	S567	4050	520.5	684	S507	2850	520.5
505	S686	6430	395.5	565	S626	5230	395.5	625	S566	4030	395.5	685	S506	2830	395.5
506	S685	6410	520.5	566	S625	5210	520.5	626	S565	4010	520.5	686	S505	2810	520.5
507	S684	6390	395.5	567	S624	5190	395.5	627	S564	3990	395.5	687	S504	2790	395.5
508	S683	6370	520.5	568	S623	5170	520.5	628	S563	3970	520.5	688	S503	2770	520.5
509	S682	6350	395.5	569	S622	5150	395.5	629	S562	3950	395.5	689	S502	2750	395.5
510	S681	6330	520.5	570	S621	5130	520.5	630	S561	3930	520.5	690	S501	2730	520.5
511	S680	6310	395.5	571	S620	5110	395.5	631	S560	3910	395.5	691	S500	2710	395.5
512	S679	6290	520.5	572	S619	5090	520.5	632	S559	3890	520.5	692	S499	2690	520.5
513	S678	6270	395.5	573	S618	5070	395.5	633	S558	3870	395.5	693	S498	2670	395.5
514	S677	6250	520.5	574	S617	5050	520.5	634	S557	3850	520.5	694	S497	2650	520.5
515	S676	6230	395.5	575	S616	5030	395.5	635	S556	3830	395.5	695	S496	2630	395.5
516	S675	6210	520.5	576	S615	5010	520.5	636	S555	3810	520.5	696	S495	2610	520.5
517	S674	6190	395.5	577	S614	4990	395.5	637	S554	3790	395.5	697	S494	2590	395.5
518	S673	6170	520.5	578	S613	4970	520.5	638	S553	3770	520.5	698	S493	2570	520.5
519	S672	6150	395.5	579	S612	4950	395.5	639	S552	3750	395.5	699	S492	2550	395.5
520	S671	6130	520.5	580	S611	4930	520.5	640	S551	3730	520.5	700	S491	2530	520.5
521	S670	6110	395.5	581	S610	4910	395.5	641	S550	3710	395.5	701	S490	2510	395.5
522	S669	6090	520.5	582	S609	4890	520.5	642	S549	3690	520.5	702	S489	2490	520.5
523	S668	6070	395.5	583	S608	4870	395.5	643	S548	3670	395.5	703	S488	2470	395.5
524	S667	6050	520.5	584	S607	4850	520.5	644	S547	3650	520.5	704	S487	2450	520.5
525	S666	6030	395.5	585	S606	4830	395.5	645	S546	3630	395.5	705	S486	2430	395.5
526	S665	6010	520.5	586	S605	4810	520.5	646	S545	3610	520.5	706	S485	2410	520.5
527	S664	5990	395.5	587	S604	4790	395.5	647	S544	3590	395.5	707	S484	2390	395.5
528	S663	5970	520.5	588	S603	4770	520.5	648	S543	3570	520.5	708	S483	2370	520.5
529	S662	5950	395.5	589	S602	4750	395.5	649	S542	3550	395.5	709	S482	2350	395.5
530	S661	5930	520.5	590	S601	4730	520.5	650	S541	3530	520.5	710	S481	2330	520.5
531	S660	5910	395.5	591	S600	4710	395.5	651	S540	3510	395.5	711	S480	2310	395.5
532	S659	5890	520.5	592	S599	4690	520.5	652	S539	3490	520.5	712	S479	2290	520.5
533	S658	5870	395.5	593	S598	4670	395.5	653	S538	3470	395.5	713	S478	2270	395.5
534	S657	5850	520.5	594	S597	4650	520.5	654	S537	3450	520.5	714	S477	2250	520.5
535	S656	5830	395.5	595	S596	4630	395.5	655	S536	3430	395.5	715	S476	2230	395.5
536	S655	5810	520.5	596	S595	4610	520.5	656	S535	3410	520.5	716	S475	2210	520.5
537	S654	5790	395.5	597	S594	4590	395.5	657	S534	3390	395.5	717	S474	2190	395.5
538	S653	5770	520.5	598	S593	4570	520.5	658	S533	3370	520.5	718	S473	2170	520.5
539	S652	5750	395.5	599	S592	4550	395.5	659	S532	3350	395.5	719	S472	2150	395.5
540	S651	5730	520.5	600	S591	4530	520.5	660	S531	3330	520.5	720	S471	2130	520.5

No.	Pad name	X	Y
721	S470	2110	395.5
722	S469	2090	520.5
723	S468	2070	395.5
724	S467	2050	520.5
725	S466	2030	395.5
726	S465	2010	520.5
727	S464	1990	395.5
728	S463	1970	520.5
729	S462	1950	395.5
730	S461	1930	520.5
731	S460	1910	395.5
732	S459	1890	520.5
733	S458	1870	395.5
734	S457	1850	520.5
735	S456	1830	395.5
736	S455	1810	520.5
737	S454	1790	395.5
738	S453	1770	520.5
739	S452	1750	395.5
740	S451	1730	520.5
741	S450	1710	395.5
742	S449	1690	520.5
743	S448	1670	395.5
744	S447	1650	520.5
745	S446	1630	395.5
746	S445	1610	520.5
747	S444	1590	395.5
748	S443	1570	520.5
749	S442	1550	395.5
750	S441	1530	520.5
751	S440	1510	395.5
752	S439	1490	520.5
753	S438	1470	395.5
754	S437	1450	520.5
755	S436	1430	395.5
756	S435	1410	520.5
757	S434	1390	395.5
758	S433	1370	520.5
759	S432	1350	395.5
760	S431	1330	520.5
761	S430	1310	395.5
762	S429	1290	520.5
763	S428	1270	395.5
764	S427	1250	520.5
765	S426	1230	395.5
766	S425	1210	520.5
767	S424	1190	395.5
768	S423	1170	520.5
769	S422	1150	395.5
770	S421	1130	520.5
771	S420	1110	395.5
772	S419	1090	520.5
773	S418	1070	395.5
774	S417	1050	520.5
775	S416	1030	395.5
776	S415	1010	520.5
777	S414	990	395.5
778	S413	970	520.5
779	S412	950	395.5
780	S411	930	520.5

No.	Pad name	X	Y
781	S410	910	395.5
782	S409	890	520.5
783	S408	870	395.5
784	S407	850	520.5
785	S406	830	395.5
786	S405	810	520.5
787	S404	790	395.5
788	S403	770	520.5
789	S402	750	395.5
790	S401	730	520.5
791	S400	710	395.5
792	S399	690	520.5
793	S398	670	395.5
794	S397	650	520.5
795	S396	630	395.5
796	S395	610	520.5
797	S394	590	395.5
798	S393	570	520.5
799	S392	550	395.5
800	S391	530	520.5
801	S390	510	395.5
802	S389	490	520.5
803	S388	470	395.5
804	S387	450	520.5
805	S386	430	395.5
806	S385	410	520.5
807	S384	390	395.5
808	S383	370	520.5
809	S382	350	395.5
810	S381	330	520.5
811	S380	310	395.5
812	S379	290	520.5
813	S378	270	395.5
814	S377	250	520.5
815	S376	230	395.5
816	S375	210	520.5
817	S374	190	395.5
818	S373	170	520.5
819	S372	150	395.5
820	S371	130	520.5
821	S370	110	395.5
822	S369	90	520.5
823	S368	70	395.5
824	S367	50	520.5
825	S366	30	395.5
826	S365	10	520.5
827	S364	-10	395.5
828	S363	-30	520.5
829	S362	-50	395.5
830	S361	-70	520.5
831	S360	-90	395.5
832	S359	-110	520.5
833	S358	-130	395.5
834	S357	-150	520.5
835	S356	-170	395.5
836	S355	-190	520.5
837	S354	-210	395.5
838	S353	-230	520.5
839	S352	-250	395.5
840	S351	-270	520.5

No.	Pad name	X	Y
841	S350	-290	395.5
842	S349	-310	520.5
843	S348	-330	395.5
844	S347	-350	520.5
845	S346	-370	395.5
846	S345	-390	520.5
847	S344	-410	395.5
848	S343	-430	520.5
849	S342	-450	395.5
850	S341	-470	520.5
851	S340	-490	395.5
852	S339	-510	520.5
853	S338	-530	395.5
854	S337	-550	520.5
855	S336	-570	395.5
856	S335	-590	520.5
857	S334	-610	395.5
858	S333	-630	520.5
859	S332	-650	395.5
860	S331	-670	520.5
861	S330	-690	395.5
862	S329	-710	520.5
863	S328	-730	395.5
864	S327	-750	520.5
865	S326	-770	395.5
866	S325	-790	520.5
867	S324	-810	395.5
868	S323	-830	520.5
869	S322	-850	395.5
870	S321	-870	520.5
871	S320	-890	395.5
872	S319	-910	520.5
873	S318	-930	395.5
874	S317	-950	520.5
875	S316	-970	395.5
876	S315	-990	520.5
877	S314	-1010	395.5
878	S313	-1030	520.5
879	S312	-1050	395.5
880	S311	-1070	520.5
881	S310	-1090	395.5
882	S309	-1110	520.5
883	S308	-1130	395.5
884	S307	-1150	520.5
885	S306	-1170	395.5
886	S305	-1190	520.5
887	S304	-1210	395.5
888	S303	-1230	520.5
889	S302	-1250	395.5
890	S301	-1270	520.5
891	S300	-1290	395.5
892	S299	-1310	520.5
893	S298	-1330	395.5
894	S297	-1350	520.5
895	S296	-1370	395.5
896	S295	-1390	520.5
897	S294	-1410	395.5
898	S293	-1430	520.5
899	S292	-1450	395.5
900	S291	-1470	520.5

No.	Pad name	X	Y
901	S290	-1490	395.5
902	S289	-1510	520.5
903	S288	-1530	395.5
904	S287	-1550	520.5
905	S286	-1570	395.5
906	S285	-1590	520.5
907	S284	-1610	395.5
908	S283	-1630	520.5
909	S282	-1650	395.5
910	S281	-1670	520.5
911	S280	-1690	395.5
912	S279	-1710	520.5
913	S278	-1730	395.5
914	S277	-1750	520.5
915	S276	-1770	395.5
916	S275	-1790	520.5
917	S274	-1810	395.5
918	S273	-1830	520.5
919	S272	-1850	395.5
920	S271	-1870	520.5
921	S270	-1890	395.5
922	S269	-1910	520.5
923	S268	-1930	395.5
924	S267	-1950	520.5
925	S266	-1970	395.5
926	S265	-1990	520.5
927	S264	-2010	395.5
928	S263	-2030	520.5
929	S262	-2050	395.5
930	S261	-2070	520.5
931	S260	-2090	395.5
932	S259	-2110	520.5
933	S258	-2130	395.5
934	S257	-2150	520.5
935	S256	-2170	395.5
936	S255	-2190	520.5
937	S254	-2210	395.5
938	S253	-2230	520.5
939	S252	-2250	395.5
940	S251	-2270	520.5
941	S250	-2290	395.5
942	S249	-2310	520.5
943	S248	-2330	395.5
944	S247	-2350	520.5
945	S246	-2370	395.5
946	S245	-2390	520.5
947	S244	-2410	395.5
948	S243	-2430	520.5
949	S242	-2450	395.5
950	S241	-2470	520.5
951	S240	-2490	395.5
952	S239	-2510	520.5
953	S238	-2530	395.5
954	S237	-2550	520.5
955	S236	-2570	395.5
956	S235	-2590	520.5
957	S234	-2610	395.5
958	S233	-2630	520.5
959	S232	-2650	395.5
960	S231	-2670	520.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
961	S230	-2690	395.5	1021	S170	-3890	395.5	1081	S110	-5090	395.5	1141	S50	-6290	395.5
962	S229	-2710	520.5	1022	S169	-3910	520.5	1082	S109	-5110	520.5	1142	S49	-6310	520.5
963	S228	-2730	395.5	1023	S168	-3930	395.5	1083	S108	-5130	395.5	1143	S48	-6330	395.5
964	S227	-2750	520.5	1024	S167	-3950	520.5	1084	S107	-5150	520.5	1144	S47	-6350	520.5
965	S226	-2770	395.5	1025	S166	-3970	395.5	1085	S106	-5170	395.5	1145	S46	-6370	395.5
966	S225	-2790	520.5	1026	S165	-3990	520.5	1086	S105	-5190	520.5	1146	S45	-6390	520.5
967	S224	-2810	395.5	1027	S164	-4010	395.5	1087	S104	-5210	395.5	1147	S44	-6410	395.5
968	S223	-2830	520.5	1028	S163	-4030	520.5	1088	S103	-5230	520.5	1148	S43	-6430	520.5
969	S222	-2850	395.5	1029	S162	-4050	395.5	1089	S102	-5250	395.5	1149	S42	-6450	395.5
970	S221	-2870	520.5	1030	S161	-4070	520.5	1090	S101	-5270	520.5	1150	S41	-6470	520.5
971	S220	-2890	395.5	1031	S160	-4090	395.5	1091	S100	-5290	395.5	1151	S40	-6490	395.5
972	S219	-2910	520.5	1032	S159	-4110	520.5	1092	S99	-5310	520.5	1152	S39	-6510	520.5
973	S218	-2930	395.5	1033	S158	-4130	395.5	1093	S98	-5330	395.5	1153	S38	-6530	395.5
974	S217	-2950	520.5	1034	S157	-4150	520.5	1094	S97	-5350	520.5	1154	S37	-6550	520.5
975	S216	-2970	395.5	1035	S156	-4170	395.5	1095	S96	-5370	395.5	1155	S36	-6570	395.5
976	S215	-2990	520.5	1036	S155	-4190	520.5	1096	S95	-5390	520.5	1156	S35	-6590	520.5
977	S214	-3010	395.5	1037	S154	-4210	395.5	1097	S94	-5410	395.5	1157	S34	-6610	395.5
978	S213	-3030	520.5	1038	S153	-4230	520.5	1098	S93	-5430	520.5	1158	S33	-6630	520.5
979	S212	-3050	395.5	1039	S152	-4250	395.5	1099	S92	-5450	395.5	1159	S32	-6650	395.5
980	S211	-3070	520.5	1040	S151	-4270	520.5	1100	S91	-5470	520.5	1160	S31	-6670	520.5
981	S210	-3090	395.5	1041	S150	-4290	395.5	1101	S90	-5490	395.5	1161	S30	-6690	395.5
982	S209	-3110	520.5	1042	S149	-4310	520.5	1102	S89	-5510	520.5	1162	S29	-6710	520.5
983	S208	-3130	395.5	1043	S148	-4330	395.5	1103	S88	-5530	395.5	1163	S28	-6730	395.5
984	S207	-3150	520.5	1044	S147	-4350	520.5	1104	S87	-5550	520.5	1164	S27	-6750	520.5
985	S206	-3170	395.5	1045	S146	-4370	395.5	1105	S86	-5570	395.5	1165	S26	-6770	395.5
986	S205	-3190	520.5	1046	S145	-4390	520.5	1106	S85	-5590	520.5	1166	S25	-6790	520.5
987	S204	-3210	395.5	1047	S144	-4410	395.5	1107	S84	-5610	395.5	1167	S24	-6810	395.5
988	S203	-3230	520.5	1048	S143	-4430	520.5	1108	S83	-5630	520.5	1168	S23	-6830	520.5
989	S202	-3250	395.5	1049	S142	-4450	395.5	1109	S82	-5650	395.5	1169	S22	-6850	395.5
990	S201	-3270	520.5	1050	S141	-4470	520.5	1110	S81	-5670	520.5	1170	S21	-6870	520.5
991	S200	-3290	395.5	1051	S140	-4490	395.5	1111	S80	-5690	395.5	1171	S20	-6890	395.5
992	S199	-3310	520.5	1052	S139	-4510	520.5	1112	S79	-5710	520.5	1172	S19	-6910	520.5
993	S198	-3330	395.5	1053	S138	-4530	395.5	1113	S78	-5730	395.5	1173	S18	-6930	395.5
994	S197	-3350	520.5	1054	S137	-4550	520.5	1114	S77	-5750	520.5	1174	S17	-6950	520.5
995	S196	-3370	395.5	1055	S136	-4570	395.5	1115	S76	-5770	395.5	1175	S16	-6970	395.5
996	S195	-3390	520.5	1056	S135	-4590	520.5	1116	S75	-5790	520.5	1176	S15	-6990	520.5
997	S194	-3410	395.5	1057	S134	-4610	395.5	1117	S74	-5810	395.5	1177	S14	-7010	395.5
998	S193	-3430	520.5	1058	S133	-4630	520.5	1118	S73	-5830	520.5	1178	S13	-7030	520.5
999	S192	-3450	395.5	1059	S132	-4650	395.5	1119	S72	-5850	395.5	1179	S12	-7050	395.5
1000	S191	-3470	520.5	1060	S131	-4670	520.5	1120	S71	-5870	520.5	1180	S11	-7070	520.5
1001	S190	-3490	395.5	1061	S130	-4690	395.5	1121	S70	-5890	395.5	1181	S10	-7090	395.5
1002	S189	-3510	520.5	1062	S129	-4710	520.5	1122	S69	-5910	520.5	1182	S9	-7110	520.5
1003	S188	-3530	395.5	1063	S128	-4730	395.5	1123	S68	-5930	395.5	1183	S8	-7130	395.5
1004	S187	-3550	520.5	1064	S127	-4750	520.5	1124	S67	-5950	520.5	1184	S7	-7150	520.5
1005	S186	-3570	395.5	1065	S126	-4770	395.5	1125	S66	-5970	395.5	1185	S6	-7170	395.5
1006	S185	-3590	520.5	1066	S125	-4790	520.5	1126	S65	-5990	520.5	1186	S5	-7190	520.5
1007	S184	-3610	395.5	1067	S124	-4810	395.5	1127	S64	-6010	395.5	1187	S4	-7210	395.5
1008	S183	-3630	520.5	1068	S123	-4830	520.5	1128	S63	-6030	520.5	1188	S3	-7230	520.5
1009	S182	-3650	395.5	1069	S122	-4850	395.5	1129	S62	-6050	395.5	1189	S2	-7250	395.5
1010	S181	-3670	520.5	1070	S121	-4870	520.5	1130	S61	-6070	520.5	1190	S1	-7270	520.5
1011	S180	-3690	395.5	1071	S120	-4890	395.5	1131	S60	-6090	395.5	1191	DUMMY55	-7290	395.5
1012	S179	-3710	520.5	1072	S119	-4910	520.5	1132	S59	-6110	520.5	1192	DUMMY56	-7350	520.5
1013	S178	-3730	395.5	1073	S118	-4930	395.5	1133	S58	-6130	395.5	1193	DUMMY57	-7370	395.5
1014	S177	-3750	520.5	1074	S117	-4950	520.5	1134	S57	-6150	520.5	1194	G1	-7390	520.5
1015	S176	-3770	395.5	1075	S116	-4970	395.5	1135	S56	-6170	395.5	1195	G3	-7410	395.5
1016	S175	-3790	520.5	1076	S115	-4990	520.5	1136	S55	-6190	520.5	1196	G5	-7430	520.5
1017	S174	-3810	395.5	1077	S114	-5010	395.5	1137	S54	-6210	395.5	1197	G7	-7450	395.5
1018	S173	-3830	520.5	1078	S113	-5030	520.5	1138	S53	-6230	520.5	1198	G9	-7470	520.5
1019	S172	-3850	395.5	1079	S112	-5050	395.5	1139	S52	-6250	395.5	1199	G11	-7490	395.5
1020	S171	-3870	520.5	1080	S111	-5070	520.5	1140	S51	-6270	520.5	1200	G13	-7510	520.5

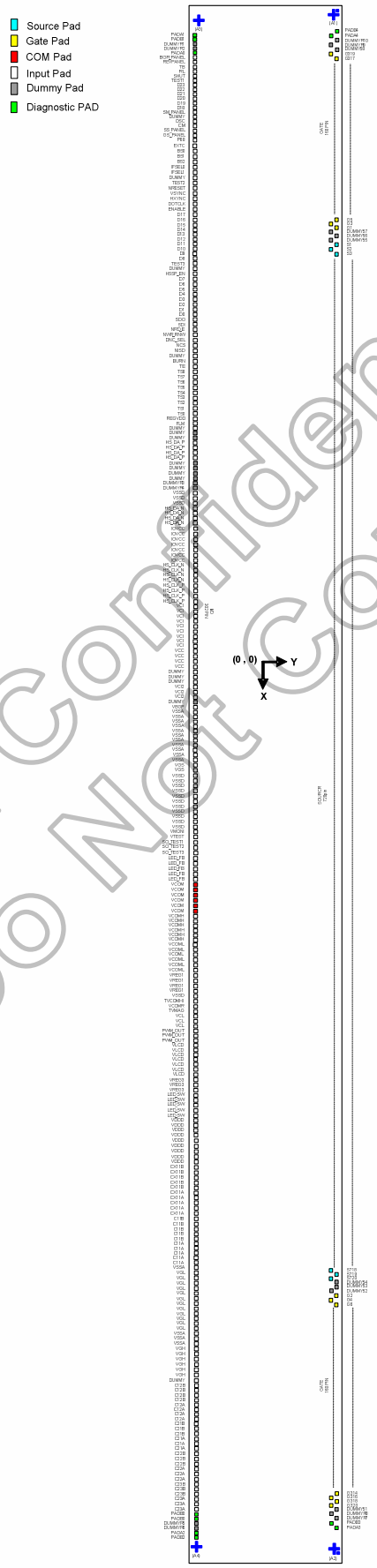
No.	Pad name	X	Y
1201	G15	-7530	395.5
1202	G17	-7550	520.5
1203	G19	-7570	395.5
1204	G21	-7590	520.5
1205	G23	-7610	395.5
1206	G25	-7630	520.5
1207	G27	-7650	395.5
1208	G29	-7670	520.5
1209	G31	-7690	395.5
1210	G33	-7710	520.5
1211	G35	-7730	395.5
1212	G37	-7750	520.5
1213	G39	-7770	395.5
1214	G41	-7790	520.5
1215	G43	-7810	395.5
1216	G45	-7830	520.5
1217	G47	-7850	395.5
1218	G49	-7870	520.5
1219	G51	-7890	395.5
1220	G53	-7910	520.5
1221	G55	-7930	395.5
1222	G57	-7950	520.5
1223	G59	-7970	395.5
1224	G61	-7990	520.5
1225	G63	-8010	395.5
1226	G65	-8030	520.5
1227	G67	-8050	395.5
1228	G69	-8070	520.5
1229	G71	-8090	395.5
1230	G73	-8110	520.5
1231	G75	-8130	395.5
1232	G77	-8150	520.5
1233	G79	-8170	395.5
1234	G81	-8190	520.5
1235	G83	-8210	395.5
1236	G85	-8230	520.5
1237	G87	-8250	395.5
1238	G89	-8270	520.5
1239	G91	-8290	395.5
1240	G93	-8310	520.5
1241	G95	-8330	395.5
1242	G97	-8350	520.5
1243	G99	-8370	395.5
1244	G101	-8390	520.5
1245	G103	-8410	395.5
1246	G105	-8430	520.5
1247	G107	-8450	395.5
1248	G109	-8470	520.5
1249	G111	-8490	395.5
1250	G113	-8510	520.5
1251	G115	-8530	395.5
1252	G117	-8550	520.5
1253	G119	-8570	395.5
1254	G121	-8590	520.5
1255	G123	-8610	395.5
1256	G125	-8630	520.5
1257	G127	-8650	395.5
1258	G129	-8670	520.5
1259	G131	-8690	395.5
1260	G133	-8710	520.5

No.	Pad name	X	Y
1261	G135	-8730	395.5
1262	G137	-8750	520.5
1263	G139	-8770	395.5
1264	G141	-8790	520.5
1265	G143	-8810	395.5
1266	G145	-8830	520.5
1267	G147	-8850	395.5
1268	G149	-8870	520.5
1269	G151	-8890	395.5
1270	G153	-8910	520.5
1271	G155	-8930	395.5
1272	G157	-8950	520.5
1273	G159	-8970	395.5
1274	G161	-8990	520.5
1275	G163	-9010	395.5
1276	G165	-9030	520.5
1277	G167	-9050	395.5
1278	G169	-9070	520.5
1279	G171	-9090	395.5
1280	G173	-9110	520.5
1281	G175	-9130	395.5
1282	G177	-9150	520.5
1283	G179	-9170	395.5
1284	G181	-9190	520.5
1285	G183	-9210	395.5
1286	G185	-9230	520.5
1287	G187	-9250	395.5
1288	G189	-9270	520.5
1289	G191	-9290	395.5
1290	G193	-9310	520.5
1291	G195	-9330	395.5
1292	G197	-9350	520.5
1293	G199	-9370	395.5
1294	G201	-9390	520.5
1295	G203	-9410	395.5
1296	G205	-9430	520.5
1297	G207	-9450	395.5
1298	G209	-9470	520.5
1299	G211	-9490	395.5
1300	G213	-9510	520.5
1301	G215	-9530	395.5
1302	G217	-9550	520.5
1303	G219	-9570	395.5
1304	G221	-9590	520.5
1305	G223	-9610	395.5
1306	G225	-9630	520.5
1307	G227	-9650	395.5
1308	G229	-9670	520.5
1309	G231	-9690	395.5
1310	G233	-9710	520.5
1311	G235	-9730	395.5
1312	G237	-9750	520.5
1313	G239	-9770	395.5
1314	G241	-9790	520.5
1315	G243	-9810	395.5
1316	G245	-9830	520.5
1317	G247	-9850	395.5
1318	G249	-9870	520.5
1319	G251	-9890	395.5
1320	G253	-9910	520.5

No.	Pad name	X	Y
1321	G255	-9930	395.5
1322	G257	-9950	520.5
1323	G259	-9970	395.5
1324	G261	-9990	520.5
1325	G263	-10010	395.5
1326	G265	-10030	520.5
1327	G267	-10050	395.5
1328	G269	-10070	520.5
1329	G271	-10090	395.5
1330	G273	-10110	520.5
1331	G275	-10130	395.5
1332	G277	-10150	520.5
1333	G279	-10170	395.5
1334	G281	-10190	520.5
1335	G283	-10210	395.5
1336	G285	-10230	520.5
1337	G287	-10250	395.5
1338	G289	-10270	520.5
1339	G291	-10290	395.5
1340	G293	-10310	520.5
1341	G295	-10330	395.5
1342	G297	-10350	520.5
1343	G299	-10370	395.5
1344	G301	-10390	520.5
1345	G303	-10410	395.5
1346	G305	-10430	520.5
1347	G307	-10450	395.5
1348	G309	-10470	520.5
1349	G311	-10490	395.5
1350	G313	-10510	520.5
1351	G315	-10530	395.5
1352	G317	-10550	520.5
1353	G319	-10570	395.5
1354	DUMMY58	-10590	520.5
1355	DUMMYR9	-10610	395.5
1356	DUMMYR10	-10630	520.5
1357	PADA4	-10650	395.5
1358	PADB4	-10670	520.5

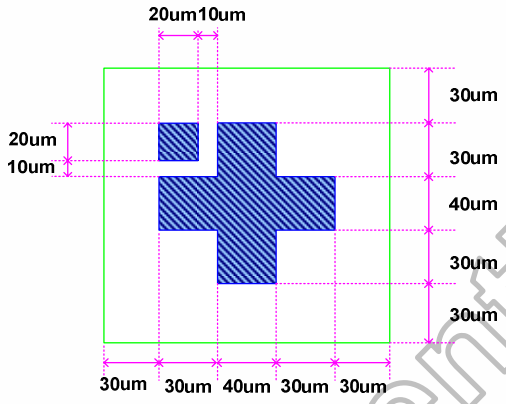
Alignment mark	X	Y
A1	-10810	366
A2	10810	366
A3	-10613	-459
A4	10613	-459

4.4 Bump arrangement

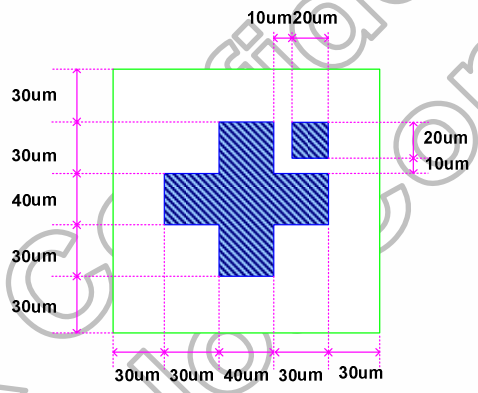


4.5 Alignment mark

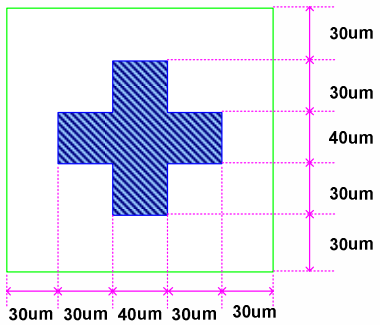
A_MARK (A1)



A_MARK (A2)

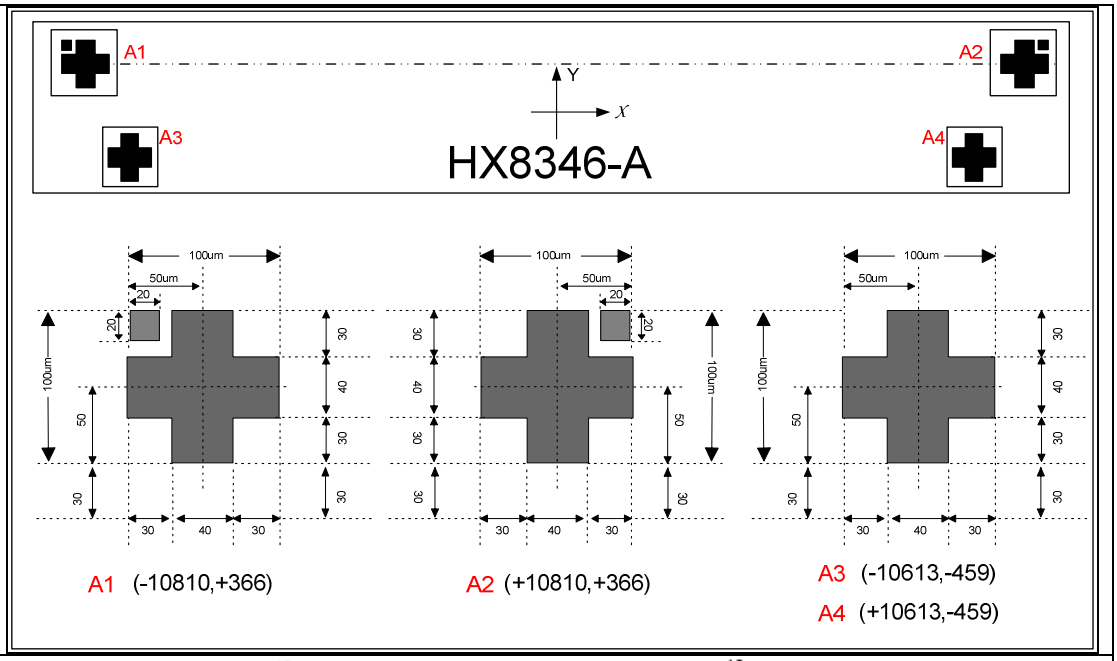


A_MARK (A3), (A4)

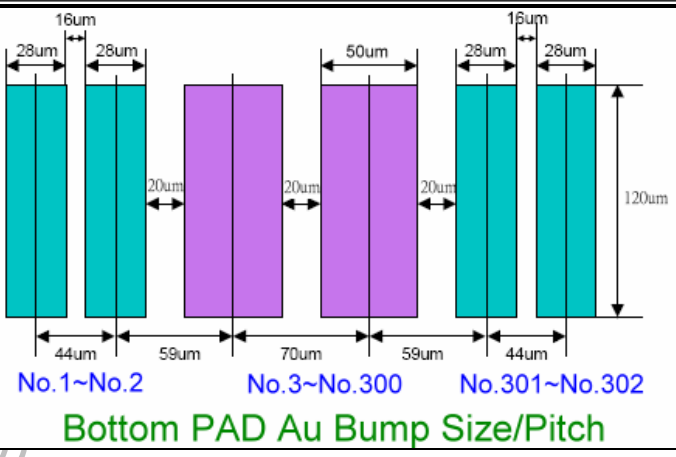


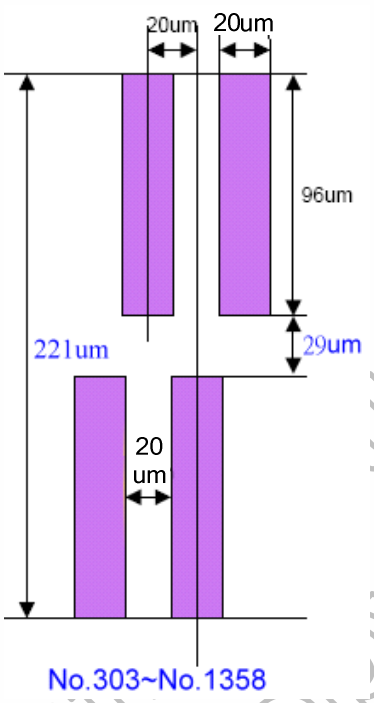
4.6 Bump size

Alignment Mark



Input PAD



Output PAD	

5. Function Description

5.1 Interface Control Mode

The HX8346-A supports four-type interface mode: Command-Parameter interface mode, Register-Content interface mode, RGB interface mode and Hardware-Control interface mode. Command-Parameter interface mode, Register-Content interface mode and Hardware-Control interface mode are selected by the external pins IFSEL1-0 setting, and RGB interface mode is selected by internal bit RGB_EN setting as shown in Table5.1. There are two-type chip access formats in HX8346-A. One is register command for chip internal operation. The other is display data for chip display.

IFSEL1	IFSEL0	RGB_EN	Register Data	Display Data
0	1	0	Register-content interface	Register-content interface
0	1	1	Register-content interface	RGB interface

Table 5. 1 Interface Mode Selection

There are two-type register groups in HX8346-A. One is accessed only via Command-Parameter interface. The other is accessed only via Register-Content interface.
This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8346-A(N) datasheet for detail.

5.1.1 Register-Content Interface Mode

The register-content interface circuit in HX8346-A supports 18-/16-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8346-A become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS(2-0) setting. For selecting the input bus format, please refer to Table5.2 and Table5.3.

In Register-Content interface, it includes an Index Register (IR) be stored index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

P68	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 5. 2 MPU selection in Register-content Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of RAM data	Transferring Method of Command
0	0	0	16-bit system interface	16-bit collective	8-bit collective
0	0	1		16-bit + 2 bit	
0	1	0	18-bit system interface	18-bit collective	
0	1	1	8-bit system interface	8-bit + 8-bit + 8-bit	
1	1	x	Serial bus transfer interface	16 or 24-bit serial	8-bit serial

Table 5. 3 Interface Selection in Register-content Interface Mode

5.1.1.1 Parallel Bus System Interface

The input / output data from data pins (D17-0) and signal operation of the I80/M68 series parallel bus interface as listed in Table 5.4 and Table 5.5.

Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5. 4 Data Pin Function for I80 Series CPU

Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	1	0	0
Reads internal status	1	1	0
Writes command into register or data into GRAM	1	0	1
Reads command from register or data from GRAM	1	1	1

Table 5. 5 Data Pin Function for M68 Series CPU

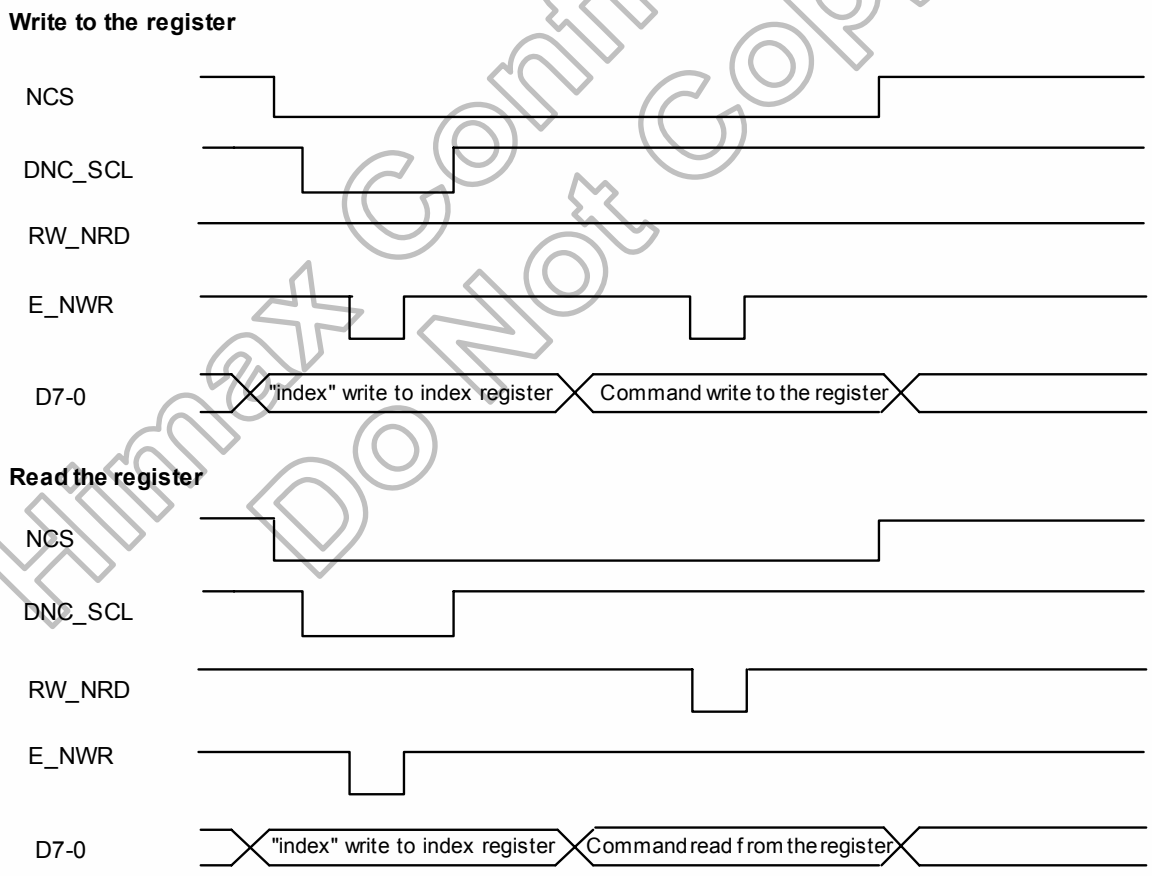


Figure 5. 1 Register read/write Timing in Parallel Bus System Interface (for I80 series MPU)

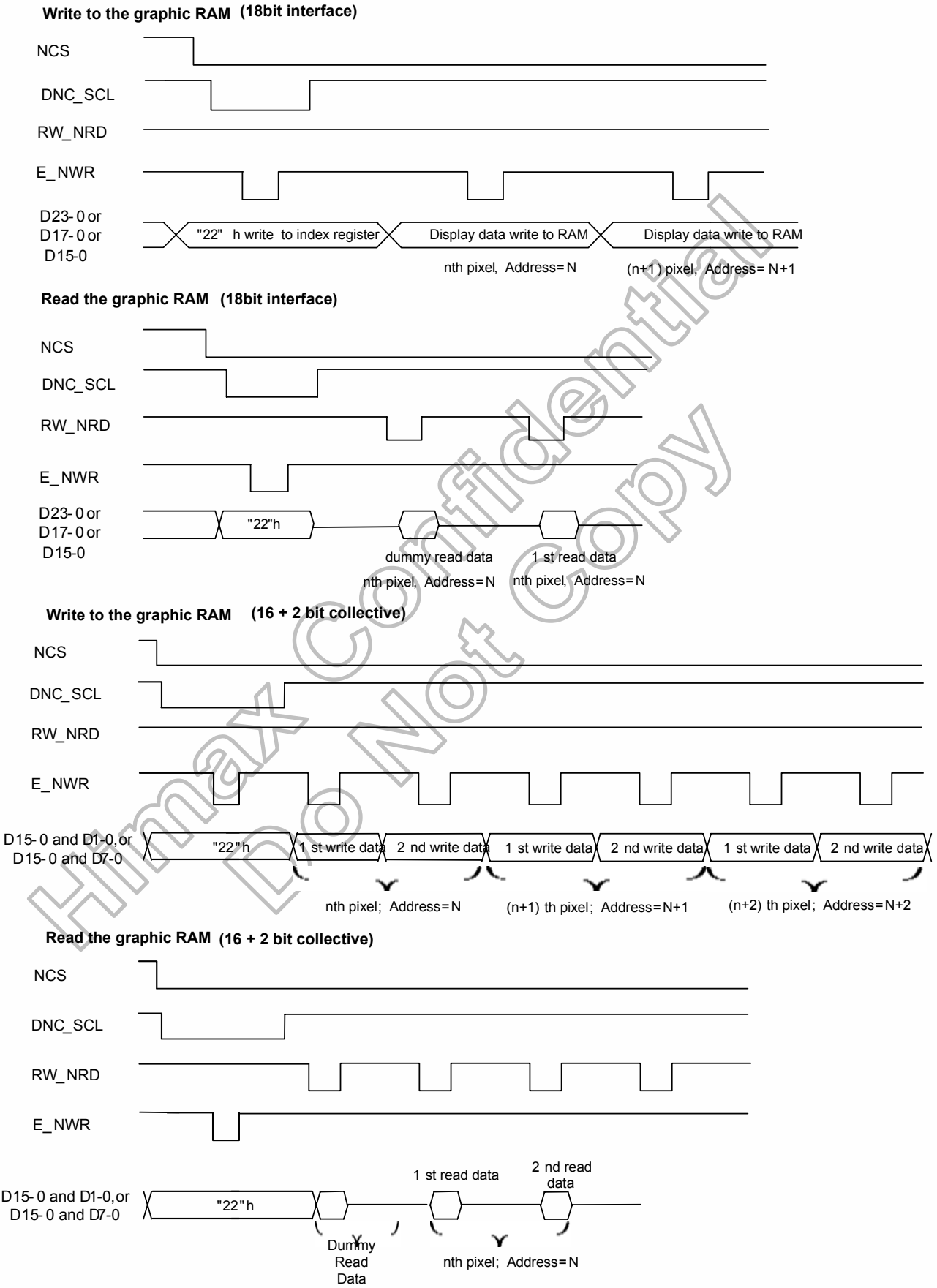


Figure 5. 2 GRAM read/write Timing in Parallel Bus System Interface (for I80 series MPU)

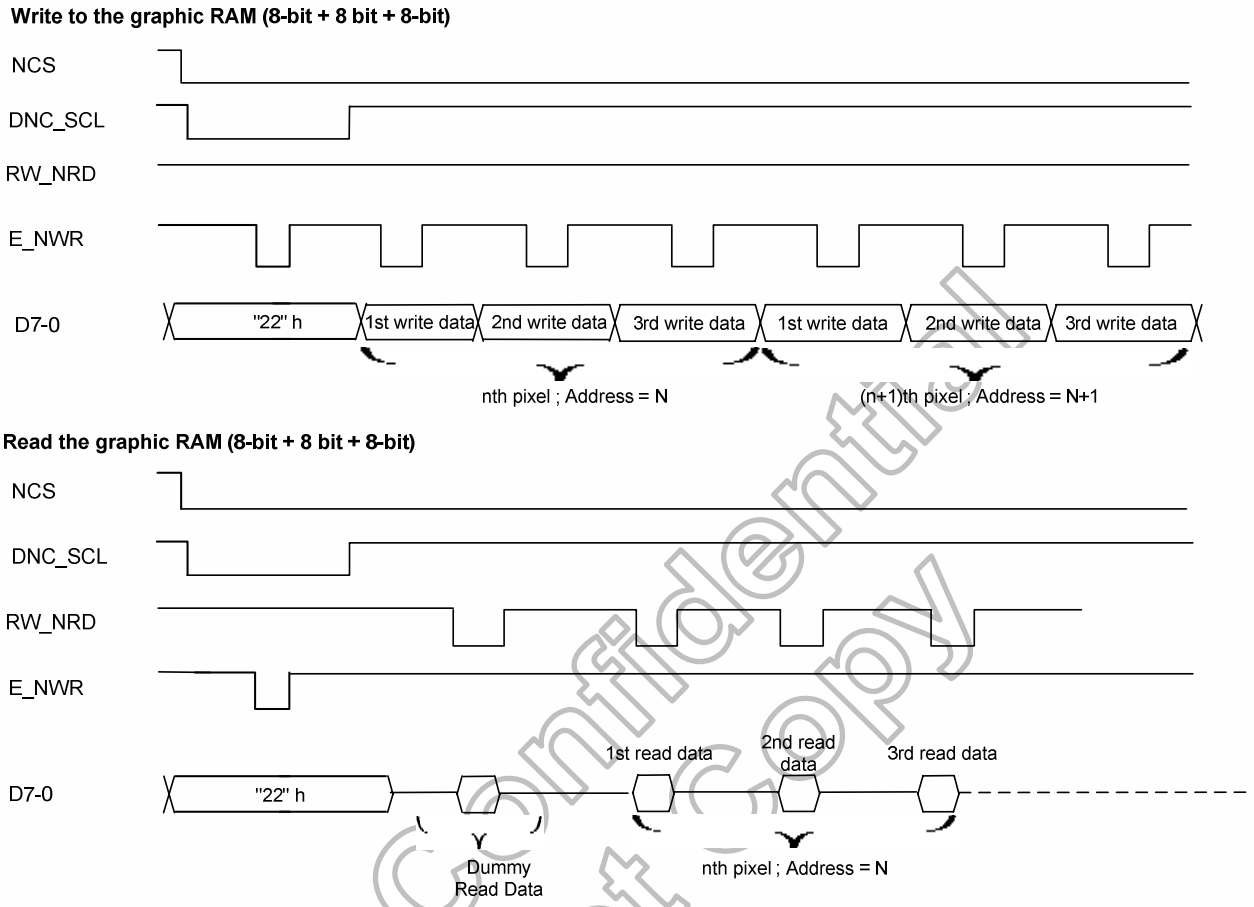


Figure 5. 3 GRAM read/write Timing in Parallel Bus System Interface (for I80 series MPU)

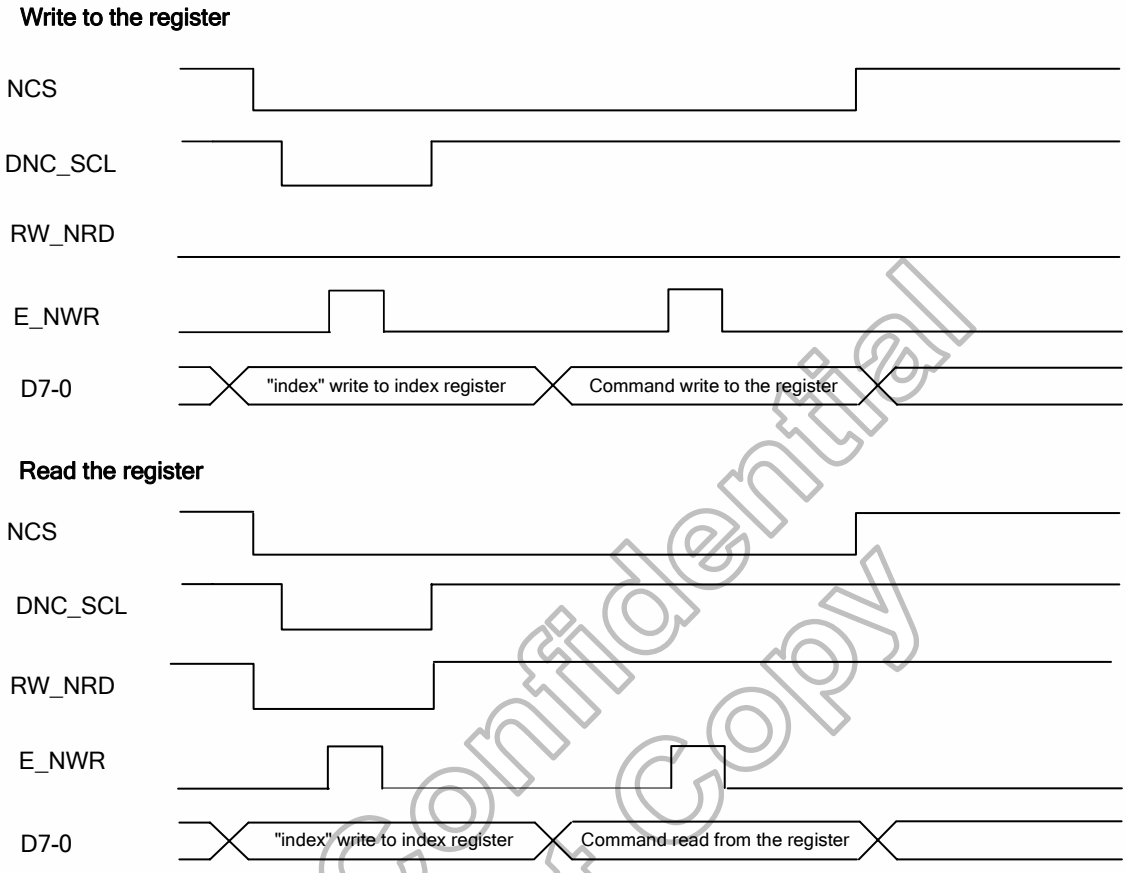


Figure 5. 4 Register read/write Timing in Parallel Bus System Interface (for M68 series MPU)

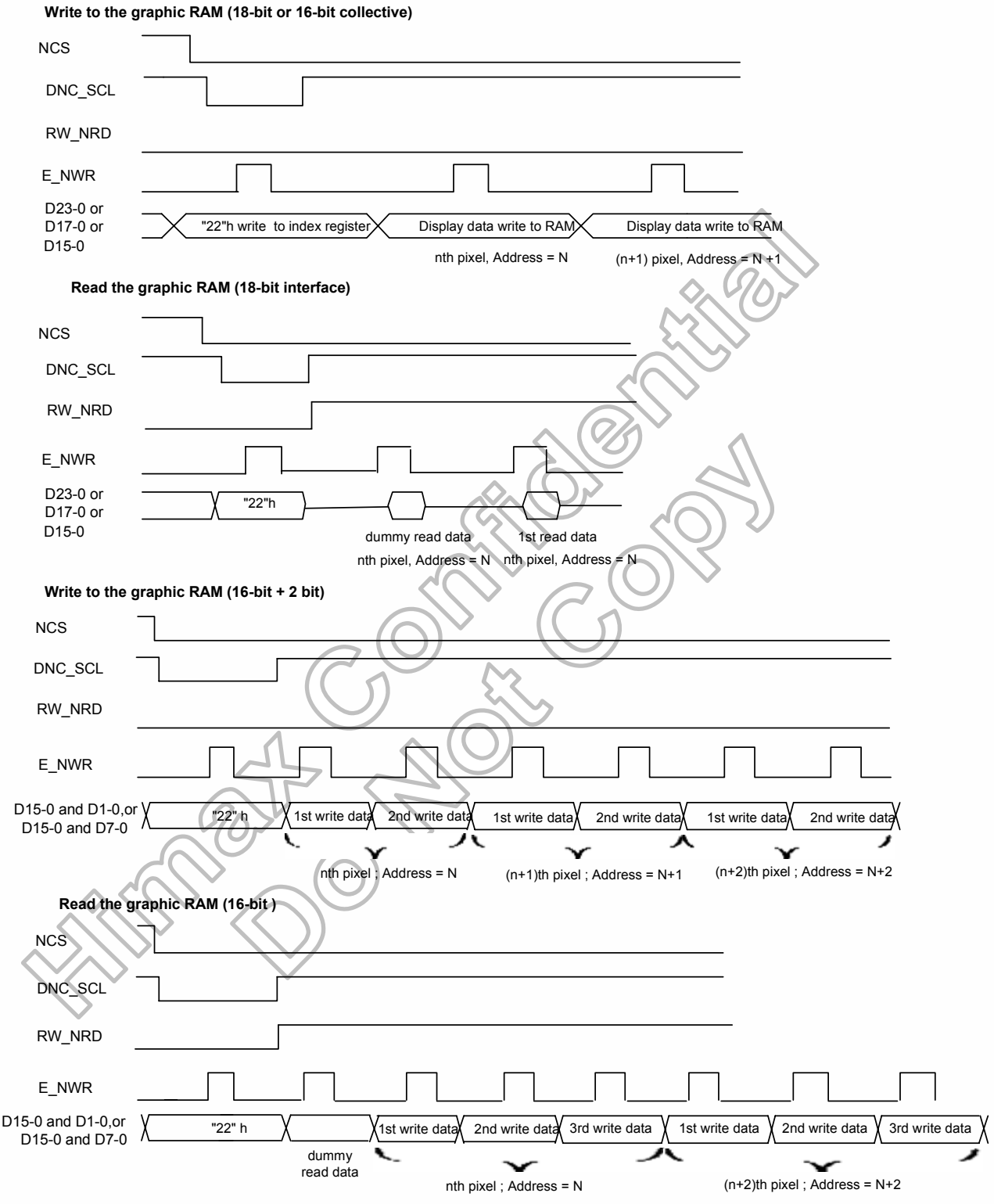


Figure 5. 5 GRAM read/write Timing in Parallel Bus System Interface (for M68 series MPU)

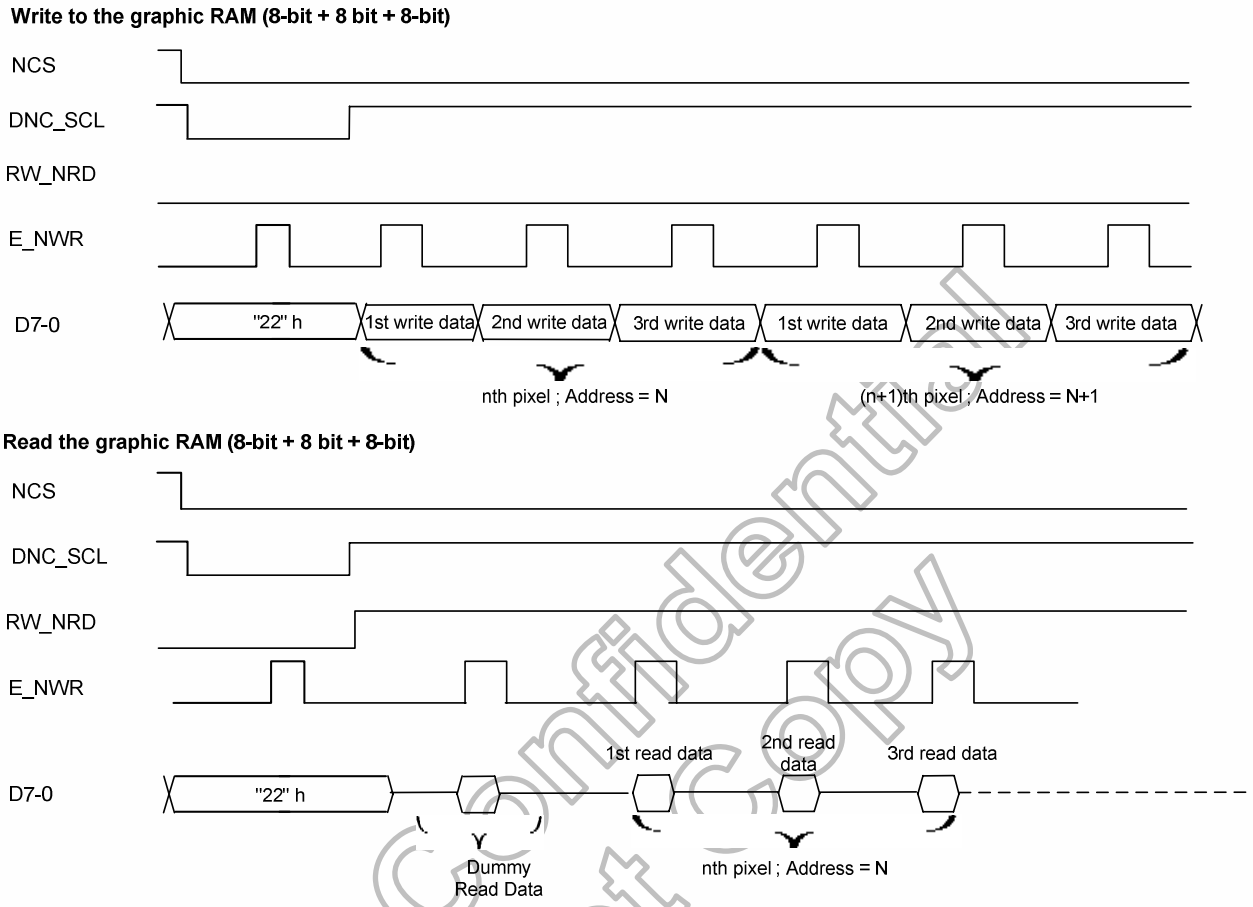


Figure 5. 6 GRAM read/write Timing in Parallel Bus System Interface (for M68 series MPU)

16-bit Parallel Bus System Interface

The I80-system 16-bit parallel bus interface in register-content interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0000” and ”0001”. And the M68-system 16-bit parallel bus interface in Register-Content interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1000” ,”1001” and “1001”. The Figure 5.7 is the example of interface with I80/M68 microcomputer system interface.

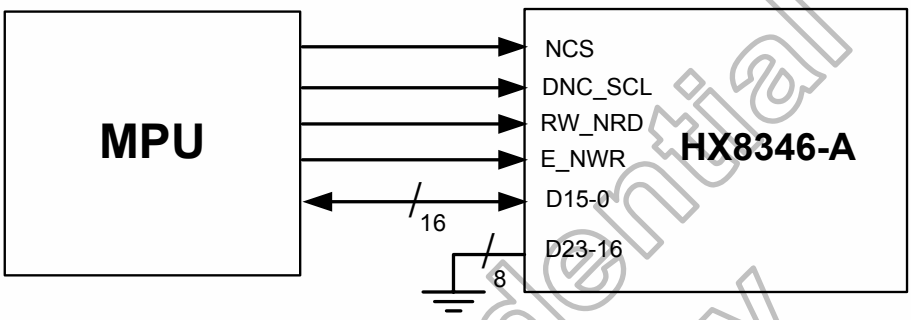


Figure 5. 7 Example of I80- / M68- System 16-bit Parallel Bus Interface

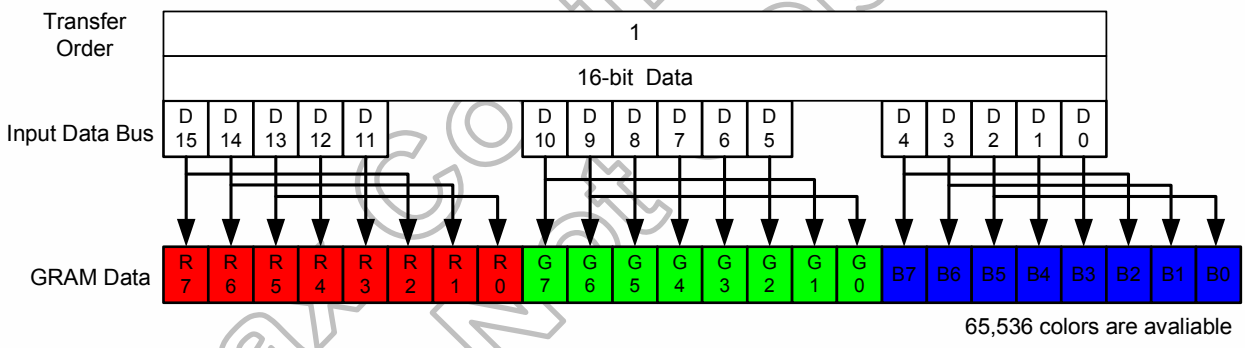


Figure 5. 8 Input Data Bus and GRAM Data Mapping in 16-bit Bus System Interface with 16 bit-Data Input (BS(2-0) = “000”)

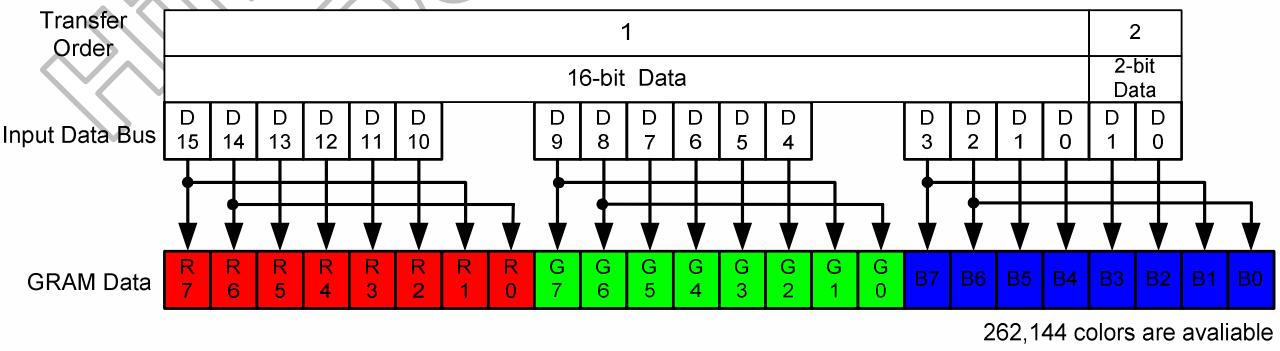
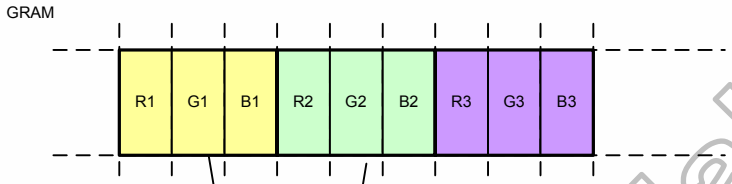


Figure 5. 9 Input Data Bus and GRAM Data Mapping in 16-bit Bus System Interface with (16 + 2) bit-Data Input (BS(2-0) = “001”)

SRAM Read pin mapping



16.7M Color Data	DNC/RS	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEM_RD	0	GRAM Read command code								-
1st Read	1	Dummy Read								-
2nd Read	1	R17	R16	R15	R14	R13	R12	R17	R16	-
3rd Read	1	G17	G16	G15	G14	G13	G12	G17	G16	-
4th Read	1	B17	B16	B15	B14	B13	B12	B17	B16	1st pixel (R1/G1/B1)
5th Read	1	R27	R26	R25	R24	R23	R22	G27	G26	-
6th Read	1	G27	G26	G25	G24	G23	G22	G27	G26	-
7th Read	1	B27	B26	B25	B24	B23	B22	B27	B26	2nd pixel (R2/G2/B2)

Figure 5. 10 Output Data Bus and GRAM Data Mapping in 16-bit Bus System Interface with (16 + 2) bit-Data Input (BS(2-0) = “001”)

18-bit Parallel Bus System Interface

The I80-system 18-bit parallel bus interface in register-content interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0010”. And the M68-system 18-bit parallel bus interface in Register-Content interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1010”. The Figure5.11 is the example of interface with I80/M68 microcomputer system interface.

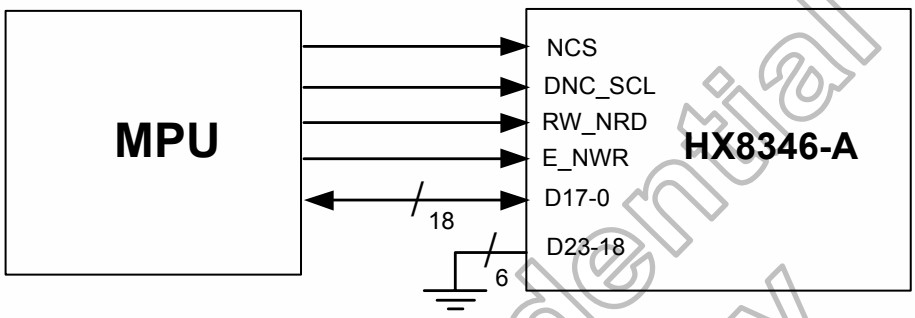


Figure 5. 11 Example of I80- / M68- System 18-bit Parallel Bus Interface

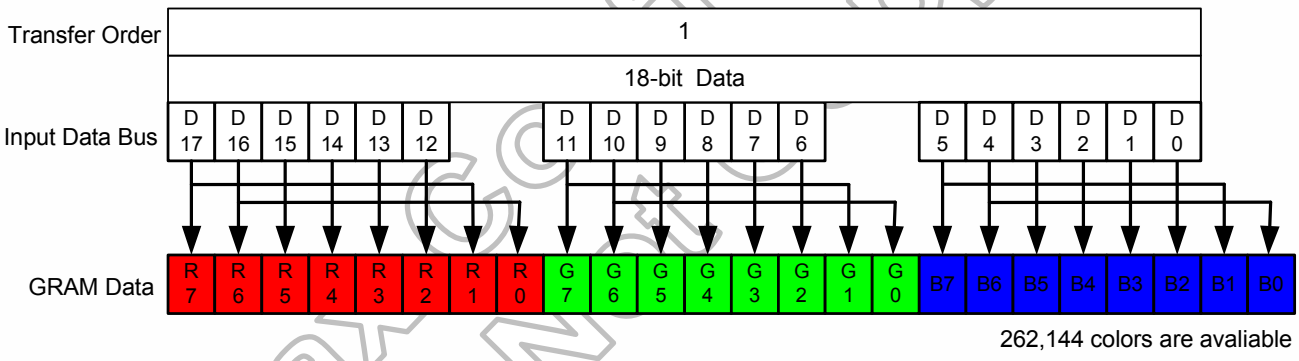
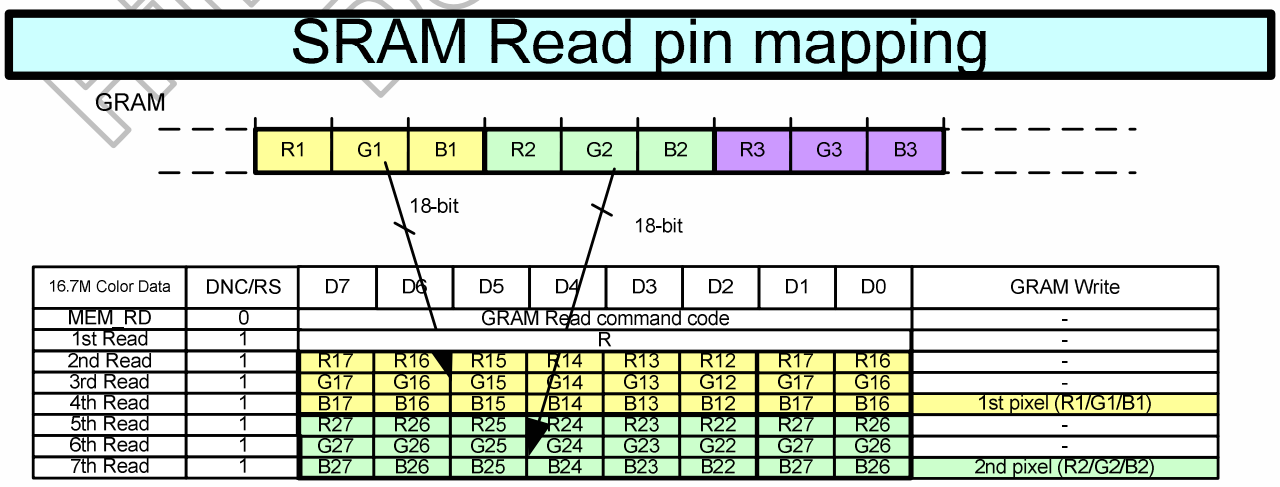


Figure 5. 12 Input Data Bus and GRAM Data Mapping in 18-bit Bus System Interface with (18) bit-Data Input (BS(2-0) = “010”)



16.7M Color Data	DNC/RS	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEM_RD	0	GRAM Read command code								-
1st Read	1	R								-
2nd Read	1	R17	R16	R15	R14	R13	R12	R17	R16	-
3rd Read	1	G17	G16	G15	G14	G13	G12	G17	G16	-
4th Read	1	B17	B16	B15	B14	B13	B12	B17	B16	1st pixel (R1/G1/B1)
5th Read	1	R27	R26	R25	R24	R23	R22	R27	R26	-
6th Read	1	G27	G26	G25	G24	G23	G22	G27	G26	-
7th Read	1	B27	B26	B25	B24	B23	B22	B27	B26	2nd pixel (R2/G2/B2)

Figure 5. 13Output Data Bus and GRAM Data Mapping in 18-bit Bus System Interface with (18) bit-Data Input (BS(2-0) = “010”)

8-bit Parallel Bus System Interface

The I80-system 8-bit parallel bus interface in register-content interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0011”. And the M68-system 8-bit parallel bus interface in Register-Content interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1011”. The Figure 5.13 is the example of interface with I80/M68 microcomputer system interface.

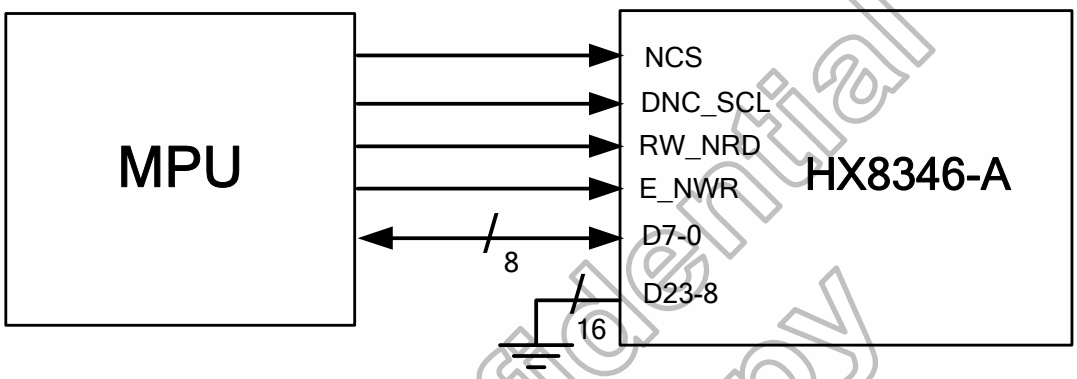


Figure 5. 14 Example of I80- / M68- System 8-bit Parallel Bus Interface

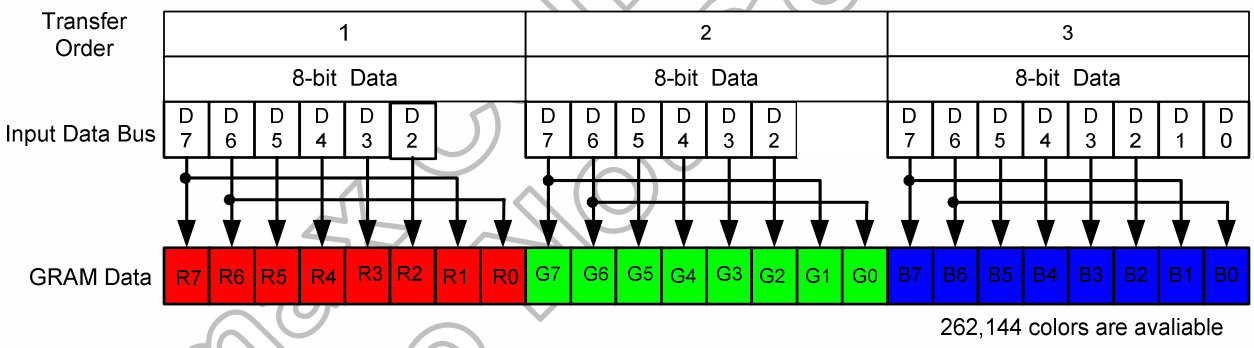
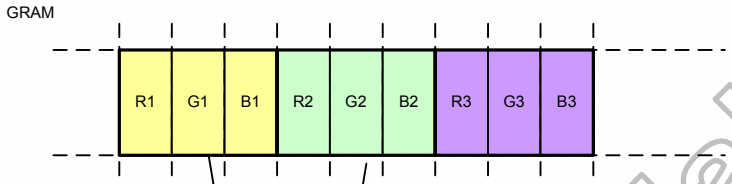


Figure 5. 15 Input Data Bus and GRAM Data Mapping in 8-bit Bus System Interface with (8 + 8 +8) bit-Data Input (BS(2-0) = “011”)

SRAM Read pin mapping



16.7M Color Data	DNC/RS	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEM_RD	0	GRAM Read command code								-
1st Read	1	Dummy Read								-
2nd Read	1	R17	R16	R15	R14	R13	R12	R17	R16	-
3rd Read	1	G17	G16	G15	G14	G13	G12	G17	G16	-
4th Read	1	B17	B16	B15	B14	B13	B12	B17	B16	1st pixel (R1/G1/B1)
5th Read	1	R27	R26	R25	R24	R23	R22	G27	G26	-
6th Read	1	G27	G26	G25	G24	G23	G22	G27	G26	-
7th Read	1	B27	B26	B25	B24	B23	B22	B27	B26	2nd pixel (R2/G2/B2)

Figure 5. 16 Output Data Bus and GRAM Data Mapping in 8-bit Bus System Interface with (8 + 8 +8) bit-Data Input (BS(2-0) = “011”)

5.1.1.2 Serial Bus System Interface

The HX8346-A supports the serial bus interface in register-content mode by setting external pins “BS2, BS1” pins to “11”. The serial bus system interface mode is enabled through the chip select line (NCS), and accessed via a control consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock signal (DNC_SCL).

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code, register select (RS) bit and read /write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determine internal index register or register, GRAM accessing. It must be setting RS as “0” when write data to the index register or read the status, and it must be setting RS as “1” when write a command or GRAM data. The read or write operation is selected by the eighth bit (RW). The Table 5.6 is specified the function of RS and R/W bit.

RS	R/W	Function
0	0	Writes Indexes into IR
1	0	Writes command into register or data into GRAM
1	1	Reads command from register or data from GRAM

Table 5. 6 The Function of RS and R/W Bit

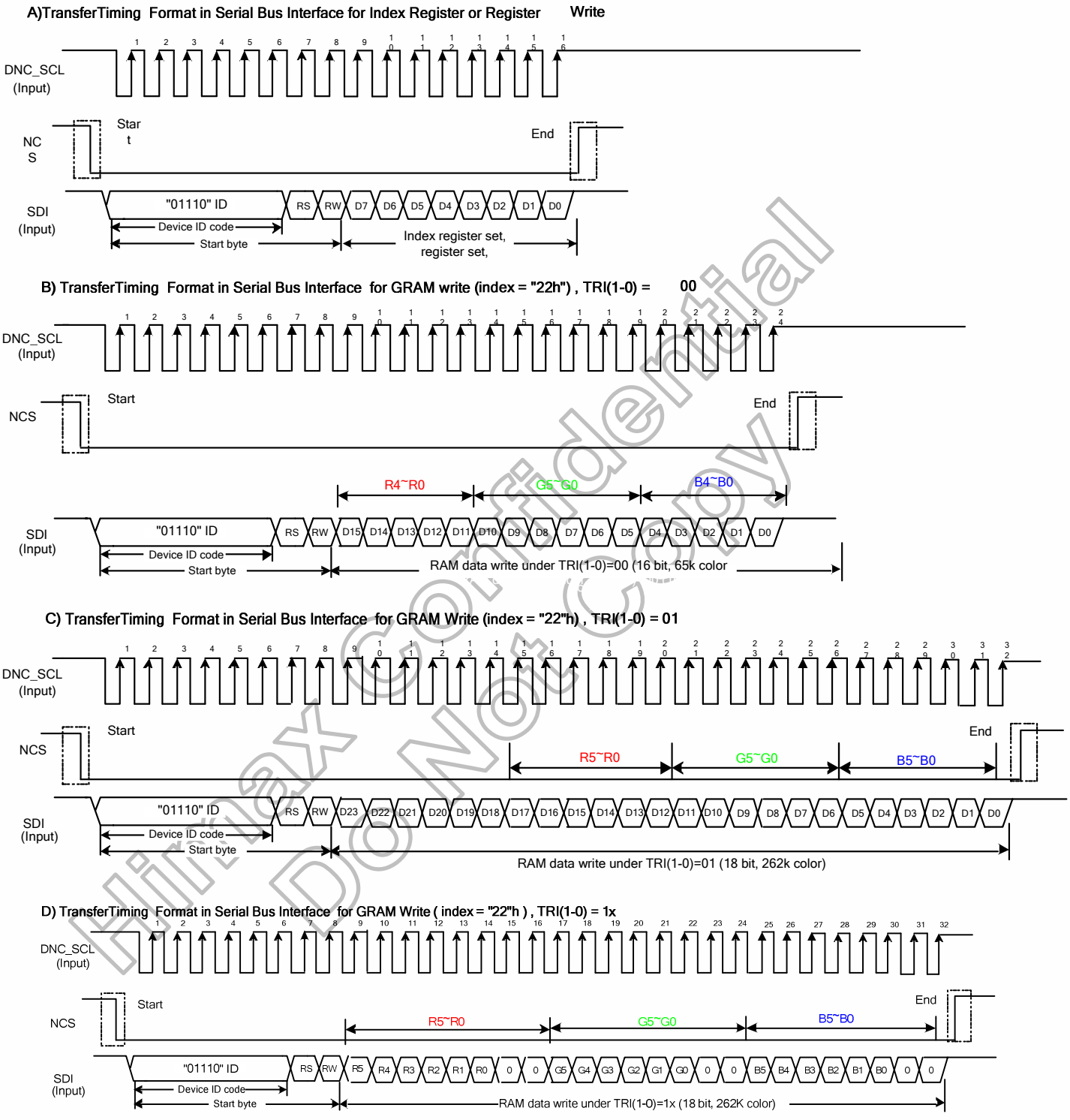
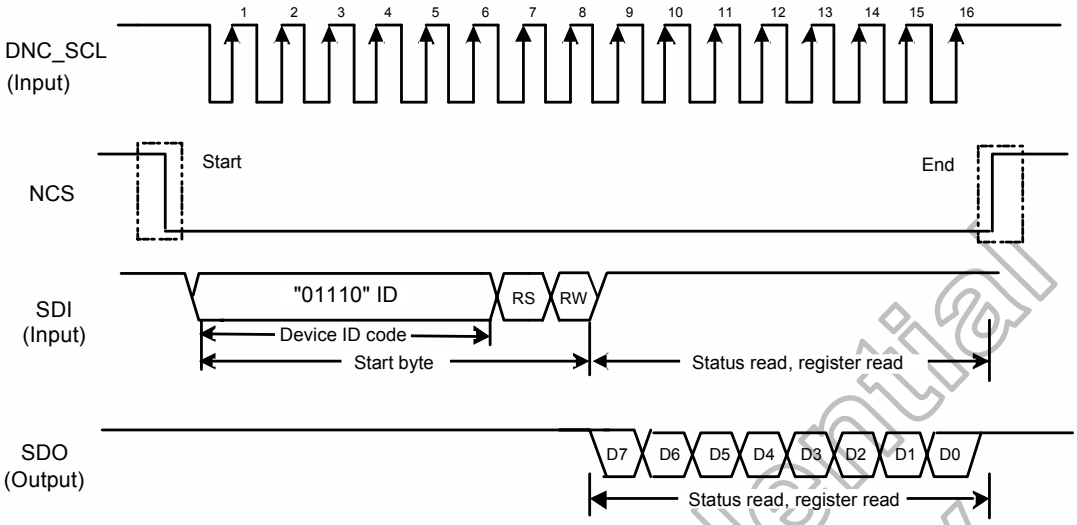


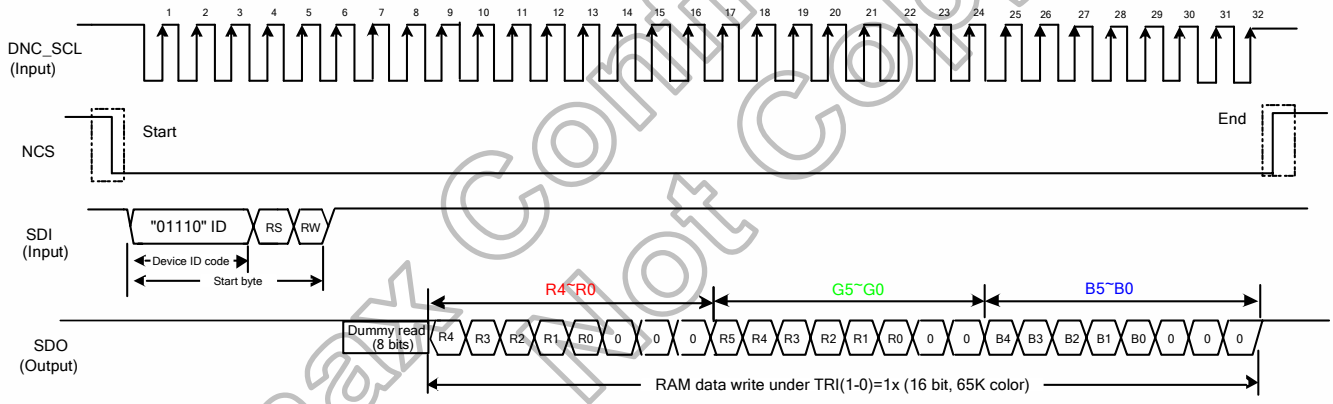
Figure 5. 17 Data Write Timing in Serial Bus System Interface

A)TransferTiming Format in Serial Bus Interface for Register Read



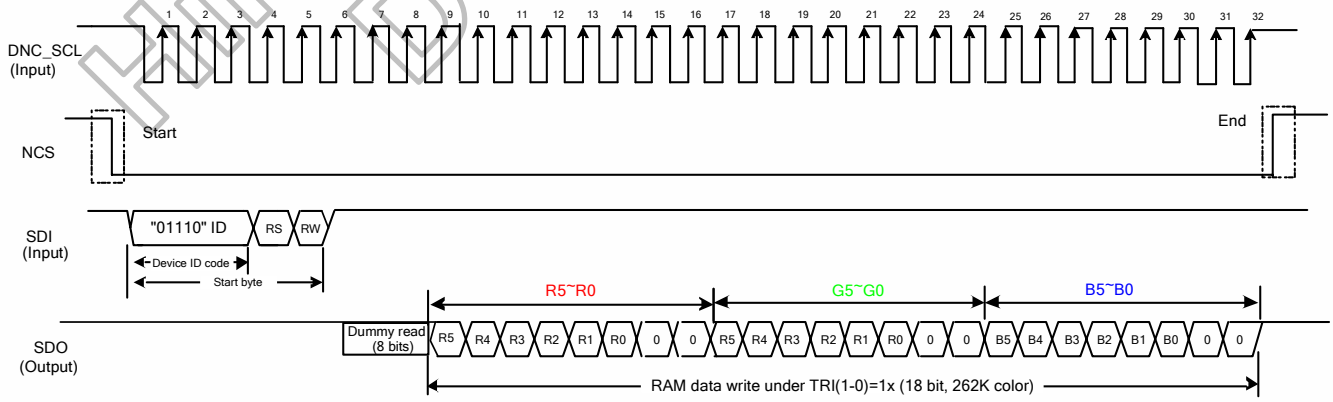
Note: This figure is specified transfer format (single read)

D) Transfer timing format in Serial Bus Interface for GRAM Read (index = "22"h) , TRI (1-0) = 00



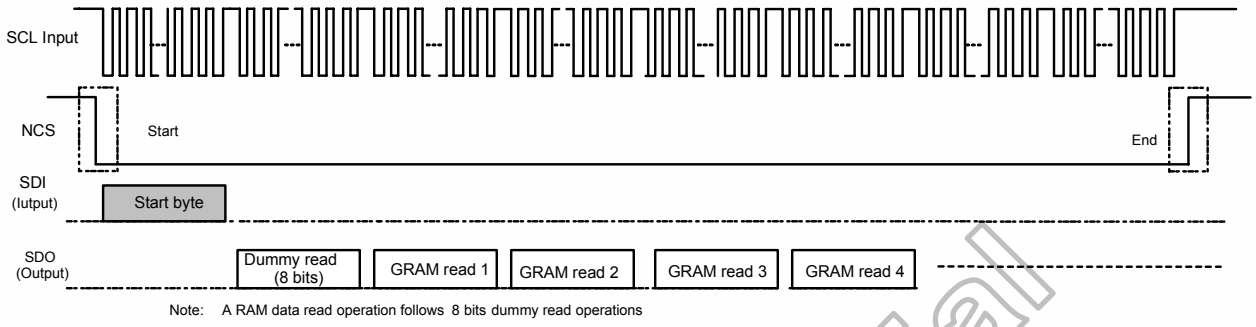
Note: This figure is specified transfer format (single read)

D) Transfer timing format in Serial Bus Interface for GRAM Read (index = "22"h) , TRI (1-0) = 1x



Note: This figure is specified transfer format (single read)

D) Timing Format of GRAM Data Read



Note: This figure is specified transfer format (multi read)

Figure 5. 18 Data Read Timing in Serial Bus System Interface

5.1.2 RGB Interface

The HX8346-A supports the RGB interface for animated display data written. The RGB interface can be selected by setting internal RGB_EN bit = 1. In RGB interface the display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK), and the display data is input via RGB interface circuit without being written to the GRAM and display directly. The display data are transferred in pixel unit via D23-0 input pins. The display data input is latched in the rising edge of DOTCLK (DPL bit = 0) or in the falling edge of DOTCLK (DPL bit = 1) by the chip when ENABLE signal is valid described in Table 5.7

EPL	ENABLE	Display
0	0	Disable
0	1	Enable
1	0	Enable
1	1	Disable

Table 5. 7 EPL bit Setting and Valid ENABLE Signal

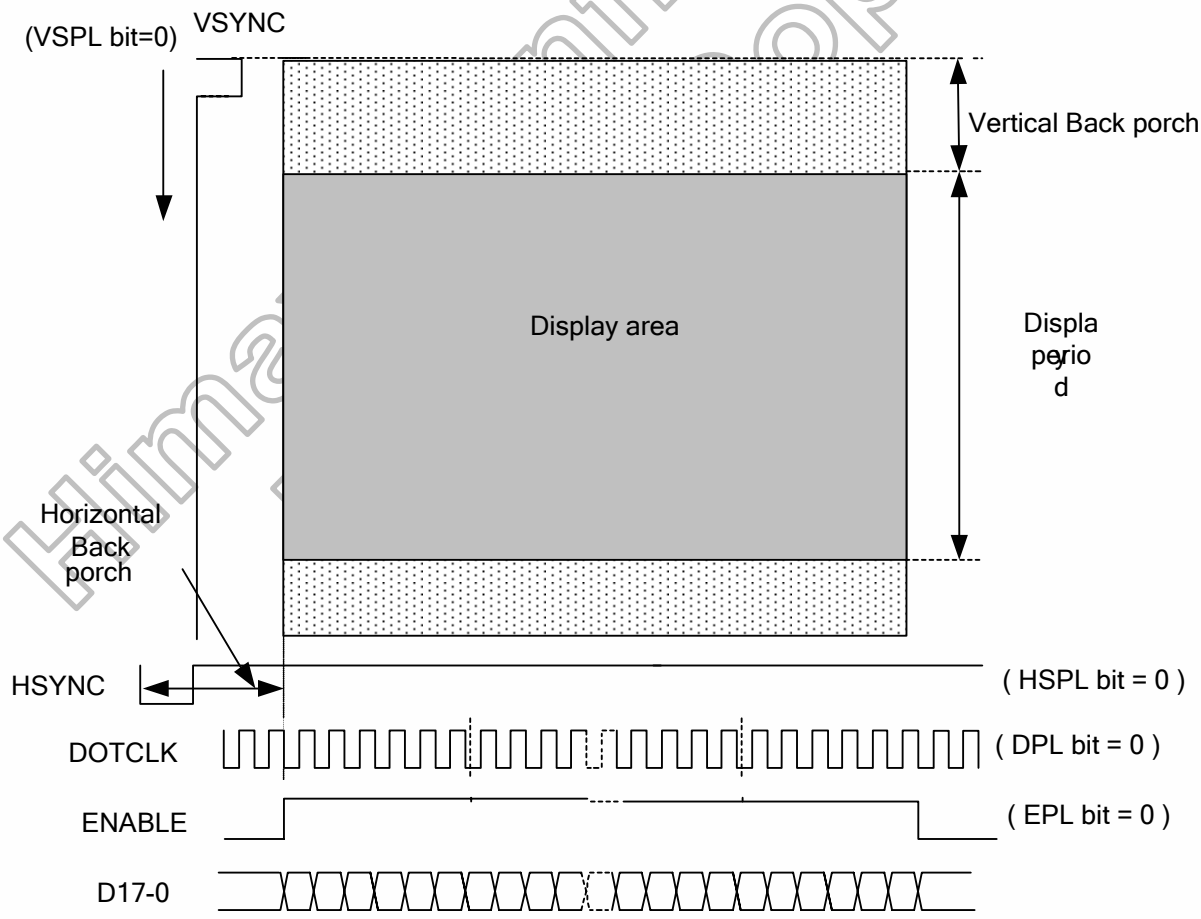


Figure 5. 19 RGB Interface Circuit Input Timing

There are three types bit format per pixel color order for write GRAM data in 16-bit bus interface selected by internal bits CSEL(2-0) setting as shown in Figure 5. 17 ~ Figure 5. 19.

(1) 16 bit/pixel color order (R 5-bit, G 6-bit, B 5-bit), 65,536 colors (CSEL(2-0) = "101")

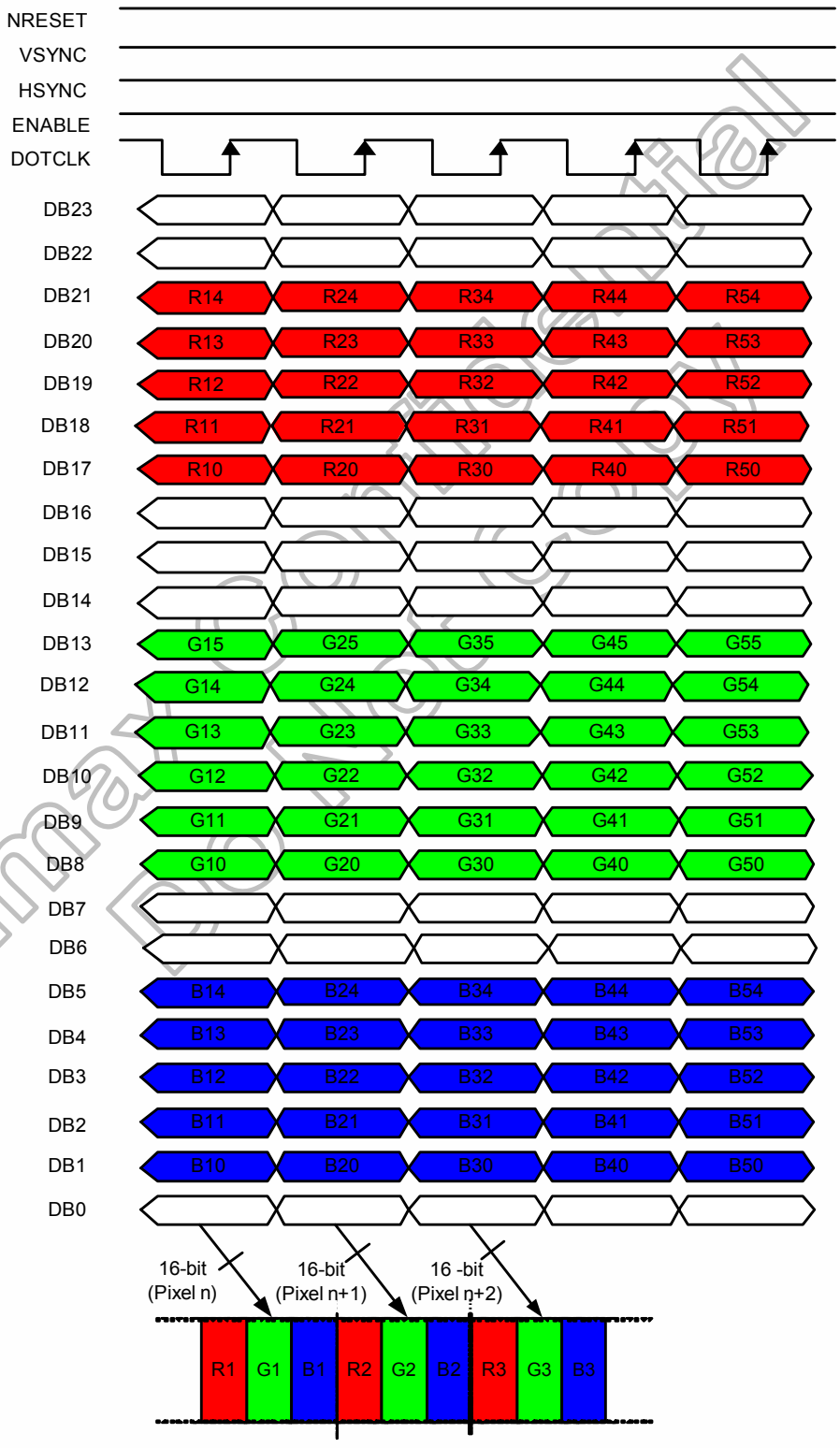


Figure 5. 20 16 bit / pixel Data Input

(2) 18 bit/pixel color order (R 6-bit, G 6-bit, B 6-bit), 262,144 colors (CSEL(2-0) = "110")

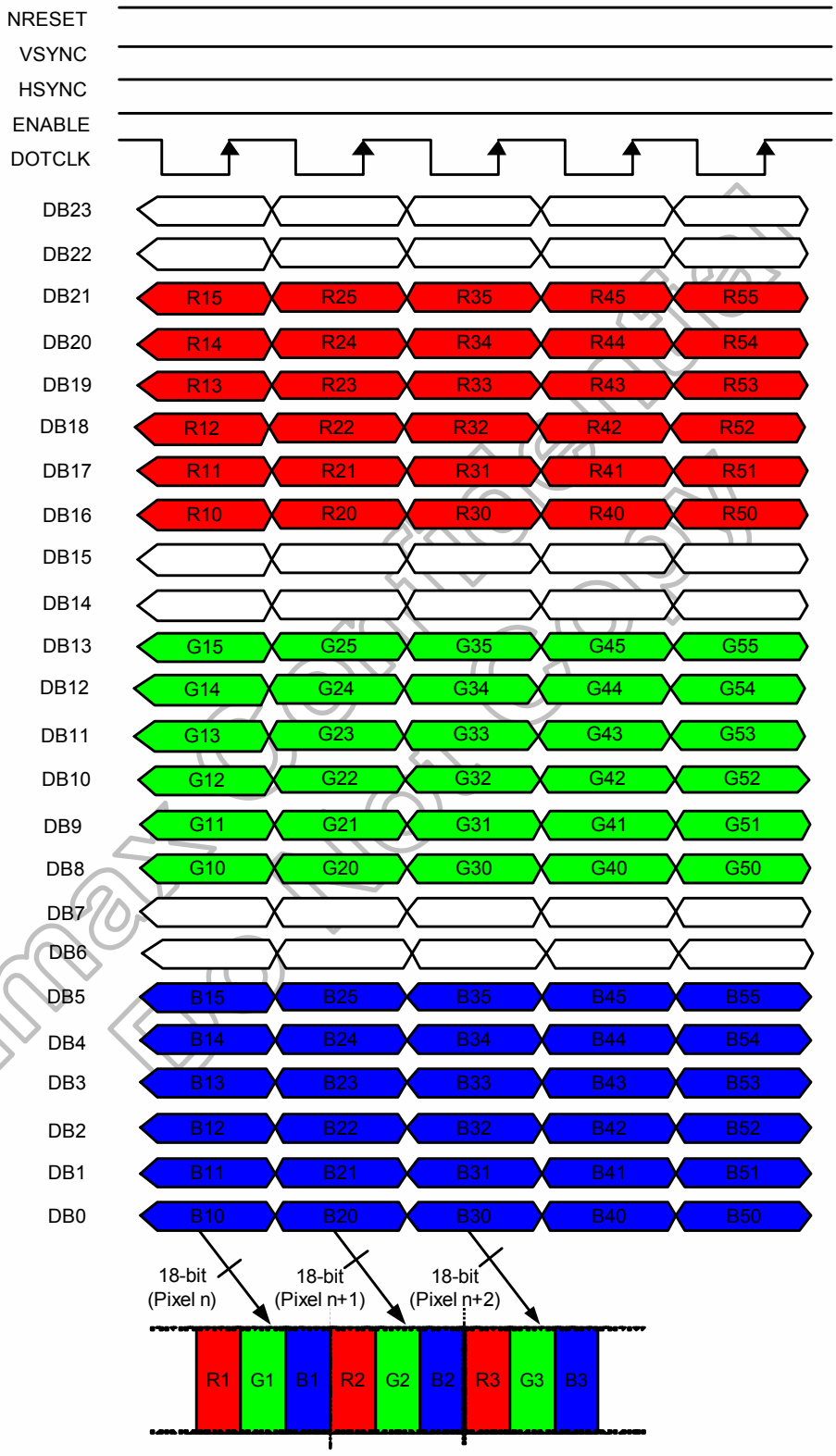


Figure 5. 21 18 bit / pixel Data Input

5.2 Address Counter(AC)

The HX8346-A contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range are: X=0~239d and Y=0~319d

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: SC, end: EC) or the vertical address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.2.1 MCU to memory write/read direction

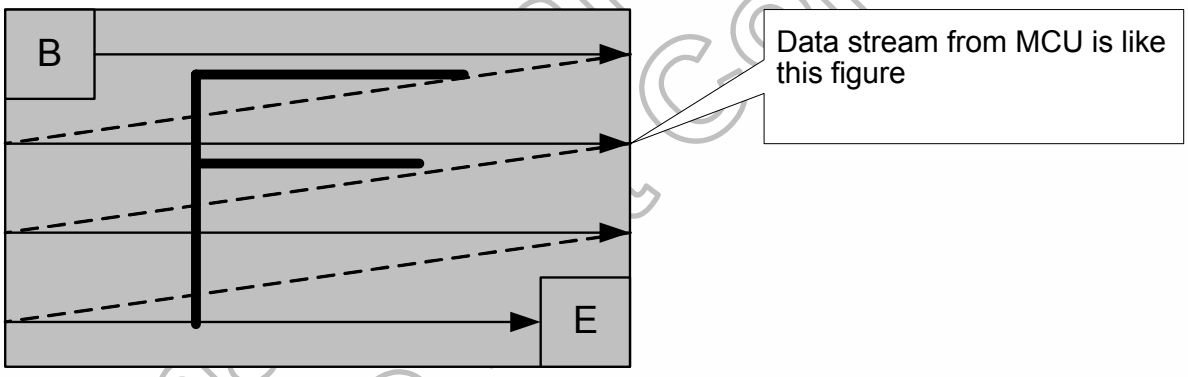


Figure 5. 22 MCU to memory write/read direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits MY, MX, MV as described below.

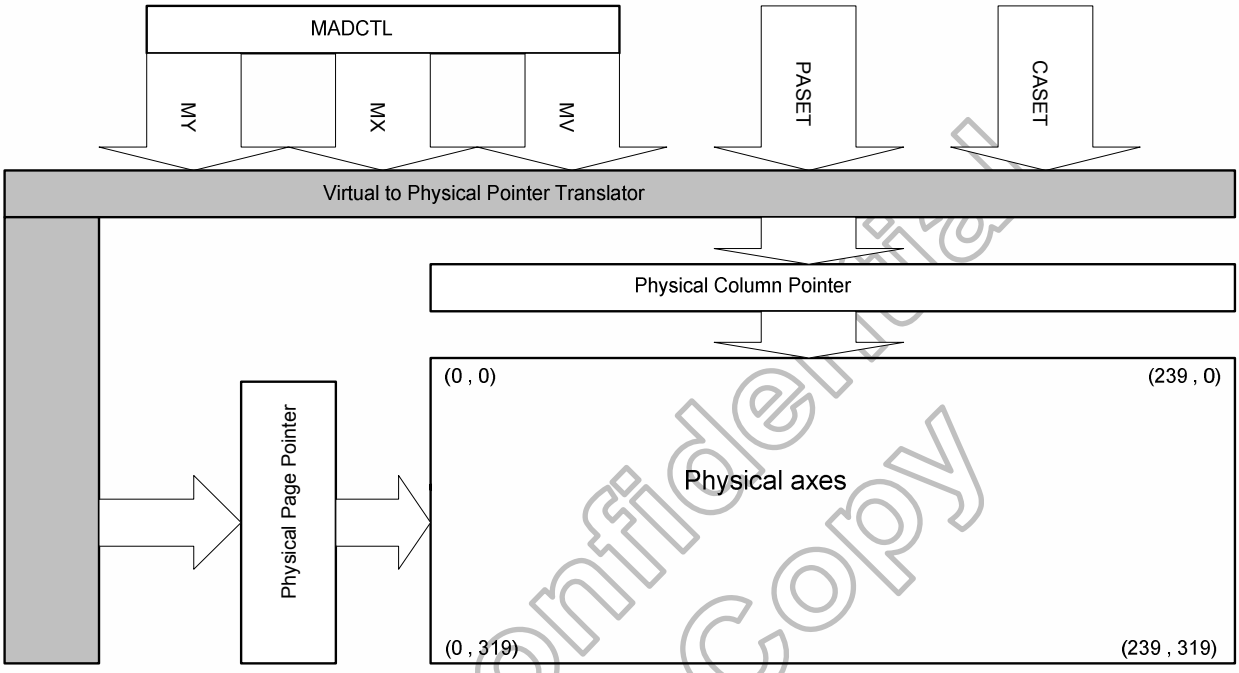


Figure 5. 23 MY, MX, MV Setting

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

Table 5. 8 MY, MX, MV Setting

The following figure depicts the update method with MV, MX and MY bit

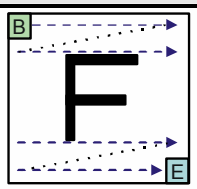
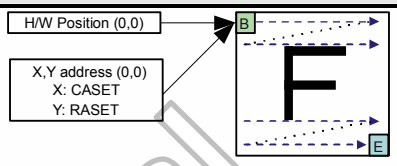
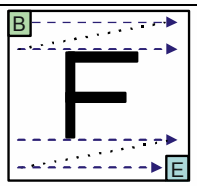
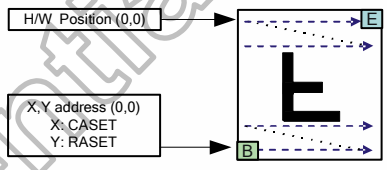
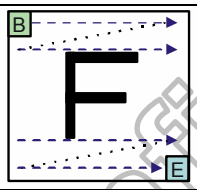
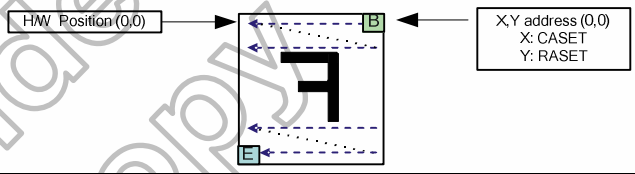
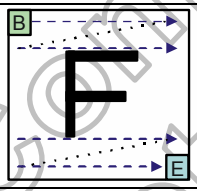
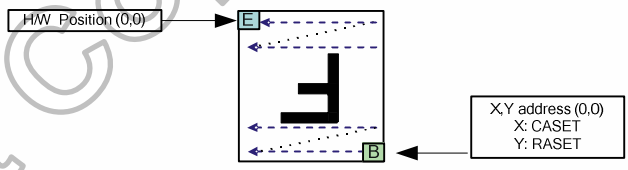
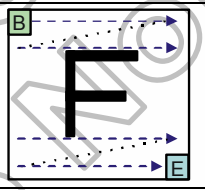
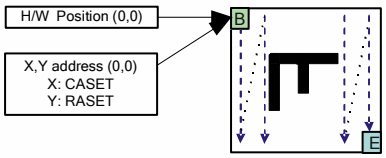
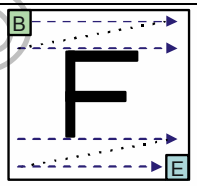
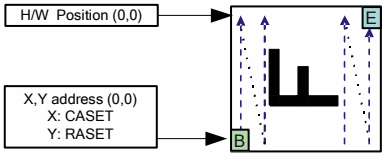
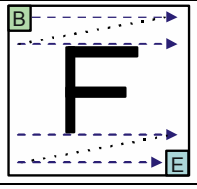
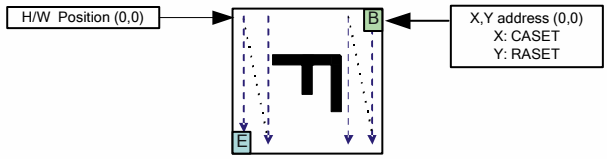
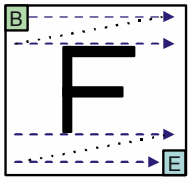
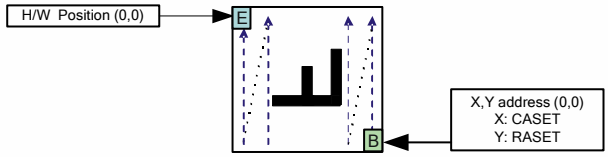
Display Data Direction	MADCTR parameter			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5. 24 Address Direction Settings

5.3 Source, Gate and Memory Map

Source Out		S1	S2	S3	S4	S5	S6	----------	S715	S716	S717	S718	S719	S720				
RA								RGB Order ——— :RGB=0 - - - - - :RGB=1							SA		Gate	
MY=0	MY=1														ML=0	ML=1	GS=0	GS=1
0	319	R0$_{7-0}$	G0$_{7-0}$	B0$_{7-0}$	R1$_{7-0}$	G1$_{7-0}$	B1$_{7-0}$	–	R238$_{7-0}$	G238$_{7-0}$	B238$_{7-0}$	R239$_{7-0}$	G239$_{7-0}$	B239$_{7-0}$	0	319	G1	G320
1	318							–							1	318	G2	G319
2	317							–							2	317	G3	G318
3	316							–							3	316	G4	G317
4	315							–							4	315	G5	G316
5	314							–							5	314	G6	G315
6	313							–							6	313	G7	G314
7	312							–							7	312	G8	G313
8	311							–							8	311	G9	G312
9	310							–							9	310	G10	G311
10	309							–							10	309	G11	G310
11	308							–							11	308	G12	G309
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
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:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
312	7							–							312	7	G313	G8
313	6							–							313	6	G314	G7
314	5							–							314	5	G315	G6
315	4							–							315	4	G316	G5
316	3							–							316	3	G317	G4
317	2							–							317	2	G318	G3
318	1							–							318	1	G319	G2
319	0							–				RN$_{7-0}$	GN$_{7-0}$	BN$_{7-0}$	319	0	G320	G1
CA	MX=0	0			1			...	238			239						
	MX=1	239			238			...	1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter)
MY = Mirror Y-axis (Row address direction parameter)
ML = Scan direction parameter
RGB= Red, Green and Blue pixel position change

Figure 5. 25 Memory Map. (240RGBx320)

5.4 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.4.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

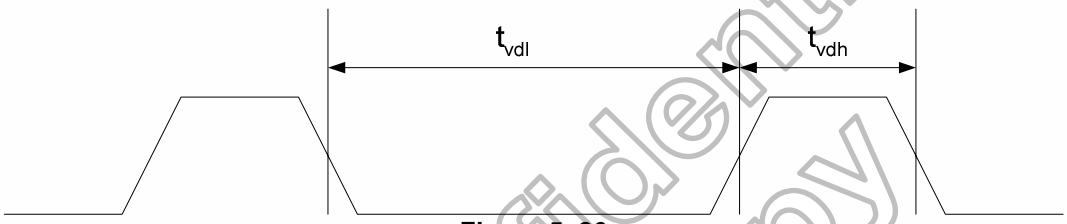


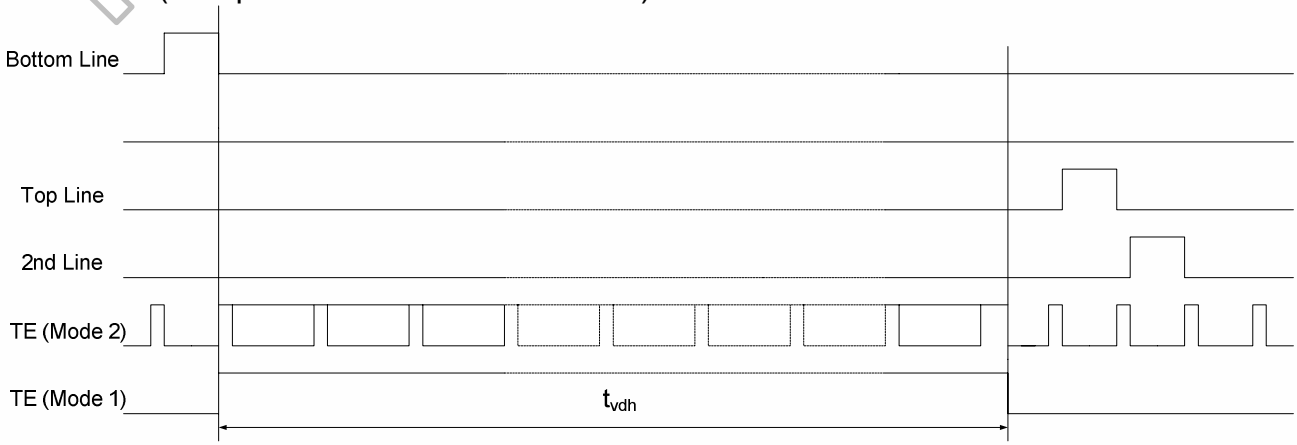
Figure 5. 26

t_{VREG1}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory
(except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.

Figure 5. 27

t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory
(except Invisible Line – see above)



Note: During STB In Mode, the Tearing Output Pin is active Low

Figure 5. 28

5.4.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.

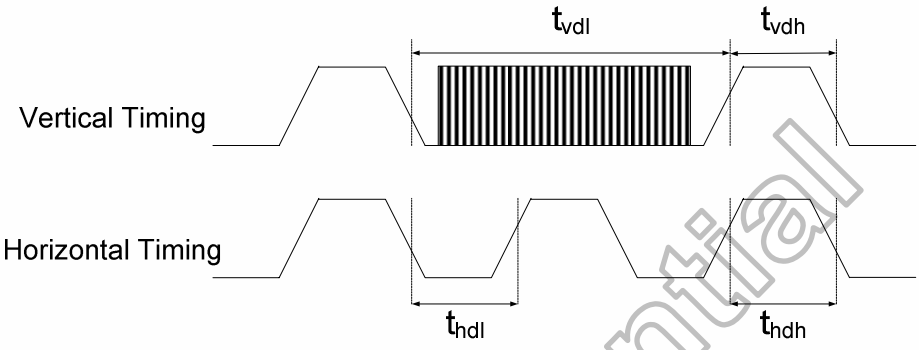


Figure 5. 29

Idle Mode Off (Frame Rate = TBD Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: The timings in Table 5.11 apply when MADCTL ML=0 and ML=1

Table 5. 9 AC characteristics of Tearing Effect Signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

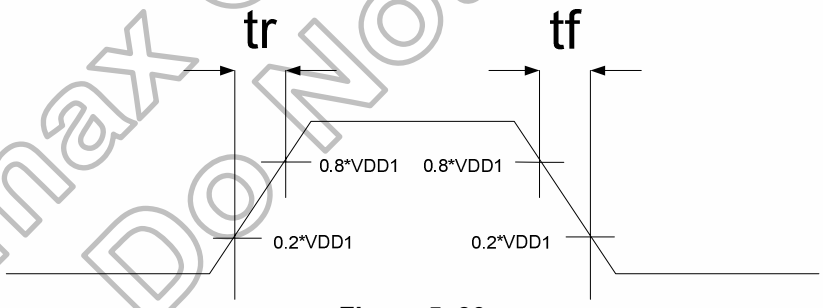


Figure 5. 30

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

5.4.3 Example 1: MPU Write is faster than Panel Read

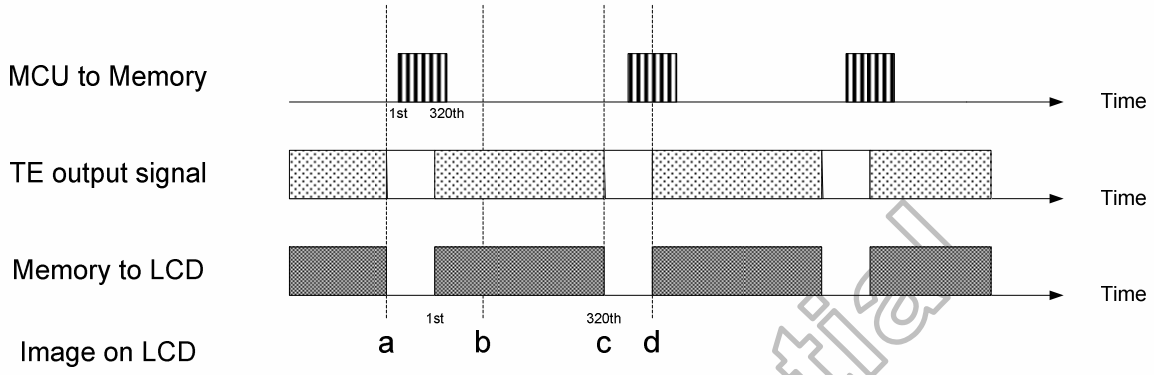


Figure 5. 31

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

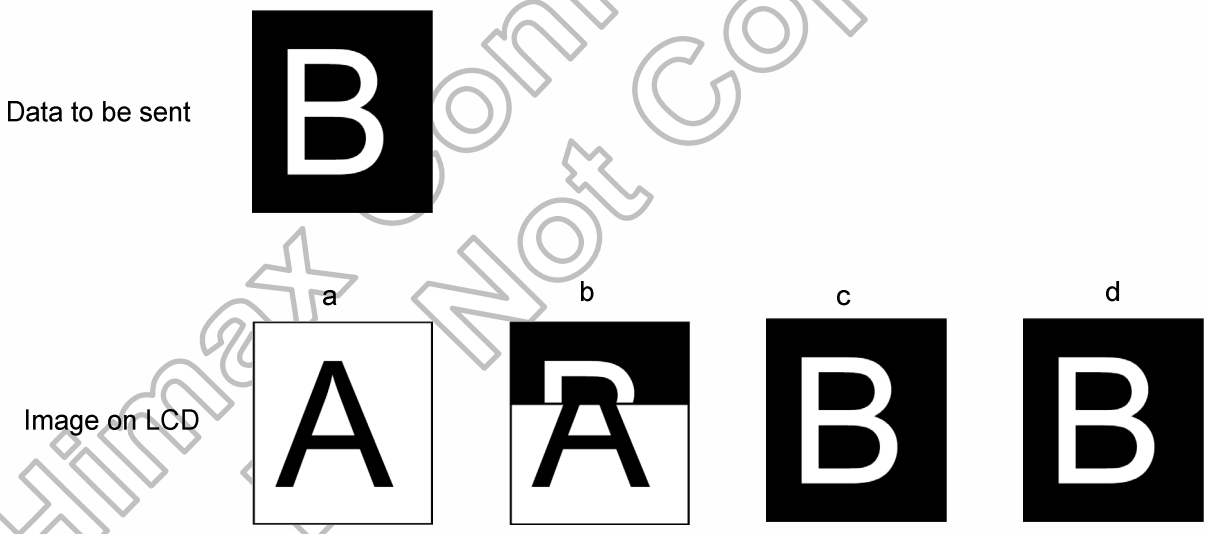


Figure 5. 32

5.4.4 Example 2: MPU Write is slower than Panel Read

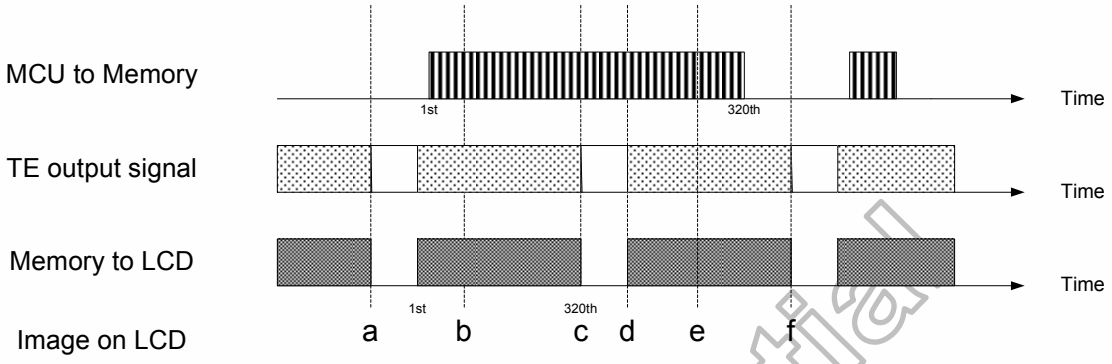


Figure 5. 33

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

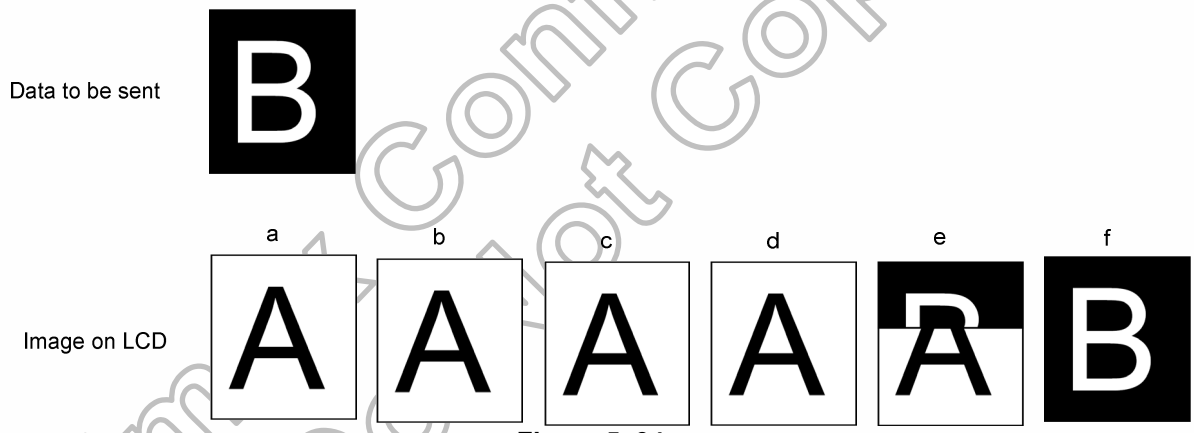


Figure 5. 34

5.5 Oscillator

The HX8346-A has an internal oscillator without extra external components that provide a source for system clock generator.

5.6 Source Driver

The HX8346-A contains a 720 channel of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately output from each channel.

5.7 Gate Driver

The HX8346-A contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.8 LCD POWER GENERATION CIRCUIT

5.8.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

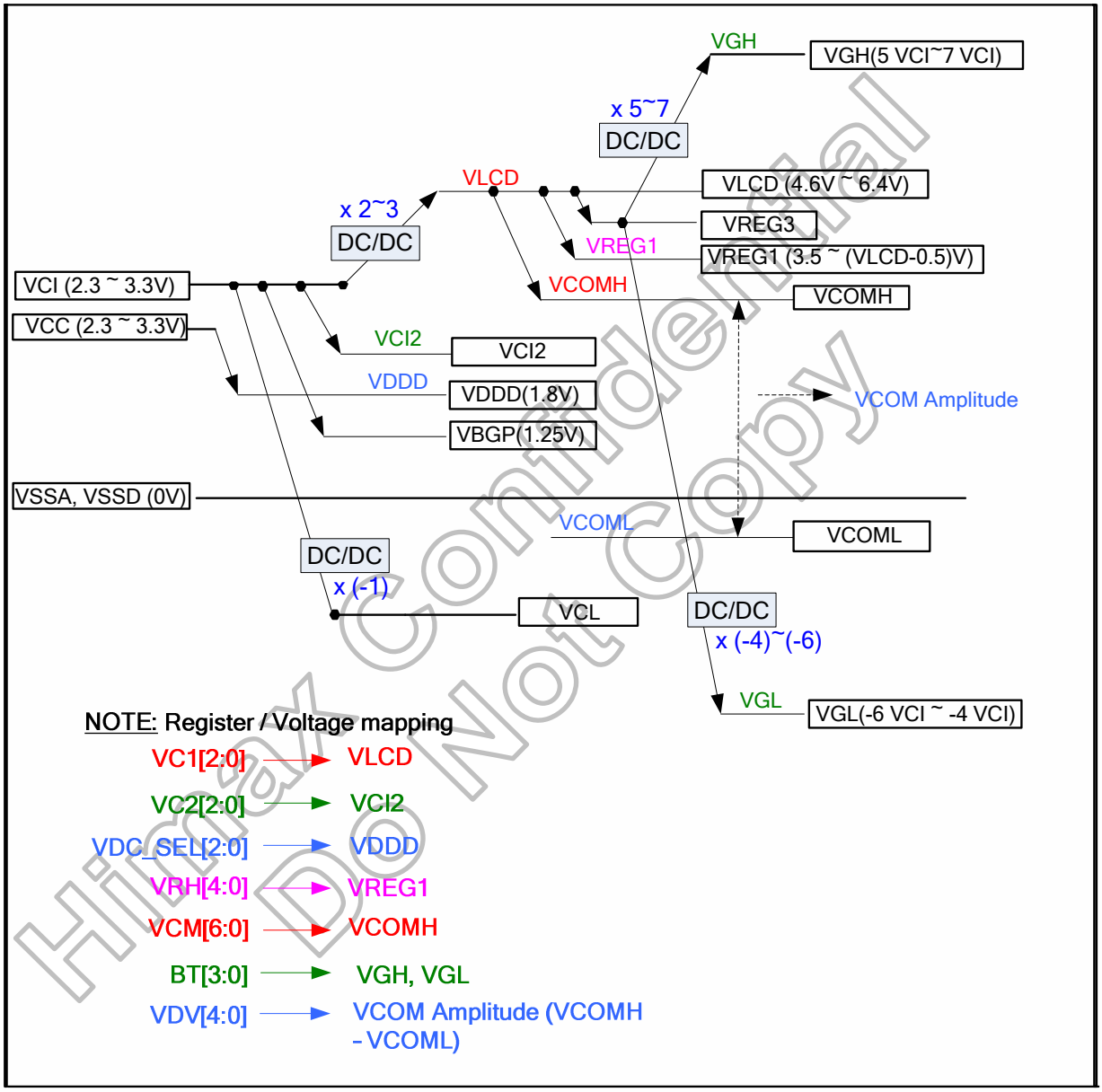


Figure 5. 35 LCD power generation scheme

5.8.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

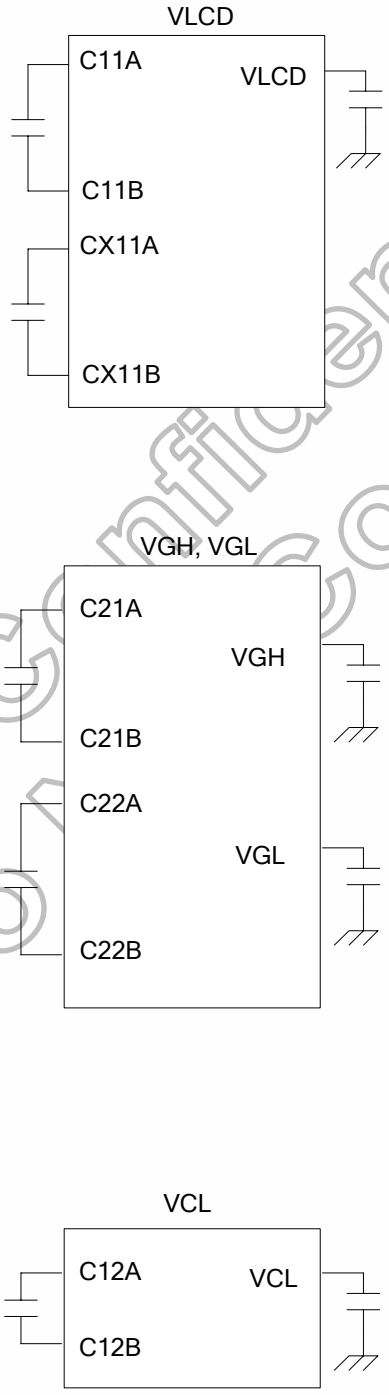


Figure 5. 36 Various boosting steps

5.9 Gray Voltage Generator for Source Driver

The HX8346-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

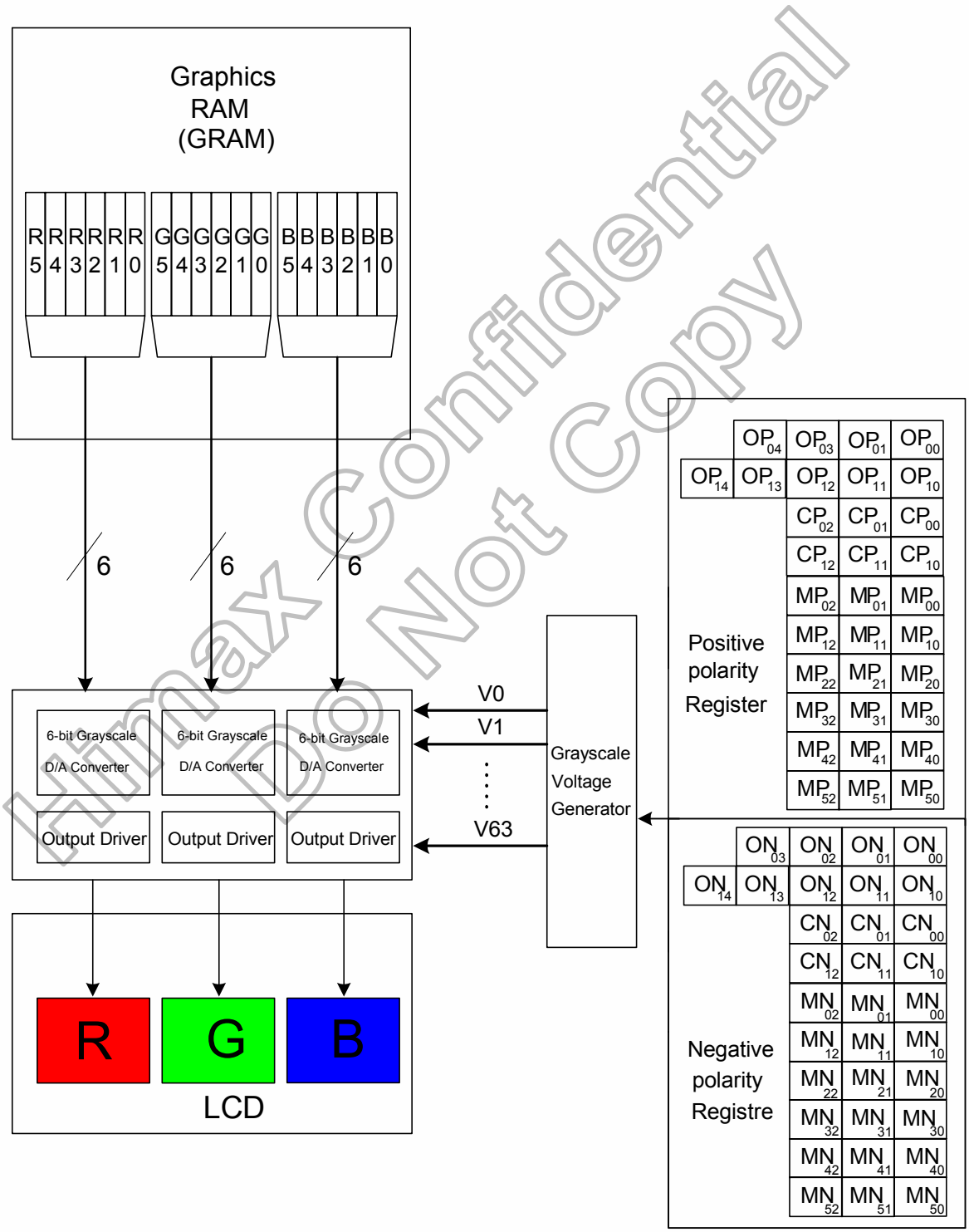


Figure 5. 37

5.9.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment , the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

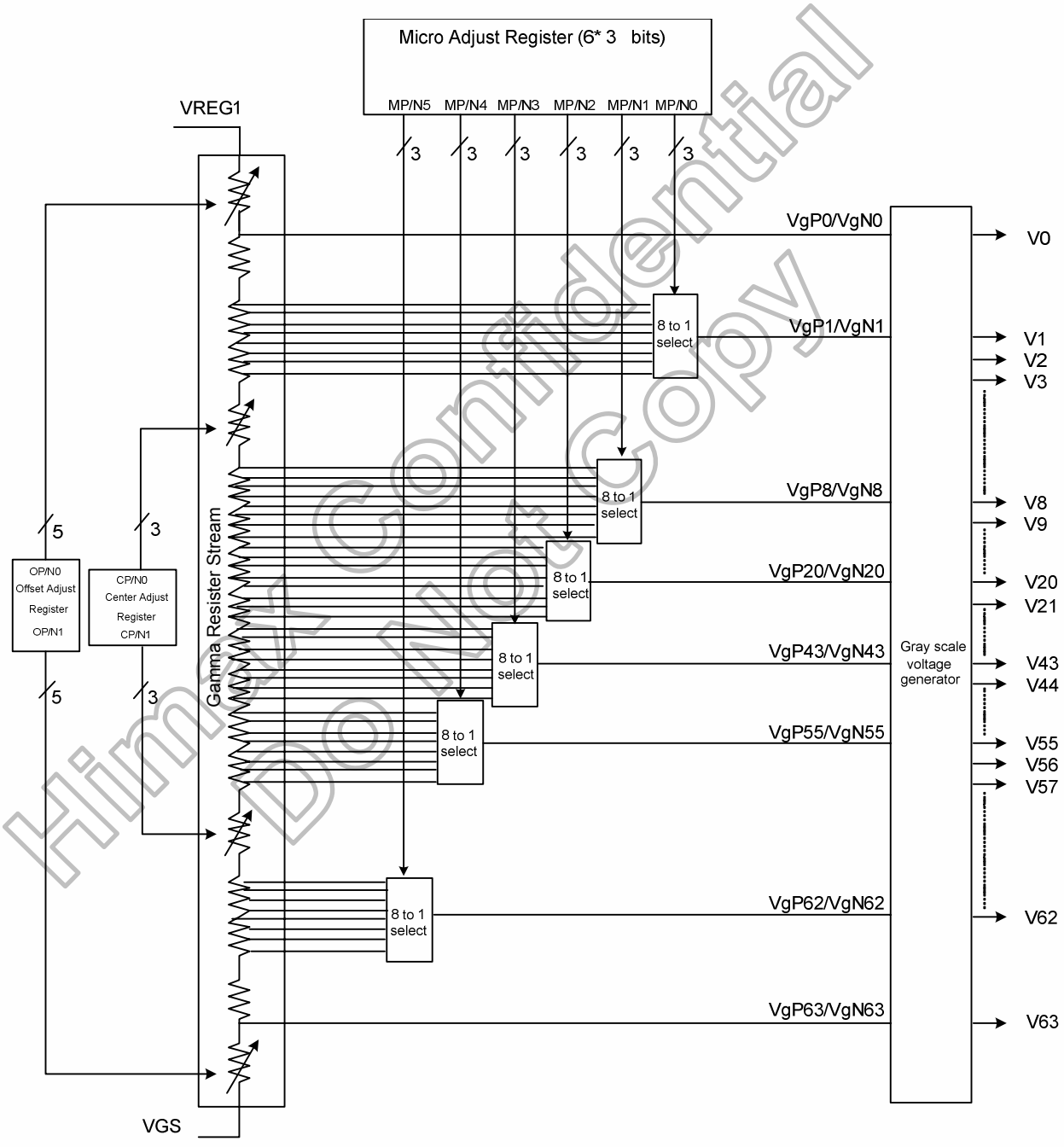


Figure 5. 38 Structure of Grayscale Voltage Generator

5.9.2 Gamma-Characteristics Adjustment Register

This HX8346-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

5.9.2.1 Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

5.9.2.2 Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

5.9.3 Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (NP/N0~5), each of which has 8 inputs and generate one reference voltage output (Vg(P/N)0, 4, 32, 80, 176, 224, 252, 256). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	NP0 2-0	NN0 2-0	8-to-1 selector (voltage level of grayscale 4)
	NP1 2-0	NN1 2-0	8-to-1 selector (voltage level of grayscale 32)
	NP2 2-0	NN2 2-0	8-to-1 selector (voltage level of grayscale 80)
	NP3 2-0	NN3 2-0	8-to-1 selector (voltage level of grayscale 176)
	NP4 2-0	NN4 2-0	8-to-1 selector (voltage level of grayscale 224)
	NP5 2-0	NN5 2-0	8-to-1 selector (voltage level of grayscale 252)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Table 5. 10 Gamma-Adjustment Registers

5.9.4 Gamma resister stream and 8 to 1 Selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

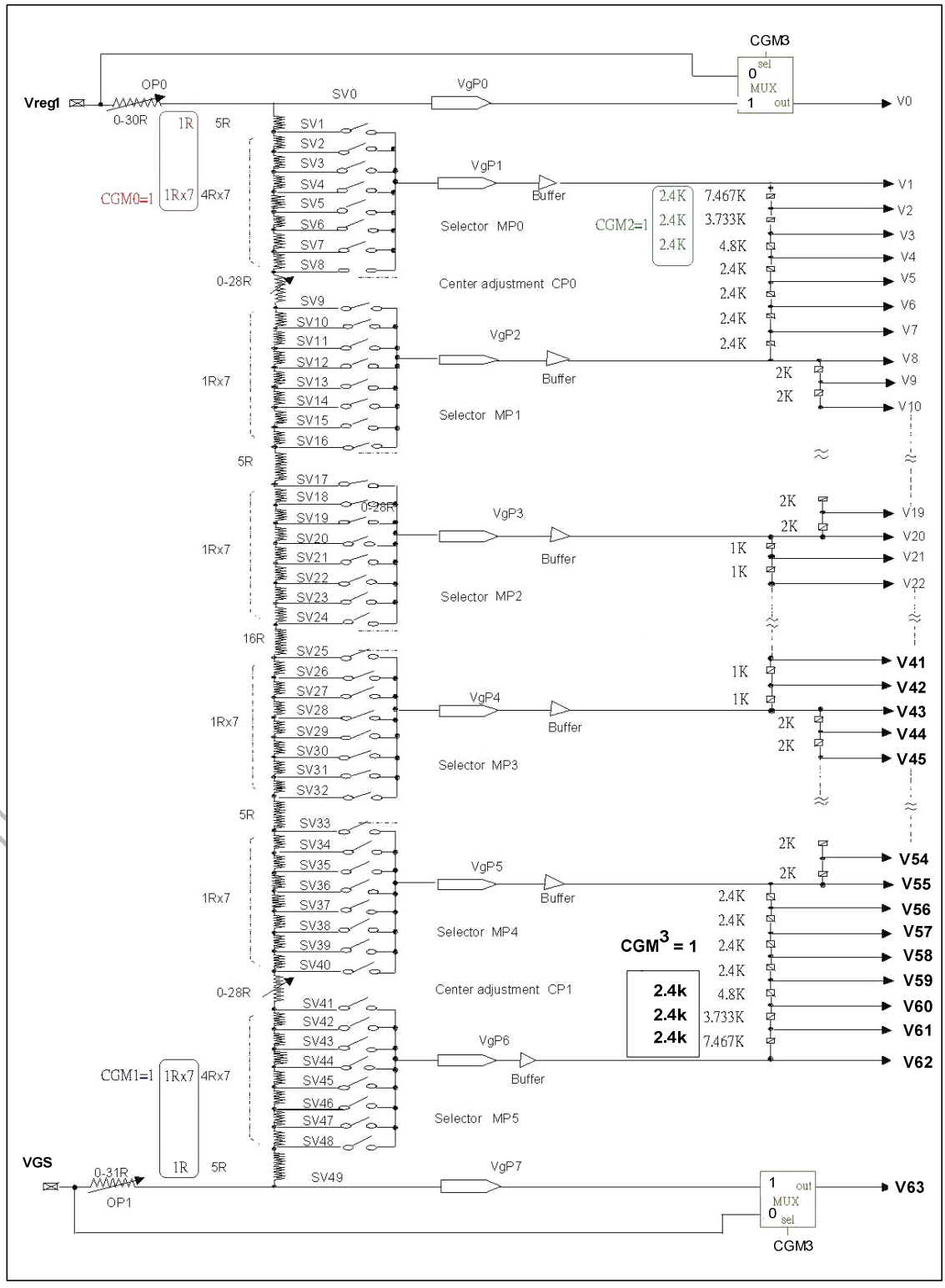


Figure 5. 39 Gamma Resister Stream and Gamma Reference Voltage

5.9.5 Variable resister

There are two types of variable resistors, one is for center adjustment, the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
• • •	• • •
1101	26R
1110	28R
1111	30R

Table 5. 11 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
• • •	• • •
11101	29R
11110	30R
11111	31R

Table 5. 12 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5. 13 Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 4	Vg(P/N) 32	Vg(P/N) 80	Vg(P/N) 176	V(P/N) 224	V(P/N) 252
000	VR1	VR9	VR17	VR25	VR33	VR41
001	VR2	VR10	VR18	VR26	VR34	VR42
010	VR3	VR11	VR19	VR27	VR35	VR43
011	VR4	VR12	VR20	VR28	VR36	VR44
100	VR5	VR13	VR21	VR29	VR37	VR45
101	VR6	VR14	VR22	VR30	VR38	VR46
110	VR7	VR15	VR23	VR31	VR39	VR47
111	VR8	VR16	VR24	VR32	VR40	VR48

Table 5. 14 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	----	[(VREG1-VD*VROP0 /SumRP)] *GSEL +VREG1-(VREG1*GSEL)	VP0
VgP1	NP0 2-0=000	VREG1-VD[(VROP0+(CGMP0*1R)+5R- (CGMP0*5R)] /SumRP	VP1
	NP0 2-0=001	VREG1-VD[(VROP0+(CGMP0*2R)+9R- (CGMP0*9R)] /SumRP	VP2
	NP0 2-0=010	VREG1-VD[(VROP0+(CGMP0*3R)+13R- (CGMP0*13R)] /SumRP	VP3
	NP0 2-0=011	VREG1-VD[(VROP0+(CGMP0*4R)+17R- (CGMP0*17R)] /SumRP	VP4
	NP0 2-0=100	VREG1-VD[(VROP0+(CGMP0*5R)+21R- (CGMP0*21R)] /SumRP	VP5
	NP0 2-0=101	VREG1-VD[(VROP0+(CGMP0*6R)+25R- (CGMP0*25R)] /SumRP	VP6
	NP0 2-0=110	VREG1-VD[(VROP0+(CGMP0*7R)+29R- (CGMP0*29R)] /SumRP	VP7
	NP0 2-0=111	VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R)] /SumRP	VP8
VgP8	NP1 2-0=000	VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R) +VRCP0] /SumRP	VP9
	NP1 2-0=001	VREG1-VD[(VROP0+(CGMP0*9R)+34R- (CGMP0*34R) +VRCP0] /SumRP	VP10
	NP1 2-0=010	VREG1-VD[(VROP0+(CGMP0*10R)+35R- (CGMP0*35R) +VRCP0] /SumRP	VP11
	NP1 2-0=011	VREG1-VD[(VROP0+(CGMP0*11R)+36R- (CGMP0*36R) +VRCP0] /SumRP	VP12
	NP1 2-0=100	VREG1-VD[(VROP0+(CGMP0*12R)+37R- (CGMP0*37R) +VRCP0] /SumRP	VP13
	NP1 2-0=101	VREG1-VD[(VROP0+(CGMP0*13R)+38R- (CGMP0*38R) +VRCP0] /SumRP	VP14
	NP1 2-0=110	VREG1-VD[(VROP0+(CGMP0*14R)+39R- (CGMP0*39R) +VRCP0] /SumRP	VP15
	NP1 2-0=111	VREG1-VD[(VROP0+(CGMP0*15R)+40R- (CGMP0*40R) +VRCP0] /SumRP	VP16
VgP20	NP2 2-0=000	VREG1-VD[(VROP0+(CGMP0*20R)+45R- (CGMP0*45R) +VRCP0] /SumRP	VP17
	NP2 2-0=001	VREG1-VD[(VROP0+(CGMP0*21R)+46R- (CGMP0*46R) +VRCP0] /SumRP	VP18
	NP2 2-0=010	VREG1-VD[(VROP0+(CGMP0*22R)+47R- (CGMP0*47R) +VRCP0] /SumRP	VP19
	NP2 2-0=011	VREG1-VD[(VROP0+(CGMP0*23R)+48R- (CGMP0*48R) +VRCP0] /SumRP	VP20
	NP2 2-0=100	VREG1-VD[(VROP0+(CGMP0*24R)+49R- (CGMP0*49R) +VRCP0] /SumRP	VP21
	NP2 2-0=101	VREG1-VD[(VROP0+(CGMP0*25R)+50R- (CGMP0*50R) +VRCP0] /SumRP	VP22
	NP2 2-0=110	VREG1-VD[(VROP0+(CGMP0*26R)+51R- (CGMP0*51R) +VRCP0] /SumRP	VP23
	NP2 2-0=111	VREG1-VD[(VROP0+(CGMP0*27R)+52R- (CGMP0*52R) +VRCP0] /SumRP	VP24
VgP43	NP3 2-0=000	VREG1-VD[(VROP0+(CGMP0*43R)+68R- (CGMP0*68R) +VRCP0] /SumRP	VP25
	NP3 2-0=001	VREG1-VD[(VROP0+(CGMP0*44R)+69R- (CGMP0*69R) +VRCP0] /SumRP	VP26
	NP3 2-0=010	VREG1-VD[(VROP0+(CGMP0*45R)+70R- (CGMP0*70R) +VRCP0] /SumRP	VP27
	NP3 2-0=011	VREG1-VD[(VROP0+(CGMP0*46R)+71R- (CGMP0*71R) +VRCP0] /SumRP	VP28
	NP3 2-0=100	VREG1-VD[(VROP0+(CGMP0*47R)+72R- (CGMP0*72R) +VRCP0] /SumRP	VP29
	NP3 2-0=101	VREG1-VD[(VROP0+(CGMP0*48R)+73R- (CGMP0*73R) +VRCP0] /SumRP	VP30
	NP3 2-0=110	VREG1-VD[(VROP0+(CGMP0*49R)+74R- (CGMP0*74R) +VRCP0] /SumRP	VP31
	NP3 2-0=111	VREG1-VD[(VROP0+(CGMP0*50R)+75R- (CGMP0*75R) +VRCP0] /SumRP	VP32
VgP55	NP4 2-0=000	VREG1-VD[(VROP0+(CGMP0*55R)+80R- (CGMP0*80R) +VRCP0] /SumRP	VP33
	NP4 2-0=001	VREG1-VD[(VROP0+(CGMP0*56R)+81R- (CGMP0*81R) +VRCP0] /SumRP	VP34
	NP4 2-0=010	VREG1-VD[(VROP0+(CGMP0*57R)+82R- (CGMP0*82R) +VRCP0] /SumRP	VP35
	NP4 2-0=011	VREG1-VD[(VROP0+(CGMP0*58R)+83R- (CGMP0*83R) +VRCP0] /SumRP	VP36
	NP4 2-0=100	VREG1-VD[(VROP0+(CGMP0*59R)+84R- (CGMP0*84R) +VRCP0] /SumRP	VP37
	NP4 2-0=101	VREG1-VD[(VROP0+(CGMP0*60R)+85R- (CGMP0*85R) +VRCP0] /SumRP	VP38
	NP4 2-0=110	VREG1-VD[(VROP0+(CGMP0*61R)+86R- (CGMP0*86R) +VRCP0] /SumRP	VP39
	NP4 2-0=111	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0] /SumRP	VP40
VgP62	NP5 2-0=000	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1] /SumRP	VP41
	NP5 2-0=001	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+4R-(4R*CGMP1)+(CGMP1*1R)] /SumRP	VP42
	NP5 2-0=010	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+8R-(8R*CGMP1)+(CGMP1*2R)] /SumRP	VP43
	NP5 2-0=011	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+12R-(12R*CGMP1)+(CGMP1*3R)] /SumRP	VP44
	NP5 2-0=100	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+16R-(16R*CGMP1)+(CGMP1*4R)] /SumRP	VP45
	NP5 2-0=101	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+20R-(20R*CGMP1)+(CGMP1*5R)] /SumRP	VP46
	NP5 2-0=110	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+24R-(24R*CGMP1)+(CGMP1*6R)] /SumRP	VP47
	NP5 2-0=111	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+28R-(28R*CGMP1)+(CGMP1*7R)] /SumRP	VP48
VgP63	----	{ VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+33R-(33R*CGMP1)+(CGMP1*8R)] /SumRP } *GSEL+VGS-(GSEL*VGS)	VP49

Table 5. 15 Voltage Calculation Formula (Positive Polarity)

SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)
VD=(VREG1-VGS)

GRAM data settings	Formula
000000	VgP63
000001	VgP62
000010	VgP62+(VgP55-VgP62) *[CGM0 (19.2 / 67.2)+CGM1(6.4/44.8) +CGM2(19.2/67.2)]
000011	VgP62+(VgP55-VgP62) *[CGM0 (28.8 / 67.2)+CGM1(12.8/44.8) +CGM2(28.8/67.2)]
000100	VgP62+(VgP55-VgP62) *[CGM0 (41.6 / 67.2)+CGM1(19.2/44.8) +CGM2(41.6/67.2)]
000101	VgP62+(VgP55-VgP62) *[CGM0 (48 / 67.2)+CGM1(25.6/44.8) +CGM2(48/67.2)]
000110	VgP62+(VgP55-VgP62) *[CGM0 (54.4 / 67.2)+CGM1(32/44.8) +CGM2(54.4/67.2)]
000111	VgP62+(VgP55-VgP62) *[CGM0 (60.8 / 67.2)+CGM1(38.4/44.8) +CGM2(60.8/67.2)]
001000	VgP55
001001	VgP55+(VgP43-VgP55) * (8 / 96)
001010	VgP55+(VgP43-VgP55) * (16 / 96)
001011	VgP55+(VgP43-VgP55) * (24 / 96)
001100	VgP55+(VgP43-VgP55) * (32 / 96)
001101	VgP55+(VgP43-VgP55) * (40 / 96)
001110	VgP55+(VgP43-VgP55) * (48 / 96)
001111	VgP55+(VgP43-VgP55) * (56 / 96)
010000	VgP55+(VgP43-VgP55) * (66 / 96)
010001	VgP55+(VgP43-VgP55) * (74 / 96)
010010	VgP55+(VgP43-VgP55) * (82 / 96)
010011	VgP55+(VgP43-VgP55) * (90 / 96)
010100	VgP43+(VgP20-VgP43) * (1 / 96)
010101	VgP43+(VgP20-VgP43) * (5 / 96)
010110	VgP43+(VgP20-VgP43) * (9 / 96)
010111	VgP43+(VgP20-VgP43) * (13 / 96)
011000	VgP43+(VgP20-VgP43) * (17 / 96)
011001	VgP43+(VgP20-VgP43) * (21 / 96)
011010	VgP43+(VgP20-VgP43) * (25 / 96)
011011	VgP43+(VgP20-VgP43) * (29 / 96)
011100	VgP43+(VgP20-VgP43) * (33 / 96)
011101	VgP43+(VgP20-VgP43) * (37 / 96)
011110	VgP43+(VgP20-VgP43) * (41 / 96)
011111	VgP43+(VgP20-VgP43) * (45 / 96)
100000	VgP43+(VgP20-VgP43) * (50 / 96)
100001	VgP43+(VgP20-VgP43) * (54 / 96)
100010	VgP43+(VgP20-VgP43) * (58 / 96)
100011	VgP43+(VgP20-VgP43) * (62 / 96)
100100	VgP43+(VgP20-VgP43) * (66 / 96)
100101	VgP43+(VgP20-VgP43) * (70 / 96)
100110	VgP43+(VgP20-VgP43) * (74 / 96)
100111	VgP43+(VgP20-VgP43) * (78 / 96)
101000	VgP43+(VgP20-VgP43) * (82 / 96)
101001	VgP43+(VgP20-VgP43) * (86 / 96)
101010	VgP43+(VgP20-VgP43) * (90 / 96)
101011	VgP43+(VgP20-VgP43) * (94 / 96)
101100	VgP20+(VgP8-VgP20) * (4 / 96)
101101	VgP20+(VgP8-VgP20) * (12 / 96)
101110	VgP20+(VgP8-VgP20) * (20 / 96)
101111	VgP20+(VgP8-VgP20) * (28 / 96)
110000	VgP20+(VgP8-VgP20) * (38 / 96)
110001	VgP20+(VgP8-VgP20) * (46 / 96)
110010	VgP20+(VgP8-VgP20) * (54 / 96)
110011	VgP20+(VgP8-VgP20) * (62 / 96)
110100	VgP20+(VgP8-VgP20) * (70 / 96)
110101	VgP20+(VgP8-VgP20) * (78 / 96)
110110	VgP20+(VgP8-VgP20) * (86 / 96)
110111	VgP20+(VgP8-VgP20) * (94 / 96)

111000	VgP8+(VgP1-VgP8)*[CGM0 (4.8 / 67.2)+CGM1(4.8/44.8) +CGM2(4.8/139.6)]
111001	VgP8+(VgP1-VgP8)*[CGM0 (11.2 / 67.2)+CGM1(11.2/44.8) +CGM2(11.2/139.6)]
111010	VgP8+(VgP1-VgP8)*[CGM0 (17.6 / 67.2)+CGM1(17.6/44.8) +CGM2(17.6/139.6)]
111011	VgP8+(VgP1-VgP8)*[CGM0 (24 / 67.2)+CGM1(24/44.8) +CGM2(24/139.6)]
111100	VgP8+(VgP1-VgP8)*[CGM0 (35.2 / 67.2)+CGM1(30.4/44.8) +CGM2(30.4/139.6)]
111101	VgP8+(VgP1-VgP8)* *[CGM0 (45.6 / 67.2)+CGM1(36.8/44.8) +CGM2(36.8/139.6)]
111110	VgP8+(VgP1-VgP8)*[CGM0 (62.4 / 67.2)+CGM1(43.2/44.8) +CGM2 (114.3/139.6)]
111111	VgP1 + (VgP0 – VgP1) * (3 / 4)

Note: CGM [2:0] =001: CGM0=1, CGM1=0, CGM2=0.
CGM [2:0] =010: CGM0=0, CGM1=1, CGM2=0.
CGM [2:0] =100: CGM0=0, CGM1=0, CGM2=1.

Table 5. 16 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	[(VREG1-VD*VRON0 /SumRN)] *GSEL +VREG1-(VREG1*GSEL)	VN0
VgN1	NN0 2-0=000	VREG1-VD[(VRON0+(CGMN0*1R)+5R- (CGMN0*5R)] /SumRN	VN1
	NN0 2-0=001	VREG1-VD[(VRON0+(CGMN0*2R)+9R- (CGMN0*9R)] /SumRN	VN2
	NN0 2-0=010	VREG1-VD[(VRON0+(CGMN0*3R)+13R- (CGMN0*13R)] /SumRN	VN3
	NN0 2-0=011	VREG1-VD[(VRON0+(CGMN0*4R)+17R- (CGMN0*17R)] /SumRN	VN4
	NN0 2-0=100	VREG1-VD[(VRON0+(CGMN0*5R)+21R- (CGMN0*21R)] /SumRN	VN5
	NN0 2-0=101	VREG1-VD[(VRON0+(CGMN0*6R)+25R- (CGMN0*25R)] /SumRN	VN6
	NN0 2-0=110	VREG1-VD[(VRON0+(CGMN0*7R)+29R- (CGMN0*29R)] /SumRN	VN7
	NN0 2-0=111	VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R)] /SumRN	VN8
VgN8	NN1 2-0=000	VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R) +VRCN0] /SumRN	VN9
	NN1 2-0=001	VREG1-VD[(VRON0+(CGMN0*9R)+34R- (CGMN0*34R) +VRCN0] /SumRN	VN10
	NN1 2-0=010	VREG1-VD[(VRON0+(CGMN0*10R)+35R- (CGMN0*35R) +VRCN0] /SumRN	VN11
	NN1 2-0=011	VREG1-VD[(VRON0+(CGMN0*11R)+36R- (CGMN0*36R) +VRCN0] /SumRN	VN12
	NN1 2-0=100	VREG1-VD[(VRON0+(CGMN0*12R)+37R- (CGMN0*37R) +VRCN0] /SumRN	VN13
	NN1 2-0=101	VREG1-VD[(VRON0+(CGMN0*13R)+38R- (CGMN0*38R) +VRCN0] /SumRN	VN14
	NN1 2-0=110	VREG1-VD[(VRON0+(CGMN0*14R)+39R- (CGMN0*39R) +VRCN0] /SumRN	VN15
	NN1 2-0=111	VREG1-VD[(VRON0+(CGMN0*15R)+40R- (CGMN0*40R) +VRCN0] /SumRN	VN16
VgN20	NN2 2-0=000	VREG1-VD[(VRON0+(CGMN0*20R)+45R- (CGMN0*45R) +VRCN0] /SumRN	VN17
	NN2 2-0=001	VREG1-VD[(VRON0+(CGMN0*21R)+46R- (CGMN0*46R) +VRCN0] /SumRN	VN18
	NN2 2-0=010	VREG1-VD[(VRON0+(CGMN0*22R)+47R- (CGMN0*47R) +VRCN0] /SumRN	VN19
	NN2 2-0=011	VREG1-VD[(VRON0+(CGMN0*23R)+48R- (CGMN0*48R) +VRCN0] /SumRN	VN20
	NN2 2-0=100	VREG1-VD[(VRON0+(CGMN0*24R)+49R- (CGMN0*49R) +VRCN0] /SumRN	VN21
	NN2 2-0=101	VREG1-VD[(VRON0+(CGMN0*25R)+50R- (CGMN0*50R) +VRCN0] /SumRN	VN22
	NN2 2-0=110	VREG1-VD[(VRON0+(CGMN0*26R)+51R- (CGMN0*51R) +VRCN0] /SumRN	VN23
	NN2 2-0=111	VREG1-VD[(VRON0+(CGMN0*27R)+52R- (CGMN0*52R) +VRCN0] /SumRN	VN24
VgN43	NN3 2-0=000	VREG1-VD[(VRON0+(CGMN0*43R)+68R- (CGMN0*68R) +VRCN0] /SumRN	VN25
	NN3 2-0=001	VREG1-VD[(VRON0+(CGMN0*44R)+69R- (CGMN0*69R) +VRCN0] /SumRN	VN26
	NN3 2-0=010	VREG1-VD[(VRON0+(CGMN0*45R)+70R- (CGMN0*70R) +VRCN0] /SumRN	VN27
	NN3 2-0=011	VREG1-VD[(VRON0+(CGMN0*46R)+71R- (CGMN0*71R) +VRCN0] /SumRN	VNP8
	NN3 2-0=100	VREG1-VD[(VRON0+(CGMN0*47R)+72R- (CGMN0*72R) +VRCN0] /SumRN	VN29
	NN3 2-0=101	VREG1-VD[(VRON0+(CGMN0*48R)+73R- (CGMN0*73R) +VRCN0] /SumRN	VN30
	NN3 2-0=110	VREG1-VD[(VRON0+(CGMN0*49R)+74R- (CGMN0*74R) +VRCN0] /SumRN	VN31
	NN3 2-0=111	VREG1-VD[(VRON0+(CGMN0*50R)+75R- (CGMN0*75R) +VRCN0] /SumRN	VN32
VgN55	NN4 2-0=000	VREG1-VD[(VRON0+(CGMN0*55R)+80R- (CGMN0*80R) +VRCN0] /SumRN	VN33
	NN4 2-0=001	VREG1-VD[(VRON0+(CGMN0*56R)+81R- (CGMN0*81R) +VRCN0] /SumRN	VN34
	NN4 2-0=010	VREG1-VD[(VRON0+(CGMN0*57R)+82R- (CGMN0*82R) +VRCN0] /SumRN	VN35
	NN4 2-0=011	VREG1-VD[(VRON0+(CGMN0*58R)+83R- (CGMN0*83R) +VRCN0] /SumRN	VN36
	NN4 2-0=100	VREG1-VD[(VRON0+(CGMN0*59R)+84R- (CGMN0*84R) +VRCN0] /SumRN	VN37
	NN4 2-0=101	VREG1-VD[(VRON0+(CGMN0*60R)+85R- (CGMN0*85R) +VRCN0] /SumRN	VN38
	NN4 2-0=110	VREG1-VD[(VRON0+(CGMN0*61R)+86R- (CGMN0*86R) +VRCN0] /SumRN	VN39
	NN4 2-0=111	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0] /SumRN	VN40
VgN62	NN5 2-0=000	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1] /SumRN	VN41
	NN5 2-0=001	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+4R-(4R*CGMN1)+(CGMN1*1R)] /SumRN	VN42
	NN5 2-0=010	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+8R-(8R*CGMN1)+(CGMN1*2R)] /SumRN	VN43
	NN5 2-0=011	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+12R-(12R*CGMN1)+(CGMN1*3R)] /SumRN	VN44
	NN5 2-0=100	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+16R-(16R*CGMN1)+(CGMN1*4R)] /SumRN	VN45
	NN5 2-0=101	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+20R-(20R*CGMN1)+(CGMN1*5R)] /SumRN	VN46
	NN5 2-0=110	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+24R-(24R*CGMN1)+(CGMN1*6R)] /SumRN	VN47
	NN5 2-0=111	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+28R-(28R*CGMN1)+(CGMN1*7R)] /SumRN	VN48
VgN63	-	{ VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+33R-(33R*CGMN1)+(CGMN1*8R)]/SumRN } *GSEL+VGS-(GSEL*VGS)	VN49

Table 5. 17 Voltage Calculation Formula (Negative Polarity)

SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)

VD=(VREG1-VGS)

GRAM data settings	Formula
000000	VgN0
000001	VgN1
000010	VgN8+(VgN1-VgN8) *[CGM0 (48 / 67.2)+CGM1(38.4/44.8) +CGM2(48/67.2)]
000011	VgN8+(VgN1-VgN8)*[CGM0 (38.4 / 67.2)+CGM1(32/44.8)+ CGM2(38.4.4/67.2)]
000100	VgN8+(VgN1-VgN8) *[CGM0 (25.6 / 67.2)+CGM1(25.6/44.8)+ CGM2(25.6/67.2)]
000101	VgN8+(VgN1-VgN8) *[CGM0 (19.2 / 67.2)+CGM1(19.2/44.8)+ CGM2(19.2/67.2)]
000110	VgN8+(VgN1-VgN8) *[CGM0 (12.8 / 67.2)+CGM1(12.8/44.8)+ CGM2(12.8/67.2)]
000111	VgN8+(VgN1-VgN8) *[CGM0 (6.4 / 67.2)+CGM1(6.4/44.8) +CGM2(6.4/139.6)]
001000	VgN8
001001	VgN20+(VgN8-VgN20) * (88 / 96)
001010	VgN20+(VgN8-VgN20) * (80 / 96)
001011	VgN20+(VgN8-VgN20) * (72 / 96)
001100	VgN20+(VgN8-VgN20) * (64 / 96)
001101	VgN20+(VgN8-VgN20) * (56 / 96)
001110	VgN20+(VgN8-VgN20) * (48 / 96)
001111	VgN20+(VgN8-VgN20) * (40 / 96)
010000	VgN20+(VgN8-VgN20) * (30 / 96)
010001	VgN20+(VgN8-VgN20) * (22 / 96)
010010	VgN20+(VgN8-VgN20) * (14 / 96)
010011	VgN20+(VgN8-VgN20) * (6 / 96)
010100	VgN43+(VgN20-VgN43) * (95 / 96)
010101	VgN43+(VgN20-VgN43) * (91 / 96)
010110	VgN43+(VgN20-VgN43) * (87 / 96)
010111	VgN43+(VgN20-VgN43) * (83 / 96)
011000	VgN43+(VgN20-VgN43) * (79 / 96)
011001	VgN43+(VgN20-VgN43) * (75 / 96)
011010	VgN43+(VgN20-VgN43) * (71 / 96)
011011	VgN43+(VgN20-VgN43) * (67 / 96)
011100	VgN43+(VgN20-VgN43) * (63 / 96)
011101	VgN43+(VgN20-VgN43) * (59 / 96)
011110	VgN43+(VgN20-VgN43) * (55 / 96)
011111	VgN43+(VgN20-VgN43) * (51 / 96)
100000	VgN43+(VgN20-VgN43) * (46 / 96)
100001	VgN43+(VgN20-VgN43) * (42 / 96)
100010	VgN43+(VgN20-VgN43) * (38 / 96)
100011	VgN43+(VgN20-VgN43) * (34 / 96)
100100	VgN43+(VgN20-VgN43) * (30 / 96)
100101	VgN43+(VgN20-VgN43) * (26 / 96)
100110	VgN43+(VgN20-VgN43) * (22 / 96)
100111	VgN43+(VgN20-VgN43) * (18 / 96)
101000	VgN43+(VgN20-VgN43) * (14 / 96)
101001	VgN43+(VgN20-VgN43) * (10 / 96)
101010	VgN43+(VgN20-VgN43) * (6 / 96)
101011	VgN43+(VgN20-VgN43) * (2 / 96)
101100	VgN55+(VgN43-VgN55) * (92 / 96)
101101	VgN55+(VgN43-VgN55) * (84 / 96)
101110	VgN55+(VgN43-VgN55) * (76 / 96)
101111	VgN55+(VgN43-VgN55) * (68 / 96)
110000	VgN55+(VgN43-VgN55) * (58 / 96)
110001	VgN55+(VgN43-VgN55) * (50 / 96)
110010	VgN55+(VgN43-VgN55) * (42 / 96)
110011	VgN55+(VgN43-VgN55) * (34 / 96)
110100	VgN55+(VgN43-VgN55) * (26 / 96)
110101	VgN55+(VgN43-VgN55) * (18 / 96)
110110	VgN55+(VgN43-VgN55) * (10 / 96)
110111	VgN55+(VgN43-VgN55) * (2 / 96)

111000	VgN62+(VgN55-VgN62) *[CGM0 (62.4 / 67.2)+CGM1(40/44.8) +CGM2 (134.8/139.6)]
111001	VgN62+(VgN55-VgN62) *[CGM0 (56 / 67.2)+CGM1(33.6/44.8) +CGM2 (128.4/139.6)]
111010	VgN62+(VgN55-VgN62) *[CGM0 (49.6 / 67.2)+CGM1(27.2/44.8) +CGM2 (122/139.6)]
111011	VgN62+(VgN55-VgN62) *[CGM0 (43.2 / 67.2)+CGM1(20.8/44.8) +CGM2 (115.6/139.6)]
111100	VgN62+(VgN55-VgN62) *[CGM0 (32 / 67.2)+CGM1(14.4/44.8) +CGM2 (109.2/139.6)]
111101	VgN62+(VgN55-VgN62) *[CGM0 (21.6 / 67.2)+CGM1(8/44.8) +CGM2 (102.8/139.6)]
111110	VgN62+(VgN55-VgN62) *[CGM0 (4.8 / 67.2)+CGM1(1.6/44.8) +CGM2 (25.3/139.6)]
111111	VgN63+(VgN62-VgN63) * (1 / 4)

Note: CGM [2:0] =001: CGM0=1, CGM1=0, CGM2=0.
CGM [2:0] =010: CGM0=0, CGM1=1, CGM2=0.
CGM [2:0] =100: CGM0=0, CGM1=0, CGM2=1.

Table 5. 18 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

Relationship between GRAM Data and Output Level (REV = "0")

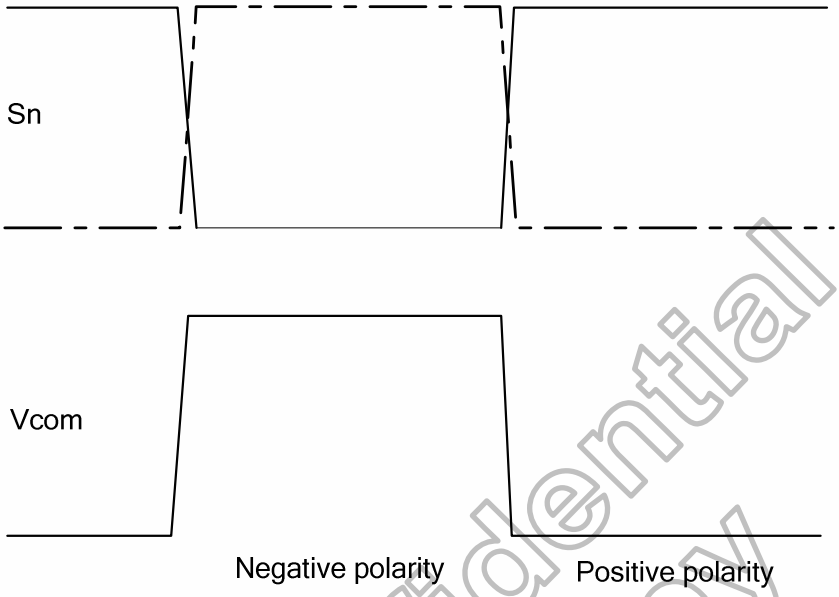
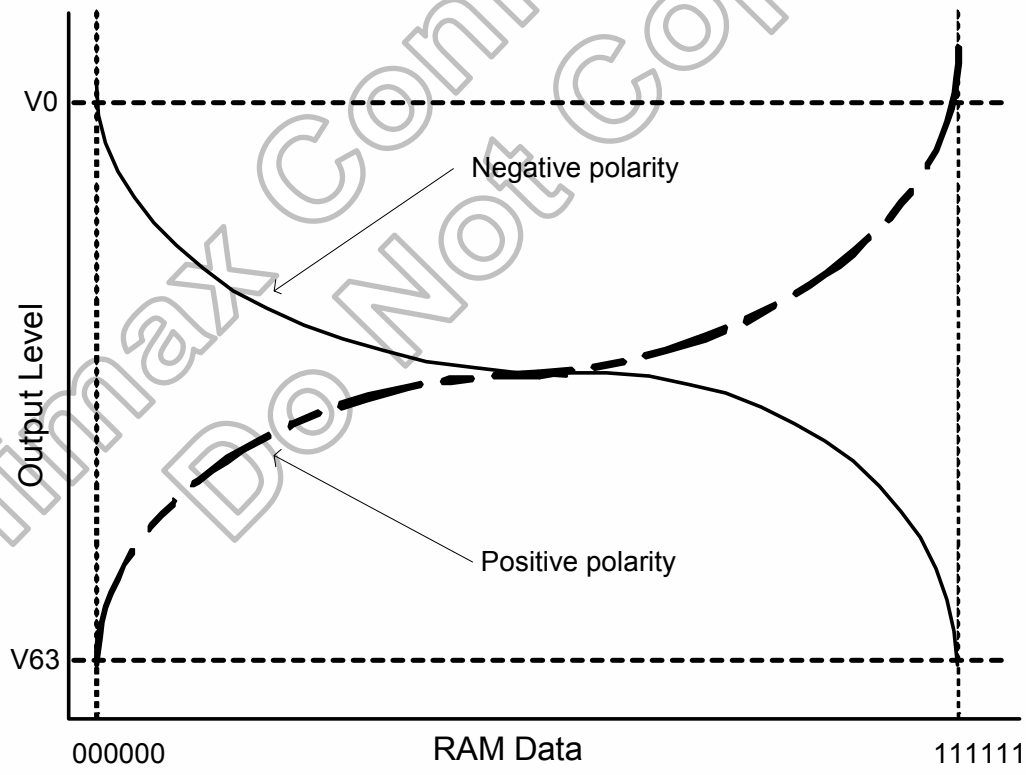


Figure 5. 40 Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 5. 41 Relationship between GRAM Data and Output Level

5.9.6 Gamma Curve Control

There are four kind of Gamma Curve is selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

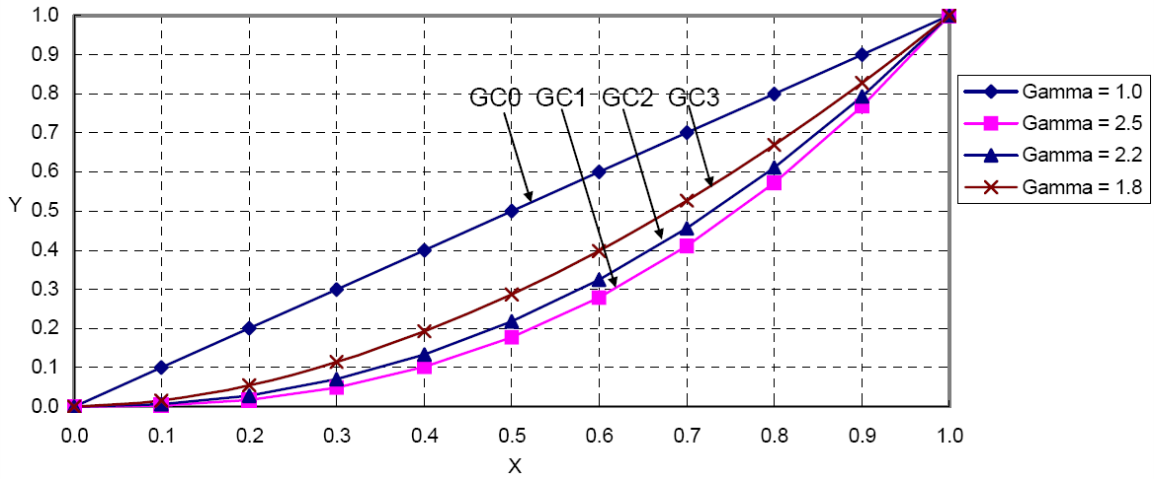


Figure 5. 42 Gamma Curve according to the GC0 to GC3 bit

5.10 Scan Mode Setting

The HX8346-A can set SM_Panel and GS_Panel pins to determine the pin assignment of gate. The combination of SM_Panel and GS_panel settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8346-A.

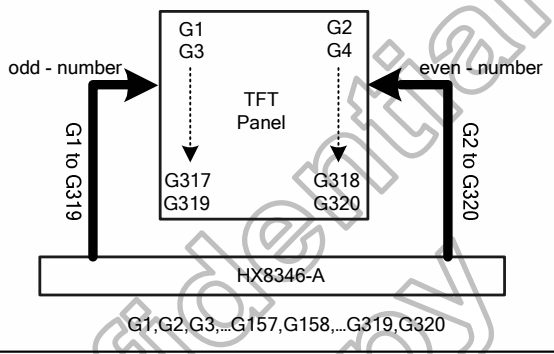
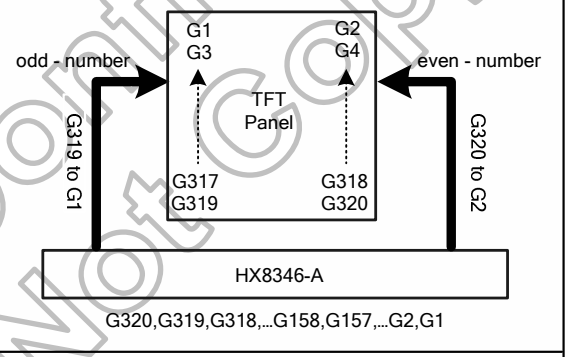
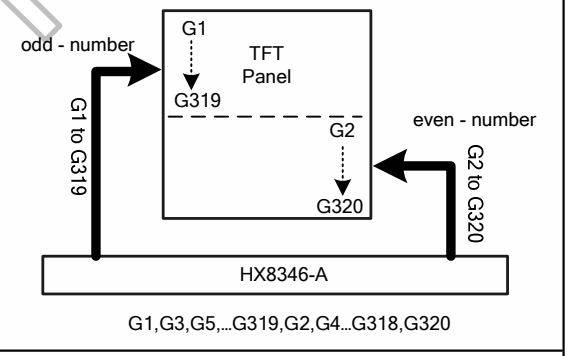
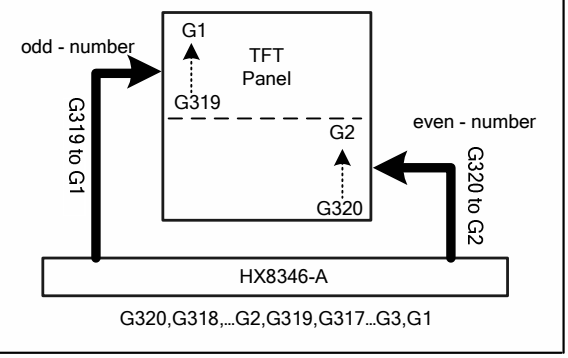
SM_Panel	GS_Panel	Scan direction
0	0	
0	1	
1	0	
1	1	

Figure 5. 43 Scan Function

5.11 Oscillator

The HX8346-A can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the OSCAD[5:0] internal register. Please refer to extended command set B0h. The default frequency is 5.58 MHz.

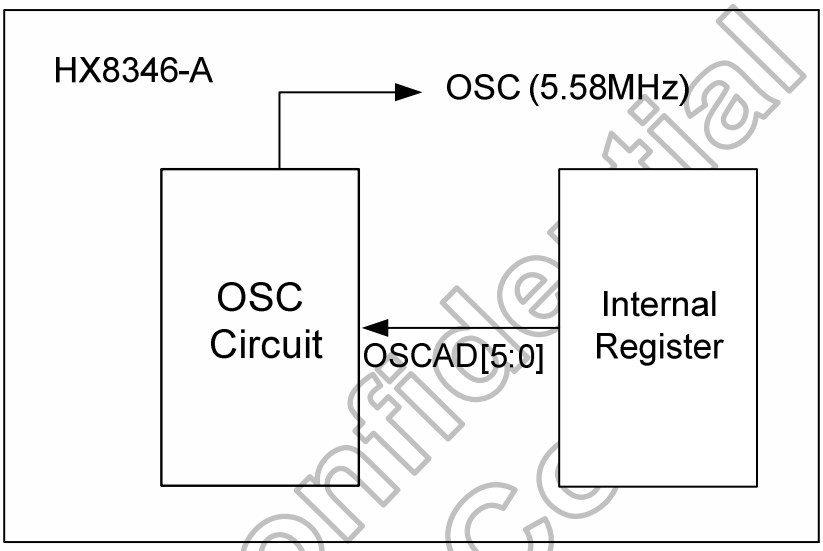


Figure 5. 44 Oscillation Circuit

5.12 Register Setting Flow (Register-Content Interface mode only)

The following are the sequences of register setting flow that applied to the HX8346-A driving the TFT display, when operate in Register-Content interface mode.

Display On/Off Set flow

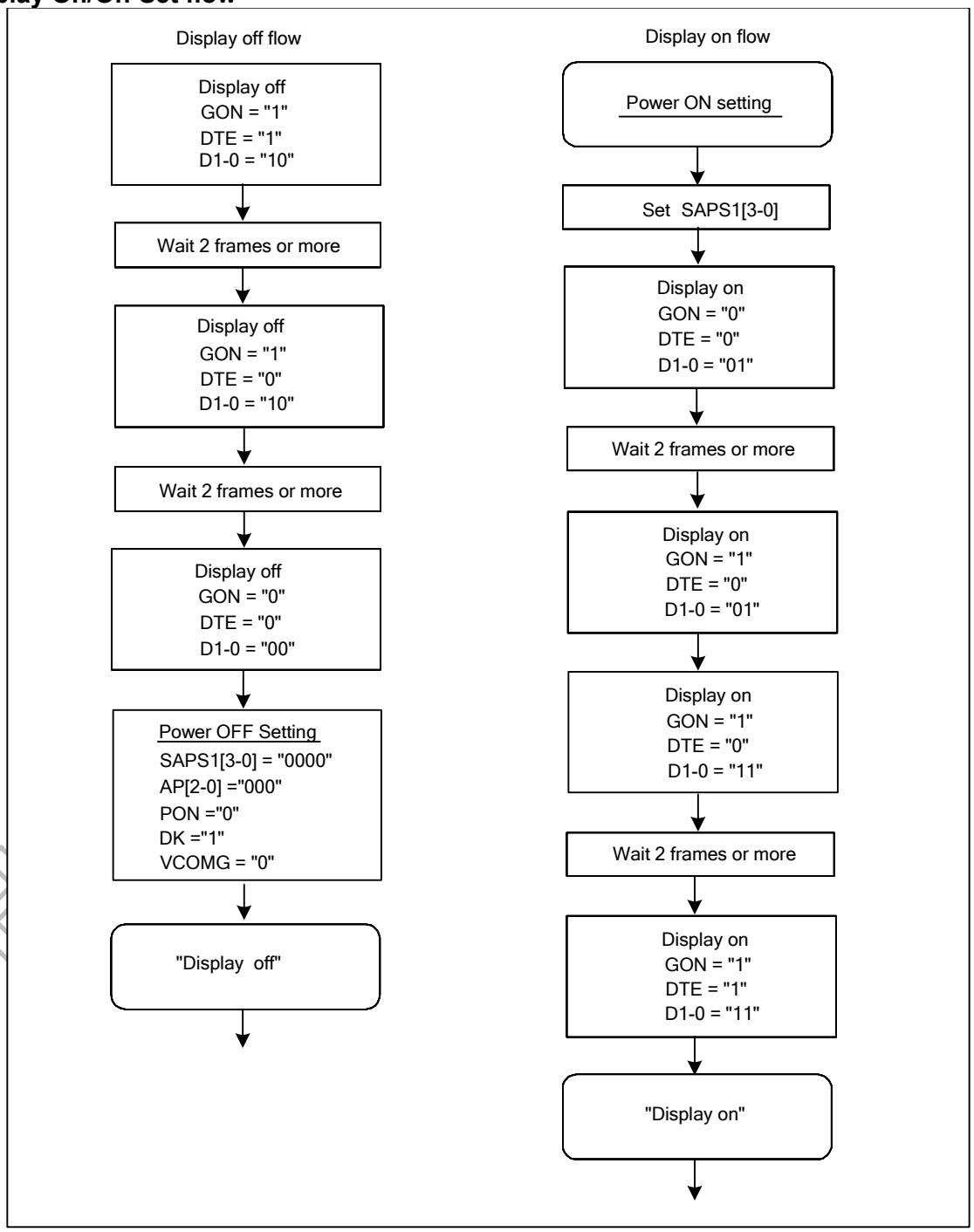
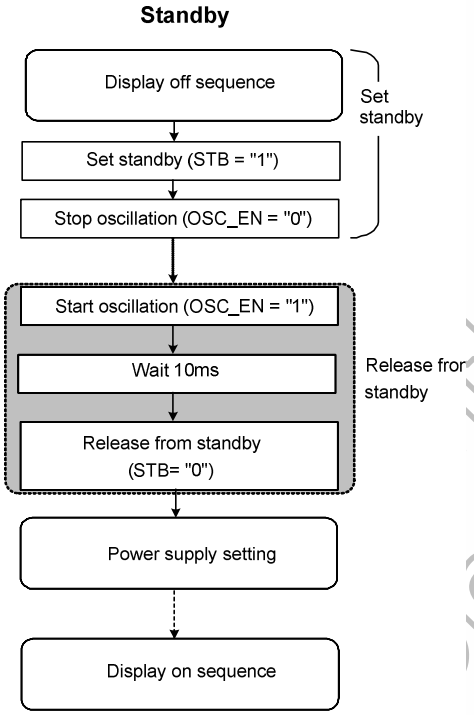


Figure 5. 45 Display On/Off Set Sequence

Standby Mode Set flow



Note: HX8346-A doesn't have the Sleep mode in Register-Content interface mode.

Figure 5. 46 Standby Mode Setting Sequence

5.13 Power Supply Setting

The power supply setting sequence of the HX8346-A is follow as blew.

Power Supply Setting Flow

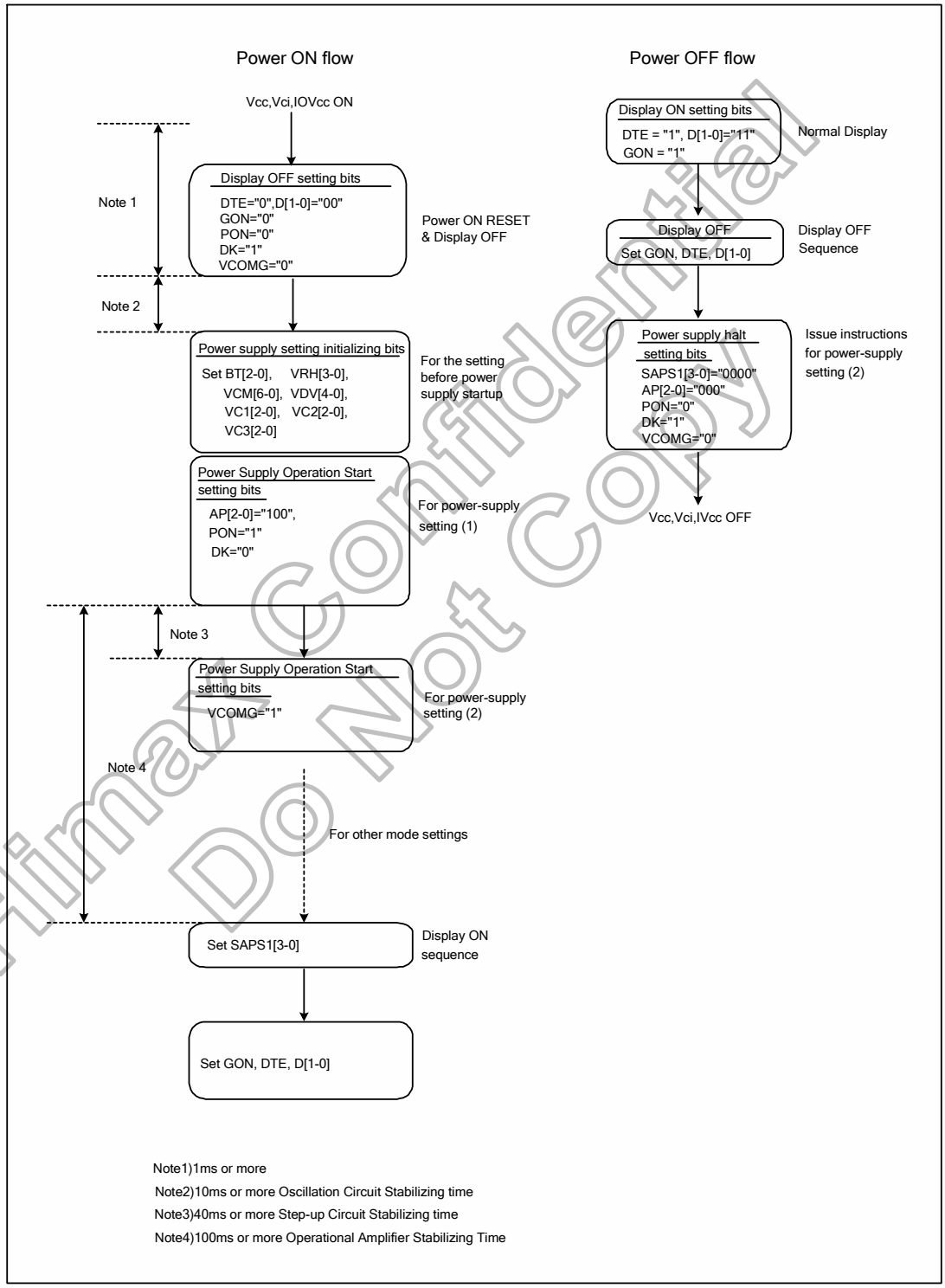


Figure 5. 47 Power Supply Setting Flow

5.14 INPUT / OUTPUT PIN STATE

5.14.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from D17-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

Table 5. 19 The State of Output or Bi-directional (I/O) Pins

5.14.2 Input Pins

Input pins	After Power On	After Hardware Reset
NRESET	Input valid	Input valid
NCS	Input valid	Input valid
DNC_SCL	Input valid	Input valid
NWR_RNW	Input valid	Input valid
NRD_E	Input valid	Input valid
D17 to D0	Input valid	Input valid
HSYNC	Input valid	Input valid
VSYNC	Input valid	Input valid
DOTCLK	Input valid	Input valid
ENABLE	Input valid	Input valid
OSC, CM, P68, BS2, BS1, BS0	Input valid	Input valid
EXTC	Input valid	Input valid

Table 5. 20 The State of Input Pins

5.15 OTP programming

Index	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x03h~0x00h	SDMYP3[7:0]								SDMYP2[7:0]								SDMYP1[7:0]								SDMYP0[7:0]							
0x07h~0x04h	(No use)			SDMYB3[4:0]					(No use)			SDMYB2[4:0]					(No use)			SDMYB1[4:0]					OTP_NVALID	(No use)			SDMYB0[4:0]		
0x0Bh~0x08h	(No use)								(No use)				VRH[3:0]				(No use)				BGP[3:0]				OTP_NVALID	(No use)		OSCADJ[5:0]				
0x0Fh~0x0Ch	(No use)		(No use)		VDV[4:0]				(No use)		VCM[6:0]						ID3[7:0]								OTP_NVALID	ID2[6:0]						
0x13h~0x10h	(No use)		(No use)		VDV[4:0]				(No use)		VCM[6:0]						ID3[7:0]								OTP_NVALID	ID2[6:0]						
0x17h~0x14h	(No use)		(No use)		VDV[4:0]				(No use)		VCM[6:0]						ID3[7:0]								OTP_NVALID	ID2[6:0]						

Programming flow

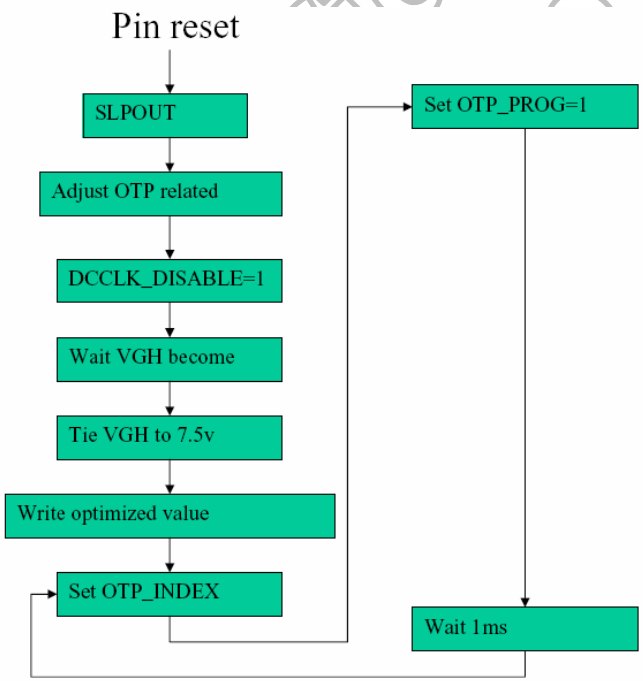


Figure 5. 48 OTP programming flow

5.16 Free Running Mode Specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60degC. In order to drive the modules this requires extra electronics. To reduce the burn-in cost it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Note, the black and the white pattern are reversed in case of a normally black display.

Parameter	Symbol	Description
Power supply pins	IOVCC, VCI, VCC	All power supply pins
Free running mode(1)	BURN	BURN = H, FR-mode is enabled, BURN = open, FR-mode is disabled
Reset	NRESET	Active low pulse in order to start the FR-mode.
Chip select(2)	NCS	This pin will be left open during FR-mode.
Data enable(2)	ENABLE	This pin will be left open during FR-mode.
Reads/not write(2)	NWR_RNW	This pin will be left open during FR-mode.
Data/not command(2)	DNC_SCL	This pin will be left open during FR-mode.
Interface select(2)	IFSEL	This pin will be left open during FR-mode.
Horizontal sync(2)	HSYNC	This pin will be left open during FR-mode.
Vertical sync(2)	VSYNC	This pin will be left open during FR-mode.
Data clock	DOTCLK	This pin will be left open during FR-mode.
CPU I/F Data(2)	D[17,0]	This pin will be left open during FR-mode.
SPI I/F Data(2)	SDI	This pin will be left open during FR-mode.
Display color mode	CM	This pin will be left open during FR-mode.
Display on	SHUT	This pin will be left open during FR-mode.

Note: (1) The BURN-pin has a pull down resistor inside the driver IC, because this pin will be left open during the normal operation in the application. The BURN-pin must be logical high for longer than 5ms before the driver IC will switch to the FR-mode in order to avoid disturbances during normal operation.

(2) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc must be disabled, all mode select pins like data-not-command, interface-select etc and all data-bus pins must be set to eider logic high or logic low during the FR-mode.

Table 5. 21 Pin Information

Power-on sequence

The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN-pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if the driver specification allows it. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN-pin and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP start to load when Reset leave low to high.

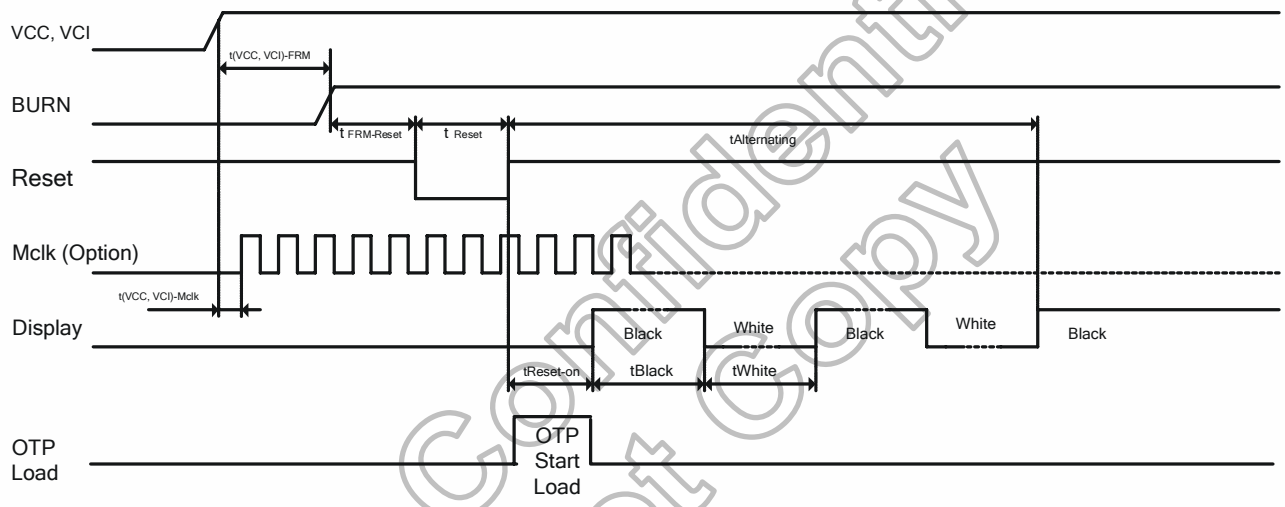


Figure 5. 49 Power on sequence of FR-mode (for Normally –White panel)

Power off sequence

The power supply can be switched off any time.

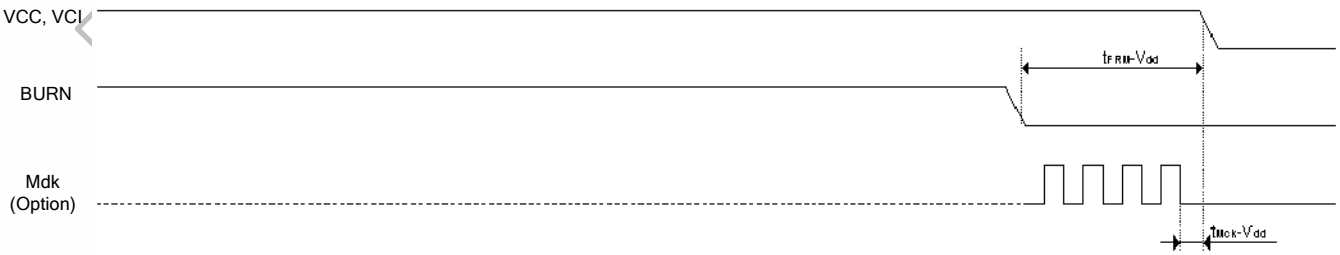


Figure 5. 50 Power off sequence of FR-mode

Free running mode display

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shall be 50%/50%. The time of the black and white pattern shall be around 1 second in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. The display is switched to a static black pattern after the alternating mode is finished. Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. It can be between 5 and 100Hz. The frame frequency will be set according to the parameter in the OTP.

Alternating black and white pattern	$t_{Alternating}$	-	5	-	min
Master clock frequency	f_{Mclk}	-	-	10	MHz

Table 5. 22 Frequency Definition of Free running mode display

7. Command Set

Register No.	Register	W/R	RS	Upper Code	Lower Code								Comment
				D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R01h	Display Mode control	W/R	1	*	*	*	*	*	IDMON (0)	INVON (0)	NORON (1)	PTLON (0)	
R02h	Column address start 2	W/R	1	*	SC[15:8] (8'b0)								
R03h	Column address start 1	W/R	1	*	SC[7:0] (8'b0)								
R04h	Column address end 2	W/R	1	*	EC[15:8] (8'b0)								
R05h	Column address end 1	W/R	1	*	EC[7:0] (8'b1110_1111)								
R06h	Row address start 2	W/R	1	*	SP[15:8] (8'b0)								
R07h	Row address start 1	W/R	1	*	SP[7:0] (8'b0)								
R08h	Row address end 2	W/R	1	*	EP[15:8] (8'b0000_0001)								
R09h	Row address end 1	W/R	1	*	EP[7:0] (8'b0011_1111)								
R0Ah	Partial area start row 2	W/R	1	*	PSL[15:8] (8'b0)								
R0Bh	Partial area start row 1	W/R	1	*	PSL[7:0] (8'b0)								
R0Ch	Partial area end row 2	W/R	1	*	PEL[15:8] (8'b0000_0001)								
R0Dh	Partial area end row 1	W/R	1	*	PEL[7:0] (8'b0011_1111)								
R0Eh	Vertical Scroll Top fixed area 2	W/R	1	*	TFA[15:8] (8'b0)								
R0Fh	Vertical Scroll Top fixed area 1	W/R	1	*	TFA[7:0] (8'b0)								
R10h	Vertical Scroll height area 2	W/R	1	*	VSA[15:8] (8'b0000_0001)								
R11h	Vertical Scroll height area 1	W/R	1	*	VSA[7:0] (8'b0011_1111)								
R12h	Vertical Scroll Button area 2	W/R	1	*	BFA[15:8] (8'b0)								
R13h	Vertical Scroll Button area 1	W/R	1	*	BFA [7:0] (8'b0)								
R14h	Vertical Scroll Start address 2	W/R	1	*	VSP [15:8] (8d'0)								
R15h	Vertical Scroll Start address 1	W/R	1	*	VSP [7:0] (8d'0)								
R16h	Memory Access control	W/R	1	*	MY(0)	MX(0)	MV(0)	*	BGR(0)	*	*	*	
R18h	Gate Scan and Scroll control	W/R	1	*	*	*	*	*	*	*	SCROLL_ EN(0))	SM(0)	
R19h	OSC Control 1	W/R	1	*	*	OSCADJ[5:0] (10_0000)						OSC_E N(1)	
R1Ah	OSC Control 2	W/R	1	*	*	*	*	*	*	*	*	OSC_ TEST(0)	
R1Bh	Power Control 1	W/R	1	*	NISDENB (0)	*	*	PON(0)	DK(0)	XDK(0)	VLCD_ TRI(0)	STB(1)	
R1Ch	Power Control 2	W/R	1	*						AP[2:0] (100)			
R1Dh	Power Control 3	W/R	1	*	*	VC2[2:0] (100)			*	VC1[2:0] (100)			
R1Eh	Power Control 4	W/R	1	*	*	*	*	*	*	VC3[2:0] (000)			
R1Fh	Power Control 5			*	*	*	*	*	VRH[3:0] (0110)				
R20h	Power Control 6	W/R	1	*	BT[3:0] (0100)				*	*	*	*	
R21h	Power Control 7	W/R	1	*	*	*	FS1[1:0] (11)		*	*	FS0[1:0] (00)		
R22h	SRAM Write Control	W/R	1	SRAM Write									
R23h	Cycle Control 1	W/R	1	*	N_DC[7:0] (1001_0101)								
R24h	Cycle Control 2	W/R	1	*	P_DC[7:0] (1001_0101)								
R25h	Cycle Control 3	W/R	1	*	I_DC[7:0] (1111_1111)								
R26h	Display Control 1	W/R	1	*	PT[1:0] (10)		GON(1)	DTE(0)	D[1:0] (00)		*	*	
R27h	Display Control 2	W/R	1	*					N_BP[3:0] (4'b0010)				
R28h	Display Control 3	W/R	1	*					N_FP[3:0] (4'b0010)				
R29h	Display Control 4	W/R	1	*					P_BP[3;0] (4'b0010)				
R2Ah	Display Control 5	W/R	1	*					P_FP[3:0] (4'b0010)				
R2Ch	Display Control 6	W/R	1	*					I_BP[3:0] (4'b0010)				
R2Dh	Display Control 7	W/R	1	*					I_FP[3:0] (4'b0010)				
R2Fh	Display Control 8	W/R	1	*	Version ID (read only)								

Register No.	Register	W/R	RS	Upper Code	Lower Code								Comment
				D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R30h	Display Control 9	W/R	1	*	-				SAPS1[3:0] (1000)				
R37h	Display Control 16	W/R	1	*	*	-	PTG[1:0] (00)		ISC[3:0] (0000)				
R38h	RGB interface control 1	W/R	1	*	*	*	*	RGB_EN(0)	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	
R3Ah	Cycle Control 1	W/R	1	*	N_RTN[3:0] (0000)				*	N_NW[2:0] (001)			
R3Bh	Cycle Control 2	W/R	1	*	P_RTN[3:0] (0000)				*	P_NW[2:0] (001)			
R3Ch	Cycle Control 3	W/R	1	*	I_RTN[3:0] (1111)				*	I_NW[2:0] (000)			
R3Dh	Cycle Control 4	W/R	1	*	*	*	*	*	*	*	DIV[1:0] (00)		
R3Eh	Cycle Control 5	W/R	1	*	SON[7:0] (8'b0011_1000)								
R40	Cycle Control 6	W/R	1	*	GDON[7:0] (8'b0000_0011)								
R41h	Cycle Control 7	W/R	1	*	GDOF[7:0] (8'b1111_1000)								
R42h	BGP Control	W/R	1	*	*	*	*	*	BGP[3:0] (1000)				
R43h	VCOM Control 1	W/R	1	*	VCOMG (1)	*	*	*	*	*	*	*	
R44h	VCOM Control 2	W/R	1	*	*	VCM[6:0] (101_1010)							
R45h	VCOM Control 3	W/R	1	*	*	*	*	VDV[4:0] (1_0001)					
R46h	r1 Control (1)	W/R	1	*	*	G1_CP12(0)	G1_CP11(1)	G1_CP10(1)	*	G1_CP02(1)	G1_CP01(0)	G1_CP00(1)	
R47h	r1 Control (2)	W/R	1	*	*	G1_CN12(1)	G1_CN11(0)	G1_CN10(1)	*	G1_CN02(0)	G1_CN01(1)	G1_CN00(1)	
R48h	r1 Control (3)	W/R	1	*	*	G1_NP12(1)	G1_NP11(0)	G1_NP10(0)	*	G1_NP02(1)	G1_NP01(1)	G1_NP00(0)	
R49h	r1 Control (4)	W/R	1	*	*	G1_NP32(0)	G1_NP31(0)	G1_NP30(1)	*	G1_NP22(1)	G1_NP21(1)	G1_NP20(0)	
R4Ah	r1 Control (5)	W/R	1	*	*	G1_NP52(0)	G1_NP51(0)	G1_NP50(0)	*	G1_NP42(0)	G1_NP41(0)	G1_NP40(0)	
R4Bh	r1 Control (6)	W/R	1	*	*	G1_NN12(1)	G1_NN11(1)	G1_NN10(1)	*	G1_NN02(1)	G1_NN01(1)	G1_NN00(1)	
R4Ch	r1 Control (7)	W/R	1	*	*	G1_NN32(0)	G1_NN31(0)	G1_NN30(1)	*	G1_NN22(1)	G1_NN21(1)	G1_NN20(0	
R4Dh	r1 Control (8)	W/R	1	*	*	G1_NN52(0)	G1_NN51(0)	G1_NN50(1)	*	G1_NN42(0)	G1_NN41(1)	G1_NN40(1)	
R4Eh	r1 Control (9)	W/R	1	*	*	*	G1_CGMP1 (0)	G1_CGMP0(0)	G1_OP03(1)	G1_OP02(1)	G1_OP01(1)	G1_OP00(1)	
R4Fh	r1 Control (10)	W/R	1	*	G1_CGM2(0)	G1_CGM1(0)	G1_CGM0 (1)	G1_OP14(0)	G1_OP13(0)	G1_OP12(1)	G1_OP11(1)	G1_OP10(1)	
R50h	r1 Control (11)	W/R	1	*	*	*	G1_CGMN1 (0)	G1_CGMN0 (0)	G1_ON03(0)	G1_ON02(1)	G1_ON01(1)	G1_ON00(1)	
R51h	r1 Control (12)	W/R	1	*	*	G1_GSEL(1)	*	G1_ON14(1)	G1_ON13(1)	G1_ON12(1)	G1_ON11(1)	G1_ON10(0)	
R52h	OTP related1	WR	1	*	OTP_MASK7 (0)	OTP_MASK6(0)	OTP_MASK5(0)	OTP_MASK4(0)	OTP_MASK3(0)	OTP_MASK2(0)	OTP_MASK1(0)	OTP_MASK0(0)	
R53h	OTP related2	WR	1	*	OTP_INDEX7(1)	OTP_INDEX6(1)	OTP_INDEX5(1)	OTP_INDEX4(1)	OTP_INDEX3(1)	OTP_INDEX2(1)	OTP_INDEX1(1)	OTP_INDEX0(1)	
R54h	OTP related3	WR	1	*	OTP_LOAD_DISABLE (0)	DCCLK_DISABLE (0)	OTP_POR (0)	OTP_PWE (0)	OTP_NVALID (1)	-	VPP_SEL (0)	OTP_PROG(0)	
R55h	Internal Use 1	W/R	1	*	*	*	*	*	*	VDC_SEL[2:0] (011)			
R56h	Internal Use 2	W/R	1	*	RPULSE[2:0] (000)			SRAM_OPT(0)	SEN_MODE(0)	SPULSE[2:0] (100)			
R57h	Internal Use 3	W/R	1	*	*	*	*	*	*	*	TEST_MODE (0)	TEST_OE(0)	
R58h	Internal Use 4	W/R	1	*	PROB[7:0] (8'b0)								
R59h	Internal Use 5	W/R	1	*	PTBA[15:8] (8'b0)								
R5Ah	Internal Use 6	W/R	1	*	PTBA[7:0] (8'b0)								
R5Bh	Internal Use 7	W/R	1	*	STBA[15:8] (8'b0)								
R5Ch	Internal Use 8	W/R	1	*	STBA[7:0] (1000_0010)								
R5Dh	Internal Use 9	W/R	1	*	*	VTESTSEL[2:0] (000)			*	*	GAOE (0)	GAM (0)	
R5Eh	Internal Use 10	W/R	1	*	BIST_CHKB1(0)	BIST_CHKB0(0)	BIST_ALL1(0)	BIST_ALL0(0)	BIST_V(0)	BIST_H(0)	BIST_OPT(0)	BIST_EN(0)	
R5Fh	Internal Use 11	W/R	1	*	ERRO_FLAG[2:0] (000)								
R60h	Internal Use 12	W/R	1	*	*	*	*	*	*	*	PULO (0)	SRAM_ADDR_MUX(0)	
R61h	Internal Use 13	W/R	1	*	*	*	*	TSA(0)	ELE(0)	TDISP_AREA(0)	TM(0)	TSC(0)	
R62h	Internal Use 14	W/R	1	*	*	*	*	*	*	*	*	TLADD[8](0)	
R63h	Internal Use 15	W/R	1	*	TLADD[7:0] (8'b0)								
R64h	Internal Use 16	R	1	*	ID1[7:0] (8'b0)								
R65h	Internal Use 17	W/R	1	*	1	ID2[7:0] (8'b0)							
R66h	Internal Use 18	W/R	1	*	ID3[7:0] (8'b0)								

Register No.	Register	W/R	RS	Upper Code	Lower Code								Comment
				D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R67h	Driver ID	R	1	*	0	1	0	0	0	1	1	0	
R68h	Internal Use 20	W/R	1	*	*	*	*	*	*	ROM_TEST_ADDR[10:8] (3'b0)			
R69h	Internal Use 21	W/R	1	*	*	*	*	*	*	ROM_ TEST(1)	ROM_ TEST_ CSB(1)	ROM_ TEST_ OEB(0)	
R70h	Logic Function register	W/R	1	*	OSC_SP EED(1)	GS(0)	SS(0)	TEMODE (0)	TEON(0)	CSEL[2:0] (111)			
R72h	Internal Use 30	W/R	1	*	*	*	*	*	*	*	TRI[1:0] (00)		
R73h	Internal Use 31	W/R	1	*	SDMYP0[7:0] (8'b1111_1111)								
R74h	Internal Use 32	W/R	1	*	*	*	*	SDMYB0[4:0](5'b1_1111)					
R75h	Internal Use 33	W/R	1	*	SDMYP1[7:0](8'b1111_1111)								
R76h	Internal Use 34	W/R	1	*	*	*	*	SDMYB1[4:0](5'b1_1111)					
R77h	Internal Use 35	W/R	1	*	SDMYP2[7:0](8'b1111_1111)								
R78h	Internal Use 36	W/R	1	*	*	*	*	SDMYB2[4:0](5'b1_1111)					
R79h	Internal Use 37	W/R	1	*	SDMYP3[7:0](8'b1111_1111)								
R7Ah	Internal Use 38	W/R	1	*	*	*	*	SDMYB3[4:0](5'b1_1111)					
R7Bh	Internal Use 39	W/R	1	*	*	*	*	SRAM_ FIX_EN (0)	*	*	*	BIST_ LOAD(0)	
R7Ch	Internal Use 40	W/R	1	*	*	*	*	*	*	*	*	DBK(1)	
R7Dh	Internal Use 41	W/R	1	*	*	*	*	*	*	BRTH[2:0] (011)			
R7Eh	Internal Use 42	W/R	1	*	*	*	*	LED_PA[3:0] (1101)					
R7Fh	Internal Use 43	W/R	1	*	*	*	*	LED_PB[3:0] (1000)					
R80h	Internal Use 44	W/R	1	*	*	*	*	PWM_PERIOD[7:3] (5'b1_1111)					
R81h	Internal Use 45	W/R	1	*	PWM_PERIOD[2:0] (3'b111)			*	*	*	*	*	
R82h	Internal Use 46	W/R	1	*				DUTY[4:0] (5'b1_1111)					
R83h	Internal Use 47	W/R	1	*	*	*	*	*	*	*	SFULL (0)	*	
R84h	Internal Use 48	W/R	1	*	*	*	*	*	*	*	IO_OPT[1:0] (2'b10)		

Table 7. 1 List Table of Register Set

7.1 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 7. 1 Index Register

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID7-0) in the range from 000000b to 1111111b in binary form.

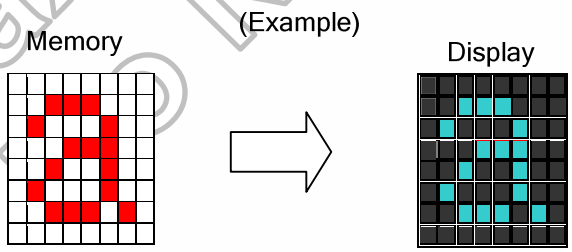
7.2 Display Mode Control Register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON	INVON (1)	NORON (1)	PTLON (0)
R	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON	INVON (1)	NORON (1)	PTLON (0)

Figure 7. 2 Display Mode Control Register (R01h)

IDMON:
This command is used for turning on/off IDLE (8-color display) mode by setting IDMON=1/0.

INVON:
This command is used to enter into display inversion mode by setting INVON=1. Vise versa, it recovers from display inversion mode by setting INVON=0. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.



NORON:
This command is used for turning on/off NORMAL mode by setting NORON=1/0.

PTLON:
This command is used for turning on/off PARTIAL mode by setting PTLON=1/0.

7.3 Column Address Start Register (R02~03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 7. 3 Column Address Start Register Upper Byte (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 7. 4 Column Address Start Register Low Byte (R03h)

7.4 Column Address End Register (R04~05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 7. 5 Column Address End Register Upper Byte (R04h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 7. 6 Column Address End Register Low Byte (R05h)

7.5 Row Address Start Register (R06~07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 7. 7 Row Address Start Register Upper Byte (R06h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 7. 8 Row Address Start Register Low Byte (R07h)

7.6 Row Address End Register (R08~09h)

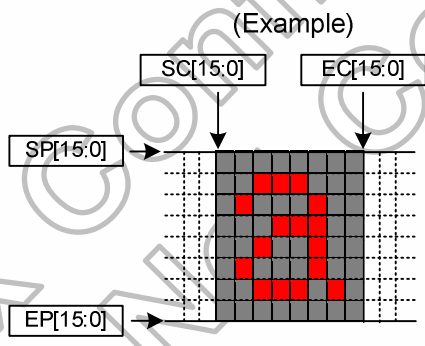
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 7. 9 Row Address End Register Upper Byte (R08h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 7. 10 Row Address End Register Low Byte (R09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. These commands make no change on the other driver status. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



7.7 Partial Area Start Row Register (R0A~0Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 7. 11 Partial Area Start Row Register Upper Byte (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 7. 12 Partial Area Start Row Register Low Byte (R0Bh)

7.8 Partial Area End Row Register (R0C~0Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

Figure 7. 13 Partial Area End Row Register Upper Byte (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

Figure 7. 14 Partial Area End Row Register Low Byte (R0Dh)

These commands (R0Ah~~0Dh) define the partial mode's display area. There are 4 parameters associated with this command, PSL[15:0], PEL[15:0], as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

7.9 Vertical Scroll Top Fixed Area Register (R0E~0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 7. 15 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 7. 16 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh)

7.10 Vertical Scroll Height Area Register (R10~11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 7. 17 Vertical Scroll Height Area Register Upper Byte (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 7. 18 Vertical Scroll Height Area Register Low Byte (R11h)

7.11 Vertical Scroll Button Fixed Area Register (R12~13h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 7. 19 Vertical Scroll Button Fixed Area Register Upper Byte (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 7. 20 Vertical Scroll Button Fixed Area Register Low Byte (R13h)

These commands (R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

7.12 Vertical Scroll Start Address Register (R14~15h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 7. 21 Vertical Scroll Start Address Register Upper Byte (R14h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

Figure 7. 22 Vertical Scroll Start Address Register Low Byte (R15h)

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display.

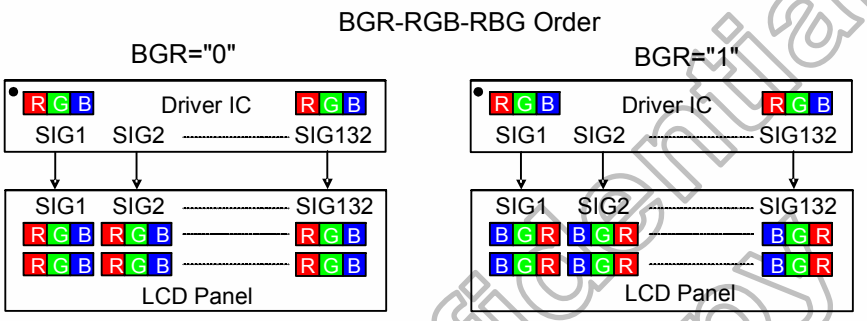
7.13 Memory Access Control Register (R16h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	MY	MX	MV	*	BGR	*	*	*
R	1	*	*	*	*	*	*	*	*	MY	MX	MV	*	BGR	*	*	*

Figure 7. 23 Memory Access Control Register (R16h)

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

BIT	NAME	DESCRIPTION
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. "MCU to memory write/read direction"
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



7.14 Gate Scan and Scroll Enable Register (R18h)

Figure 7. 24 Gate Scan and Scroll Enable Register (R18h)

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin

SCROLL_EN: Enable scroll function.
Enable: Set to high.
Disable: Set to low.

7.15 OSC Control 1 Register (R19h)

Figure 7. 25 OSC Control 1 Register (R12h)

This command is used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, High active
OSCADJ[5:0]: Internal oscillator frequency adjust, default is 5.58MHz

OSCADJ[5:0]: Internal oscillator frequency, default is 5.58MHz

OSCADJ5	OSCADJ4	OSCADJ3	OSCADJ2	OSCADJ1	OSCADJ0	Internal oscillator frequency
0	0	0	0	0	0	73.7%
0	0	0	0	0	1	74.4%
0	0	0	0	1	0	75.2%
0	0	0	0	1	1	75.9%
0	0	0	1	0	0	76.6%
0	0	0	1	0	1	77.3%
0	0	0	1	1	0	78.0%
0	0	0	1	1	1	78.7%
0	0	1	0	0	0	79.5%
0	0	1	0	0	1	80.2%
0	0	1	0	1	0	81.1%
0	0	1	0	1	1	82.0%
0	0	1	1	0	0	82.9%
0	0	1	1	0	1	83.8%
0	0	1	1	1	0	84.5%
0	0	1	1	1	1	85.4%
0	1	0	0	0	0	86.1%
0	1	0	0	0	1	86.8%
0	1	0	0	1	0	87.5%
0	1	0	0	1	1	88.2%
0	1	0	1	0	0	89.1%
0	1	0	1	0	1	89.8%
0	1	0	1	1	0	90.7%
0	1	0	1	1	1	91.6%
0	1	1	0	0	0	92.5%
0	1	1	0	0	1	93.6%
0	1	1	0	1	0	94.5%
0	1	1	0	1	1	95.2%
0	1	1	1	0	0	96.3%
0	1	1	1	0	1	97.4%
0	1	1	1	1	0	98.2%
0	1	1	1	1	1	99.3%
1	0	0	0	0	0	99.5%
1	0	0	0	0	1	100.4%
1	0	0	0	1	0	101.3%
1	0	0	0	1	1	102.2%
1	0	0	1	0	0	103.1%
1	0	0	1	0	1	104.2%
1	0	0	1	1	0	105.0%
1	0	0	1	1	1	105.9%
1	0	1	0	0	0	107.0%
1	0	1	0	0	1	108.1%
1	0	1	0	1	0	109.2%
1	0	1	0	1	1	110.2%
1	0	1	1	0	0	111.5%
1	0	1	1	0	1	112.6%
1	0	1	1	1	0	113.6%
1	0	1	1	1	1	114.9%
1	1	0	0	0	0	111.3%
1	1	0	0	0	1	112.4%
1	1	0	0	1	0	113.3%
1	1	0	0	1	1	114.2%
1	1	0	1	0	0	115.2%
1	1	0	1	0	1	116.3%
1	1	0	1	1	0	117.4%
1	1	0	1	1	1	118.5%
1	1	1	0	0	0	119.5%
1	1	1	0	0	1	120.8%
1	1	1	0	1	0	122.0%
1	1	1	0	1	1	123.1%
1	1	1	1	0	0	124.4%
1	1	1	1	0	1	125.6%
1	1	1	1	1	0	126.9%
1	1	1	1	1	1	128.1%

7.16 OSC Control 2 Register (R1Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_TEST
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_TEST

Figure 7. 26 OSC Control Register 2 (R1Ah)

OSC_TEST: If OSC is fed from OSC pin, please set OSC_TEST to 1

7.17 Power Control 1 Register (R1Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	NISD ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
R	1	*	*	*	*	*	*	*	*	NISD ENB	*	*	PON	DK	XDK	VLCD _TRI	STB

Figure 7. 27 Power Control 1 Register (R1Bh)

NISDENB: This stands for abnormal power-off supervisal function when the power is off. It's for monitoring power status by NISD pad when NISDENB is set to 0.

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation. For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

DK: Specify on/off control of step-up circuit 1 for VLCD voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

STB: When STB = "1", the HX8346-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

XDK, VLCD_TRI: Specify the ratio of step-up circuit for VLCD voltage generation.

VLCD_TRI	XDK	Step up circuit 1	Capacitor connection pins
0	0	2 x VCI	C11A, C11B
0	1	2 x VCI	C11A, C11B, CX11A, CX11B
1	0	3 x VCI	C11A, C11B, CX11A, CX11B
1	1	inhabit	inhabit

7.18 Power Control 2 Register (R1Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0

Figure 7. 28 Power Control 3 Register (R1Ch)

AP(2-0)

Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption, AP(2-0) can be set as “000” when display is off, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Power Circuit Off
0	0	1	Ignore
0	1	0	Ignore
0	1	1	Ignore
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

7.19 Power Control 3 Register (R1Dh)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VC22	VC21	VC20	*	*	VC12	VC11	VC10
R	1	*	*	*	*	*	*	*	*	VC22	VC21	VC20	*	*	VC12	VC11	VC10

Figure 7. 29 Power Control 3 Register (R1Dh)

VC1(2-0):
Specify the ratio of VBGP for VLCD voltage adjusting.

VC12	VC11	VC10	VLCD
0	0	0	inhibit
0	0	1	VBGP * 5.13
0	1	0	VBGP * 4.82
0	1	1	VBGP * 4.56
1	0	0	VBGP * 4.32
1	0	1	VBGP * 4.10
1	1	0	VBGP * 3.91
1	1	1	VBGP * 3.73

Note: VBGP is the internal reference voltage equals to 1.25V

VC2(2-0):
Specify the reference voltage VCI2 (the factor of VCI) for VGH,VGL voltage adjusting.

VC22	VC21	VC20	VCI2
0	0	0	VCI
0	0	1	0.75 x VCI
0	1	0	0.5 x VCI
0	1	1	0.25 x VCI
1	0	0	0
1	0	1	Ignore
1	1	0	Ignore
1	1	1	Ignore

7.20 Power Control 4 Register (R1Eh)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC32	VC31	VC30
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC32	VC31	VC30

Figure 7. 30 VREG3 Control Register (R1Eh)

VC3(2-0):
Specify the reference voltage VREG3 (the factor of VCI) for VGL voltage adjusting

VC32	VC31	VC30	VREG3
0	0	0	VLCD
0	0	1	2 X VCI
0	1	0	1.92 X VCI
0	1	1	1.84 X VCI
1	0	0	1.76 X VCI
1	0	1	1.68 X VCI
1	1	0	1.60 X VCI
1	1	1	HZ

7.21 Power Control 5 Register (R1Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	VRH 3	VRH 2	VRH 1	VRH 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	VRH 3	VRH 2	VRH 1	VRH 0

Figure 7. 31 Power Control 5 Register (R1Fh)

VRH(3-0):
Set the magnification of amplification for VREG1 voltage (Source output voltage range) for gamma voltage setting. It allows magnify the amplification of VBGP from 2.8 to 4.8 times.

VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	VBGP x 2.8
0	0	0	1	VBGP x 3.0
0	0	1	0	VBGP x 3.2
0	0	1	1	VBGP x 3.3
0	1	0	0	VBGP x 3.4
0	1	0	1	VBGP x 3.5
• •	• •	• •	• •	• •
1	0	0	1	VBGP x 3.9
1	0	1	0	VBGP x 4.0
1	0	1	1	VBGP x 4.2
1	1	0	0	VBGP x 4.4
1	1	0	1	VBGP x 4.6
1	1	1	0	VBGP x 4.8
1	1	1	1	Inhibited

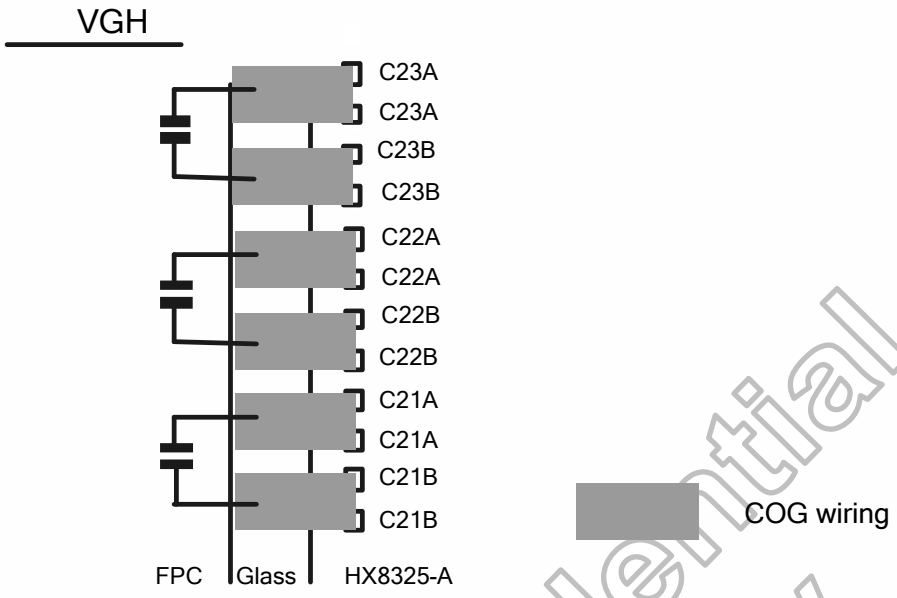
Note: VBGP is the internal reference voltage equals to 1.25V

7.22 Power Control 6 Register (R20h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	*	*
R	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	*	*

Figure 7. 32 Power Control 6 Register (R20h)

BT(3-0):
Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.



Capacitor Connection for VGH, VGL Voltage Generation

BT3	BT2	BT1	BT0	VCL	VGH	VGL	Capacitor connection pins
0	0	0	0	-1 x VCI	VREG3X3+VCI	VCI2-(VREG3X3)	VGH, VGL, VCL, C12 A/B, C21 A/B, C22A/B, C23A/B
0	0	0	1	-1 x VCI	VREG3X3+VCI	VCI2-(VREG3X2+VCI)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	0	1	0	-1 x VCI	VREG3X3+VCI	VCI2-(VREG3X2)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	0	1	1	-1 x VCI	VREG3X3	VCI2-(VREG3X3)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	1	0	0	-1 x VCI	VREG3X2+VCIX2	VCI2-(VREG3X2+VCI)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	1	0	1	-1 x VCI	VREG3X3	VCI2-(VREG3X2)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	1	1	0	-1 x VCI	VREG3X3-VCI	VCI2-(VREG3X3)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
0	1	1	1	-1 x VCI	VREG3X2+VCI	VCI2-(VREG3X2+VCI)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
1	0	0	0	-1 x VCI	VREG3X3-VCI	VCI2-(VREG3X2)	VGH, VGL, VCL, C12A/B, C21A/B, C22A/B, C23A/B
1	*	*	*	Setting Inhibited			

Note: The conditions of VCL ≦ -3.3V, VGH-VGL ≦ 32V must be satisfied.

7.23 Power Control 7 Register (R21h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*		FS11	FS10	*		FS01	FS00
R	1	*	*	*	*	*	*	*	*	*		FS11	FS10	*		FS01	FS00

Figure 7. 33 Power Control 7 Register (R21h)

FS0(1-0):
Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for VLCD voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS01	FS0	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

FS1(1-0):
Set the operating frequency of the step-up circuit 2 and 3 for VGH,VGL,VCL voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

Note : Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

7.24 Read Data Register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 7. 34 Read Data Register (R22h)

RD17-0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

Write Data Register (R22h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 7. 35 Write Data Register (R22h)

WD[15:0] : Transforms the data into 16-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

7.25 Cycle Control 1~3 Register (R23~25h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_DC 7	N_DC 6	N_DC 5	N_DC 4	N_DC 3	N_DC 2	N_DC 1	N_DC 0
R	1	*	*	*	*	*	*	*	*	N_DC 7	N_DC 6	N_DC 5	N_DC 4	N_DC 3	N_DC 2	N_DC 1	N_DC 0

Figure 7. 36 Cycle Control 1 Register (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_DC 7	P_DC 6	P_DC 5	P_DC 4	P_DC 3	P_DC 2	P_DC 1	P_DC 0
R	1	*	*	*	*	*	*	*	*	P_DC 7	P_DC 6	P_DC 5	P_DC 4	P_DC 3	P_DC 2	P_DC 1	P_DC 0

Figure 7. 37 Cycle Control 2 Register (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_DC 7	I_DC 6	I_DC 5	I_DC 4	I_DC 3	I_DC 2	I_DC 1	I_DC 0
R	1	*	*	*	*	*	*	*	*	I_DC 7	I_DC 6	I_DC 5	I_DC 4	I_DC 3	I_DC 2	I_DC 1	I_DC 0

Figure 7. 38 Cycle Control 3 Register (R25h)

N_DC: Normal mode
P_DC: Partial mode
I_DC: Idle mode

DC(7-0):
specify the clock frequency for DC/DC converter operating.

fosc = R-C oscillation frequency

DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCDCf
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	fosc
0	0	0	0	0	0	1	0	fosc/ 2
				•				•
				•				•
1	1	1	1	1	1	1	0	fosc/ 254
1	1	1	1	1	1	1	1	fosc / 255

Note: It is recommended to set DC(7-0) as “20”h, which means one charge bump clock periods 32 internal oscillation clocks.

7.26 Display Control 1 Register (R26h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*
R	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*

Figure 7. 39 Display Control 1 Register (R26h)

D[1:0]: When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8346-A can control the charging current for the LCD with AC driving. When D1–0 = 01, the internal display of the HX8346-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

PT[1:0] : Non-display area source output control see follow table

INVON /REV_PANEL	GRAM data	Source output level							
		Display area		Non-display area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 ~ 18'h3FFFF	V63 ~ V0	V0 ~ V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 ~ 18'h3FFFF	V0 ~ V63	V63 ~ V0	V0	V63	VSSD	VSSD	Hi-z	Hi-z

7.27 Display Control 2~7 Register (R27~2Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0

Figure 7. 40 Display Control 2 Register (R27h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP 3	N_BP 2	N_BP 1	N_BP 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP 3	N_BP 2	N_BP 1	N_BP 0

Figure 7. 41 Display Control 3 Register (R28h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	P_BP 3	P_BP 2	P_BP 1	P_BP 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	P_BP 3	P_BP 2	P_BP 1	P_BP 0

Figure 7. 42 Display Control 4 Register (R29h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	P_FP 3	P_FP 2	P_FP 1	P_FP 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	P_FP 3	P_FP 2	P_FP 1	P_FP 0

Figure 7. 43 Display Control 5 Register (R2Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	I_BP3	I_BP2	I_BP1	I_BP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	I_BP3	I_BP2	I_BP1	I_BP0

Figure 7. 44 Display Control 6 Register (R2Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	I_FP3	I_FP2	I_FP1	I_FP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	I_FP3	I_FP2	I_FP1	I_FP0

Figure 7. 45 Display Control 7 Register (R2Dh)

N_BP, N_FP: Back Porch and Front Porch setting in Normal mode
P_BP, P_FP: Back Porch and Front Porch setting in Partial mode
I_BP, P_FP: Back Porch and Front Porch setting in Idle mode

FP[3:0]: Specify the amount of scan line for front porch (FP).
BP[3:0]: Specify the amount of scan line for back porch (BP).

FP3 / BP3	FP2 / BP2	FP1 / BP1	FP0 / BP0	Number of FP Line / Number of BP Line
0	0	0	0	Ignore
0	0	0	1	Ignore
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Ignore

Operation Mode	BP	FP	BP + FP
System Interface	≥2 lines	≥2 lines	≤ 16 lines
RGB Interface	≥2 lines	≥2 lines	≤ 16 lines

7.28 Display Control 8 Register (R30h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	SAPS 13	SAPS 12	SAPS 11	SAPS 10
R	1	*	*	*	*	*	*	*	*	*	*	*	*	SAPS 13	SAPS 12	SAPS 11	SAPS 10

Figure 7. 46 Display Control 9 Register (R30h)

SAPS1[3:0] : Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAPS1[3–0] = 4'b0000, the current consumption can be reduced by stopping the operational amplifier.

SAPS1[3:0]				Source output driving ability
0	0	0	0	Source output all stop
0	0	0	1	0.125
0	0	1	0	0.25
0	0	1	1	0.375
0	1	0	0	0.5
0	1	0	1	0.625
0	1	1	0	0.75
0	1	1	1	0.875
1	0	0	0	1
1	0	0	1	1.125
1	0	1	0	1.25
1	0	1	1	1.375
1	1	0	0	1.5
1	1	0	1	1.625
1	1	1	0	1.75
1	1	1	1	1.875

7.29 Display Control 9 Register (R37h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	PTG 1	PTG 0	ISC 3	ISC 2	ISC 1	ISC 0
R	1	*	*	*	*	*	*	*	*	*	*	PTG 1	PTG 0	ISC 3	ISC 2	ISC 1	ISC 0

Figure 7. 47 Display Control 6 Register (R37h)

PTG[1:0]: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate outputs in non-display area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

ISC[3:0] : Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

7.30 RGB Interface Control 1 Register (R38h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
R	1	*	*	*	*	*	*	*	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL

Figure 7. 48 RGB Interface Control 1 Register (R38h)

This command is used to set RGB interface related register

EPL: Specify the polarity of Enable pin in RGB interface mode.EPL=0, the Enable is High active; EPL=1, the Enable is Low active

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

7.31 Cycle Control 1~3 Register (R3A~3Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_RTN 3	N_RTN 2	N_RTN 1	N_RTN 0	*	N_NW 2	N_NW 1	N_NW 0
R	1	*	*	*	*	*	*	*	*	N_RTN 3	N_RTN 2	N_RTN 1	N_RTN 0	*	N_NW 2	N_NW 1	N_NW 0

Figure 7. 49 Cycle Control 1 Register (R3Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_RTN 3	P_RTN 2	P_RTN 1	P_RTN 0	*	P_NW 2	P_NW 1	P_NW 0
R	1	*	*	*	*	*	*	*	*	P_RTN 3	P_RTN 2	P_RTN 1	P_RTN 0	*	P_NW 2	P_NW 1	P_NW 0

Figure 7. 50 Cycle Control 2 Register (R3Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_RTN 3	I_RTN 2	I_RTN 1	I_RTN 0	*	I_NW 2	I_NW 1	I_NW 0
R	1	*	*	*	*	*	*	*	*	I_RTN 3	I_RTN 2	I_RTN 1	I_RTN 0	*	I_NW 2	I_NW 1	I_NW 0

Figure 7. 51 Cycle Control 3 Register (R3Ch)

The driver IC support individual inversion type and clock per line for Normal display mode, Partial display mode and Idle (8-color) display mode. The resultant NW and RTN will be selected automatically according display mode.

N_ NW, N_ RTN: Normal mode
P_ NW , P_ RTN: Partial mode
I_ NW, I_ RTN: Idle mode

NW[2:0]: Frame Inversion and N-line inversion control for normal display mode.

NW[2:0]	Inversion Type
0	Frame inversion
1	1-line inversion
2	2-line inversion
3	3-line inversion
..	..
7	7-line inversion

RTN[3:0]: Set the 1-line period in a clock unit for normal display mode.

Clock cycles=1/internal operation clock frequency

RTN[3:0]	Clock Cycles per Line
4'b0000	245
4'b0001	246
4'b0010	247
4'b0011	248
….	….
4'b1110	259
4'b1111	260

7.32 Cycle Control 4 Register (R3Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DIV 1	DIV 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DIV 1	DIV 0

Figure 7. 52 Cycle Control 4 Register (R3Dh)

DIV1-0: The division ratio of clocks for internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV1-0. Frame frequency can be adjusted along with the 1H period (RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Formula for the Frame Frequency:
Frame frequency = fosc/(RTN × DIV × (NL+BP+FP)) [HZ]
fosc: RC oscillation frequency

7.33 Cycle Control 5 Register (R3Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0
R	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0

Figure 7. 53 Display Control 5 Register (R3Eh)

7.34 Cycle Control 6 Register (R40h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0
R	1	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0

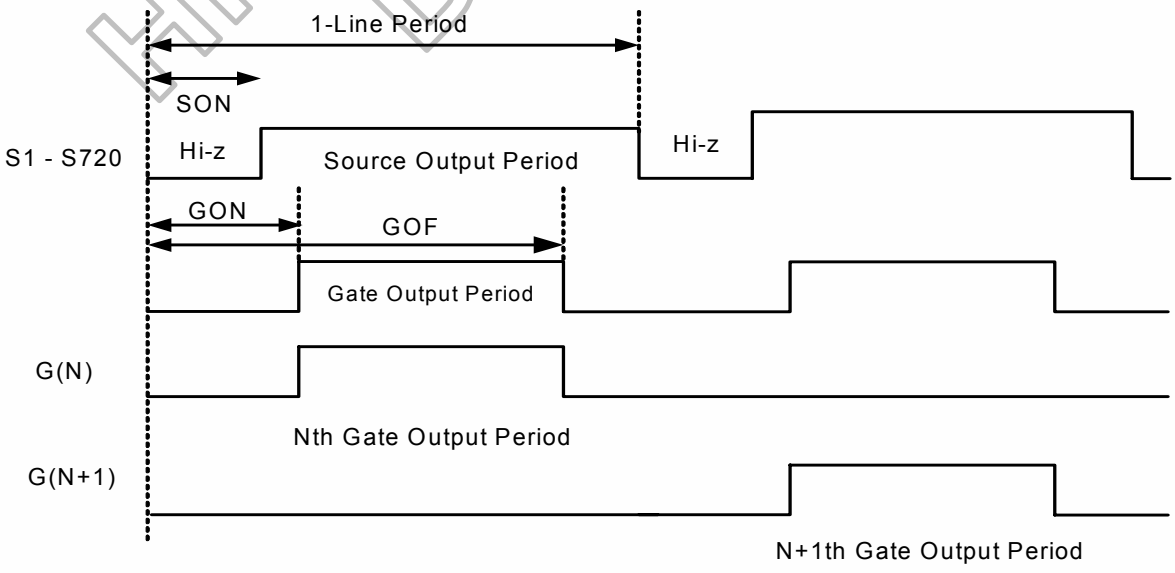
Figure 7. 54 Display Control 6 Register (R40h)

7.35 Display Control 14 Register (R41h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0
R	1	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0

Figure 7. 55 Display Control 3 Register (R41h)

The HX8346-A can control the display operation period time for LCD panel driving as follow:



SON7-0: Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number. (Please note that the setting “00h” and “01h” is inhibited).

GON7-0: Specify the valid gate output start time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the setting “00h”,“01h”, “02h” is inhibited).

GOF7-0: Specify the gate output end time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the GOF8-0 ≤ HCK-1).

7.36 BGP Control Register (R42h)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	BGP3	BGP2	BGP1	BGP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	BGP3	BGP2	BGP1	BGP0

Figure 7. 56 BGP Control 1 Register (R42h)

BGP[3:0]: band gap voltage control

BGP[3:0]	VBGP output
4’b0000	1.182
4’b0001	1.192
4’b0010	1.200
4’b0011	1.210
4’b0100	1.221
4’b0101	1.228
4’b0110	1.236
4’b0111	1.246
4’b1000	**1.256**
4’b1001	1.264
4’b1010	1.274
4’b1011	1.282
4’b1100	1.292
4’b1101	1.300
4’b1110	1.308
4’b1111	1.315

7.37 Vcom Control 1 Register (R43h)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	VCOMG	*	*	*	*	*	*	*
R	1	*	*	*	*	*	*	*	*	VCOMG	*	*	*	*	*	*	*

Figure 7. 57 Vcom Control 1 Register (R43h)

VCOMG:
When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ VCI+0.5V).
When VCOMG = 0, VCOML outputs VSSA and VDV(4-0) setting are invalid. Then, low power consumption is accomplished.

7.38 Vcom Control 2 Register (R44h)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R	1	*	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 7. 58 Vcom Control 2 Register

VCM(6-0):
Set the VCOMH voltage (High level voltage of VCOM) It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VREG1 * 0.4
0	0	0	0	0	0	1	VREG1 * 0.405
0	0	0	0	0	1	0	VREG1 * 0.41
0	0	0	0	0	1	1	VREG1 * 0.415
0	0	0	0	1	0	0	VREG1 * 0.42
0	0	0	0	1	0	1	VREG1 * 0.425
0	0	0	0	1	1	0	VREG1 * 0.43
0	0	0	0	1	1	1	VREG1 * 0.435
0	0	0	1	0	0	0	VREG1 * 0.44
0	0	0	1	0	0	1	VREG1 * 0.445
0	0	0	1	0	1	0	VREG1 * 0.45
0	0	0	1	0	1	1	VREG1 * 0.455
0	0	0	1	1	0	0	VREG1 * 0.46
0	0	0	1	1	0	1	VREG1 * 0.465
0	0	0	1	1	1	0	VREG1 * 0.47
0	0	0	1	1	1	1	VREG1 * 0.475
0	0	1	0	0	0	0	VREG1 * 0.48
0	0	1	0	0	0	1	VREG1 * 0.485
0	0	1	0	0	1	0	VREG1 * 0.49
0	0	1	0	0	1	1	VREG1 * 0.495
0	0	1	0	1	0	0	VREG1 * 0.5
0	0	1	0	1	0	1	VREG1 * 0.505
0	0	1	0	1	1	0	VREG1 * 0.51
0	0	1	0	1	1	1	VREG1 * 0.515
0	0	1	1	0	0	0	VREG1 * 0.52
0	0	1	1	0	0	1	VREG1 * 0.525
0	0	1	1	0	1	0	VREG1 * 0.53
0	0	1	1	0	1	1	VREG1 * 0.535
0	0	1	1	1	0	0	VREG1 * 0.54
0	0	1	1	1	0	1	VREG1 * 0.545
0	0	1	1	1	1	0	VREG1 * 0.55
0	0	1	1	1	1	1	VREG1 * 0.555
0	1	0	0	0	0	0	VREG1 * 0.56
0	1	0	0	0	0	1	VREG1 * 0.565
0	1	0	0	0	1	0	VREG1 * 0.57
0	1	0	0	0	1	1	VREG1 * 0.575
0	1	0	0	1	0	0	VREG1 * 0.58
0	1	0	0	1	0	1	VREG1 * 0.585
0	1	0	0	1	1	0	VREG1 * 0.59
0	1	0	0	1	1	1	VREG1 * 0.595
0	1	0	1	0	0	0	VREG1 * 0.6
0	1	0	1	0	0	1	VREG1 * 0.605
0	1	0	1	0	1	0	VREG1 * 0.61
0	1	0	1	0	1	1	VREG1 * 0.615
0	1	0	1	1	0	0	VREG1 * 0.62
0	1	0	1	1	0	1	VREG1 * 0.625
0	1	0	1	1	1	0	VREG1 * 0.63
0	1	0	1	1	1	1	VREG1 * 0.635

0	1	1	0	0	0	0	VREG1 * 0.64
0	1	1	0	0	0	1	VREG1 * 0.645
0	1	1	0	0	1	0	VREG1 * 0.65
0	1	1	0	0	1	1	VREG1 * 0.655
0	1	1	0	1	0	0	VREG1 * 0.66
0	1	1	0	1	0	1	VREG1 * 0.665
0	1	1	0	1	1	0	VREG1 * 0.67
0	1	1	0	1	1	1	VREG1 * 0.675
0	1	1	1	0	0	0	VREG1 * 0.68
0	1	1	1	0	0	1	VREG1 * 0.685
0	1	1	1	0	1	0	VREG1 * 0.69
0	1	1	1	0	1	1	VREG1 * 0.695
0	1	1	1	1	0	0	VREG1 * 0.7
0	1	1	1	1	0	1	VREG1 * 0.705
0	1	1	1	1	1	0	VREG1 * 0.71
0	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister),
1	0	0	0	0	0	0	VREG1 * 0.715
1	0	0	0	0	0	1	VREG1 * 0.72
1	0	0	0	0	1	0	VREG1 * 0.725
1	0	0	0	0	1	1	VREG1 * 0.73
1	0	0	0	1	0	0	VREG1 * 0.735
1	0	0	0	1	0	1	VREG1 * 0.74
1	0	0	0	1	1	0	VREG1 * 0.745
1	0	0	0	1	1	1	VREG1 * 0.75
1	0	0	1	0	0	0	VREG1 * 0.755
1	0	0	1	0	0	1	VREG1 * 0.76
1	0	0	1	0	1	0	VREG1 * 0.765
1	0	0	1	0	1	1	VREG1 * 0.77
1	0	0	1	1	0	0	VREG1 * 0.775
1	0	0	1	1	0	1	VREG1 * 0.78
1	0	0	1	1	1	0	VREG1 * 0.785
1	0	0	1	1	1	1	VREG1 * 0.79
1	0	1	0	0	0	0	VREG1 * 0.795
1	0	1	0	0	0	1	VREG1 * 0.8
1	0	1	0	0	1	0	VREG1 * 0.805
1	0	1	0	0	1	1	VREG1 * 0.81
1	0	1	0	1	0	0	VREG1 * 0.815
1	0	1	0	1	0	1	VREG1 * 0.82
1	0	1	0	1	1	0	VREG1 * 0.825
1	0	1	0	1	1	1	VREG1 * 0.83
1	0	1	1	0	0	0	VREG1 * 0.835
1	0	1	1	0	0	1	VREG1 * 0.84
1	0	1	1	0	1	0	VREG1 * 0.845
1	0	1	1	0	1	1	VREG1 * 0.85
1	0	1	1	1	0	0	VREG1 * 0.855
1	0	1	1	1	0	1	VREG1 * 0.86
1	0	1	1	1	1	0	VREG1 * 0.865
1	0	1	1	1	1	1	VREG1 * 0.87

1	1	0	0	0	0	0	VREG1 * 0.875
1	1	0	0	0	0	1	VREG1 * 0.88
1	1	0	0	0	1	0	VREG1 * 0.885
1	1	0	0	0	1	1	VREG1 * 0.89
1	1	0	0	1	0	0	VREG1 * 0.895
1	1	0	0	1	0	1	VREG1 * 0.9
1	1	0	0	1	1	0	VREG1 * 0.905
1	1	0	0	1	1	1	VREG1 * 0.91
1	1	0	1	0	0	0	VREG1 * 0.915
1	1	0	1	0	0	1	VREG1 * 0.92
1	1	0	1	0	1	0	VREG1 * 0.925
1	1	0	1	0	1	1	VREG1 * 0.93
1	1	0	1	1	0	0	VREG1 * 0.935
1	1	0	1	1	0	1	VREG1 * 0.94
1	1	0	1	1	1	0	VREG1 * 0.945
1	1	0	1	1	1	1	VREG1 * 0.95
1	1	1	0	0	0	0	VREG1 * 0.955
1	1	1	0	0	0	1	VREG1 * 0.96
1	1	1	0	0	1	0	VREG1 * 0.965
1	1	1	0	0	1	1	VREG1 * 0.97
1	1	1	0	1	0	0	VREG1 * 0.975
1	1	1	0	1	0	1	VREG1 * 0.98
1	1	1	0	1	1	0	inhibit
1	1	1	0	1	1	1	inhibit
1	1	1	1	0	0	0	inhibit
1	1	1	1	0	0	1	inhibit
1	1	1	1	0	1	0	inhibit
1	1	1	1	0	1	1	inhibit
1	1	1	1	1	0	0	inhibit
1	1	1	1	1	0	1	inhibit
1	1	1	1	1	1	0	inhibit
1	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister),,

7.39 Vcom Control 3 Register (R45h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	VDV4	VDV3	VDV2	VDV1	VDV0
R	1	*	*	*	*	*	*	*	*	*	*	*	VDV4	VDV3	VDV2	VDV1	VDV0

Figure 7. 59 Vcom Control 3 Register (R45h)

VDV(4-0):
Specify the VCOM amplitude factors for panel common driving (VCOML = VCOMH – VCOM amplitude, VCOML>= VCL+0.5V). It is possible to setup from 0.6 to 1.23 times of VREG1. When VCOMG = 0, the VDV(4-0) setup is invalid and VCOML is output VSSA.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VREG1*0.6
0	0	0	0	1	VREG1*0.63
0	0	0	1	0	VREG1*0.66
0	0	0	1	1	VREG1*0.69
0	0	1	0	0	VREG1*0.72
0	0	1	0	1	VREG1*0.75
0	0	1	1	0	VREG1*0.78
0	0	1	1	1	VREG1*0.81
0	1	0	0	0	VREG1*0.84
0	1	0	0	1	VREG1*0.87
0	1	0	1	0	VREG1*0.9
0	1	0	1	1	VREG1*0.93
0	1	1	0	0	VREG1*0.96
0	1	1	0	1	VREG1*0.99
0	1	1	1	0	VREG1*1.02
0	1	1	1	1	Inhibit
1	0	0	0	0	VREG1*1.05
1	0	0	0	1	VREG1*1.08
1	0	0	1	0	VREG1*1.11
1	0	0	1	1	VREG1*1.14
1	0	1	0	0	VREG1*1.17
1	0	1	0	1	VREG1*1.2
1	0	1	1	0	VREG1*1.23
1	0	1	1	1	Inhibit
1	1	0	0	0	Inhibit
1	1	0	0	1	Inhibit
1	1	0	1	0	Inhibit
1	1	0	1	1	Inhibit
1	1	1	0	0	Inhibit
1	1	1	0	1	Inhibit
1	1	1	1	0	Inhibit
1	1	1	1	1	Inhibit

7.40 GAMMA Control 1~12 Register (R46~51h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_C P12	G1_C P11	G1_C P10	*	G1_C P02	G1_C P01	G1_C P00
R	1	*	*	*	*	*	*	*	*	*	G1_C P12	G1_C P11	G1_C P10	*	G1_C P02	G1_C P01	G1_C P00

Figure 7. 60 GAMMA Control 1 Register (R46h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_C N12	G1_C N11	G1_C N10	*	G1_C N02	G1_C N01	G1_C N00
R	1	*	*	*	*	*	*	*	*	*	G1_C N12	G1_C N11	G1_C N10	*	G1_C N02	G1_C N01	G1_C N00

Figure 7. 61 GAMMA Control 2 Register (R47h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N P12	G1_N P11	G1_N P10	*	G1_N P02	G1_N P01	G1_N P00
R	1	*	*	*	*	*	*	*	*	*	G1_N P12	G1_N P11	G1_N P10	*	G1_N P02	G1_N P01	G1_N P00

Figure 7. 62 GAMMA Control 3 Register (R48h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N P32	G1_N P31	G1_N P30	*	G1_N P22	G1_N P21	G1_N P20
R	1	*	*	*	*	*	*	*	*	*	G1_N P32	G1_N P31	G1_N P30	*	G1_N P22	G1_N P21	G1_N P20

Figure 7. 63 GAMMA Control 4 Register (R49h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N P52	G1_N P51	G1_N P50	*	G1_N P42	G1_N P41	G1_N P40
R	1	*	*	*	*	*	*	*	*	*	G1_N P52	G1_N P51	G1_N P50	*	G1_N P42	G1_N P41	G1_N P40

Figure 7. 64 GAMMA Control 5 Register (R4Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N N12	G1_N N11	G1_N N10	*	G1_N N02	G1_N N01	G1_N N00
R	1	*	*	*	*	*	*	*	*	*	G1_N N12	G1_N N11	G1_N N10	*	G1_N N02	G1_N N01	G1_N N00

Figure 7. 65 GAMMA Control 6 Register (R4Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N N32	G1_N N31	G1_N N30	*	G1_N N22	G1_N N21	G1_N N20
R	1	*	*	*	*	*	*	*	*	*	G1_N N32	G1_N N31	G1_N N30	*	G1_N N22	G1_N N21	G1_N N20

Figure 7. 66 GAMMA Control 7 Register (R4Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_N N52	G1_N N51	G1_N N50	*	G1_N N52	G1_N N51	G1_N N50
R	1	*	*	*	*	*	*	*	*	*	G1_N N52	G1_N N51	G1_N N50	*	G1_N N52	G1_N N51	G1_N N50

Figure 7. 67 GAMMA Control8 Register (R4Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	G1_C GMP1	G1_C GMP0	G1_O P03	G1_O P02	G1_O P01	G1_O P00
R	1	*	*	*	*	*	*	*	*	*	*	G1_C GMP1	G1_C GMP0	G1_O P03	G1_O P02	G1_O P01	G1_O P00

Figure 7. 68 GAMMA Control 9 Register (R4Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	G1_C GM2	G1_C GM1	G1_C GM0	G1_O P14	G1_O P13	G1_O P12	G1_O P11	G1_O P10
R	1	*	*	*	*	*	*	*	*	G1_C GM2	G1_C GM1	G1_C GM0	G1_O P14	G1_O P13	G1_O P12	G1_O P11	G1_O P10

Figure 7. 69 GAMMA Control 10 Register (R4Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	G1_C GMN1	G1_C GMN0	G1_O N03	G1_O N02	G1_O N01	G1_O N00
R	1	*	*	*	*	*	*	*	*	*	*	G1_C GMN1	G1_C GMN0	G1_O N03	G1_O N02	G1_O N01	G1_O N00

Figure 7. 70 GAMMA Control 11 Register (R50h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	G1_GS EL	*	G1_O N14	G1_O N13	G1_O N12	G1_O N11	G1_O N10
R	1	*	*	*	*	*	*	*	*	*	G1_GS EL	*	G1_O N14	G1_O N13	G1_O N12	G1_O N11	G1_O N10

Figure 7. 71 GAMMA Control 12 Register (R51h)

G1_CP1-0 [2:0]: Gamma Center Adjustment registers for positive polarity output
G1_CN1-0 [2:0]: Gamma Center Adjustment registers for negative polarity output
G1_NP5-0 [2:0]: Gamma Macro Adjustment registers for positive polarity output
G1_NN5-0 [2:0]: Gamma Macro Adjustment registers for negative polarity output
G1_OP0 [3:0]/OP1 [4:0]: Gamma Offset Adjustment register for positive polarity output
G1_ON0 [3:0]/ON1 [4:0]: Gamma Offset Adjustment register for negative polarity output
G1_CGMP [1:0]: Gamma Tap Adjustment register for positive polarity output
G1_CGMN [1:0]: Gamma Tap Adjustment register for negative polarity output
G1_CGM [2:0]: Gamma Harmony adjustment register for positive/negative polarity output
GSEL: V0, V256 reference voltage selection. GSEL=1, V0=VgP/N0, V256= VgP/N7; If G1_GSEL=0, V0=VREG1, V256= VGS. For details, please refer to 5.9.4 Gamma resister stream and 8 to 1 Selector.

This command is used to set Gamma Curve 1 Related Setting

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	NP0 2-0	NN0 2-0	8-to-1 selector (voltage level of grayscale 4)
	NP1 2-0	NN1 2-0	8-to-1 selector (voltage level of grayscale 32)
	NP2 2-0	NN2 2-0	8-to-1 selector (voltage level of grayscale 80)
	NP3 2-0	NN3 2-0	8-to-1 selector (voltage level of grayscale 176)
	NP4 2-0	NN4 2-0	8-to-1 selector (voltage level of grayscale 224)
	NP5 2-0	NN5 2-0	8-to-1 selector (voltage level of grayscale 252)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

7.41 OTP Related register 1(R52h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_MASK 7	OTP_MASK 6	OTP_MASK 5	OTP_MASK 4	OTP_MASK 3	OTP_MASK 2	OTP_MASK 1	OTP_MASK 0
R	1	*	*	*	*	*	*	*	*	OTP_MASK 7	OTP_MASK 6	OTP_MASK 5	OTP_MASK 4	OTP_MASK 3	OTP_MASK 2	OTP_MASK 1	OTP_MASK 0

Figure 7. 72 OTP Related Register 1(R52h)

OTP_MASK7 [7:0]: Bit programming mask, if set to 1, it means that it doesn't program this bit

7.42 OTP Related register 1(R53h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_INDEX 7	OTP_INDEX 6	OTP_INDEX 5	OTP_INDEX 4	OTP_INDEX 3	OTP_INDEX 2	OTP_INDEX 1	OTP_INDEX 0
R	1	*	*	*	*	*	*	*	*	OTP_INDEX 7	OTP_INDEX 6	OTP_INDEX 5	OTP_INDEX 4	OTP_INDEX 3	OTP_INDEX 2	OTP_INDEX 1	OTP_INDEX 0

Figure 7. 73 OTP Related Register 2(R53h)

OTP_INDEX[7:0]: Set location of OTP programming.

7.43 OTP Related register 1(R54h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG
R	1	*	*	*	*	*	*	*	*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG

Figure 7. 74 OTP Related Register 3(R54h)

OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLPOUT command is received. Nevertheless, if this bit was set to 1, it would disable the auto loading function when the SLPOUT command was received. In general, this bit is used when OTP is not yet programmed.

DCCLK_DISABLE: When written to 1, disable internal pumping Clock.

VPP_SEL: When it set to 1, VGH voltage is fed to OTP

OTP_PROG: When it set to 1, the internal register begin to write to OTP.

7.44 Internal Use 1(R55h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	VDC_SEL1	VDC_SEL0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	VDC_SEL1	VDC_SEL0

Figure 7. 75 Internal Use 1(R55h)

This command is used to set internal digital voltage for digital circuit and GRAM.

VDC_SEL[1:0]: Not open

7.45 Internal Use 2 (R56h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	RPULSE2	RPULSE1	RPULSE0	SRAM_OPT	SEN_MODE	SPULSE2	SPULSE1	SPULSE0
R	1	*	*	*	*	*	*	*	*	RPULSE2	RPULSE1	RPULSE0	SRAM_OPT	SEN_MODE	SPULSE2	SPULSE1	SPULSE0

Figure 7. 76 Internal Use 2(R56h)

This command is used to set GRAM arbiter pulse width.

SPULSE[2:0]: Not open

7.46 Internal Use 3 (R57h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEST_MODE	TEST_OE
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEST_MODE	TEST_OE

Figure 7. 77 Internal register access enable (R57h)

TEST_MODE: Not open

7.47 Internal Use 4 (R58h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PROBE7	PROBE6	PROBE5	PROBE4	PROBE3	PROBE2	PROBE1	PROBE0
R	1	*	*	*	*	*	*	*	*	PROBE7	PROBE6	PROBE5	PROBE4	PROBE3	PROBE2	PROBE1	PROBE0

Figure 7. 78 Internal Use 4 (R58h)

This command is used to set which group of signals to be observed
PROBE[7:0]: Not open

7.48 Internal Use 5 (R59h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PTBA15	PTBA14	PTBA13	PTBA12	PTBA11	PTBA10	PTBA9	PTBA8
R	1	*	*	*	*	*	*	*	*	PTBA15	PTBA14	PTBA13	PTBA12	PTBA11	PTBA10	PTBA9	PTBA8

Figure 7. 79 Internal Use 5 (R59h)

This command is used to set which group of signals to be observed

7.49 Internal Use 6 (R5Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PTBA7	PTBA6	PTBA5	PTBA4	PTBA3	PTBA2	PTBA1	PTBA0
R	1	*	*	*	*	*	*	*	*	PTBA7	PTBA6	PTBA5	PTBA4	PTBA3	PTBA2	PTBA1	PTBA0

Figure 7. 80 Internal Use 6 (R5Ah)

This command is used to set power circuit option
PTBA[15:0]: Not open

7.50 Internal Use 7(R5Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	STBA15	STBA14	STBA13	STBA12	STBA11	STBA10	STBA9	STBA8
R	1	*	*	*	*	*	*	*	*	STBA15	STBA14	STBA13	STBA12	STBA11	STBA10	STBA9	STBA8

Figure 7. 81 Internal Use 7(R5Bh)

For internal use and not open.

7.51 Internal Use 8 (R5Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	STB A7	STB A6	STB A5	STB A4	STB A3	STB A2	STB A1	STB A0
R	1	*	*	*	*	*	*	*	*	STB A7	STB A6	STB A5	STB A4	STB A3	STB A2	STB A1	STB A0

Figure 7. 82 Internal Use 9 (R5Ch)

For internal use and not open.

7.52 Internal Use 9 (R5Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	VTEST SEL2	VTEST SEL1	VTEST SEL0	*	*	GAOE	GMA
R	1	*	*	*	*	*	*	*	*	*	VTEST SEL2	VTEST SEL1	VTEST SEL0	*	*	GAOE	GMA

Figure 7. 83 Internal Use 9 (R5Dh)

For internal use and not open.

7.53 Internal Use 10 (R5Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BIST_ CB1	BIST_ CB0	BIST_ ALL1	BIST_ ALL0	BIST_V	BIST_H	BIST_ OPT	BIST_ EN
R	1	*	*	*	*	*	*	*	*	BIST_ CB1	BIST_ CB0	BIST_ ALL1	BIST_ ALL0	BIST_V	BIST_H	BIST_ OPT	BIST_ EN

Figure 7. 84 Internal Use 10 (R5Eh)

For internal use and not open.

7.54 Internal Use 11 (R5Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	ERR0_ FLAG2	ERR0_ FLAG1	ERR0_ FLAG0	*	*	*	*
R	1	*	*	*	*	*	*	*	*	*	ERR0_ FLAG2	ERR0_ FLAG1	ERR0_ FLAG0	*	*	*	*

Figure 7. 85 Internal Use 11 (R5Fh)

For internal use and not open.

7.55 Internal Use 12 (R60h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	PULO	SRAM_AD DR_MUX
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	PULO	SRAM_AD DR_MUX

Figure 7. 86 Internal Use 12 (R60h)

For internal use and not open.

7.56 Internal Use 13 (R61h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	TSA	ELE	TDISP_AREA	TM	TSC
R	1	*	*	*	*	*	*	*	*	*	*	*	TSA	ELE	TDISP_AREA	TM	TSC

Figure 7. 87 Internal Use 13 (R61h)

For internal use and not open.

7.57 Internal Use 14 (R62h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TLADD8
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TLADD8

Figure 7. 88 Internal Use 14 (R62h)

For internal use and not open.

7.58 Internal Use 15 (R63h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TLA DD7	TLA DD6	TLA DD5	TLA DD4	TLA DD3	TLA DD2	TLA DD1	TLA DD0
R	1	*	*	*	*	*	*	*	*	TLA DD7	TLA DD6	TLA DD5	TLA DD4	TLA DD3	TLA DD2	TLA DD1	TLA DD0

Figure 7. 89 Internal Use 15 (R63h)

For internal use and not open.

7.59 Internal Use 16 (R64h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	*	*	*	*	*	*	*	*	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 7. 90 Internal Use 16 (R64h)

For internal use and not open.

7.60 Internal Use 17 (R65h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	*	*	*	*	*	*	*	*	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 7. 91 Internal Use 17 (R65h)

For internal use and not open.

7.61 Internal Use 18 (R66h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	*	*	*	*	*	*	*	*	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 7. 92 Internal Use 18 (R66h)

For internal use and not open.

7.62 Internal Use 49 (R67h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	*	*	*	*	*	*	*	*	HXID7	HXID6	HXID5	HXID4	HXID3	HXID2	HXID1	HXID0

Figure 7. 93 Internal Use 27 (R67h)

HXID[7:0]:
When the read commend is issued, 46h is read.

7.63 Internal Use 20 (R68h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	ROM_TEST_ADDR10	ROM_TEST_ADDR9	ROM_TEST_ADDR8
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	ROM_TEST_ADDR10	ROM_TEST_ADDR9	ROM_TEST_ADDR8

Figure 7. 94 Internal Use 20 (R68h)

For internal use and not open.

7.64 Internal Use 21 (R69h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	ROM_TEST	ROM_TEST_CSB	ROM_TEST_OEB
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	ROM_TEST	ROM_TEST_CSB	ROM_TEST_OEB

Figure 7. 95 Internal Use 21 (R69h)

For internal use and not open.

7.65 Internal Use 27 (R2Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	*	*	*	*	*	*	*	*	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0

Figure 7. 96 Internal Use 27 (R2Fh)

Version ID for read only.

7.66 Logic Function Register (R70h)

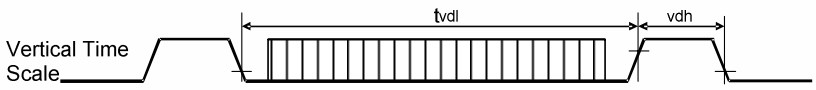
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OSC_SPEED	GS	SS	TEMODE	TEON	CSEL2	CSEL1	CSEL0
R	1	*	*	*	*	*	*	*	*	OSC_SPEED	GS	SS	TEMODE	TEON	CSEL2	CSEL1	CSEL0

Figure 7. 97 Logic Function Register (R70h)

TEMODE: Specify the Tearing-Effect mode.

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only.

When TEMODE =1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information



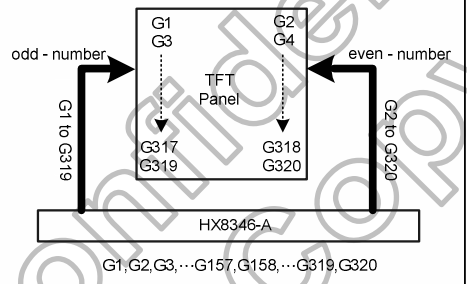
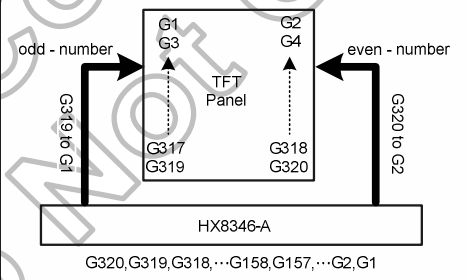
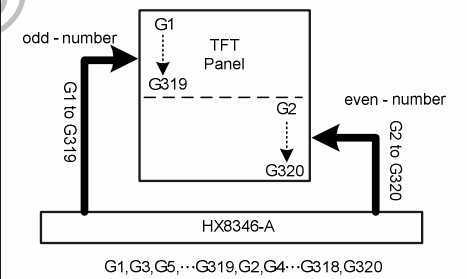
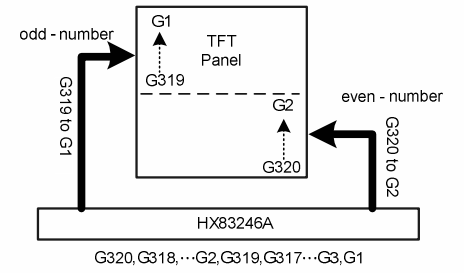
Note: During STB Mode with Tearing Effect Line On, Tearing Effect Output pin active low

TEON:
This command is used to turn ON the Tearing Effect output signal from the TE signal line.
This output is not affected by changing MADCTL bit B4.

CSEL[2:0]:
This command is used to define the format of RGB picture data, which is to be transferred via the RGB Interface. The formats are shown in the table:

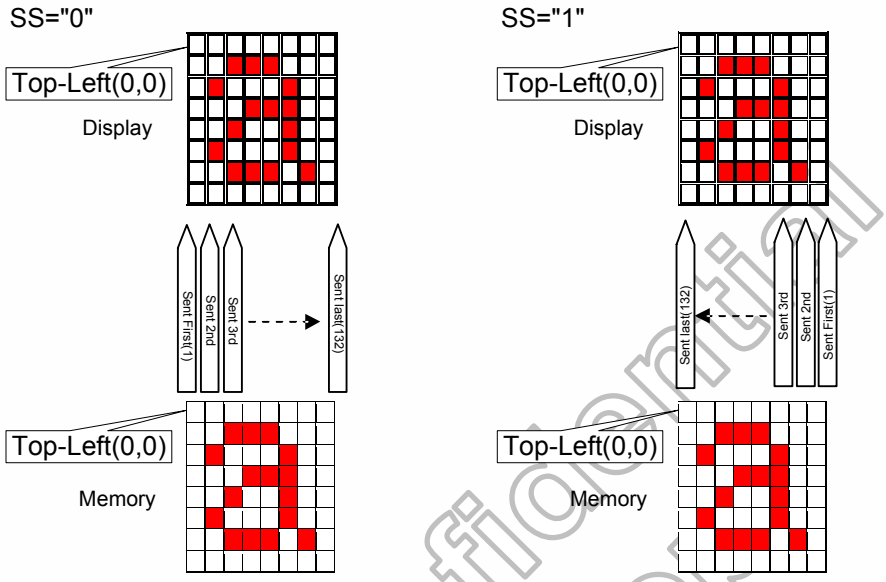
Interface Format	CSEL2	CSEL1	CSEL0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0

GS: Gate scan sequence.

SM	GS	Scan direction
0	0	
0	1	
1	0	
1	1	

SS:

SS-Horizontal Updating order



Note: Top-Left (0,0) means a physical memory location.

7.67 Serial Bus Interface control register (R72h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TRI1	TRI0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TRI1	TRI0

Figure 7. 98 Serial Bus Interface control register (R72h)

TRI[1:0]	GRAM
00	16 bit-color/per pixel data
01	18 bit-color/per pixel data
1X	24 bit-color/per pixel data

For details, please refer to serial bus system interface.

7.68 Internal Use 31 (R73h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SDM YP07	SDM YP06	SDM YP05	SDM YP04	SDM YP03	SDM YP02	SDM YP01	SDM YP00
R	1	*	*	*	*	*	*	*	*	SDM YP07	SDM YP06	SDM YP05	SDM YP04	SDM YP03	SDM YP02	SDM YP01	SDM YP00

Figure 7. 99 Internal Use 31 (R73h)

For internal use and not open.

7.69 Internal Use 32 (R74h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB04	SDM YB03	SDM YB02	SDM YB01	SDM YB00
R	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB04	SDM YB03	SDM YB02	SDM YB01	SDM YB00

Figure 7. 100 Internal Use 32 (R74h)

For internal use and not open.

7.70 Internal Use 33 (R75h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SDM YP17	SDM YP16	SDM YP15	SDM YP14	SDM YP13	SDM YP12	SDM YP11	SDM YP10
R	1	*	*	*	*	*	*	*	*	SDM YP17	SDM YP16	SDM YP15	SDM YP14	SDM YP13	SDM YP12	SDM YP11	SDM YP10

Figure 7. 101 Internal Use 33 (R75h)

For internal use and not open.

7.71 Internal Use 34 (R76h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB14	SDM YB13	SDM YB12	SDM YB11	SDM YB10
R	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB14	SDM YB13	SDM YB12	SDM YB11	SDM YB10

Figure 7. 102 Internal Use 34 (R76h)

For internal use and not open.

7.72 Internal Use 35 (R77h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SDM YP27	SDM YP26	SDM YP25	SDM YP24	SDM YP23	SDM YP22	SDM YP21	SDM YP20
R	1	*	*	*	*	*	*	*	*	SDM YP27	SDM YP26	SDM YP25	SDM YP24	SDM YP23	SDM YP22	SDM YP21	SDM YP20

Figure 7. 103 Internal Use 35 (R77h)

For internal use and not open.

7.73 Internal Use 36 (R78h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB24	SDM YB23	SDM YB22	SDM YB21	SDM YB20
R	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB24	SDM YB23	SDM YB22	SDM YB21	SDM YB20

Figure 7. 104 Internal Use 36 (R78h)

For internal use and not open.

7.74 Internal Use 37 (R79h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SDM YP37	SDM YP36	SDM YP35	SDM YP34	SDM YP33	SDM YP32	SDM YP31	SDM YP30
R	1	*	*	*	*	*	*	*	*	SDM YP37	SDM YP36	SDM YP35	SDM YP34	SDM YP33	SDM YP32	SDM YP31	SDM YP30

Figure 7. 105 Internal Use 37 (R79h)

For internal use and not open.

7.75 Internal Use 38 (R7Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB34	SDM YB33	SDM YB32	SDM YB31	SDM YB30
R	1	*	*	*	*	*	*	*	*	*	*	*	SDM YB34	SDM YB33	SDM YB32	SDM YB31	SDM YB30

Figure 7. 106 Internal Use 38 (R7Ah)

For internal use and not open.

7.76 Internal Use 39 (R7Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SRAM_FIX_EN	*	*	*	BIST_LOAD
R	1	*	*	*	*	*	*	*	*	*	*	*	SRAM_FIX_EN	*	*	*	BIST_LOAD

Figure 7. 107 Internal Use 39 (R7Bh)

For internal use and not open.

7.77 Backlight Control 1~7 Register (R7C~82h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DBK
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DBK

Figure 7. 108 Backlight Control 1 Register (R7Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	BRTH2	BRTH1	BRTH0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	BRTH2	BRTH1	BRTH0

Figure 7. 109 Backlight Control 2 Register (R7Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	LED_PA3	LED_PA2	LED_PA1	LED_PA0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	LED_PA3	LED_PA2	LED_PA1	LED_PA0

Figure 7. 110 Backlight Control 3 Register (R7Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	LED_PB3	LED_PB2	LED_PB1	LED_PB0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	LED_PB3	LED_PB2	LED_PB1	LED_PB0

Figure 7. 111 Backlight Control 4 Register (R7Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	PWM_PERI OD7	PWM_PERI OD6	PWM_PERI OD5	PWM_PERI OD4	PWM_PERI OD3
R	1	*	*	*	*	*	*	*	*	*	*	*	PWM_PERI OD7	PWM_PERI OD6	PWM_PERI OD5	PWM_PERI OD4	PWM_PERI OD3

Figure 7. 112 Backlight Control 5 Register (R80h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PWM_PERI OD2	PWM_PERI OD1	PWM_PERI OD0	*	*	*	*	*
R	1	*	*	*	*	*	*	*	*	PWM_PERI OD2	PWM_PERI OD1	PWM_PERI OD0	*	*	*	*	*

Figure 7. 113 Backlight Control 6 Register (R81h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	DUTY 4	DUTY 3	DUTY 2	DUTY 1	DUTY 0
R	1	*	*	*	*	*	*	*	*	*	*	*	DUTY 4	DUTY 3	DUTY 2	DUTY 1	DUTY 0

Figure 7. 114 Backlight Control 7 Register (R82h)

DBK: ON/OFF the operation of backlight control circuit.

DBK	Operation of backlight control circuit
0	ON
1	OFF

LED_PA [3:0] : Set the pumping cycle of the backlight control circuit.
Tosc=1/Fosc = R-C oscillation frequency

LED_PA[3]	LED_PA[2]	LED_PA[1]	LED_PA[0]	pumping cycle of LED_SW
0	0	0	0	0
0	0	0	1	1 * Tosc
0	0	1	0	2 * Tosc
0	0	1	1	3 * Tosc
0	1	0	0	4 * Tosc
0	1	0	1	5 * Tosc
0	1	1	0	6 * Tosc
0	1	1	1	7 * Tosc
1	0	0	0	8 * Tosc
1	0	0	1	9 * Tosc
1	0	1	0	10 * Tosc
1	0	1	1	11 * Tosc
1	1	0	0	12 * Tosc
1	1	0	1	13 * Tosc
1	1	1	0	14 * Tosc
1	1	1	1	15 * Tosc

LED_PB [3:0] : Set the pumping duty pulse of the backlight control circuit.
Tosc=1/Fosc = R-C oscillation frequency

LED_PB[3]	LED_PB[2]	LED_PB[1]	LED_PB[0]	pumping duty plus of LED_SW
0	0	0	0	0
0	0	0	1	1 * Tosc
0	0	1	0	2 * Tosc
0	0	1	1	3 * Tosc
0	1	0	0	4 * Tosc
0	1	0	1	5 * Tosc
0	1	1	0	6 * Tosc
0	1	1	1	7 * Tosc
1	0	0	0	8 * Tosc
1	0	0	1	9 * Tosc
1	0	1	0	10 * Tosc
1	0	1	1	11 * Tosc
1	1	0	0	12 * Tosc
1	1	0	1	13 * Tosc
1	1	1	0	14 * Tosc
1	1	1	1	15 * Tosc

BTRH[2:0]: Set backlight control circuit to control the LED current IBC

BTRH2	BTRH1	BTRH0	I_{BC}
0	0	0	$(4/35*VBGP)/R_{BC}$
0	0	1	$(5/35*VBGP)/R_{BC}$
0	1	0	$(6/35*VBGP)/R_{BC}$
0	1	1	$(7/35*VBGP)/R_{BC}$
1	0	0	$(8/35*VBGP)/R_{BC}$
1	0	1	$(9/35*VBGP)/R_{BC}$
1	1	0	$(10/35*VBGP)/R_{BC}$
1	1	1	$(11/35*VBGP)/R_{BC}$

PWM_PERIOD[7:0] : Set the operating frequency of the backlight control circuit. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

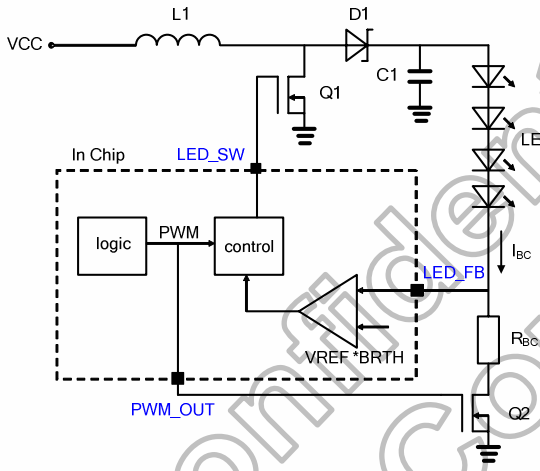
Fosc = R-C oscillation frequency

PWM_PERIOD [7:0]	Operation Frequency of backlight control circuit
0000 0000	Inhibit
0000 0001	Fosc / 32
0000 0010	Fosc / 64
0000 0011	Fosc / 96
:	:
1111 1110	Fosc / 8128
1111 1111	Fosc / 8160

DUTY[4:0] : Set the operating duty cycle of the backlight control circuit.

DUTY [4:0]	Operation duty cycle of backlight control circuit
0 0000	1/32*PWM_PERIOD
0 0001	2/32*PWM_PERIOD
:	:
1 1110	31/32*PWM_PERIOD
1 1111	PWM_PERIOD

Block Diagram of backlight control circuit



7.78 Internal Use 47 (R83h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SFULL	*
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SFULL	*

Figure 7. 115 Internal Use 47 (R83h)

For internal use and not open.

7.79 Internal Use 48 (R84h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	IO_O PT1	IO_O PT0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	IO_O PT1	IO_O PT0

Figure 7. 116 Internal Use 48 (R84h)

This command is used to be observed.
For internal use and not open.

8. Electrical Characteristic

8.1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage (1)	VCC,IOVCC	V	-0.3 to +4.6	1,2
Power Supply Voltage (2)	VCI ~ VSSA	V	-0.3 to +4.6	1,2
Power Supply Voltage (3)	VLCD ~ VSSA	V	-0.3 to +6.6	3
Power Supply Voltage (4)	VSSA ~ VCL	V	-0.3 to +4.6	4
Power Supply Voltage (5)	VLCD ~ VCL	V	-0.3 to +9	5
Power Supply Voltage (6)	VGH ~ VSSA	V	-0.3 to +18.5	6
Power Supply Voltage (7)	VSSA ~ VGL	V	0 to -16.5	7
Input Voltage	Vi	V	-0.3 to VCC+0.3	-
Operating Temperature	Topr	°C	-40 to +85	8,9
Storage Temperature	Tstg	°C	-55 to +110	8,9

Note:
1.VCC, VSSD must be maintained.
2.To make sure IOVCC ≥ VSSD.
3.To make sure VCI ≥ VSSA.
4.To make sure VLCD ≥ VSSA.
5.To make sure VLCD ≥ VCL.
6.To make sure VGH ≥ VSSA.
7.To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
8.For die and wafer products, specified up to +85℃.
9.This temperature specifications apply to the TCP package.

8.5 Maximum Series Resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCC	Power supply	20	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
CM, SHUT, RL, TB, P68, BS[1:0], EXTC, IFSEL, BURN, REGVDD,	Input	100	Ω
NRD_E, NWR_RNW, DNC_SCL, NCS, SDIO	Input	100	Ω
NRESET	Input	100	Ω
D[17:0], DOTCLK, ENABLE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
VLCD	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	30	Ω
VREG3	Capacitor connection	20	Ω
VCOMH, VCOML	Capacitor connection	20	Ω
VCI2	Capacitor connection	30	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
C23A, C23B	Capacitor connection	15	Ω
VCOMR	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
LED_FB	Input	20	Ω
PWM_OUT	Output	20	Ω
LED_SW	Output	10	Ω
SO_TEST[3:0]	Output	100	Ω
VBGP	Output	100	Ω

Table 8. 1 Maximun series resistance

8.6 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVcc= 1.65 ~ 3.3V	0.8xIOVcc	-	IOVcc	-
Input low voltage	V_{IL}	V	IOVcc= 1.65 ~ 3.3V	-0.3V	-	0.2xIOVcc	-
Output high voltage(1) (D0-17 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVcc	-	-	-
Output low voltage (D0-17 Pins)	V_{OL1}	V	IOVcc= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVcc	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ Vcc	-1	-	1	-
Current consumption during normal operation (Vcc – VSSD)+ (IOVcc-VSSD)	$I_{OP(Vcc)}$	µA	Vci=IOVcc=Vcc=2.8V , Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, FS0=00, FS1=11, BT=1000, VC1=111,VC2=100, VC3=000 VRH=0011, VCM=0100000,VDV=01110, VCOMG=1 No panel load	-	150	300	-
Current consumption during normal operation (Vci – VSSD)	$I_{OP(Vci)}$	mA		-	2.7	3.0	-
Current consumption during standby mode (Vcc – VSSD) + (IOVcc-VSSD)	$I_{ST(VCC)}$	µA	Vcc=2.8V , Ta=25°C	-	5	20	-
Current consumption during standby mode (Vci – VSSD)	$I_{ST(VCi)}$	µA			0.5	1	
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 8. 2 DC Characteristic (Vcc = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C)

8.7 AC CHARACTERISTICS

8.7.1 Parallel Interface Characteristics (8080-series MPU)

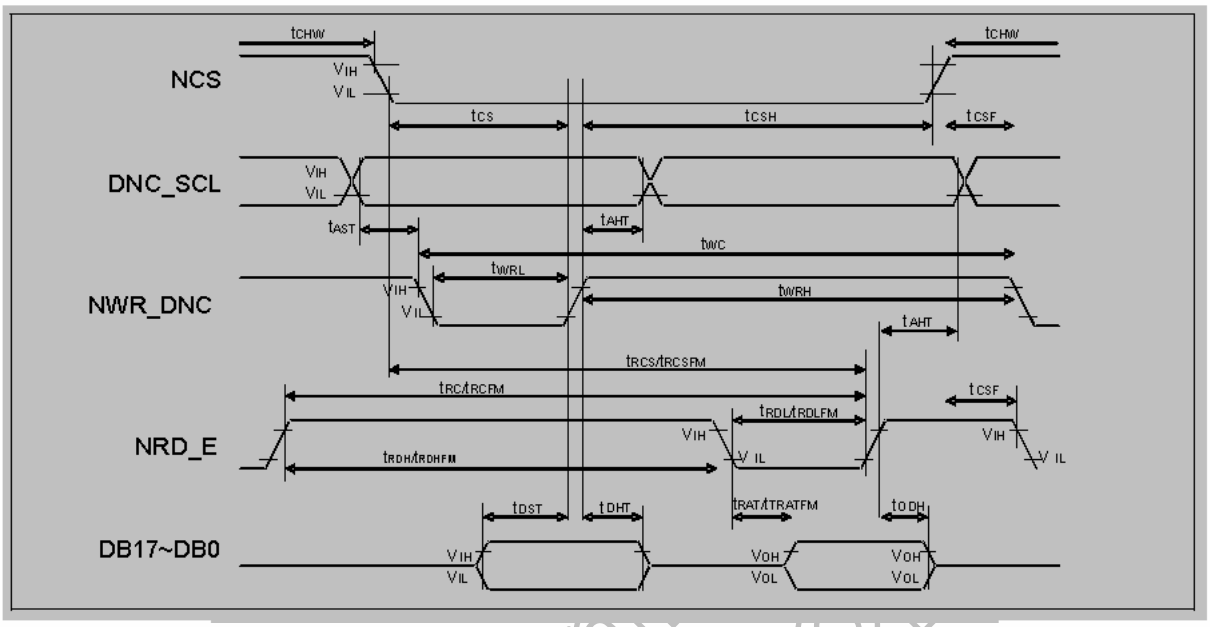
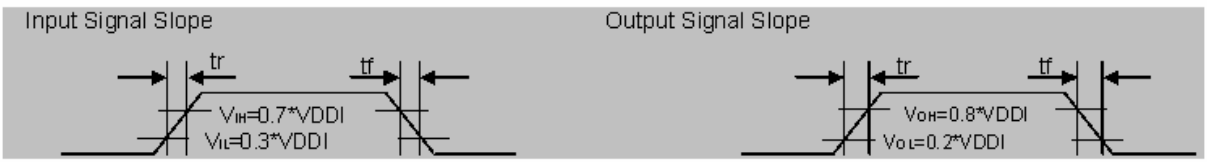


Figure 8. 1 Parallel Interface Characteristics (8080-series MPU)

(VSSA=0V, VCC=1.65V to 2.50V, VCI=2.3V to 2.9V,Ta = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time Chip select wait time (Write/Read) Chip select hold time	0 35 355 10 10	- - - - - -	ns	-
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 35 35	- - -	ns	-
NRD_E	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle Control pulse “H” duration Control pulse “L” duration	450 90 355	- - -	ns	When read from GRAM
D17 to D0	t_{DST} t_{DHT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time Output disable time	15 10 - 20	- - 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



Note: VDDI means IOVCC

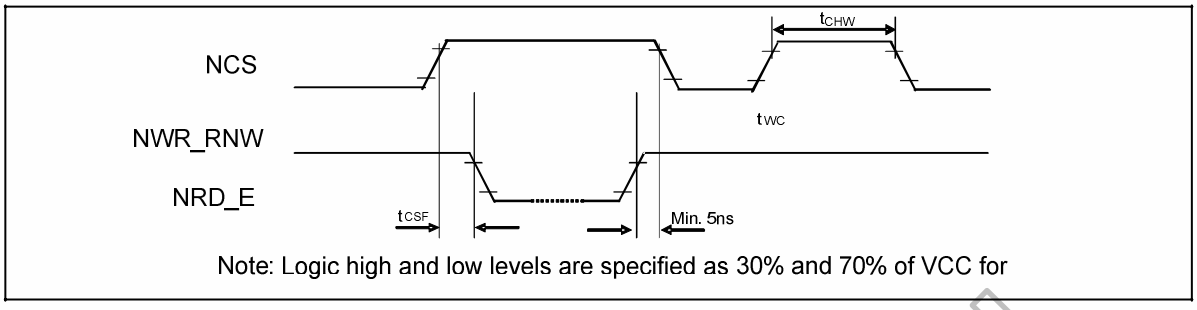


Figure 8. 2 Chip Select Timing

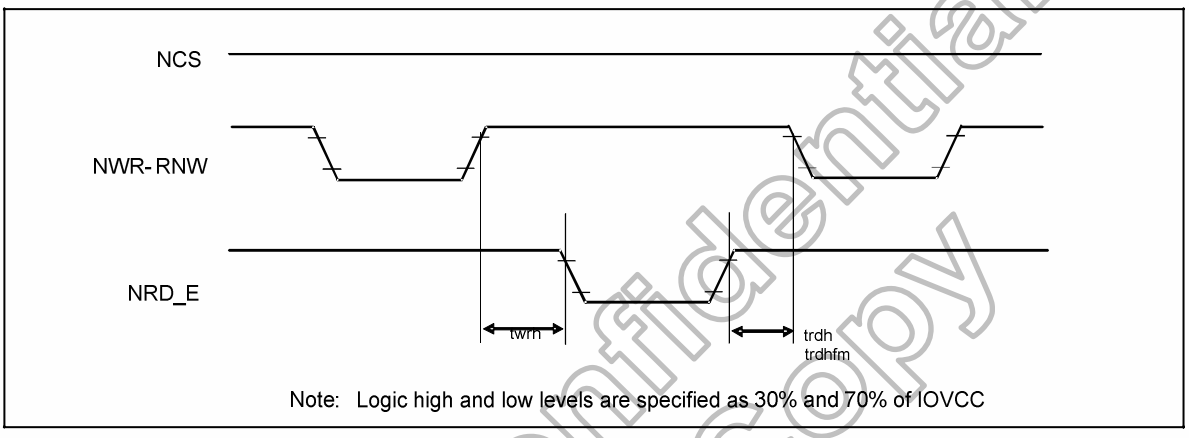


Figure 8. 3 Write to Read and Read to Write Timing

8.7.2 Parallel Interface Characteristics (6800-series MPU)

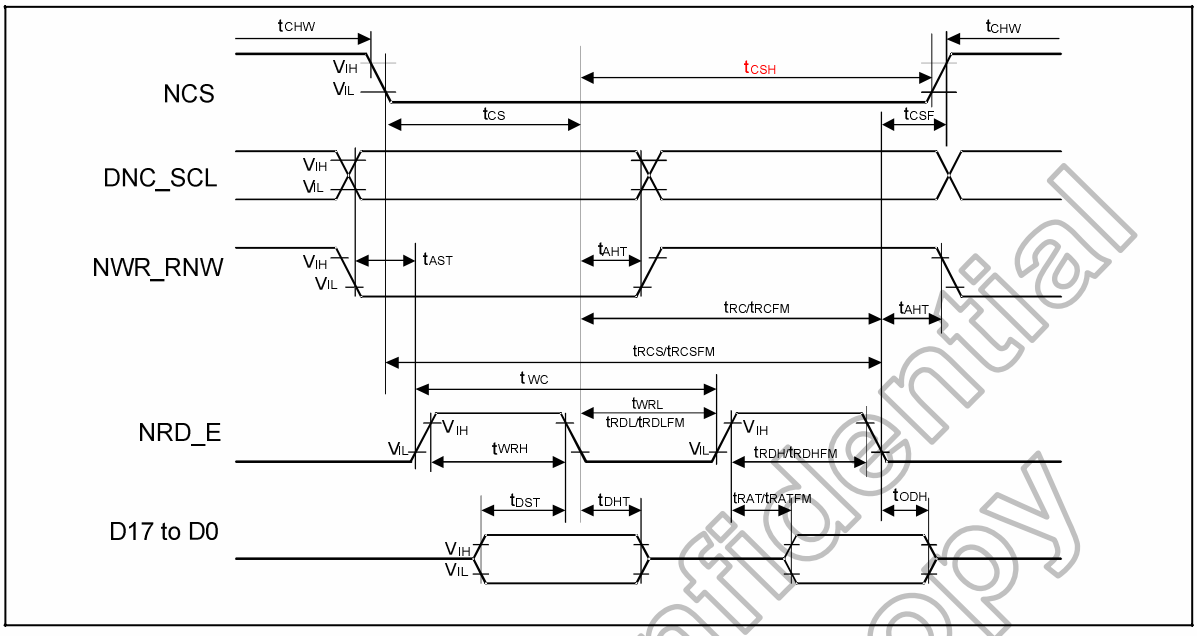
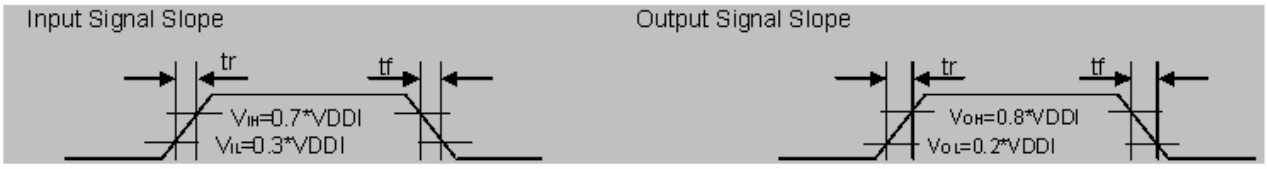


Figure 8. 4 Parallel Interface Characteristics (6800-series MPU)

(VSSA=0V, VCC=1.65V to 2.50V, VCI=2.3V to 2.9V,Ta = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
NCS	t_{CHW} t_{CS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time Chip select wait time (Write/Read) Chip select hold time	0 35 355 10 10	- - - - - -	ns	-
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 35 35	- - -	ns	-
NRD_E	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle Control pulse “H” duration Control pulse “L” duration	450 90 355	- - -	ns	When read from GRAM
D17 to D0	T_{dst} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - 40 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



Note: VDDI means IOVCC

8.7.3 Serial Interface Characteristics

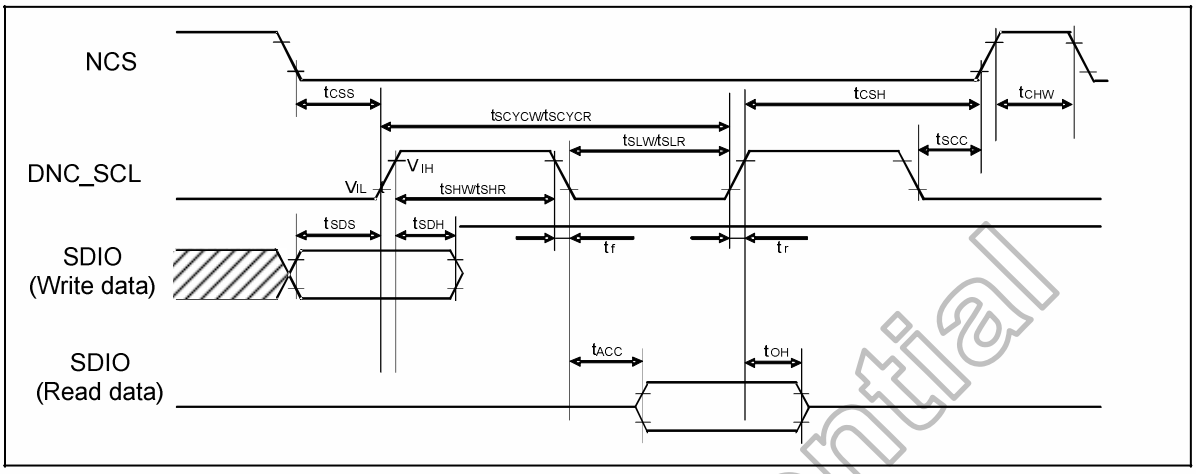
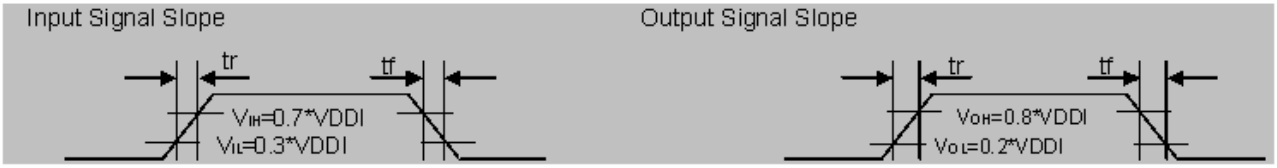


Figure 8. 5 Serial interface characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Maz.	Unit
Serial clock cycle (Write) DNC_SCL "H" pulse width (Write) DNC_SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	DNC_SCL	100 35 35	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDIO	30 30	- -	- -	ns
Serial clock cycle (Read) DNC_SCL "H" pulse width (Read) DNC_SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	DNC_SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDIO for maximum C_L=30pF For minimum C_L=8pF	45	-	100	ns
Output disable time	t_{OH}	SDIO For maximum C_L=30pF For minimum C_L=8pF	15	-	100	ns
DNC_SCL to Chip select	t_{SCC}	DNC_SCL, NCS	15	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	45	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 65	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



Note: VDDI means IOVCC

8.7.4 RGB Interface Characteristics

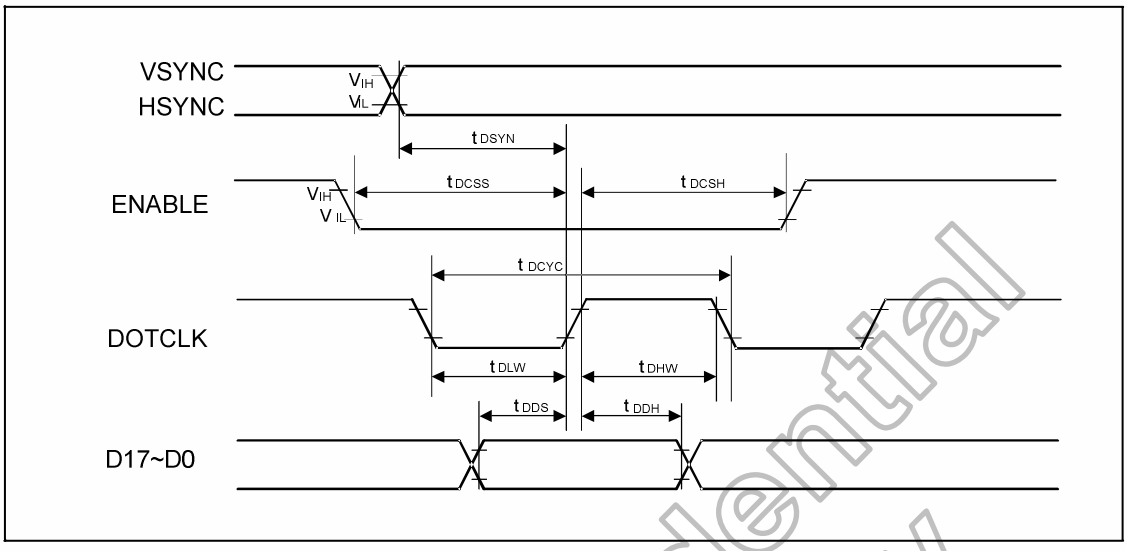
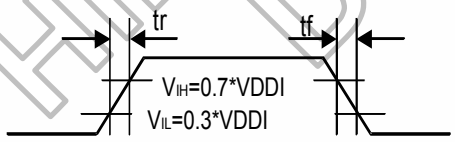


Figure 8. 6 RGB Interface characteristics

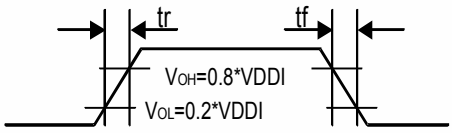
Symbol	Parameter	Conditions	Related Pins	Min.	Typ.	Max.	Unit
t_{DCYC}	DOTCLK cycle time	VRR = Min . 50 Hz Max. 65 Hz	DOTCLK	60 (note2)	-	226 (note3)	ns
t_{DLW} t_{CHW}	DOTCLK Low time DOTCLK High time			15 15	-	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	DOTCLK, D17-D0	15 15	- -	- -	ns
t_{DCSS} t_{DCSH}	ENABLE setup time ENABLE hold Time	-	ENABLE	15 15	-	-	ns
t_{DSYN}	SYNC setup time	-	DOTCLK, HSYNC, VSYNC	15	-	-	ns

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2)16.6 MHz
(3) 4.4MHz

Input Signal Slope



Output Signal Slope



Note: VDDI means IOVCC

Table 8. 3 RGB interface timing

8.7.5 Reset Input Timing

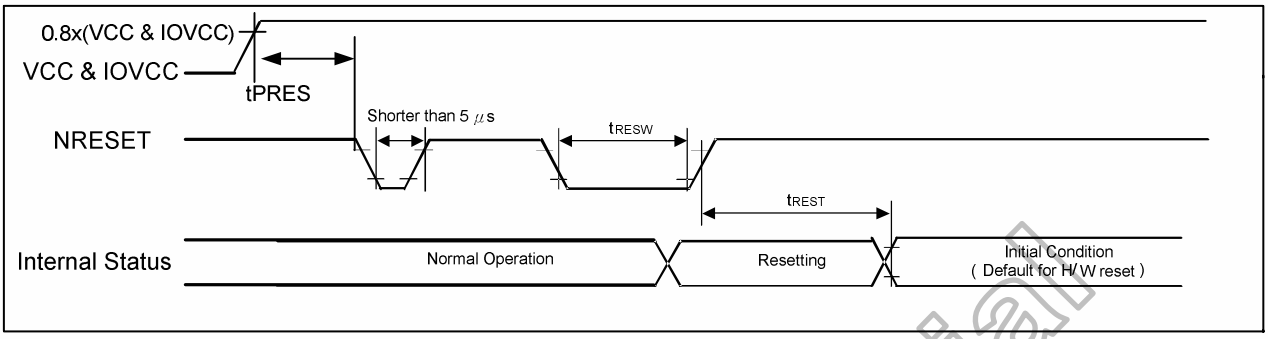


Figure 8. 7 Reset input timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	μs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & VCC/IOVCC	1	-	-	Reset goes high level after Power on	ms

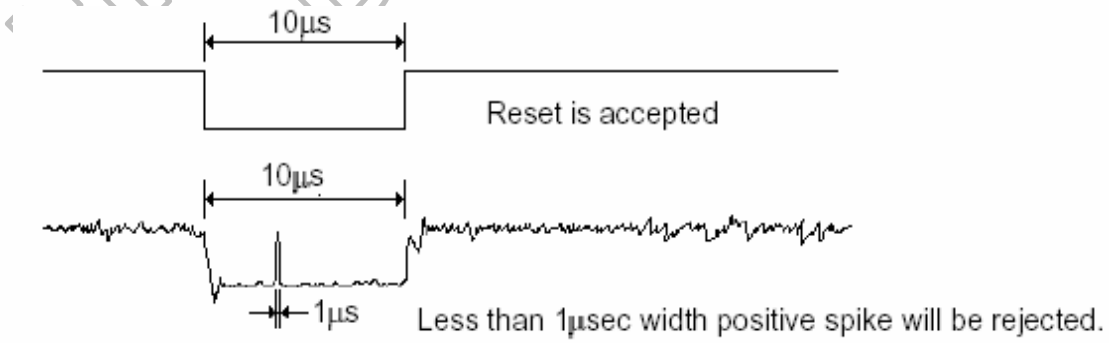
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 μ	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

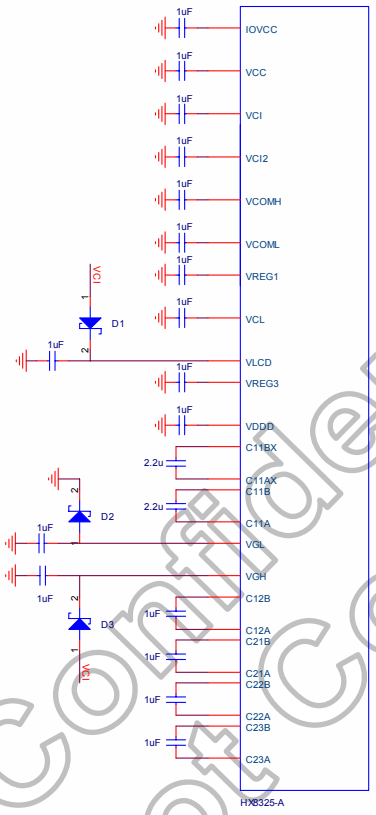


(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out command cannot be sent for 120msec.

Table 8. 4 Reset timing

9. REFERENCE APPLICATIONS

9.1 CONNECTION EXAMPLE WITH EXTERNAL COMPONENTS



9.2 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical value
VCOMH	Connect to Capacitor (Max 6V): VCOMH---(+)----| |--- (-)------ VSSA	1.0 uF
VCOML	Connect to Capacitor (Max 3V): VCOML ---(-)----| |--- (+)----- VSSA	1.0 uF
VGL	Connect to Capacitor (Max 16V): VGL ---(-)----| |--- (+)----- VSSA	1.0 uF
VGH	Connect to Capacitor (Max 21V): VGH ---(+)----| |--- (-)----- VSSA	1.0 uF
VCL	Connect to Capacitor (Max 5V): VCL ---(-)----| |--- (+)----- VSSA	1.0 uF
C23A,C23B	Connect to Capacitor (Max 5V): C23A ---(+)----| |--- (-)-----C23B	1.0 uF
C22A,C22B	Connect to Capacitor (Max 7V): C22A ---(+)----| |--- (-)-----C22B	1.0 uF
C21A,C21B	Connect to Capacitor (Max 7V): C21A ---(+)----| |--- (-)-----C21B	1.0 uF
CX11A,CX11B	Connect to Capacitor (Max 7V): CX11A ---(+)----| |--- (-)-----CX11B	2.2 uF
C11A,C11B	Connect to Capacitor (Max 5V): C11A ---(+)----| |--- (-)-----C11B	2.2 uF
C12A,C12B	Connect to Capacitor (Max 6V): C12A ---(+)----| |--- (-)-----C12B	1.0 uF
VCI2	Connect to Capacitor (Max 6V): VCI2 ---(+)----| |--- (-)-----VSSA	1.0 uF
VREG1	Connect to Capacitor (Max 6V): VREG1 ---(+)----| |--- (-)-----VSSA	1.0 uF
VREG3	Connect to Capacitor (Max 7V): VREG3 ---(+)----| |--- (-)-----VSSA	1.0 uF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 uF
VLCD	Connect to Capacitor (Max 6V): VLCD ---(+)----| |--- (-)-----VSSA	1.0 uF
VCI	Connect to Capacitor (Max 6V): VCI ---(+)----| |--- (-)-----VSSA	1.0 uF
VCC	Connect to Capacitor (Max 6V): VCC ---(+)----| |--- (-)-----VSSA	1.0 uF
IOVCC	Connect to Capacitor (Max 6V): IOVCC---(+)----| |--- (-)-----VSSA	1.0 uF
VSSD – VGL, VCI – VGH, VCI – VLCD	Connect to Schottky Diode	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 9. 1 External component table

10. Ordering information

Part NO.	Package
HX8346-A000 PDxxx	PD : mean COG xxx : mean chip thickness (μm) , (default 400 μm)

11. Revision History

Version	Date	Description of Changes
01	2007/01/22	New setup (HX8346-A For Register-Content interface)
	2007/03/13	1. Modify some typing errors 2. Modify Table 5. 16 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)
	2007/6/21	1. Modify the setting of the PWM_PERIOD[7:0] on R80h and R81h (page 126 and page127)
	2007/6/29	1. Modify the format and timing of GRAM R/W (page 33 and page 47)