# DATA SHEET

*( DOC No. HX8347-A01-DS )*

## HX8347-A01

240RGB x 320 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

*Version 02 November, 2007*

**Himax Technologies, Inc.**
http://www.himax.com.tw

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# 1. General Description

This document describes HX8347-A01 240RGBx320 dots resolution driving controller. The HX8347-A01 is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-A01 can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-A01 also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-A01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

The HX8347-A01 supports three interface modes: Command-Parameter interface mode, Register-Content interface mode and RGB interface mode. Command-Parameter interface mode and Register-Content interface mode are selected by the external pins IFSEL0 setting, and RGB interface mode is selected by internal bit RGB_EN.

This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8347-A(N) datasheet for detail.

# 2. Features

## 2.1 Display

- Resolution: 240(H) x RGB(H) x 320(V)
- Display Color modes
  - A. Normal Display Mode On
    - a. Command-Parameter interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
    - b. Register-Content interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
      - ii. 65,536(R(5),G(6),B(5)) colors
  - B. Idle Mode On
    - a. 8 (R(1),G(1),B(1)) colors.

## 2.2 Display Module

- AM-LCD glass 240xRGBx320
- Gamma correction (4 preset gamma curves)
- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - A. DDVDH = 4.6 to 6.0V (Source output voltage range)
  - B. VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - C. VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240 (H) x 320 (V) x 18 bit

## 2.3 Display/Control Interface

- Display Interface types supported
  - A. Command-Parameter interface mode
    - 8-/16-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.
  - B. Register-Content interface mode
    - 8-/16-/18-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.

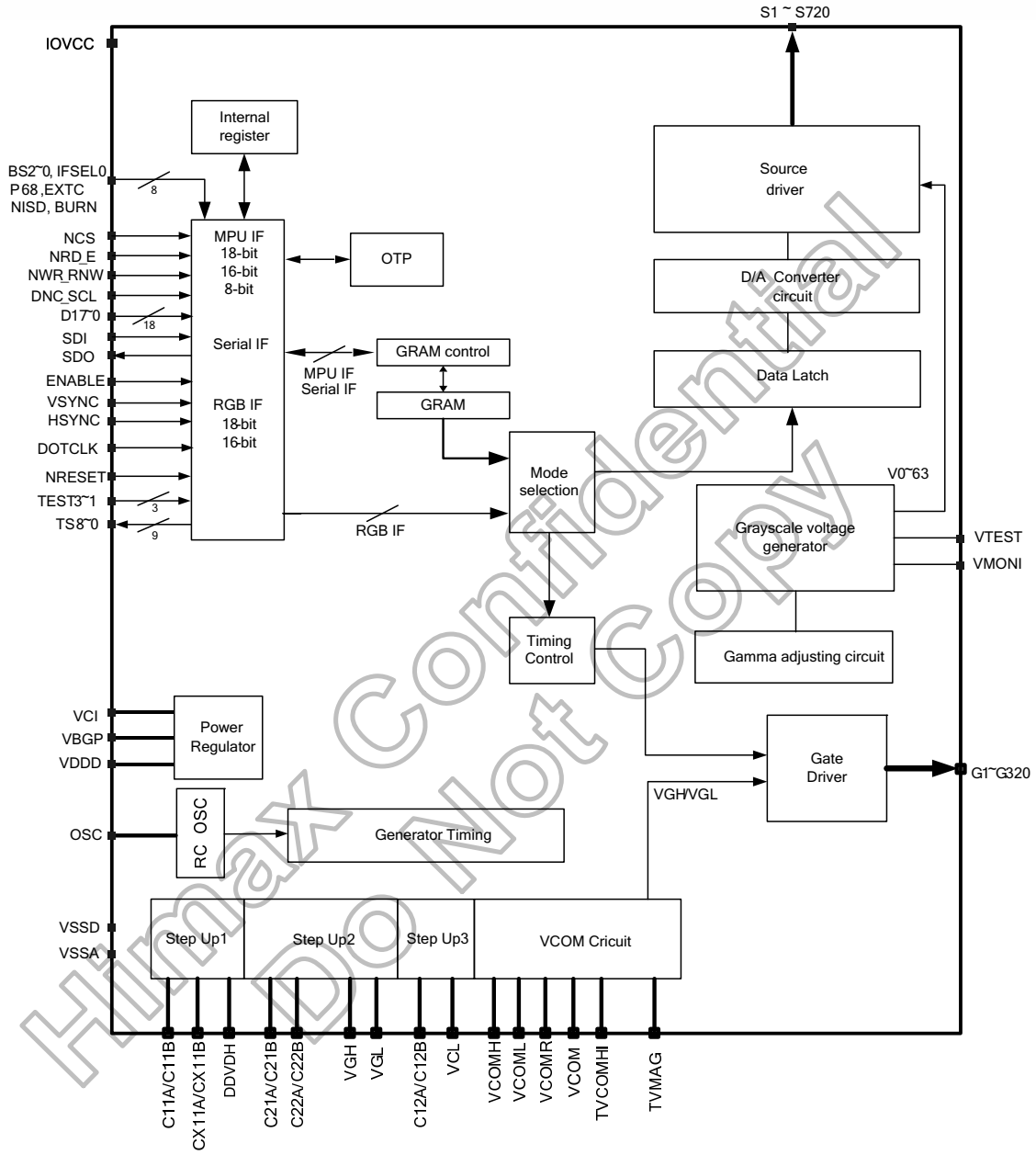
- Control Interface types supported
  - A. Command-Parameter interface mode.( IFSEL0= 0 )
  - B. Register-Content interface mode (IFSEL0 = 1)

- Logic voltage (IOVCC): 1.65 ~ 3.3V
- Driver power supply (VCI): 2.3 ~ 3.3V
- Color modes
  - A. 16 bit/pixel: R(5), G(6), B(5)
  - B. 18 bit/pixel: R(6), G(6), B(6)

## 2.4 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
  - Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support RGB through mode with lower power consumption
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (one-time-programming) non-volatile memory

# 3. Block Diagram



# 4. Pin Description

## 4.1 Pin Description

<table>
<tr><th colspan="8">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="4">Description</th></tr>
<tr><td rowspan="14">P68, BS2,BS1,BS0</td><td rowspan="14">I</td><td rowspan="14">4</td><td rowspan="14">VSSD/ IOVCC</td><td colspan="4">Select the MPU interface mode as listed below<br>Use with IFSEL0=1 Register-content interface mode</td></tr>
<tr><td>P68</td><td>BS2</td><td>BS1</td><td>BS0</td><td>Interface mode</td><td>DB pins</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 65K-Color</td><td>D17-D16: Unused,<br>D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system, 262K-color</td><td>D17-D16: Unused,<br>D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 80-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 80-system, 262K-Color</td><td>D17-D8: Unused<br>D7-D0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 262K-Color</td><td>D17-D16: Unused<br>D15-D0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface, 80-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 65K-Color</td><td>D17-D16: Unused,<br>D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system, 262K-color</td><td>D17-D16: Unused,<br>D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 68-system, 262K-Color</td><td>D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 68-system, 262K-color</td><td>D17-D8:Unused<br>D7-D0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 262K-Color</td><td>D17-D16: Unused<br>D15-D0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface, 68-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>ID</td><td>Serial bus IF</td><td>DNC_SCL, SDO,SDI</td></tr>
<tr><td>IFSEL0</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Interface format select pin<br><table><tr><th>IFSEL0</th><th>Interface Format Selection</th></tr><tr><td>0</td><td>Command-Parameter interface mode</td></tr><tr><td>1</td><td>Register-content interface mode</td></tr></table>In this case, the IFSEL0 has to be connected to IOVCC.</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Chip select signal.<br>Low: chip can be accessed;<br>High: chip cannot be accessed.<br>Must be connected to VSSD if not in use.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">I80 system: Serves as a write signal and writes data at the rising edge.<br>M68 system: 0: Write, 1: Read.<br>Fix it to IOVCC or VSSD level when using serial buss interface.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">I80 system: Serves as a read signal and read data at the low level.<br>M68 system: 0: Read/Write disable, 1: Read/Write enable.<br>Fix it to IOVCC or VSSD level when using serial buss interface.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Free Running mode<br>If BURN=Hi, this can enable free running mode for burn in test.<br>The display data alternates between full black and full white independent of input data in free running mode.</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Serial data input pin.<br>If not used, please let it connected to IOVCC or VSSD.</td></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">The signal for command or parameter select under parallel mode(i.e. Not serial interface):<br>Low: command.<br>High: parameter.<br>When under serial interface, it servers as SCL.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.</td></tr>
</table>

| Input Parts | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| ENABLE | I | 1 | MPU | A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level if unused (High active, if EPL=0). |
| DOTCLK | I | 1 | MPU | Dot clock signal. Has to be fixed to VSSD level if is not used. |
| NRESET | I | 1 | MPU or reset circuit | Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. |
| OSC | I | 1 | Oscillation Resistor | Oscillator input for test purpose.<br>If not used, please let it open or connected to VSSD. |
| VCOMR | I | 1 | Resistor or open | A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8347-A01. |
| VGS | I | 1 | VSSD or external resistor | Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used. |

| Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| S1~S720 | O | 720 | LCD | Output voltages applied to the liquid crystal. |
| G1~G320 | O | 320 | LCD | Gate driver output pins. These pins output VGH, VGL.(If not used, should be open) |
| VCOM | O | 1 | TFT common electrode | The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel. |
| TE | O | 1 | MPU | Tearing effect output.<br>If not used, please open this pin. |
| SDO | O | 1 | MPU | Serial data output. If not use, let it to open. |
| NISD | O | 1 | Open | Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation. |

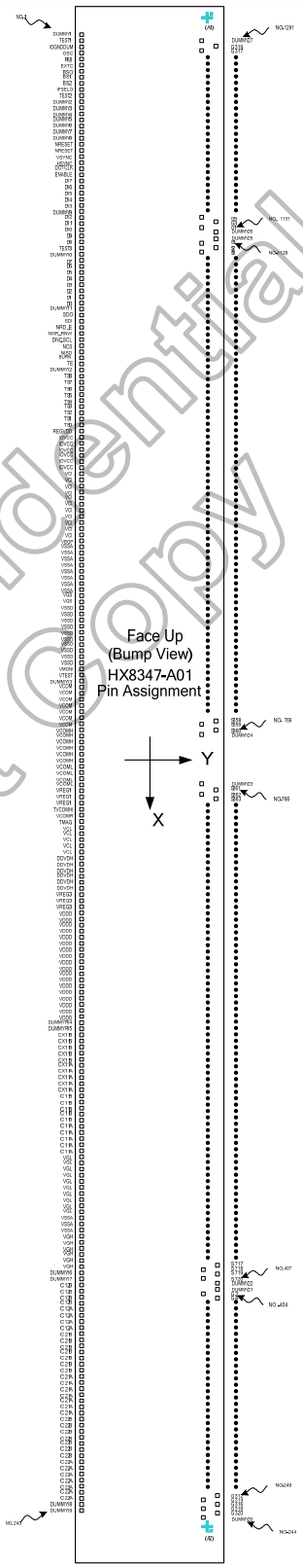
| Input/Output Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| C11A,C11B<br>C12A,C12B | I/O | 4 | Step-up Capacitor | Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used. |
| CX11A, CX11B | I/O | 2 | Step-up Capacitor | Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used. |
| C21A,C21B<br>C22A,C22B | I/O | 4 | Step-up Capacitor | Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them. |
| D17~0 | I/O | 18 | MPU | 1. 18-bit bi-directional data bus for system interface.<br>8-bit bus: use D7-D0 and D17-D8 unused.<br>16-bit bus: use D15-D0 and D17-D16 unused.<br>18-bit bus: use D17-D0<br>2. 18-bit data bus for RGB interface<br>16-bit bus: use D17-D13, D11-D1 and D12, D0 unused.<br>18-bit bus: use D17-D0<br>Those unused pins have to open.<br>Notice: When register RGB_EN=1 and pin ENABLE=1, D[17:0] is used as stream image data for display. It means MPU data bus and RGB data bus is shared. |

| Power Part | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| IOVCC | P | 1 | Power Supply | Digital IO Pad power supply |
| VCI | P | 1 | Power Supply | Analog power supply |
| VSSD | P | 1 | Ground | Digital ground |
| VSSA | P | 1 | Ground | Analog ground |
| VDDD | O | 1 | Stabilizing Capacitor | Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor |
| REGVDD | I | 1 | MPU | If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the VDDD voltage range is 1.65~1.95V.<br>The REGVDD pin must be connected to IOVCC or VSSD. |
| VBGP | - | 1 | Open | Band Gap Voltage. Let it to be open. |
| VREG1 | P | 1 | Stabilizing Capacitor | Internal generated stable power for source driver unit. |
| VREG3 | P | 1 | Stabilizing Capacitor | A reference voltage for VGH&VGL. |
| VCOMH | P | 1 | Stabilizing capacitor | Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation. |
| VCOML | P | 1 | Stabilizing capacitor | When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization. |
| VCL | P | 1 | Stabilizing capacitor | A negative voltage for VCOML circuit, VCL=-VCI |
| DDVDH | P | 1 | Stabilizing capacitor | An output from the step-up circuit1.<br>Connect to a stabilizing capacitor between VSSA and DDVDH.<br>Place a schotkey barrier diode (see “configuration of the power supply”). |
| VGH | P | 1 | Stabilizing capacitor | An output from the step-up circuit2.or 4 ~ 6 time the VCI level.<br>The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH. Place a schottkey barrier diode between VCI and VGH. Place a schottkey barrier diode (see “configuration of the power supply”). |
| VGL | P | 1 | Stabilizing capacitor | An output from the step-up circuit2.or –3 ~ -5 time the VCI level.<br>The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”). |

| Test pin and others | | | | |
|---|---|---|---|---|
| **Signals** | **I/O** | **Pin Number** | **Connected with** | **Description** |
| TEST3-1 | I | 3 | GND | Test pin input (Internal pull low) |
| TS8~0 | O | 9 | Open | A test pin. Disconnect it. |
| VMONI | O | 1 | Open | A test pin. Disconnect it. |
| VTEST | O | 1 | Open | Gamma voltage of Panel test pin output. Must be left open. |
| TVCOMHI | O | 1 | Open | A test pin output. Must be left open. |
| TVMAG | O | 1 | Open | A test pin output. Must be left open. |
| DUMMYR14-15 | - | 2 | Open | Dummy pads. Available for measuring the COG contact resistance. DUMMYR14 and DUMMYR15 are short-circuited within the chip. |
| DUMMY1-13<br>DUMMY16-27 | - | 25 | Open | Dummy pads |
| IOGNDDUM | O | 1 | Open | Short-circuited within the chip |

## 4.2 Pin Assignment

- Chip Size: 17820 um x 865 um
  (Including Seal-ring 20 um *2,
  Scribe line 40 um *2)
- Chip Thickness: 300 um (typ.)
- Pad Location: Pad center
- Coordinate Origin: Chip center
- Au Bump Size:
  1. 50 um x 120 um
     Input/Output
     (No. 1~ No. 243)
  2. 16 um x 98 um
     Staggered LCD output side
     (No. 244 ~ No. 1291)



## 4.3 PAD Coordinates

| No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | DUMMY1 | -8610 | -307.5 | 61 | TS4 | -4130 | -307.5 | 121 | VCOML | 70 | -307.5 | 181 | C11A | 4270 | -307.5 |
| 2 | TEST1 | -8540 | -307.5 | 62 | TS3 | -4060 | -307.5 | 122 | VCOML | 140 | -307.5 | 182 | C11A | 4340 | -307.5 |
| 3 | IOGNDDUM | -8470 | -307.5 | 63 | TS2 | -3990 | -307.5 | 123 | VCOML | 210 | -307.5 | 183 | C11A | 4410 | -307.5 |
| 4 | OSC | -8400 | -307.5 | 64 | TS1 | -3920 | -307.5 | 124 | VCOML | 280 | -307.5 | 184 | C11A | 4480 | -307.5 |
| 5 | P68 | -8330 | -307.5 | 65 | TS0 | -3850 | -307.5 | 125 | VREG1 | 350 | -307.5 | 185 | VGL | 4550 | -307.5 |
| 6 | EXTC | -8260 | -307.5 | 66 | REGVDD | -3780 | -307.5 | 126 | VREG1 | 420 | -307.5 | 186 | VGL | 4620 | -307.5 |
| 7 | BS0 | -8190 | -307.5 | 67 | IOVCC | -3710 | -307.5 | 127 | VREG1 | 490 | -307.5 | 187 | VGL | 4690 | -307.5 |
| 8 | BS1 | -8120 | -307.5 | 68 | IOVCC | -3640 | -307.5 | 128 | TVCOMHI | 560 | -307.5 | 188 | VGL | 4760 | -307.5 |
| 9 | BS2 | -8050 | -307.5 | 69 | IOVCC | -3570 | -307.5 | 129 | VCOMR | 630 | -307.5 | 189 | VGL | 4830 | -307.5 |
| 10 | IFSEL0 | -7980 | -307.5 | 70 | IOVCC | -3500 | -307.5 | 130 | TMAG | 700 | -307.5 | 190 | VGL | 4900 | -307.5 |
| 11 | TEST2 | -7910 | -307.5 | 71 | IOVCC | -3430 | -307.5 | 131 | VCL | 770 | -307.5 | 191 | VGL | 4970 | -307.5 |
| 12 | DUMMY2 | -7840 | -307.5 | 72 | IOVCC | -3360 | -307.5 | 132 | VCL | 840 | -307.5 | 192 | VGL | 5040 | -307.5 |
| 13 | DUMMY3 | -7770 | -307.5 | 73 | VCI | -3290 | -307.5 | 133 | VCL | 910 | -307.5 | 193 | VGL | 5110 | -307.5 |
| 14 | DUMMY4 | -7700 | -307.5 | 74 | VCI | -3220 | -307.5 | 134 | VCL | 980 | -307.5 | 194 | VGL | 5180 | -307.5 |
| 15 | DUMMY5 | -7630 | -307.5 | 75 | VCI | -3150 | -307.5 | 135 | VCL | 1050 | -307.5 | 195 | VSSA | 5250 | -307.5 |
| 16 | DUMMY6 | -7560 | -307.5 | 76 | VCI | -3080 | -307.5 | 136 | DDVDH | 1120 | -307.5 | 196 | VSSA | 5320 | -307.5 |
| 17 | DUMMY7 | -7490 | -307.5 | 77 | VCI | -3010 | -307.5 | 137 | DDVDH | 1190 | -307.5 | 197 | VSSA | 5390 | -307.5 |
| 18 | DUMMY8 | -7420 | -307.5 | 78 | VCI | -2940 | -307.5 | 138 | DDVDH | 1260 | -307.5 | 198 | VGH | 5460 | -307.5 |
| 19 | NRESET | -7350 | -307.5 | 79 | VCI | -2870 | -307.5 | 139 | DDVDH | 1330 | -307.5 | 199 | VGH | 5530 | -307.5 |
| 20 | NRESET | -7280 | -307.5 | 80 | VCI | -2800 | -307.5 | 140 | DDVDH | 1400 | -307.5 | 200 | VGH | 5600 | -307.5 |
| 21 | VSYNC | -7210 | -307.5 | 81 | VCI | -2730 | -307.5 | 141 | DDVDH | 1470 | -307.5 | 201 | VGH | 5670 | -307.5 |
| 22 | HSYNC | -7140 | -307.5 | 82 | VCI | -2660 | -307.5 | 142 | VREG3 | 1540 | -307.5 | 202 | VGH | 5740 | -307.5 |
| 23 | DOTCLK | -7070 | -307.5 | 83 | VCI | -2590 | -307.5 | 143 | VREG3 | 1610 | -307.5 | 203 | VGH | 5810 | -307.5 |
| 24 | ENABLE | -7000 | -307.5 | 84 | VBGP | -2520 | -307.5 | 144 | VREG3 | 1680 | -307.5 | 204 | DUMMY16 | 5880 | -307.5 |
| 25 | D17 | -6905 | -307.5 | 85 | VSSA | -2450 | -307.5 | 145 | VDDD | 1750 | -307.5 | 205 | DUMMY17 | 5950 | -307.5 |
| 26 | D16 | -6825 | -307.5 | 86 | VSSA | -2380 | -307.5 | 146 | VDDD | 1820 | -307.5 | 206 | C12B | 6020 | -307.5 |
| 27 | D15 | -6745 | -307.5 | 87 | VSSA | -2310 | -307.5 | 147 | VDDD | 1890 | -307.5 | 207 | C12B | 6090 | -307.5 |
| 28 | D14 | -6665 | -307.5 | 88 | VSSA | -2240 | -307.5 | 148 | VDDD | 1960 | -307.5 | 208 | C12B | 6160 | -307.5 |
| 29 | D13 | -6585 | -307.5 | 89 | VSSA | -2170 | -307.5 | 149 | VDDD | 2030 | -307.5 | 209 | C12B | 6230 | -307.5 |
| 30 | DUMMY9 | -6495 | -307.5 | 90 | VSSA | -2100 | -307.5 | 150 | VDDD | 2100 | -307.5 | 210 | C12A | 6300 | -307.5 |
| 31 | D12 | -6405 | -307.5 | 91 | VSSA | -2030 | -307.5 | 151 | VDDD | 2170 | -307.5 | 211 | C12A | 6370 | -307.5 |
| 32 | D11 | -6325 | -307.5 | 92 | VSSA | -1960 | -307.5 | 152 | VDDD | 2240 | -307.5 | 212 | C12A | 6440 | -307.5 |
| 33 | D10 | -6245 | -307.5 | 93 | VGS | -1890 | -307.5 | 153 | VDDD | 2310 | -307.5 | 213 | C12A | 6510 | -307.5 |
| 34 | D9 | -6165 | -307.5 | 94 | VGS | -1820 | -307.5 | 154 | VDDD | 2380 | -307.5 | 214 | C21B | 6580 | -307.5 |
| 35 | D8 | -6085 | -307.5 | 95 | VSSD | -1750 | -307.5 | 155 | VDDD | 2450 | -307.5 | 215 | C21B | 6650 | -307.5 |
| 36 | TEST3 | -5990 | -307.5 | 96 | VSSD | -1680 | -307.5 | 156 | VDDD | 2520 | -307.5 | 216 | C21B | 6720 | -307.5 |
| 37 | DUMMY10 | -5920 | -307.5 | 97 | VSSD | -1610 | -307.5 | 157 | VDDD | 2590 | -307.5 | 217 | C21B | 6790 | -307.5 |
| 38 | D7 | -5825 | -307.5 | 98 | VSSD | -1540 | -307.5 | 158 | VDDD | 2660 | -307.5 | 218 | C21B | 6860 | -307.5 |
| 39 | D6 | -5745 | -307.5 | 99 | VSSD | -1470 | -307.5 | 159 | VDDD | 2730 | -307.5 | 219 | C21B | 6930 | -307.5 |
| 40 | D5 | -5665 | -307.5 | 100 | VSSD | -1400 | -307.5 | 160 | VDDD | 2800 | -307.5 | 220 | C21B | 7000 | -307.5 |
| 41 | D4 | -5585 | -307.5 | 101 | VSSD | -1330 | -307.5 | 161 | VDDD | 2870 | -307.5 | 221 | C21A | 7070 | -307.5 |
| 42 | D3 | -5505 | -307.5 | 102 | VSSD | -1260 | -307.5 | 162 | VDDD | 2940 | -307.5 | 222 | C21A | 7140 | -307.5 |
| 43 | D2 | -5425 | -307.5 | 103 | VSSD | -1190 | -307.5 | 163 | DUMMYR14 | 3010 | -307.5 | 223 | C21A | 7210 | -307.5 |
| 44 | D1 | -5345 | -307.5 | 104 | VSSD | -1120 | -307.5 | 164 | DUMMYR15 | 3080 | -307.5 | 224 | C21A | 7280 | -307.5 |
| 45 | D0 | -5265 | -307.5 | 105 | VMONI | -1050 | -307.5 | 165 | CX11B | 3150 | -307.5 | 225 | C21A | 7350 | -307.5 |
| 46 | DUMMY11 | -5180 | -307.5 | 106 | VTEST | -980 | -307.5 | 166 | CX11B | 3220 | -307.5 | 226 | C21A | 7420 | -307.5 |
| 47 | SDO | -5110 | -307.5 | 107 | DUMMY13 | -910 | -307.5 | 167 | CX11B | 3290 | -307.5 | 227 | C21A | 7490 | -307.5 |
| 48 | SDI | -5040 | -307.5 | 108 | VCOM | -840 | -307.5 | 168 | CX11B | 3360 | -307.5 | 228 | C22B | 7560 | -307.5 |
| 49 | NRD_E | -4970 | -307.5 | 109 | VCOM | -770 | -307.5 | 169 | CX11B | 3430 | -307.5 | 229 | C22B | 7630 | -307.5 |
| 50 | NWR_RNW | -4900 | -307.5 | 110 | VCOM | -700 | -307.5 | 170 | CX11A | 3500 | -307.5 | 230 | C22B | 7700 | -307.5 |
| 51 | DNC_SCL | -4830 | -307.5 | 111 | VCOM | -630 | -307.5 | 171 | CX11A | 3570 | -307.5 | 231 | C22B | 7770 | -307.5 |
| 52 | NCS | -4760 | -307.5 | 112 | VCOM | -560 | -307.5 | 172 | CX11A | 3640 | -307.5 | 232 | C22B | 7840 | -307.5 |
| 53 | NISD | -4690 | -307.5 | 113 | VCOM | -490 | -307.5 | 173 | CX11A | 3710 | -307.5 | 233 | C22B | 7910 | -307.5 |
| 54 | BURN | -4620 | -307.5 | 114 | VCOM | -420 | -307.5 | 174 | CX11A | 3780 | -307.5 | 234 | C22B | 7980 | -307.5 |
| 55 | TE | -4550 | -307.5 | 115 | VCOMH | -350 | -307.5 | 175 | C11B | 3850 | -307.5 | 235 | C22A | 8050 | -307.5 |
| 56 | DUMMY12 | -4480 | -307.5 | 116 | VCOMH | -280 | -307.5 | 176 | C11B | 3920 | -307.5 | 236 | C22A | 8120 | -307.5 |
| 57 | TS8 | -4410 | -307.5 | 117 | VCOMH | -210 | -307.5 | 177 | C11B | 3990 | -307.5 | 237 | C22A | 8190 | -307.5 |
| 58 | TS7 | -4340 | -307.5 | 118 | VCOMH | -140 | -307.5 | 178 | C11B | 4060 | -307.5 | 238 | C22A | 8260 | -307.5 |
| 59 | TS6 | -4270 | -307.5 | 119 | VCOMH | -70 | -307.5 | 179 | C11B | 4130 | -307.5 | 239 | C22A | 8330 | -307.5 |
| 60 | TS5 | -4200 | -307.5 | 120 | VCOMH | 0 | -307.5 | 180 | C11A | 4200 | -307.5 | 240 | C22A | 8400 | -307.5 |

| No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y |
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| 242 | DUMMY18 | 8540 | -307.5 | 302 | G206 | 7731 | 202.5 | 362 | G86 | 6771 | 202.5 | 422 | S705 | 5791 | 319.5 |
| 243 | DUMMY19 | 8610 | -307.5 | 303 | G204 | 7715 | 319.5 | 363 | G84 | 6755 | 319.5 | 423 | S704 | 5775 | 202.5 |
| 244 | DUMMY20 | 8659 | 202.5 | 304 | G202 | 7699 | 202.5 | 364 | G82 | 6739 | 202.5 | 424 | S703 | 5759 | 319.5 |
| 245 | G320 | 8643 | 319.5 | 305 | G200 | 7683 | 319.5 | 365 | G80 | 6723 | 319.5 | 425 | S702 | 5743 | 202.5 |
| 246 | G318 | 8627 | 202.5 | 306 | G198 | 7667 | 202.5 | 366 | G78 | 6707 | 202.5 | 426 | S701 | 5727 | 319.5 |
| 247 | G316 | 8611 | 319.5 | 307 | G196 | 7651 | 319.5 | 367 | G76 | 6691 | 319.5 | 427 | S700 | 5711 | 202.5 |
| 248 | G314 | 8595 | 202.5 | 308 | G194 | 7635 | 202.5 | 368 | G74 | 6675 | 202.5 | 428 | S699 | 5695 | 319.5 |
| 249 | G312 | 8579 | 319.5 | 309 | G192 | 7619 | 319.5 | 369 | G72 | 6659 | 319.5 | 429 | S698 | 5679 | 202.5 |
| 250 | G310 | 8563 | 202.5 | 310 | G190 | 7603 | 202.5 | 370 | G70 | 6643 | 202.5 | 430 | S697 | 5663 | 319.5 |
| 251 | G308 | 8547 | 319.5 | 311 | G188 | 7587 | 319.5 | 371 | G68 | 6627 | 319.5 | 431 | S696 | 5647 | 202.5 |
| 252 | G306 | 8531 | 202.5 | 312 | G186 | 7571 | 202.5 | 372 | G66 | 6611 | 202.5 | 432 | S695 | 5631 | 319.5 |
| 253 | G304 | 8515 | 319.5 | 313 | G184 | 7555 | 319.5 | 373 | G64 | 6595 | 319.5 | 433 | S694 | 5615 | 202.5 |
| 254 | G302 | 8499 | 202.5 | 314 | G182 | 7539 | 202.5 | 374 | G62 | 6579 | 202.5 | 434 | S693 | 5599 | 319.5 |
| 255 | G300 | 8483 | 319.5 | 315 | G180 | 7523 | 319.5 | 375 | G60 | 6563 | 319.5 | 435 | S692 | 5583 | 202.5 |
| 256 | G298 | 8467 | 202.5 | 316 | G178 | 7507 | 202.5 | 376 | G58 | 6547 | 202.5 | 436 | S691 | 5567 | 319.5 |
| 257 | G296 | 8451 | 319.5 | 317 | G176 | 7491 | 319.5 | 377 | G56 | 6531 | 319.5 | 437 | S690 | 5551 | 202.5 |
| 258 | G294 | 8435 | 202.5 | 318 | G174 | 7475 | 202.5 | 378 | G54 | 6515 | 202.5 | 438 | S689 | 5535 | 319.5 |
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| 260 | G290 | 8403 | 202.5 | 320 | G170 | 7443 | 202.5 | 380 | G50 | 6483 | 202.5 | 440 | S687 | 5503 | 319.5 |
| 261 | G288 | 8387 | 319.5 | 321 | G168 | 7427 | 319.5 | 381 | G48 | 6467 | 319.5 | 441 | S686 | 5487 | 202.5 |
| 262 | G286 | 8371 | 202.5 | 322 | G166 | 7411 | 202.5 | 382 | G46 | 6451 | 202.5 | 442 | S685 | 5471 | 319.5 |
| 263 | G284 | 8355 | 319.5 | 323 | G164 | 7395 | 319.5 | 383 | G44 | 6435 | 319.5 | 443 | S684 | 5455 | 202.5 |
| 264 | G282 | 8339 | 202.5 | 324 | G162 | 7379 | 202.5 | 384 | G42 | 6419 | 202.5 | 444 | S683 | 5439 | 319.5 |
| 265 | G280 | 8323 | 319.5 | 325 | G160 | 7363 | 319.5 | 385 | G40 | 6403 | 319.5 | 445 | S682 | 5423 | 202.5 |
| 266 | G278 | 8307 | 202.5 | 326 | G158 | 7347 | 202.5 | 386 | G38 | 6387 | 202.5 | 446 | S681 | 5407 | 319.5 |
| 267 | G276 | 8291 | 319.5 | 327 | G156 | 7331 | 319.5 | 387 | G36 | 6371 | 319.5 | 447 | S680 | 5391 | 202.5 |
| 268 | G274 | 8275 | 202.5 | 328 | G154 | 7315 | 202.5 | 388 | G34 | 6355 | 202.5 | 448 | S679 | 5375 | 319.5 |
| 269 | G272 | 8259 | 319.5 | 329 | G152 | 7299 | 319.5 | 389 | G32 | 6339 | 319.5 | 449 | S678 | 5359 | 202.5 |
| 270 | G270 | 8243 | 202.5 | 330 | G150 | 7283 | 202.5 | 390 | G30 | 6323 | 202.5 | 450 | S677 | 5343 | 319.5 |
| 271 | G268 | 8227 | 319.5 | 331 | G148 | 7267 | 319.5 | 391 | G28 | 6307 | 319.5 | 451 | S676 | 5327 | 202.5 |
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| 273 | G264 | 8195 | 319.5 | 333 | G144 | 7235 | 319.5 | 393 | G24 | 6275 | 319.5 | 453 | S674 | 5295 | 202.5 |
| 274 | G262 | 8179 | 202.5 | 334 | G142 | 7219 | 202.5 | 394 | G22 | 6259 | 202.5 | 454 | S673 | 5279 | 319.5 |
| 275 | G260 | 8163 | 319.5 | 335 | G140 | 7203 | 319.5 | 395 | G20 | 6243 | 319.5 | 455 | S672 | 5263 | 202.5 |
| 276 | G258 | 8147 | 202.5 | 336 | G138 | 7187 | 202.5 | 396 | G18 | 6227 | 202.5 | 456 | S671 | 5247 | 319.5 |
| 277 | G256 | 8131 | 319.5 | 337 | G136 | 7171 | 319.5 | 397 | G16 | 6211 | 319.5 | 457 | S670 | 5231 | 202.5 |
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| 282 | G246 | 8051 | 202.5 | 342 | G126 | 7091 | 202.5 | 402 | G6 | 6131 | 202.5 | 462 | S665 | 5151 | 319.5 |
| 283 | G244 | 8035 | 319.5 | 343 | G124 | 7075 | 319.5 | 403 | G4 | 6115 | 319.5 | 463 | S664 | 5135 | 202.5 |
| 284 | G242 | 8019 | 202.5 | 344 | G122 | 7059 | 202.5 | 404 | G2 | 6099 | 202.5 | 464 | S663 | 5119 | 319.5 |
| 285 | G240 | 8003 | 319.5 | 345 | G120 | 7043 | 319.5 | 405 | DUMMY21 | 6083 | 319.5 | 465 | S662 | 5103 | 202.5 |
| 286 | G238 | 7987 | 202.5 | 346 | G118 | 7027 | 202.5 | 406 | DUMMY22 | 6047 | 319.5 | 466 | S661 | 5087 | 319.5 |
| 287 | G236 | 7971 | 319.5 | 347 | G116 | 7011 | 319.5 | 407 | S720 | 6031 | 202.5 | 467 | S660 | 5071 | 202.5 |
| 288 | G234 | 7955 | 202.5 | 348 | G114 | 6995 | 202.5 | 408 | S719 | 6015 | 319.5 | 468 | S659 | 5055 | 319.5 |
| 289 | G232 | 7939 | 319.5 | 349 | G112 | 6979 | 319.5 | 409 | S718 | 5999 | 202.5 | 469 | S658 | 5039 | 202.5 |
| 290 | G230 | 7923 | 202.5 | 350 | G110 | 6963 | 202.5 | 410 | S717 | 5983 | 319.5 | 470 | S657 | 5023 | 319.5 |
| 291 | G228 | 7907 | 319.5 | 351 | G108 | 6947 | 319.5 | 411 | S716 | 5967 | 202.5 | 471 | S656 | 5007 | 202.5 |
| 292 | G226 | 7891 | 202.5 | 352 | G106 | 6931 | 202.5 | 412 | S715 | 5951 | 319.5 | 472 | S655 | 4991 | 319.5 |
| 293 | G224 | 7875 | 319.5 | 353 | G104 | 6915 | 319.5 | 413 | S714 | 5935 | 202.5 | 473 | S654 | 4975 | 202.5 |
| 294 | G222 | 7859 | 202.5 | 354 | G102 | 6899 | 202.5 | 414 | S713 | 5919 | 319.5 | 474 | S653 | 4959 | 319.5 |
| 295 | G220 | 7843 | 319.5 | 355 | G100 | 6883 | 319.5 | 415 | S712 | 5903 | 202.5 | 475 | S652 | 4943 | 202.5 |
| 296 | G218 | 7827 | 202.5 | 356 | G98 | 6867 | 202.5 | 416 | S711 | 5887 | 319.5 | 476 | S651 | 4927 | 319.5 |
| 297 | G216 | 7811 | 319.5 | 357 | G96 | 6851 | 319.5 | 417 | S710 | 5871 | 202.5 | 477 | S650 | 4911 | 202.5 |
| 298 | G214 | 7795 | 202.5 | 358 | G94 | 6835 | 202.5 | 418 | S709 | 5855 | 319.5 | 478 | S649 | 4895 | 319.5 |
| 299 | G212 | 7779 | 319.5 | 359 | G92 | 6819 | 319.5 | 419 | S708 | 5839 | 202.5 | 479 | S648 | 4879 | 202.5 |
| 300 | G210 | 7763 | 202.5 | 360 | G90 | 6803 | 202.5 | 420 | S707 | 5823 | 319.5 | 480 | S647 | 4863 | 319.5 |

| No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y |
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| 481 | S646 | 4847 | 202.5 | 541 | S586 | 3887 | 202.5 | 601 | S526 | 2927 | 202.5 | 661 | S466 | 1967 | 202.5 |
| 482 | S645 | 4831 | 319.5 | 542 | S585 | 3871 | 319.5 | 602 | S525 | 2911 | 319.5 | 662 | S465 | 1951 | 319.5 |
| 483 | S644 | 4815 | 202.5 | 543 | S584 | 3855 | 202.5 | 603 | S524 | 2895 | 202.5 | 663 | S464 | 1935 | 202.5 |
| 484 | S643 | 4799 | 319.5 | 544 | S583 | 3839 | 319.5 | 604 | S523 | 2879 | 319.5 | 664 | S463 | 1919 | 319.5 |
| 485 | S642 | 4783 | 202.5 | 545 | S582 | 3823 | 202.5 | 605 | S522 | 2863 | 202.5 | 665 | S462 | 1903 | 202.5 |
| 486 | S641 | 4767 | 319.5 | 546 | S581 | 3807 | 319.5 | 606 | S521 | 2847 | 319.5 | 666 | S461 | 1887 | 319.5 |
| 487 | S640 | 4751 | 202.5 | 547 | S580 | 3791 | 202.5 | 607 | S520 | 2831 | 202.5 | 667 | S460 | 1871 | 202.5 |
| 488 | S639 | 4735 | 319.5 | 548 | S579 | 3775 | 319.5 | 608 | S519 | 2815 | 319.5 | 668 | S459 | 1855 | 319.5 |
| 489 | S638 | 4719 | 202.5 | 549 | S578 | 3759 | 202.5 | 609 | S518 | 2799 | 202.5 | 669 | S458 | 1839 | 202.5 |
| 490 | S637 | 4703 | 319.5 | 550 | S577 | 3743 | 319.5 | 610 | S517 | 2783 | 319.5 | 670 | S457 | 1823 | 319.5 |
| 491 | S636 | 4687 | 202.5 | 551 | S576 | 3727 | 202.5 | 611 | S516 | 2767 | 202.5 | 671 | S456 | 1807 | 202.5 |
| 492 | S635 | 4671 | 319.5 | 552 | S575 | 3711 | 319.5 | 612 | S515 | 2751 | 319.5 | 672 | S455 | 1791 | 319.5 |
| 493 | S634 | 4655 | 202.5 | 553 | S574 | 3695 | 202.5 | 613 | S514 | 2735 | 202.5 | 673 | S454 | 1775 | 202.5 |
| 494 | S633 | 4639 | 319.5 | 554 | S573 | 3679 | 319.5 | 614 | S513 | 2719 | 319.5 | 674 | S453 | 1759 | 319.5 |
| 495 | S632 | 4623 | 202.5 | 555 | S572 | 3663 | 202.5 | 615 | S512 | 2703 | 202.5 | 675 | S452 | 1743 | 202.5 |
| 496 | S631 | 4607 | 319.5 | 556 | S571 | 3647 | 319.5 | 616 | S511 | 2687 | 319.5 | 676 | S451 | 1727 | 319.5 |
| 497 | S630 | 4591 | 202.5 | 557 | S570 | 3631 | 202.5 | 617 | S510 | 2671 | 202.5 | 677 | S450 | 1711 | 202.5 |
| 498 | S629 | 4575 | 319.5 | 558 | S569 | 3615 | 319.5 | 618 | S509 | 2655 | 319.5 | 678 | S449 | 1695 | 319.5 |
| 499 | S628 | 4559 | 202.5 | 559 | S568 | 3599 | 202.5 | 619 | S508 | 2639 | 202.5 | 679 | S448 | 1679 | 202.5 |
| 500 | S627 | 4543 | 319.5 | 560 | S567 | 3583 | 319.5 | 620 | S507 | 2623 | 319.5 | 680 | S447 | 1663 | 319.5 |
| 501 | S626 | 4527 | 202.5 | 561 | S566 | 3567 | 202.5 | 621 | S506 | 2607 | 202.5 | 681 | S446 | 1647 | 202.5 |
| 502 | S625 | 4511 | 319.5 | 562 | S565 | 3551 | 319.5 | 622 | S505 | 2591 | 319.5 | 682 | S445 | 1631 | 319.5 |
| 503 | S624 | 4495 | 202.5 | 563 | S564 | 3535 | 202.5 | 623 | S504 | 2575 | 202.5 | 683 | S444 | 1615 | 202.5 |
| 504 | S623 | 4479 | 319.5 | 564 | S563 | 3519 | 319.5 | 624 | S503 | 2559 | 319.5 | 684 | S443 | 1599 | 319.5 |
| 505 | S622 | 4463 | 202.5 | 565 | S562 | 3503 | 202.5 | 625 | S502 | 2543 | 202.5 | 685 | S442 | 1583 | 202.5 |
| 506 | S621 | 4447 | 319.5 | 566 | S561 | 3487 | 319.5 | 626 | S501 | 2527 | 319.5 | 686 | S441 | 1567 | 319.5 |
| 507 | S620 | 4431 | 202.5 | 567 | S560 | 3471 | 202.5 | 627 | S500 | 2511 | 202.5 | 687 | S440 | 1551 | 202.5 |
| 508 | S619 | 4415 | 319.5 | 568 | S559 | 3455 | 319.5 | 628 | S499 | 2495 | 319.5 | 688 | S439 | 1535 | 319.5 |
| 509 | S618 | 4399 | 202.5 | 569 | S558 | 3439 | 202.5 | 629 | S498 | 2479 | 202.5 | 689 | S438 | 1519 | 202.5 |
| 510 | S617 | 4383 | 319.5 | 570 | S557 | 3423 | 319.5 | 630 | S497 | 2463 | 319.5 | 690 | S437 | 1503 | 319.5 |
| 511 | S616 | 4367 | 202.5 | 571 | S556 | 3407 | 202.5 | 631 | S496 | 2447 | 202.5 | 691 | S436 | 1487 | 202.5 |
| 512 | S615 | 4351 | 319.5 | 572 | S555 | 3391 | 319.5 | 632 | S495 | 2431 | 319.5 | 692 | S435 | 1471 | 319.5 |
| 513 | S614 | 4335 | 202.5 | 573 | S554 | 3375 | 202.5 | 633 | S494 | 2415 | 202.5 | 693 | S434 | 1455 | 202.5 |
| 514 | S613 | 4319 | 319.5 | 574 | S553 | 3359 | 319.5 | 634 | S493 | 2399 | 319.5 | 694 | S433 | 1439 | 319.5 |
| 515 | S612 | 4303 | 202.5 | 575 | S552 | 3343 | 202.5 | 635 | S492 | 2383 | 202.5 | 695 | S432 | 1423 | 202.5 |
| 516 | S611 | 4287 | 319.5 | 576 | S551 | 3327 | 319.5 | 636 | S491 | 2367 | 319.5 | 696 | S431 | 1407 | 319.5 |
| 517 | S610 | 4271 | 202.5 | 577 | S550 | 3311 | 202.5 | 637 | S490 | 2351 | 202.5 | 697 | S430 | 1391 | 202.5 |
| 518 | S609 | 4255 | 319.5 | 578 | S549 | 3295 | 319.5 | 638 | S489 | 2335 | 319.5 | 698 | S429 | 1375 | 319.5 |
| 519 | S608 | 4239 | 202.5 | 579 | S548 | 3279 | 202.5 | 639 | S488 | 2319 | 202.5 | 699 | S428 | 1359 | 202.5 |
| 520 | S607 | 4223 | 319.5 | 580 | S547 | 3263 | 319.5 | 640 | S487 | 2303 | 319.5 | 700 | S427 | 1343 | 319.5 |
| 521 | S606 | 4207 | 202.5 | 581 | S546 | 3247 | 202.5 | 641 | S486 | 2287 | 202.5 | 701 | S426 | 1327 | 202.5 |
| 522 | S605 | 4191 | 319.5 | 582 | S545 | 3231 | 319.5 | 642 | S485 | 2271 | 319.5 | 702 | S425 | 1311 | 319.5 |
| 523 | S604 | 4175 | 202.5 | 583 | S544 | 3215 | 202.5 | 643 | S484 | 2255 | 202.5 | 703 | S424 | 1295 | 202.5 |
| 524 | S603 | 4159 | 319.5 | 584 | S543 | 3199 | 319.5 | 644 | S483 | 2239 | 319.5 | 704 | S423 | 1279 | 319.5 |
| 525 | S602 | 4143 | 202.5 | 585 | S542 | 3183 | 202.5 | 645 | S482 | 2223 | 202.5 | 705 | S422 | 1263 | 202.5 |
| 526 | S601 | 4127 | 319.5 | 586 | S541 | 3167 | 319.5 | 646 | S481 | 2207 | 319.5 | 706 | S421 | 1247 | 319.5 |
| 527 | S600 | 4111 | 202.5 | 587 | S540 | 3151 | 202.5 | 647 | S480 | 2191 | 202.5 | 707 | S420 | 1231 | 202.5 |
| 528 | S599 | 4095 | 319.5 | 588 | S539 | 3135 | 319.5 | 648 | S479 | 2175 | 319.5 | 708 | S419 | 1215 | 319.5 |
| 529 | S598 | 4079 | 202.5 | 589 | S538 | 3119 | 202.5 | 649 | S478 | 2159 | 202.5 | 709 | S418 | 1199 | 202.5 |
| 530 | S597 | 4063 | 319.5 | 590 | S537 | 3103 | 319.5 | 650 | S477 | 2143 | 319.5 | 710 | S417 | 1183 | 319.5 |
| 531 | S596 | 4047 | 202.5 | 591 | S536 | 3087 | 202.5 | 651 | S476 | 2127 | 202.5 | 711 | S416 | 1167 | 202.5 |
| 532 | S595 | 4031 | 319.5 | 592 | S535 | 3071 | 319.5 | 652 | S475 | 2111 | 319.5 | 712 | S415 | 1151 | 319.5 |
| 533 | S594 | 4015 | 202.5 | 593 | S534 | 3055 | 202.5 | 653 | S474 | 2095 | 202.5 | 713 | S414 | 1135 | 202.5 |
| 534 | S593 | 3999 | 319.5 | 594 | S533 | 3039 | 319.5 | 654 | S473 | 2079 | 319.5 | 714 | S413 | 1119 | 319.5 |
| 535 | S592 | 3983 | 202.5 | 595 | S532 | 3023 | 202.5 | 655 | S472 | 2063 | 202.5 | 715 | S412 | 1103 | 202.5 |
| 536 | S591 | 3967 | 319.5 | 596 | S531 | 3007 | 319.5 | 656 | S471 | 2047 | 319.5 | 716 | S411 | 1087 | 319.5 |
| 537 | S590 | 3951 | 202.5 | 597 | S530 | 2991 | 202.5 | 657 | S470 | 2031 | 202.5 | 717 | S410 | 1071 | 202.5 |
| 538 | S589 | 3935 | 319.5 | 598 | S529 | 2975 | 319.5 | 658 | S469 | 2015 | 319.5 | 718 | S409 | 1055 | 319.5 |
| 539 | S588 | 3919 | 202.5 | 599 | S528 | 2959 | 202.5 | 659 | S468 | 1999 | 202.5 | 719 | S408 | 1039 | 202.5 |
| 540 | S587 | 3903 | 319.5 | 600 | S527 | 2943 | 319.5 | 660 | S467 | 1983 | 319.5 | 720 | S407 | 1023 | 319.5 |

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| 722 | S405 | 991 | 319.5 |
| 723 | S404 | 975 | 202.5 |
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| 727 | S400 | 911 | 202.5 |
| 728 | S399 | 895 | 319.5 |
| 729 | S398 | 879 | 202.5 |
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| 735 | S392 | 783 | 202.5 |
| 736 | S391 | 767 | 319.5 |
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| 738 | S389 | 735 | 319.5 |
| 739 | S388 | 719 | 202.5 |
| 740 | S387 | 703 | 319.5 |
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| 743 | S384 | 655 | 202.5 |
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| 745 | S382 | 623 | 202.5 |
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| 750 | S377 | 543 | 319.5 |
| 751 | S376 | 527 | 202.5 |
| 752 | S375 | 511 | 319.5 |
| 753 | S374 | 495 | 202.5 |
| 754 | S373 | 479 | 319.5 |
| 755 | S372 | 463 | 202.5 |
| 756 | S371 | 447 | 319.5 |
| 757 | S370 | 431 | 202.5 |
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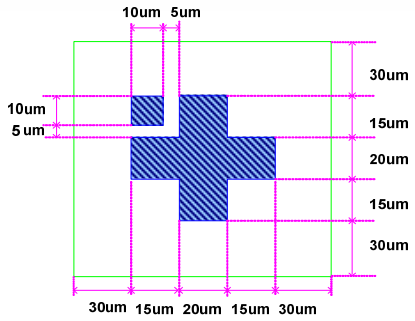
| 1268 | G275 | -8291 | 319.5 |
| 1269 | G277 | -8307 | 202.5 |
| 1270 | G279 | -8323 | 319.5 |
| 1271 | G281 | -8339 | 202.5 |
| 1272 | G283 | -8355 | 319.5 |
| 1273 | G285 | -8371 | 202.5 |
| 1274 | G287 | -8387 | 319.5 |
| 1275 | G289 | -8403 | 202.5 |
| 1276 | G291 | -8419 | 319.5 |
| 1277 | G293 | -8435 | 202.5 |
| 1278 | G295 | -8451 | 319.5 |
| 1279 | G297 | -8467 | 202.5 |
| 1280 | G299 | -8483 | 319.5 |
| 1281 | G301 | -8499 | 202.5 |
| 1282 | G303 | -8515 | 319.5 |
| 1283 | G305 | -8531 | 202.5 |
| 1284 | G307 | -8547 | 319.5 |
| 1285 | G309 | -8563 | 202.5 |
| 1286 | G311 | -8579 | 319.5 |
| 1287 | G313 | -8595 | 202.5 |
| 1288 | G315 | -8611 | 319.5 |
| 1289 | G317 | -8627 | 202.5 |
| 1290 | G319 | -8643 | 319.5 |
| 1291 | DUMMY27 | -8659 | 202.5 |

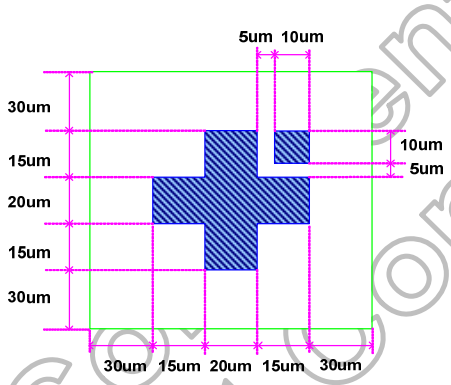
| Alignment mark | X | Y |
|---|---|---|
| A1 | -8751 | 269 |
| A2 | 8751 | 269 |

## 4.4 Alignment Mark

A_MARK (A1)

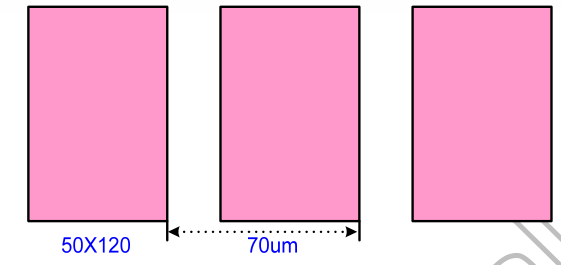



A_MARK (A2)

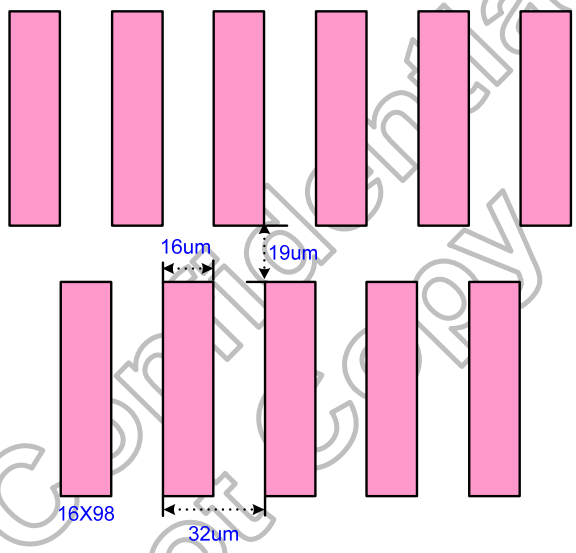


### 4.5 Bump Size

Input PAD




Output PAD



# 5. Function Description

## 5.1 Interface Control Mode

The HX8347-A01 supports three-type interface mode: Command-Parameter interface mode, Register-Content interface mode, and RGB interface mode

Command-Parameter interface mode or Register-Content interface mode is active by the external pins IFSEL0.

RGB interface mode is active by internal bit RGB_EN setting as shown in Table5.1. There are two-type chip access formats in HX8347-A01. One is register command for chip internal operation; the other is display data for chip display.

RGB_EN is stored in OTP for user application.

| IFSEL0 | RGB_EN | Register Data | Display Data |
|---|---|---|---|
| 0 | 0 | Command-parameter interface (Parallel interface) | From SRAM |
| 0 | 1 | Command-parameter interface (Serial interface) | Sleep out Normal Display On : From RGB interface<br>Sleep out Partial Mode On : From SRAM |
| 1 | 0 | Register-content interface (Parallel interface) | From SRAM |
| 1 | 1 | Register-content interface (Serial interface) | Normal display: From RGB interface<br>Partial Mode: From SRAM |

**Table 5. 1 Interface Mode Selection**

There are two-type register groups in HX8347-A01. One is accessed only via Command-Parameter interface. The other is accessed only via Register-Content interface.

This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8347-A(N) datasheet for detail.

### 5.1.1 Register-Content Interface Mode

The register-content interface circuit in HX8347-A01 supports 18-/16-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and serial bus system interface for serial data input. When NCS = “L”, the parallel and serial bus system interface of the HX8347-A01 become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS (2-0) setting. For selecting the input bus format, please refer to Table5.2 and Table5.3.

In Register-Content interface, it includes an Index Register (IR) to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

| P68 | Input Signal Format Selection |
|---|---|
| 0 | Format for I80 series MPU |
| 1 | Format for M68 series MPU |

**Table 5. 2 MPU Selection in Command-Parameter Interface Circuit**

| BS2 | BS1 | BS0 | Interface | Transferring Method of GRAM data | Transferring Method of Command |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 16-bit system interface | 16-bit 65K-color | 8-bit collective |
| 0 | 0 | 1 | 16-bit system interface | 18-bit 262K-color (16+2) | |
| 0 | 1 | 0 | 18-bit system interface | 18-bit 262K-color | |
| 0 | 1 | 1 | 8-bit system interface | 18-bit 262K-color (6+6+6) | |
| 1 | 0 | 0 | 16-bit system interface | 18-bit 262K-color (6+6+6) | |
| 1 | 0 | 1 | 18-bit system interface | 18-bit 262K-color | |
| 1 | 1 | ID | Serial interface | RGB_EN=0,Select by register 72h | |

**Table 5. 3 Interface Selection in Register-Content Interface Mode**

### 5.1.2 Parallel Bus System Interface

The input / output data from data pins (D17-0) and signal operation of the I80/M68 series parallel bus interface are listed in Table 5.4 and Table 5.5.

| Operations | E_NWR | RW_NRD | DNC_SCL |
|---|---|---|---|
| Writes Indexes into IR | 0 | 1 | 0 |
| Reads internal status | 1 | 0 | 0 |
| Writes command into register or data into GRAM | 0 | 1 | 1 |
| Reads command from register or data from GRAM | 1 | 0 | 1 |

**Table 5. 4 Data Pin Function for I80 Series CPU**

| Operations | E_NWR | RW_NRD | DNC_SCL |
|---|---|---|---|
| Writes Indexes into IR | 1 | 0 | 0 |
| Reads internal status | 1 | 1 | 0 |
| Writes command into register or data into GRAM | 1 | 0 | 1 |
| Reads command from register or data from GRAM | 1 | 1 | 1 |

**Table 5. 5 Data Pin Function for M68 Series CPU**

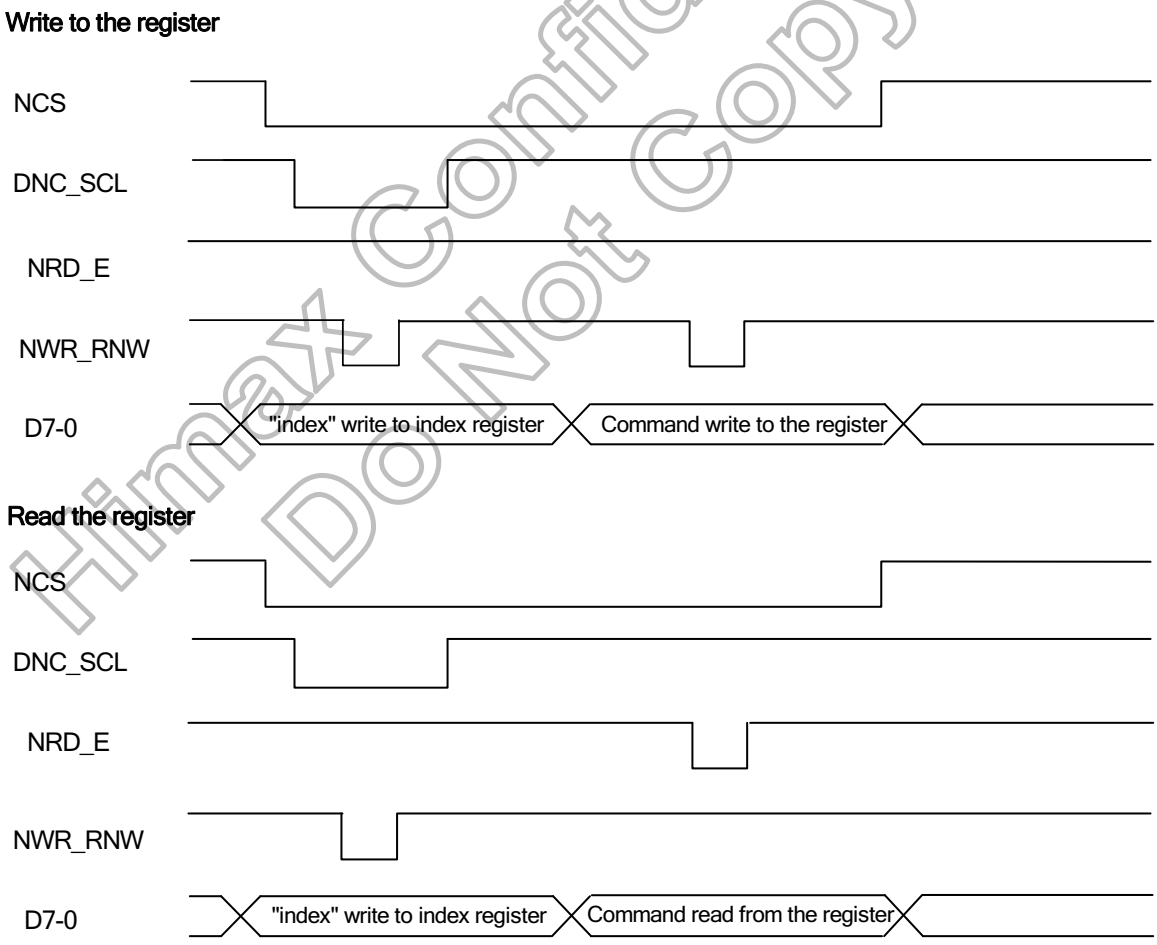



**Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)**

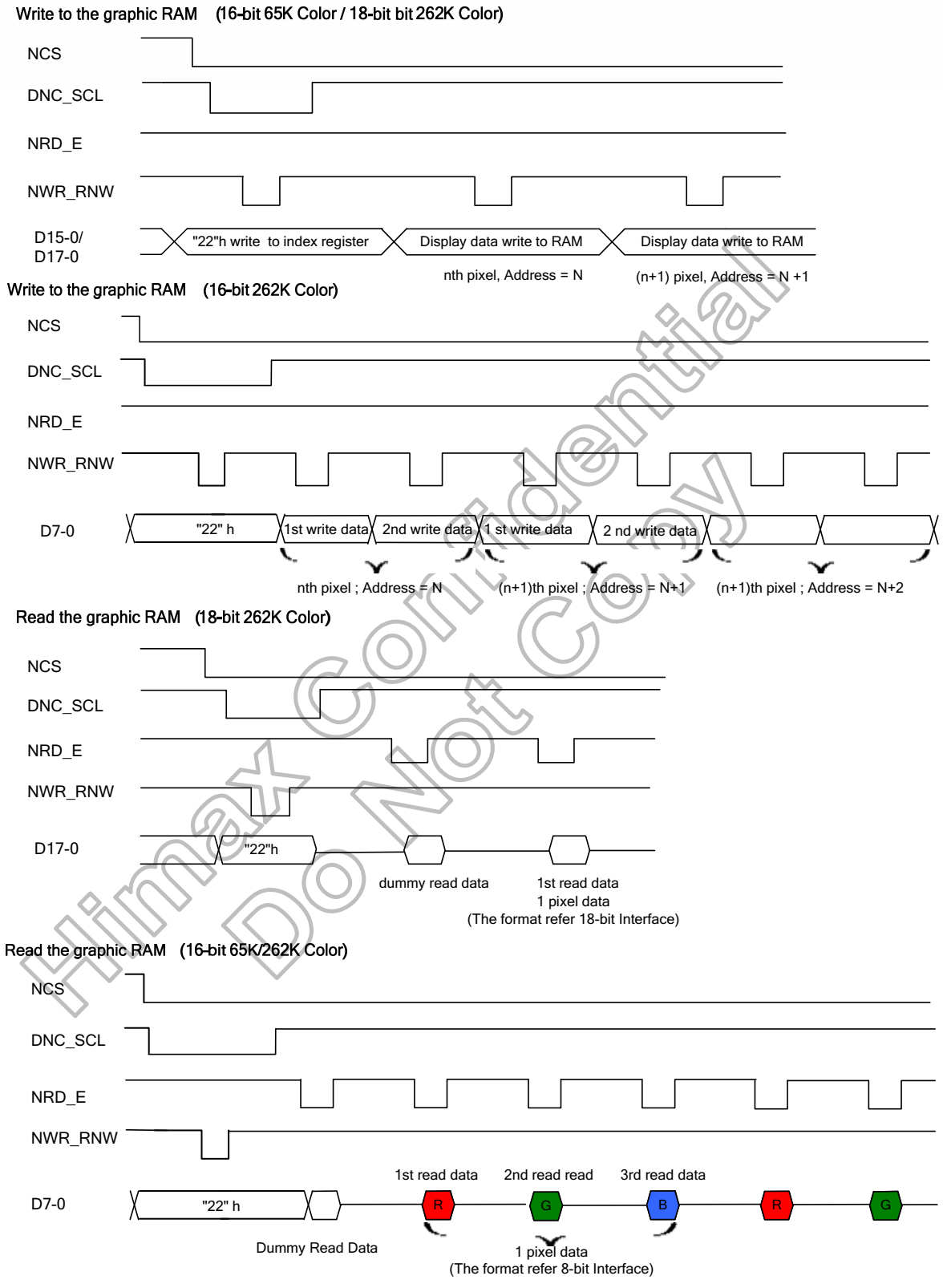
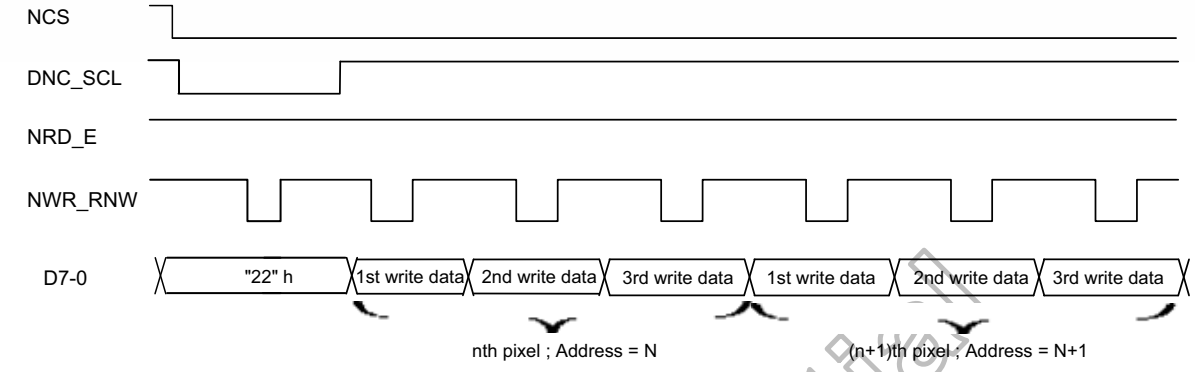



**Figure 5. 2 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for I80 Series MPU)**

**Write to the graphic RAM (8-bit 262K Color)**




**Read the graphic RAM (8-bit 262K Color)**

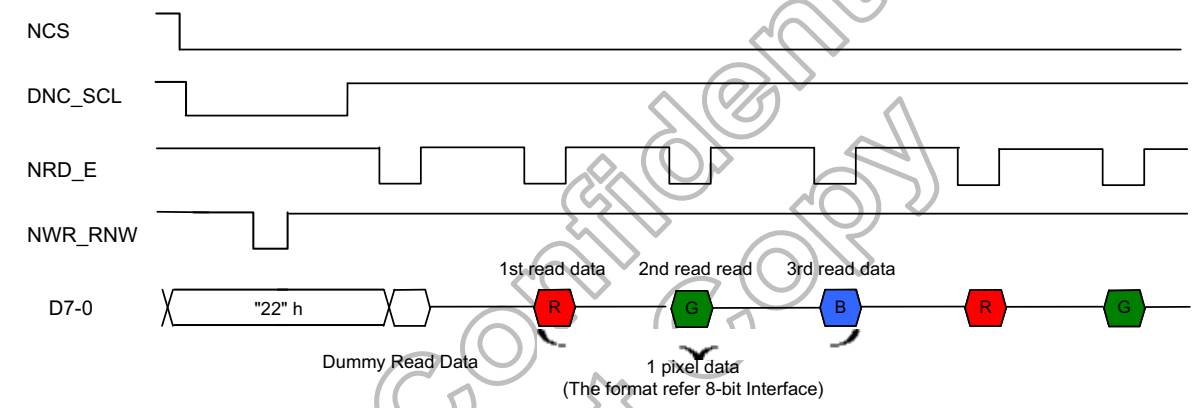



**Figure 5. 3 GRAM Read/Write Timing in 8-Bit Parallel Bus System Interface (for I80 Series MPU)**

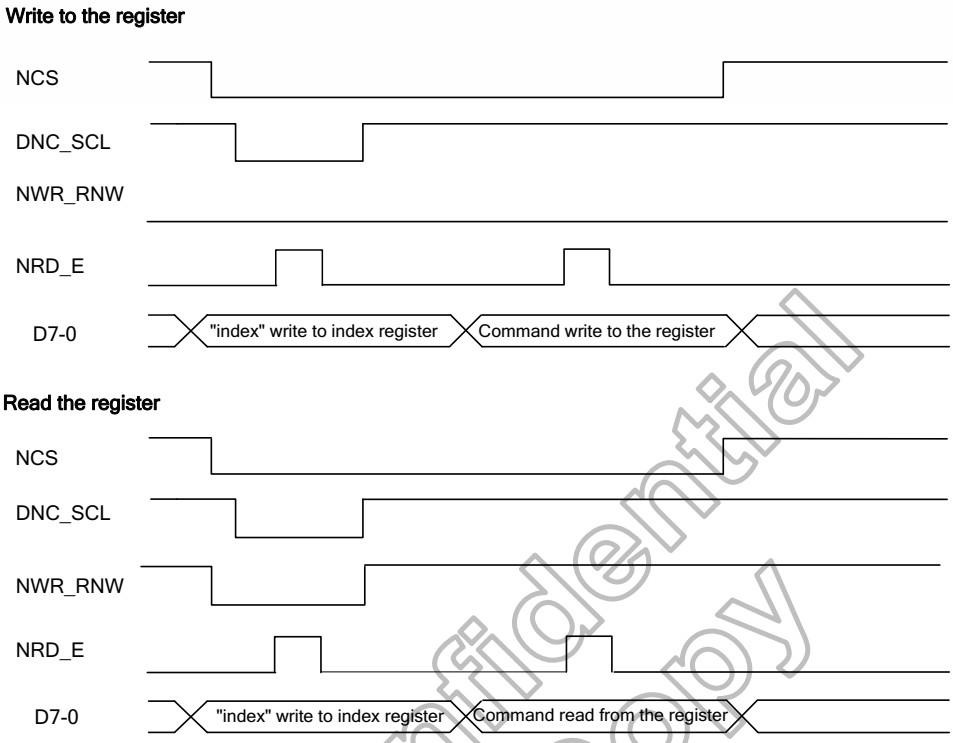
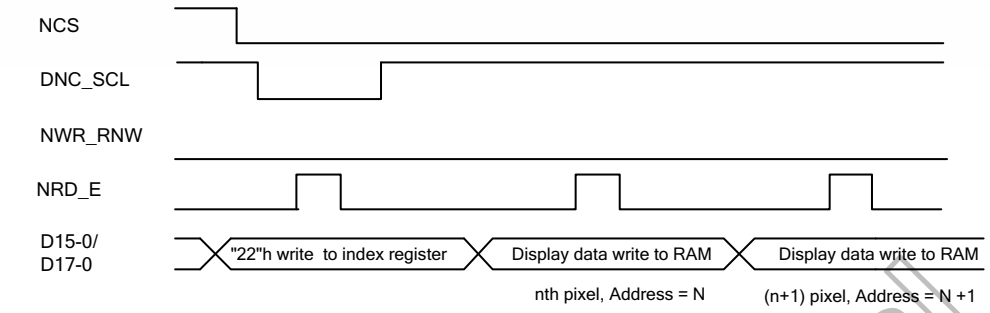
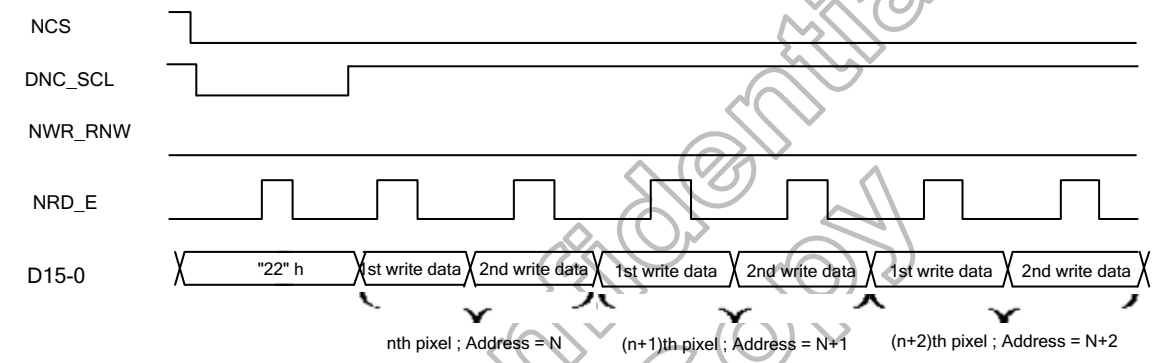



**Figure 5. 4 Register Read/Write Timing in Parallel Bus System Interface (for M68 Series MPU)**

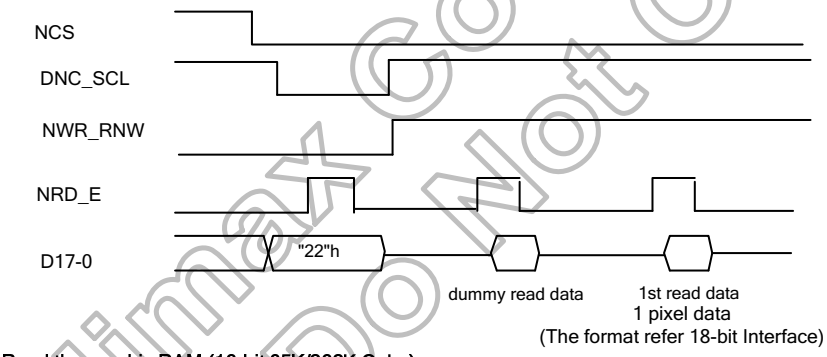
Write to the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)




Write to the graphic RAM (16+2-bit 262K Color)




Read the graphic RAM (18-bit bit 262K Color)




Read the graphic RAM (16-bit 65K/262K Color)

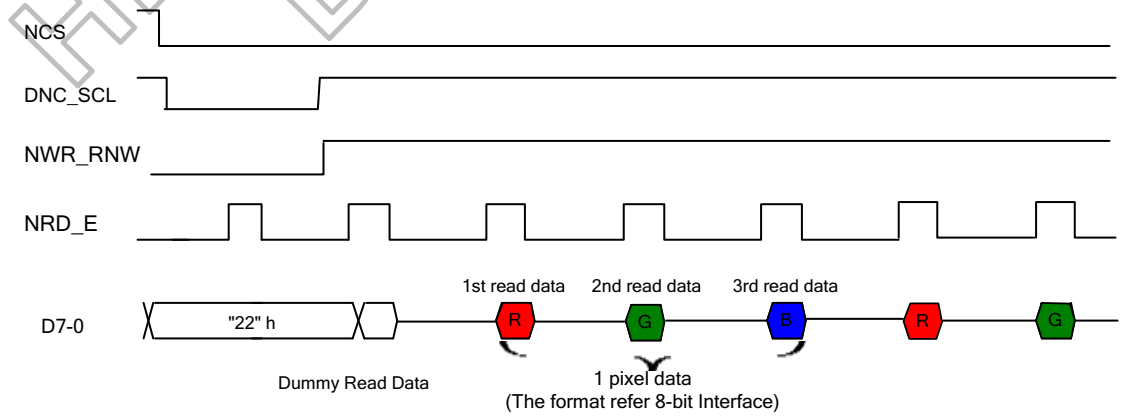
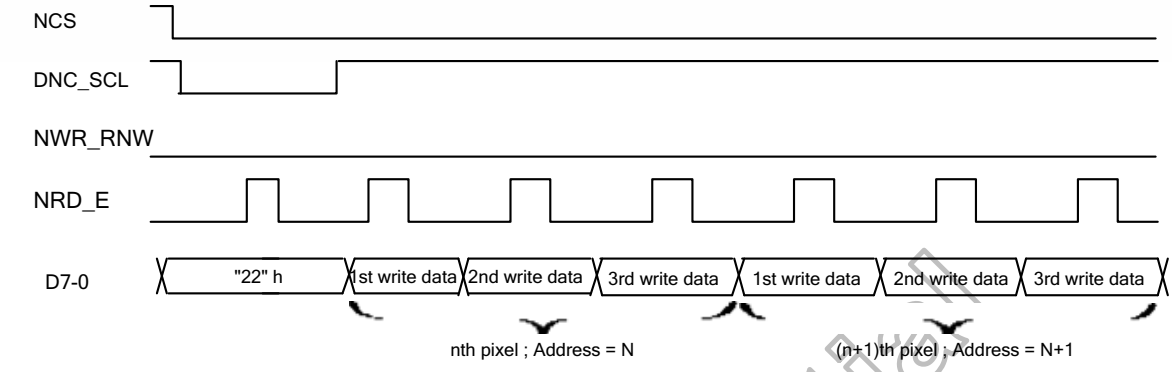



**Figure 5. 5 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for M68 Series MPU)**

Write to the graphic RAM (8-bit 262K Color)




Read the graphic RAM (8-bit 262K Color)

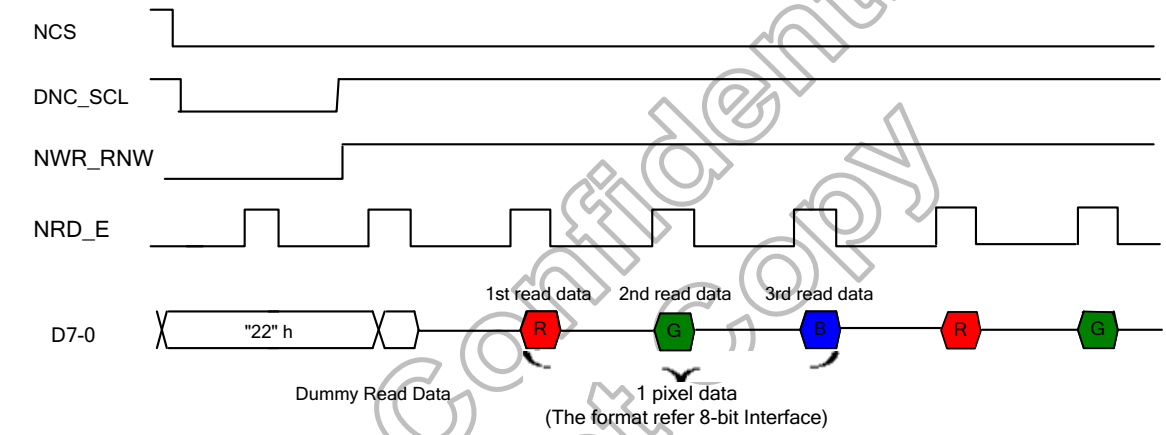



**Figure 5. 6 GRAM Read/Write Timing in 8-bit Parallel Bus System Interface (for M68 Series MPU)**

### 18-bit Parallel Bus System Interface

The I80-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0010” or “0101”. And the M68-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1010” or “1101”. Figure 5.7 is the example of interface with I80/M68 microcomputer system interface.

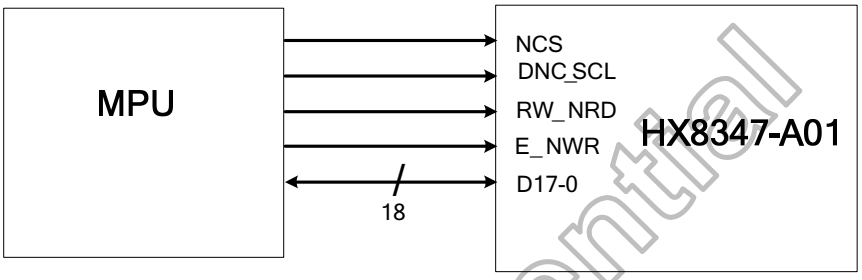



**Figure 5. 7 Example of I80- / M68- System 18-Bit Parallel Bus Interface**

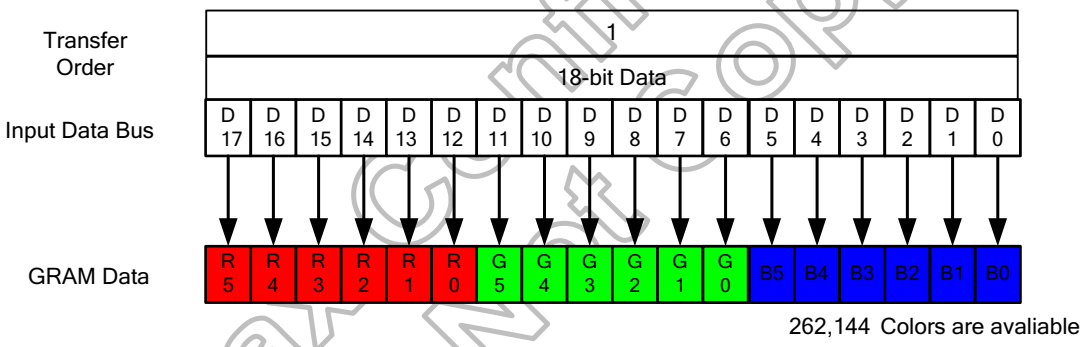



**Figure 5. 8 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface (“BS2, BS1, BS0”=”010” or ”101”)**

## 16-bit Parallel Bus System Interface

The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0000”, “0001”, “0100”. And the M68-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1000”, “1001”, “1100”. Figure 5.9 is the example of interface with I80/M68 microcomputer system interface.

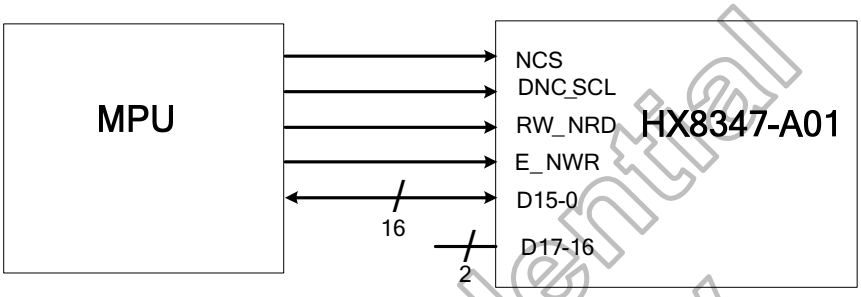



**Figure 5. 9 Example of I80- / M68- System 16-bit Parallel Bus Interface**

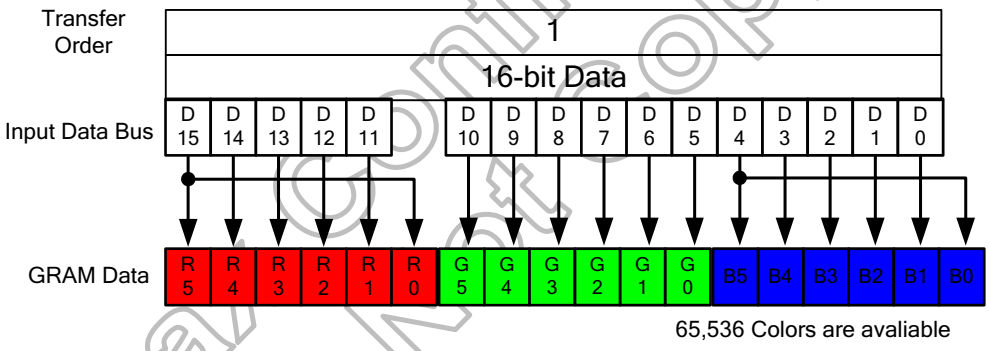



**Figure 5. 10 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (“BS2, BS1, BS0”=”000”)**

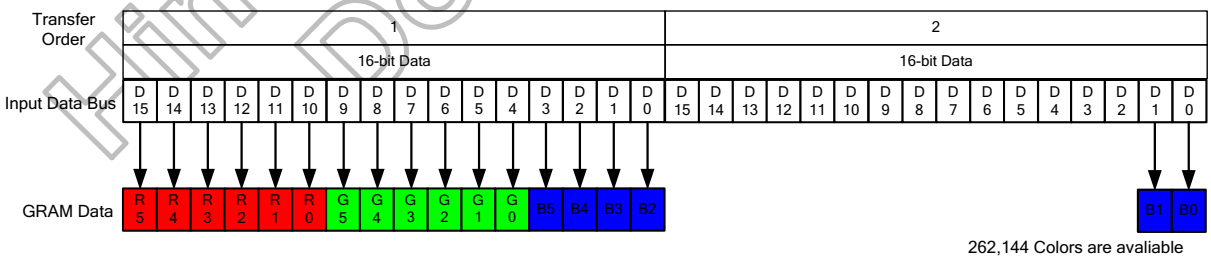



**Figure 5. 11 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (“BS2, BS1, BS0”=”001”)**

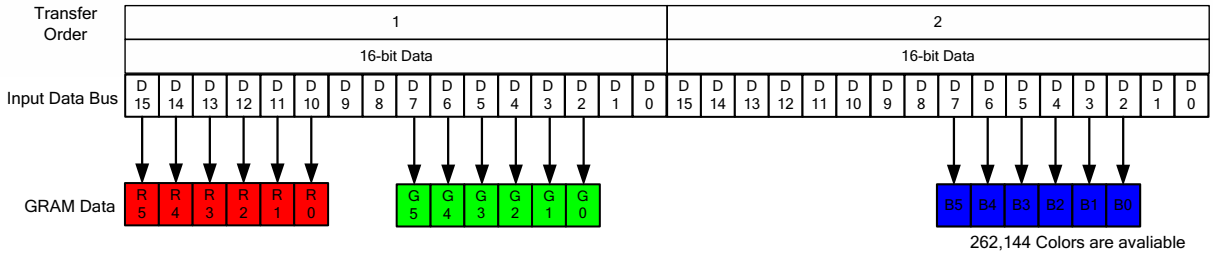



**Figure 5. 12 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(6+6+6) Bit-Data Input ("BS2, BS1, BS0"="100")**

## 8-bit Parallel Bus System Interface

The I80-system 8-bit parallel bus interface in register-content interface mode can be used by setting external pins "P68, BS2, BS1, BS0" pins to "0011". And the M68-system 8-bit parallel bus interface in command-parameter interface mode can be used by setting "P68, BS2, BS1, BS0" pins to "1011". Figure 5.13 is the example of interface with I80/M68 microcomputer system interface.

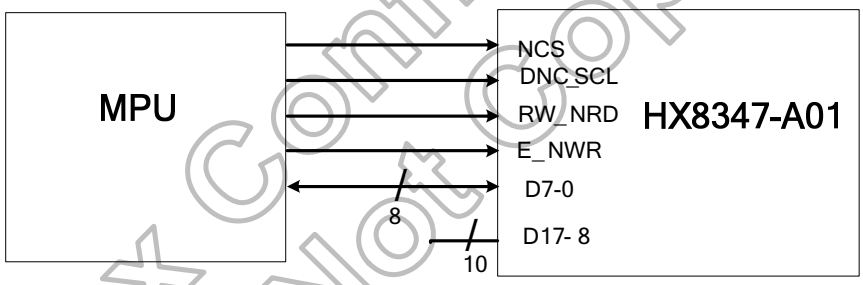



**Figure 5. 13 Example of I80- / M68- System 8-Bit Parallel Bus Interface**

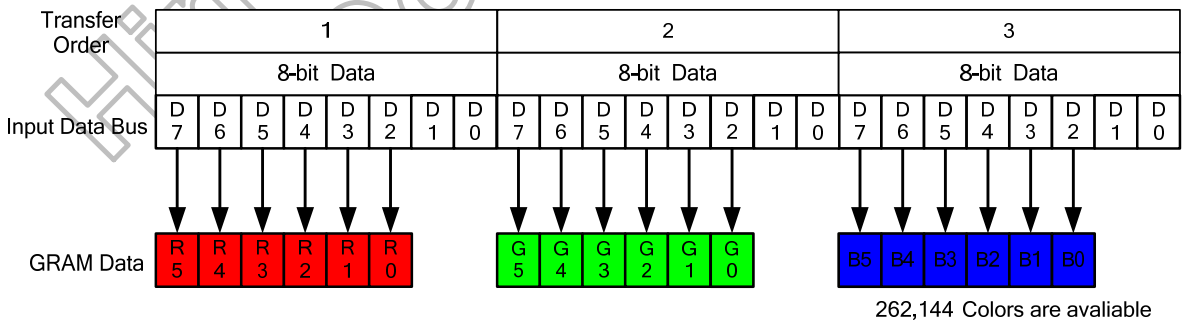



**Figure 5. 14 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18( 6 + 6 + 6 ) Bit-Data Input ("BS2, BS1, BS0"="011")**

### 5.1.3 Serial Bus System Interface

The HX8347-A01 supports the serial bus interface in register-content mode by setting external pins “BS2, BS1” pins to “11”. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), serial output data (SDO) and the serial transfer clock signal (DNC_SCL).

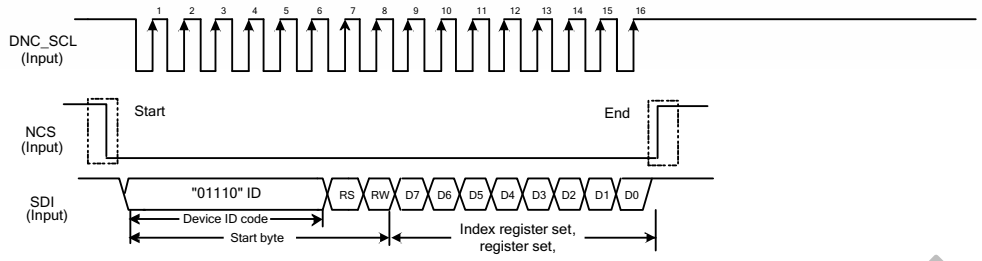
As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code, register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status, and it must be set to “1” when writing or reading an command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

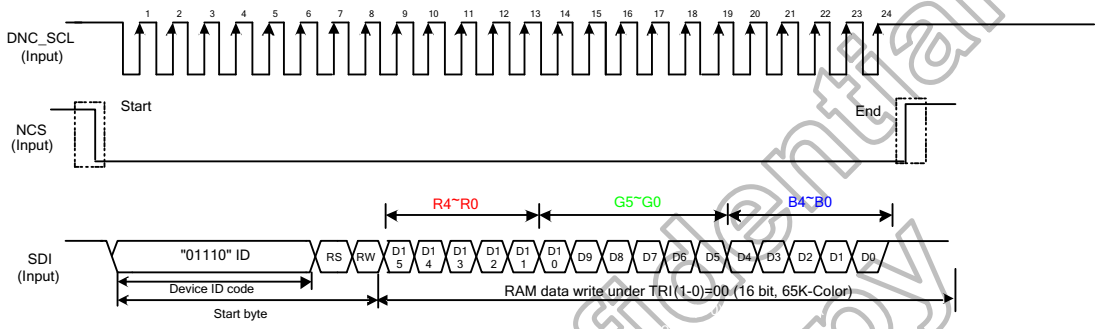
| RS | R/W | Function |
|---|---|---|
| 0 | 0 | Writes Indexes into IR |
| 1 | 0 | Writes command into register or data into GRAM |
| 1 | 1 | Reads command from register or data from GRAM |

**Table 5. 6 The Function of RS and R/W Bit bus**

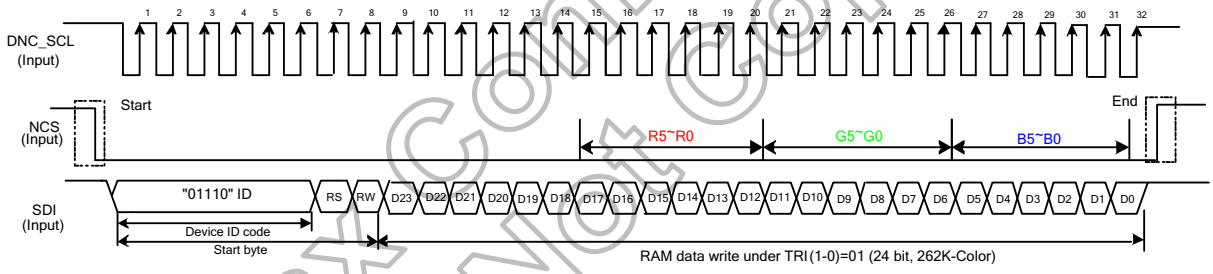
A)TransferTiming Format in Serial Bus Interface for Index Register or Register Wirte




B) TransferTiming Format in Serial Bus Interface for GRAM write (index = "22h") , TRI(1-0) = 00




C) TransferTiming Format in Serial Bus Interface for GRAM Write (index = "22"h) , TRI(1-0) = 01




D) TransferTiming Format in Serial Bus Interface for GRAM Write (index = "22"h) , TRI(1-0) = 1x

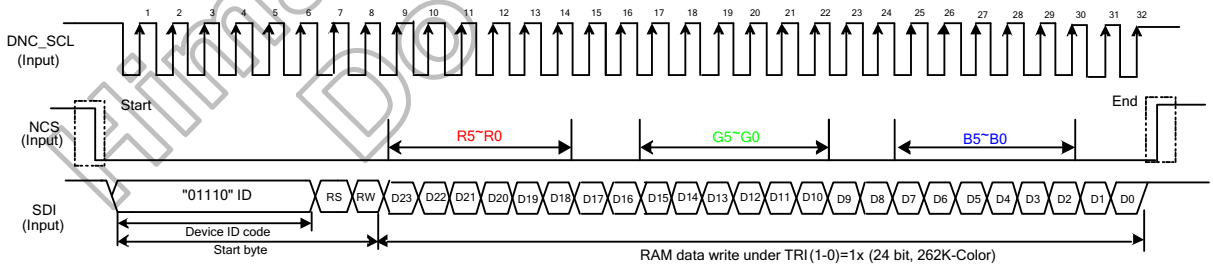



**Figure 5. 15 Data Write Timing in Serial Bus System Interface**

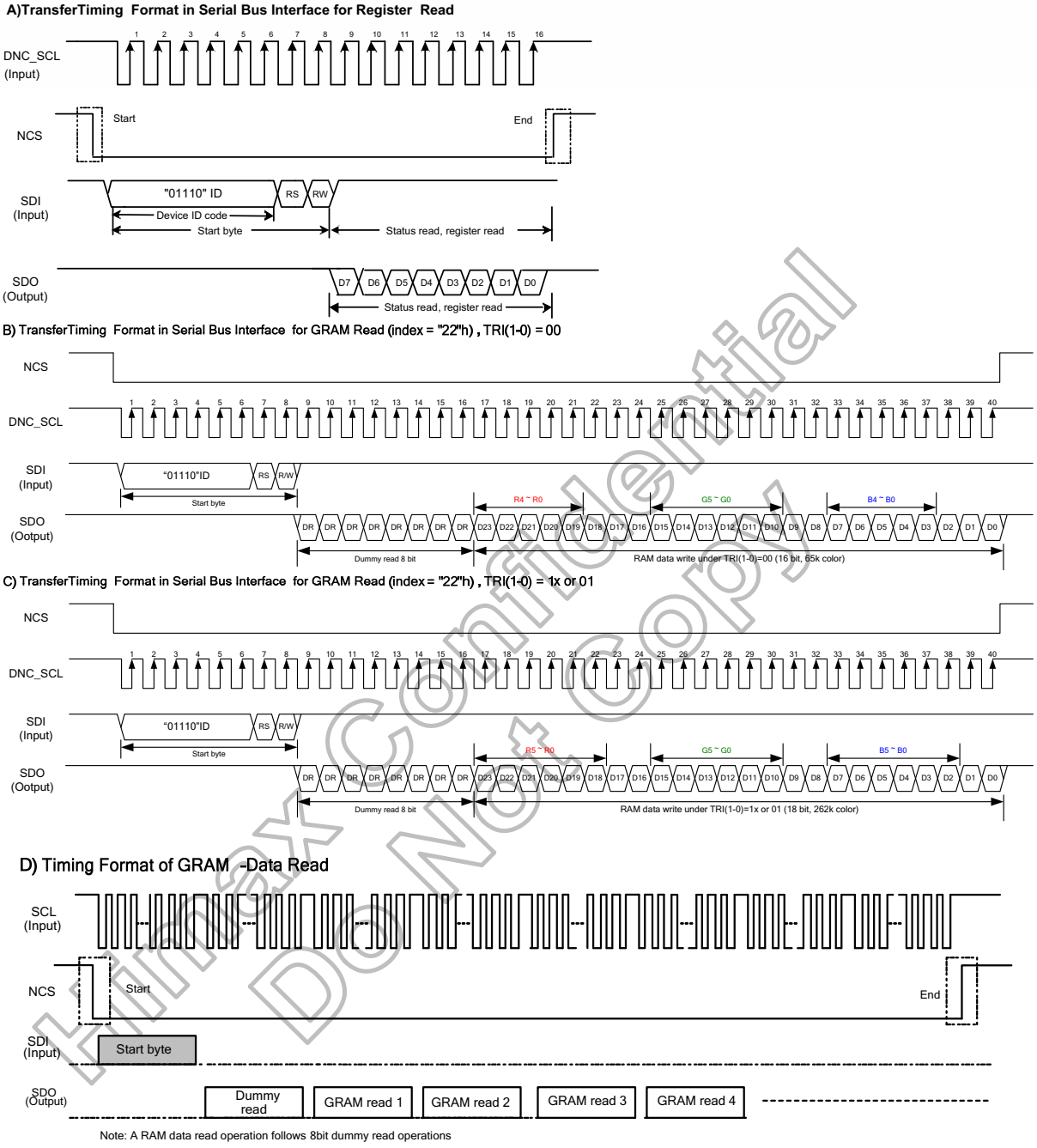



**Figure 5. 16 Data Read Timing in Serial Bus System Interface**

### 5.1.4 RGB Interface

The HX8347-A01 supports the RGB interface for writing animated display data. The RGB interface can be selected by setting internal RGB_EN bit = 1. In RGB interface, the display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK), and the display data is inputted via RGB interface circuit without being written to the GRAM and display directly. The display data are transferred in pixel unit via D17-0 input pins. The display data input is latched on the rising edge of DOTCLK (DPL bit = 0) or the falling edge of DOTCLK (DPL bit = 1) by the chip when ENABLE signal is valid. Please refer to Table 5.7.

| EPL | ENABLE | Display Data to Panel |
|---|---|---|
| 0 | 0 | Disable |
| 0 | 1 | Enable |
| 1 | 0 | Enable |
| 1 | 1 | Disable |

**Table 5. 7 EPL Bit Setting and Valid Enable Signal**

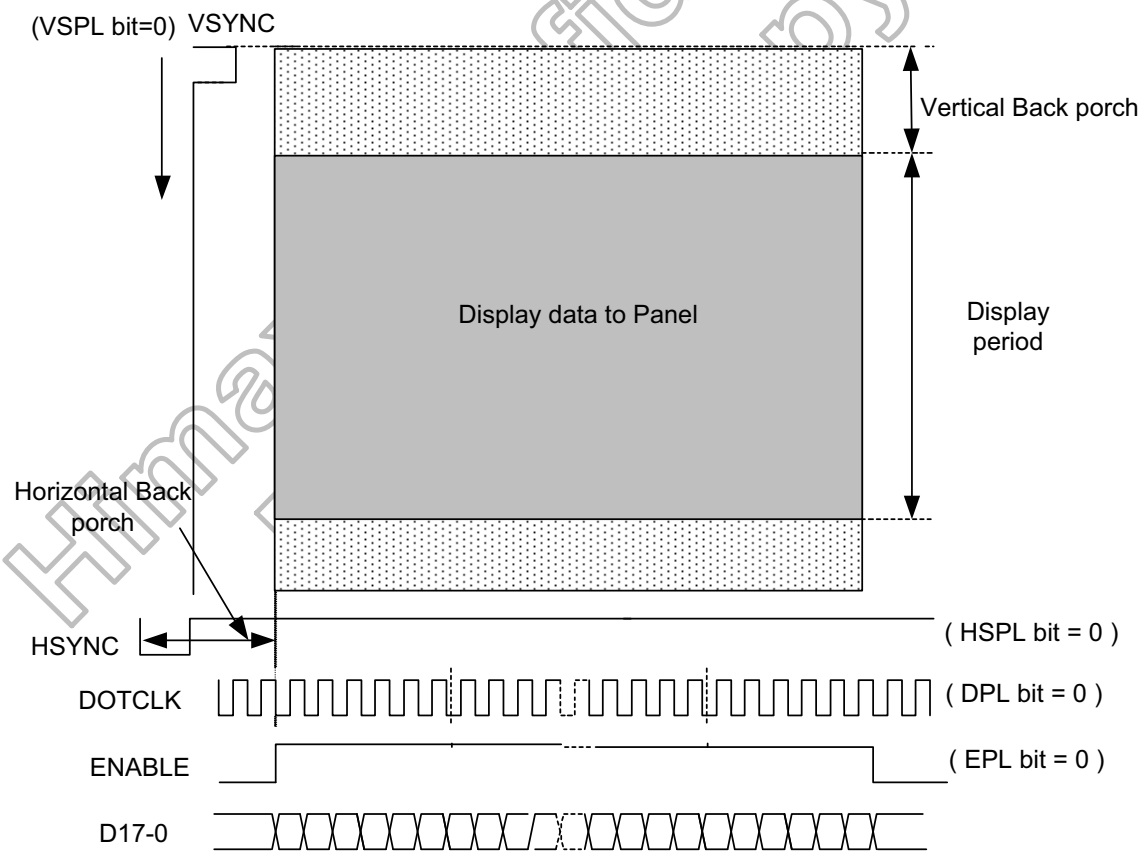



**Figure 5. 17 RGB Interface Circuit Input Timing**

There are two types bit format per pixel color order for writing GRAM data in 18-bit bus interface selected by internal bits CSEL(2-0). The setting is shown in Figure5. 18 and Figure 5. 19.

**(1) 16 bit/pixel color order (R 5-bit, G 6-bit, B 5-bit), 65,536 colors (CSEL(2-0) = "101")**

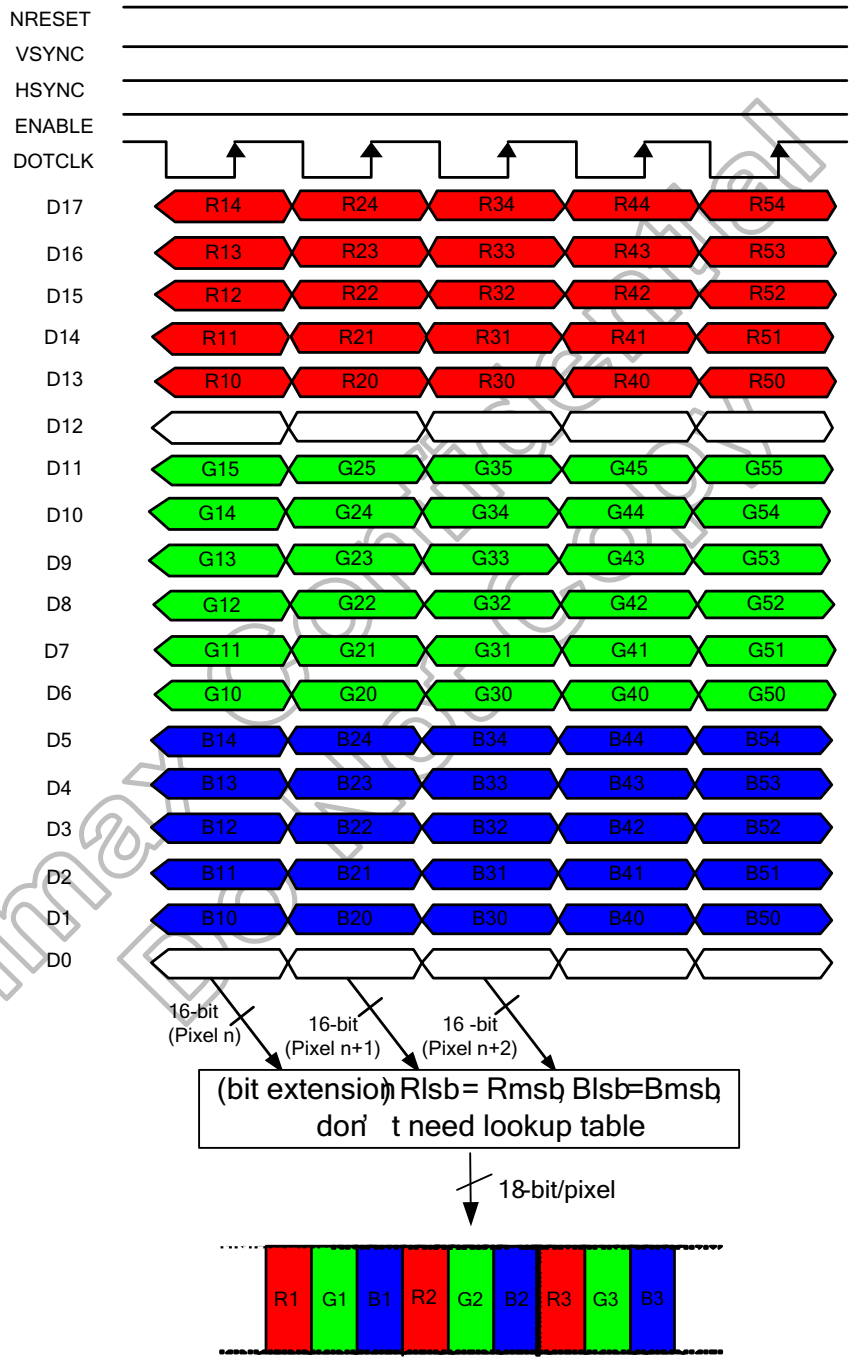



**Figure 5. 18 16-Bit / Pixel Data Input of RGB Interface**

**(2) 18 bit/pixel color order (R 6-bit, G 6-bit, B 6-bit), 262,144 colors (CSEL(2-0) = "110")**

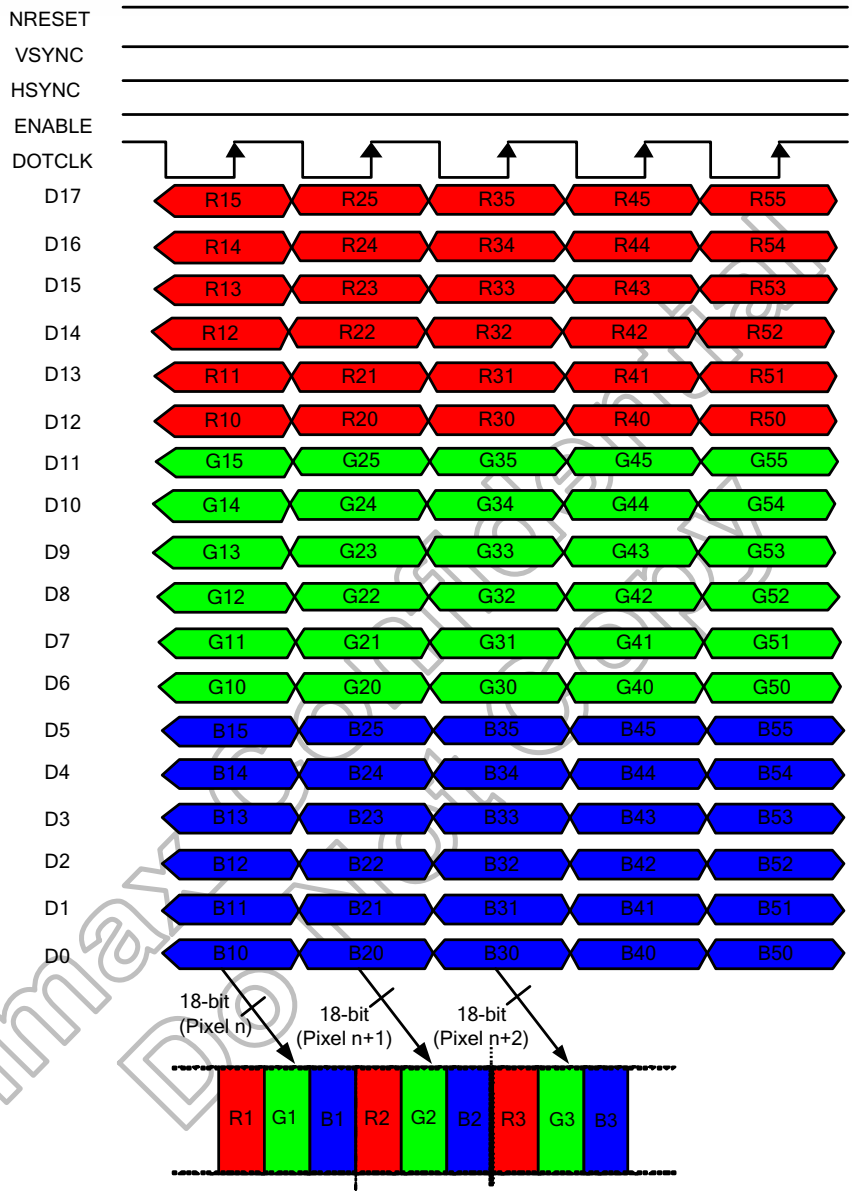



**Figure 5. 19 18-Bit / Pixel Data Input of RGB Interface**

### 5.2 Address Counter (AC)

The HX8347-A01 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range X=0~239d and Y=0~319d.

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: SC, end: EC) or the vertical address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

### 5.2.1 MCU to Memory Write/Read Direction

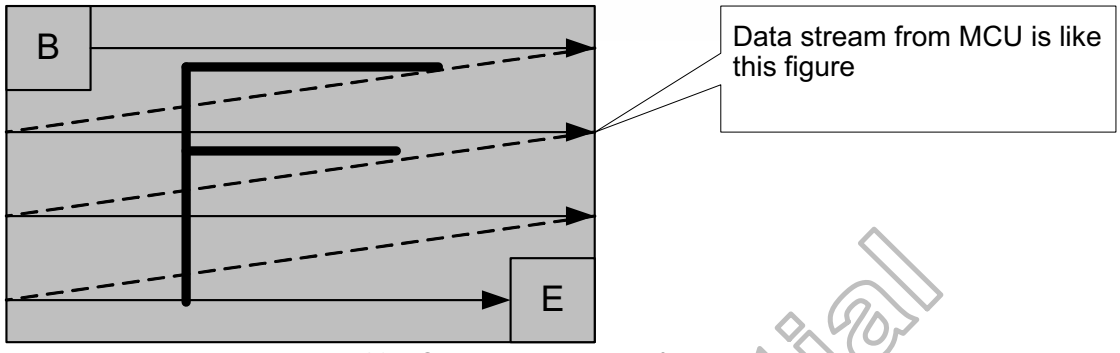



**Figure 5. 20 MCU to Memory Write/Read Direction**

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

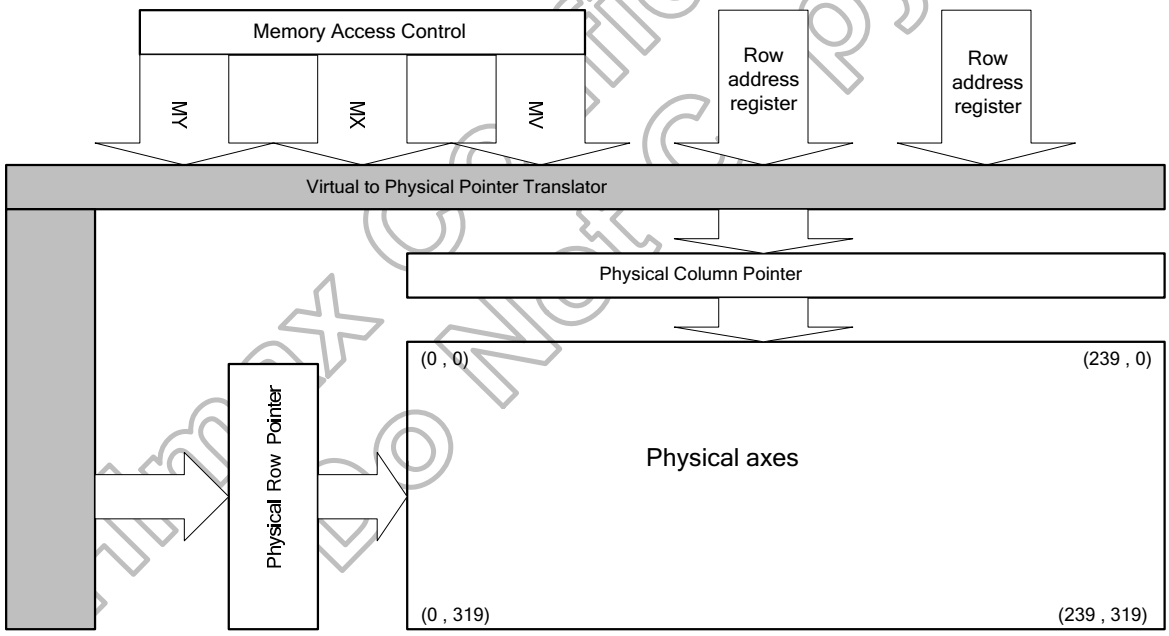



**Figure 5. 21 MY, MX, MV Setting**

| MY | MX | MV | CASET | PASET |
|---|---|---|---|---|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Page Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (319-Physical Page Pointer) |
| 0 | 1 | 0 | Direct to (239-Physical Column Pointer) | Direct to Physical Page Pointer |
| 0 | 1 | 1 | Direct to (239-Physical Column Pointer) | Direct to (319-Physical Page Pointer) |
| 1 | 0 | 0 | Direct to Physical Page Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (319-Physical Page Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Page Pointer | Direct to (239-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (319-Physical Page Pointer) | Direct to (239-Physical Column Pointer) |

**Table 5. 8 MY, MX, MV Setting**

The following figure depicts the update method set by MV, MX and MY bit.

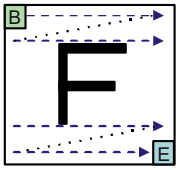
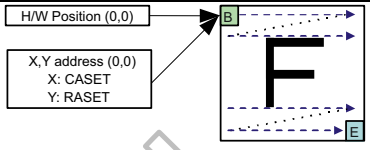
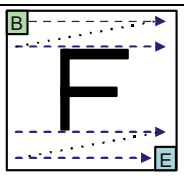
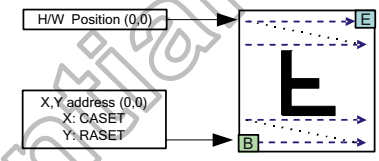
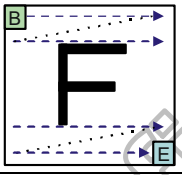
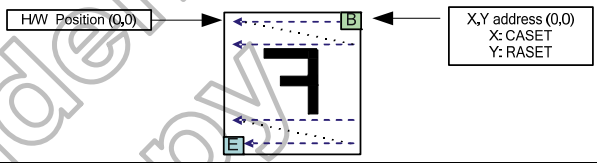
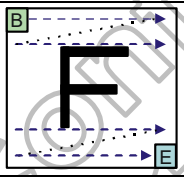
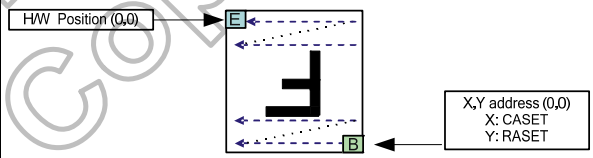
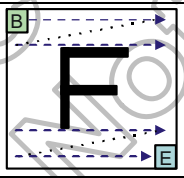
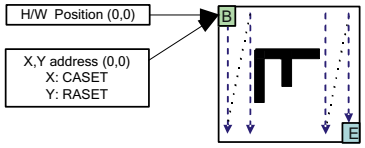
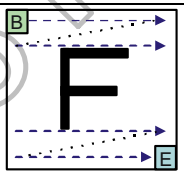
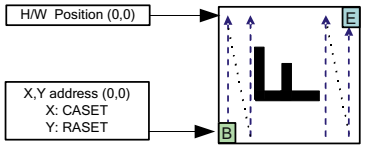
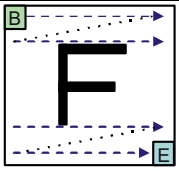
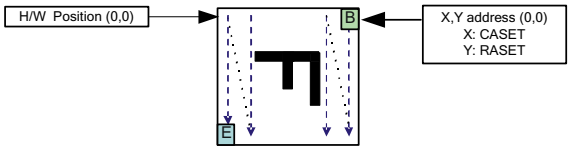
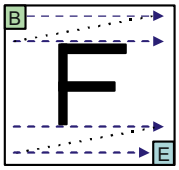
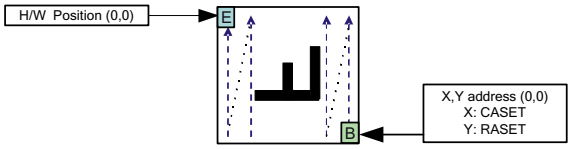
| Display Data Direction | MADCTR parameter | | | Image in the Host | Image in the Driver (GRAM) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 |  |  |
| X-Y Exchange X-Mirror | 1 | 1 | 0 |  |  |
| X-Y Exchange X-Mirror Y-Mirror | 1 | 1 | 1 |  |  |



**Figure 5. 22 Address Direction Settings**

## 5.3 Source, Gate and Memory Map


| Source Out | | S1 | S2 | S3 | S4 | S5 | S6 | ---------- | S715 | S716 | S717 | S718 | S719 | S720 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA | | | | | | | | RGB Order —— :BGR=0 ----- :BGR=1 | | | | | | |
| MY=0 | MY=1 | | | | | | | | | | | | | |
| 0 | 319 | $R0_{5-0}$ | $G0_{5-0}$ | $B0_{5-0}$ | $R1_{5-0}$ | $G1_{5-0}$ | $B1_{5-0}$ | – | $R238_{5-0}$ | $G238_{5-0}$ | $B238_{5-0}$ | $R239_{5-0}$ | $G239_{5-0}$ | $B239_{5-0}$ |
| 1 | 318 | | | | | | | – | | | | | | |
| 2 | 317 | | | | | | | – | | | | | | |
| 3 | 316 | | | | | | | – | | | | | | |
| 4 | 315 | | | | | | | – | | | | | | |
| 5 | 314 | | | | | | | – | | | | | | |
| 6 | 313 | | | | | | | – | | | | | | |
| 7 | 312 | | | | | | | – | | | | | | |
| 8 | 311 | | | | | | | – | | | | | | |
| 9 | 310 | | | | | | | – | | | | | | |
| 10 | 309 | | | | | | | – | | | | | | |
| 11 | 308 | | | | | | | – | | | | | | |
| : | : | : | : | : | : | : | : | -- | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | | : | : | : | : | : | : |
| 312 | 7 | | | | | | | – | | | | | | |
| 313 | 6 | | | | | | | – | | | | | | |
| 314 | 5 | | | | | | | – | | | | | | |
| 315 | 4 | | | | | | | – | | | | | | |
| 316 | 3 | | | | | | | – | | | | | | |
| 317 | 2 | | | | | | | – | | | | | | |
| 318 | 1 | | | | | | | – | | | | | | |
| 319 | 0 | | | | | | | – | | | | $RN_{7-0}$ | $GN_{7-0}$ | $BN_{7-0}$ |
| CA | MX=0 | 0 | | | 1 | | | | 238 | | | 239 | | |
| | MX=1 | 239 | | | 238 | | | | 1 | | | 0 | | |



**Figure 5. 23 Memory Map (240RGBx320)**

**Note:** RA = Row Address,
CA = Column Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control command
BGR= Red, Green and Blue pixel position change, D3 parameter of Memory Access Control command

### 5.4 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

#### 5.4.1 Tearing Effect Line Modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:

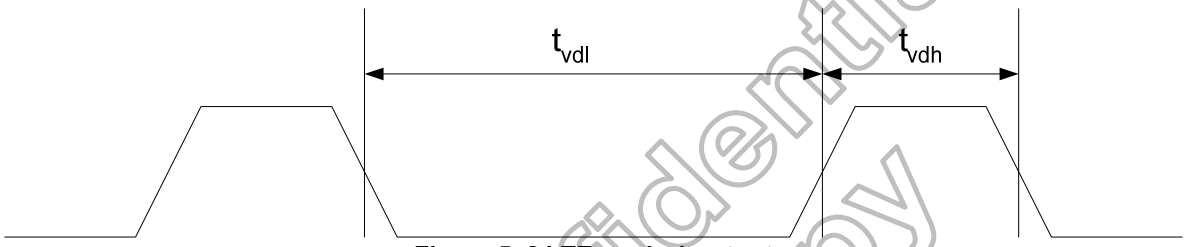



**Figure 5. 24 TE mode 1 output**

**$t_{vdh}$** = The LCD display is not updated from the Frame Memory
**$t_{vdl}$** = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.

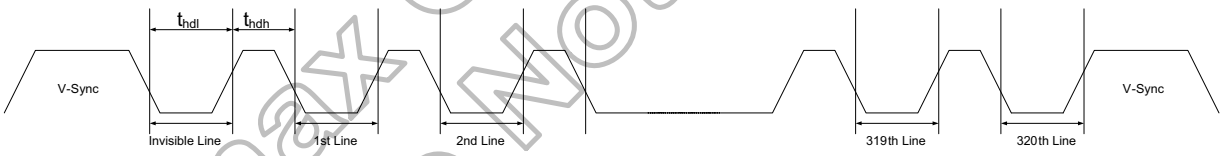



**Figure 5. 25 TE mode 2 output**

**$t_{hdh}$**= The LCD display is not updated from the Frame Memory
**$t_{hdl}$**= The LCD display is updated from the Frame Memory (except Invisible Line – see above)


**Figure 5. 26 TE output waveform**

**Note:** During Sleep In Mode, the Tearing Output Pin is active Low

### 5.4.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.

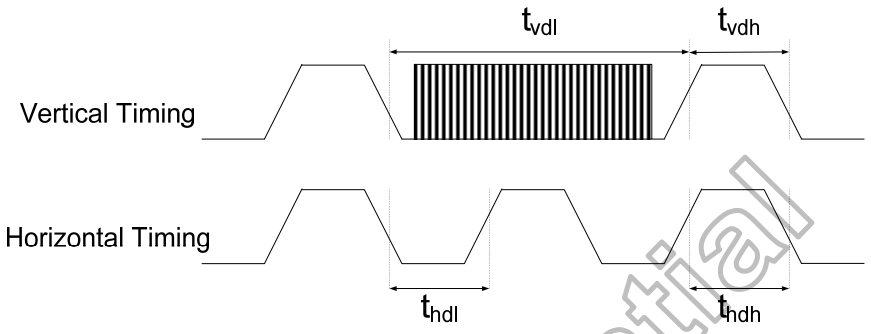



**Figure 5. 27 Waveform of Tearing Effect Signal**

Idle Mode Off (Frame Rate = TBD Hz)

| Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|
| tvdl | Vertical Timing Low Duration | TBD | - | ms | - |
| tvdh | Vertical Timing High Duration | BP+FP(1) | - | us | - |
| thdl | Horizontal Timing Low Duration | TBD | - | us | - |
| thdh | Horizontal Timing High Duration | TBD | 500 | us | - |

Note: (1) BP = Back porch, FP = Font porch.

**Table 5. 9 AC characteristics of Tearing Effect Signal**

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

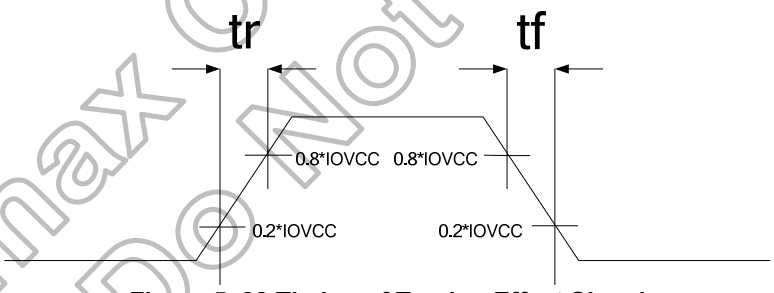



**Figure 5. 28 Timing of Tearing Effect Signal**

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

### 5.4.3 Example 1: MPU Write is faster than Panel Read

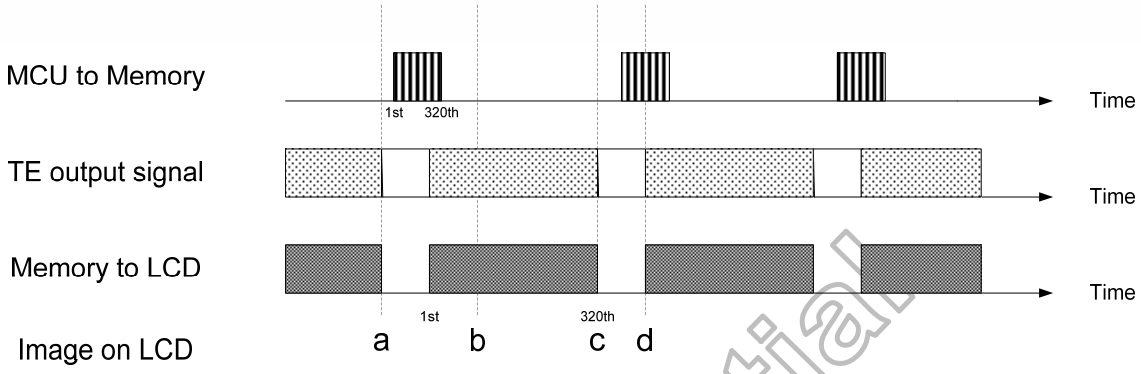



**Figure 5. 29**

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

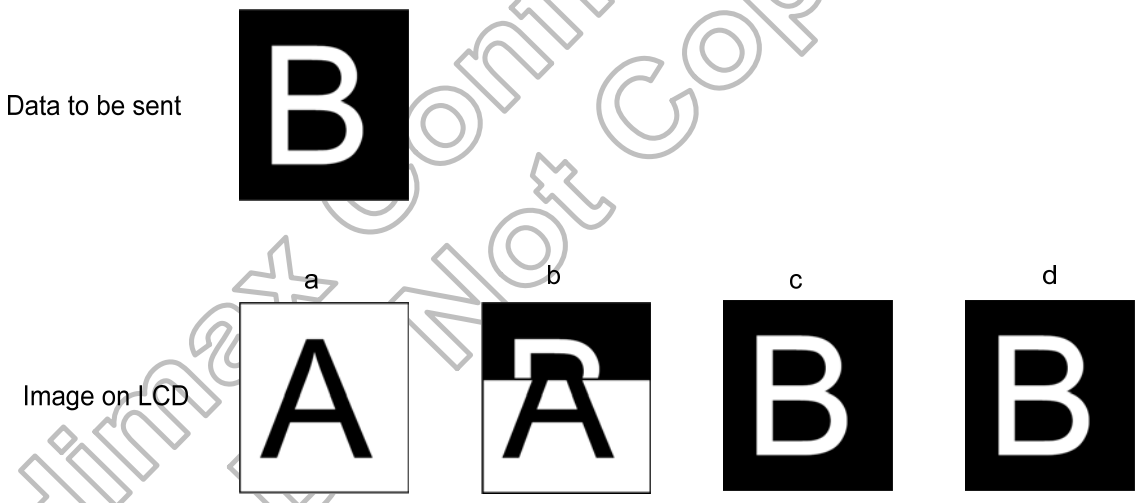



**Figure 5. 30**

### 5.4.4 Example 2: MPU Write is slower than Panel Read

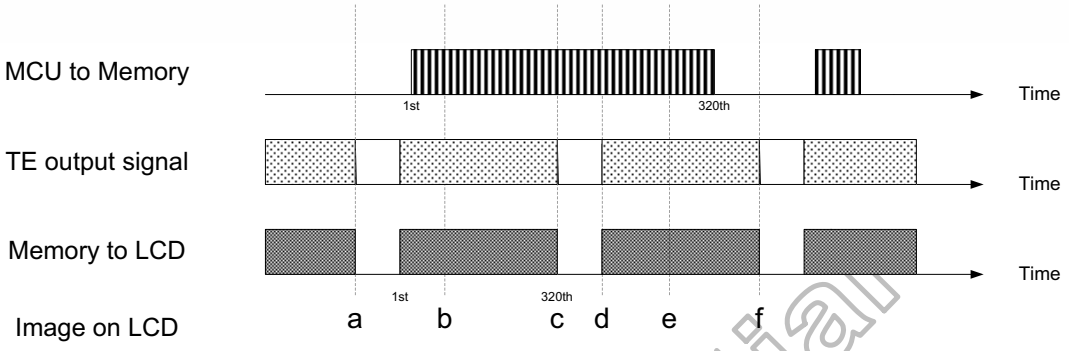



**Figure 5. 31**

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

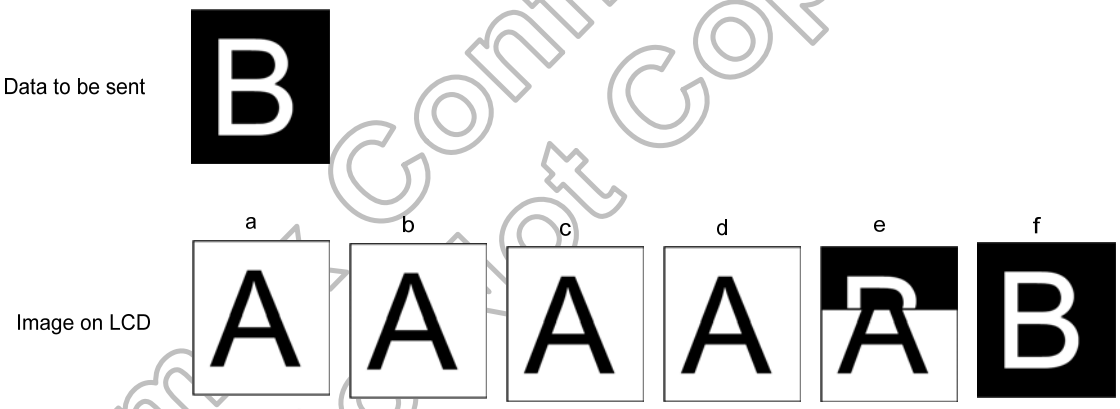



**Figure 5. 32**

### 5.5 Oscillator

The HX8347-A01 has an internal oscillator without extra external components that provide a source for system clock generator. The default frequency is 5.5MHz.

### 5.6 Source Driver

The HX8347-A01 contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

### 5.7 Gate Driver

The HX8347-A01 contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

## 5.8 LCD Power Generation Circuit

### 5.8.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

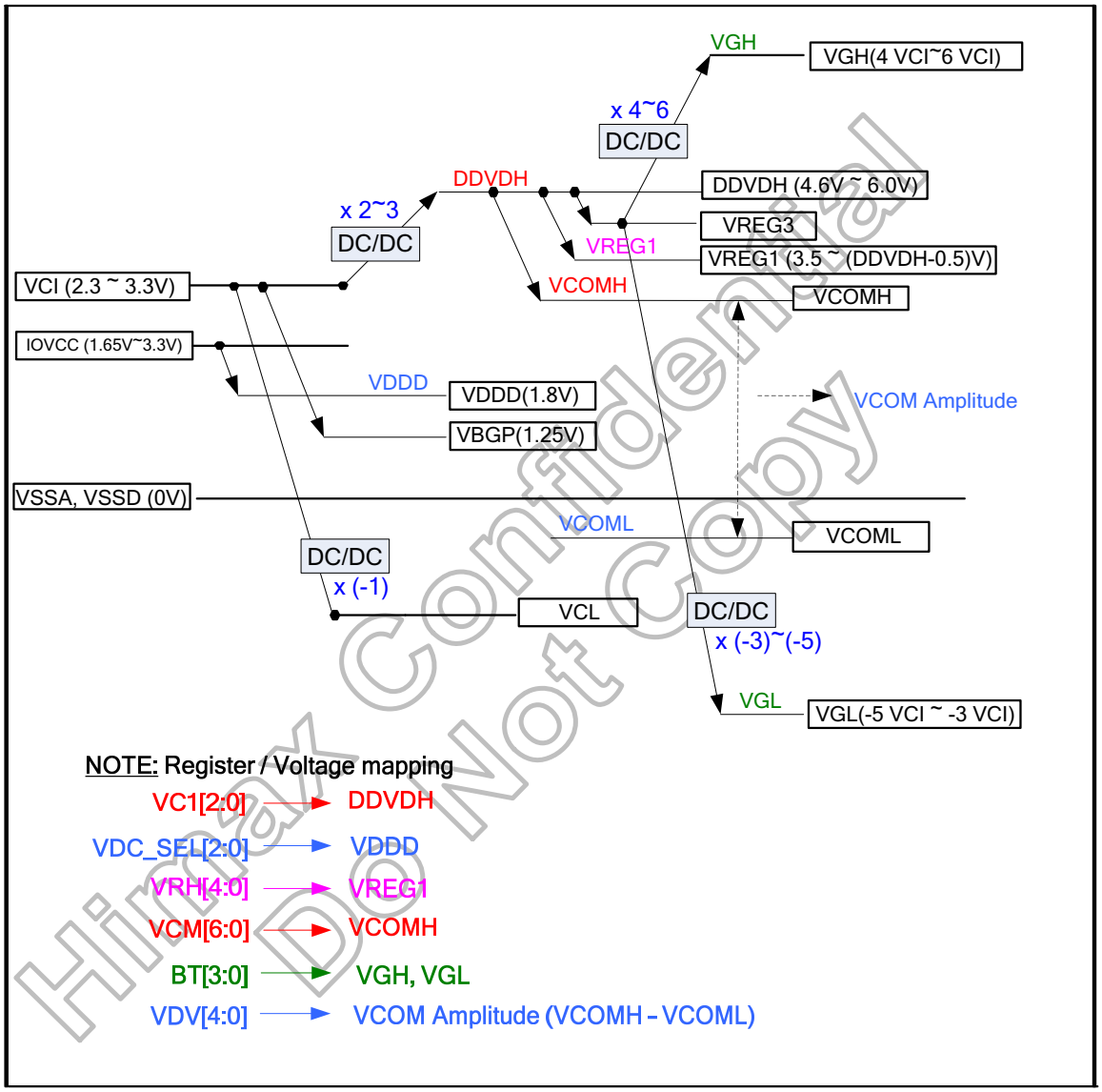



**Figure 5. 33 LCD Power Generation Scheme**

### 5.8.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

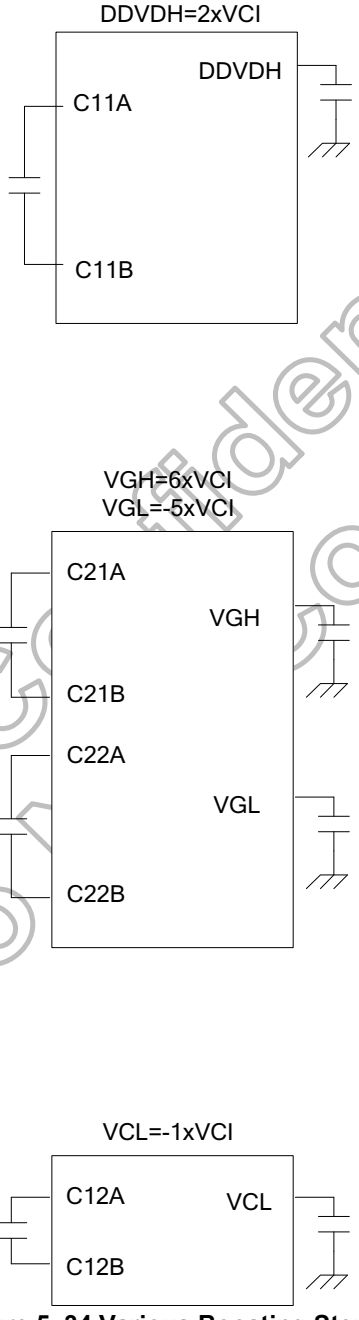



**Figure 5. 34 Various Boosting Steps**

## 5.9 Gray Voltage Generator for Source Driver

The HX8347-A01 incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

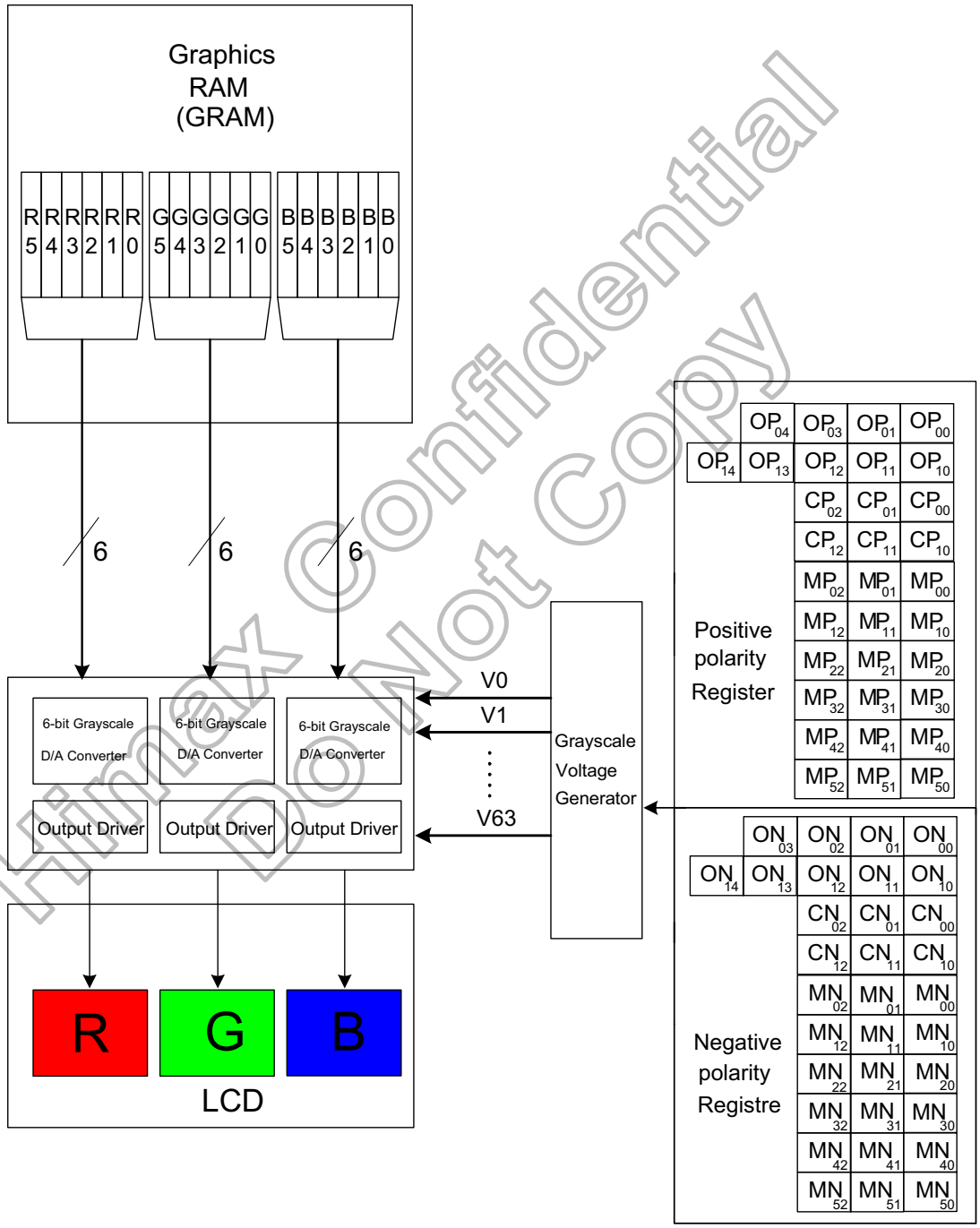



**Figure 5. 35 Grayscale Control**

### 5.9.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel.

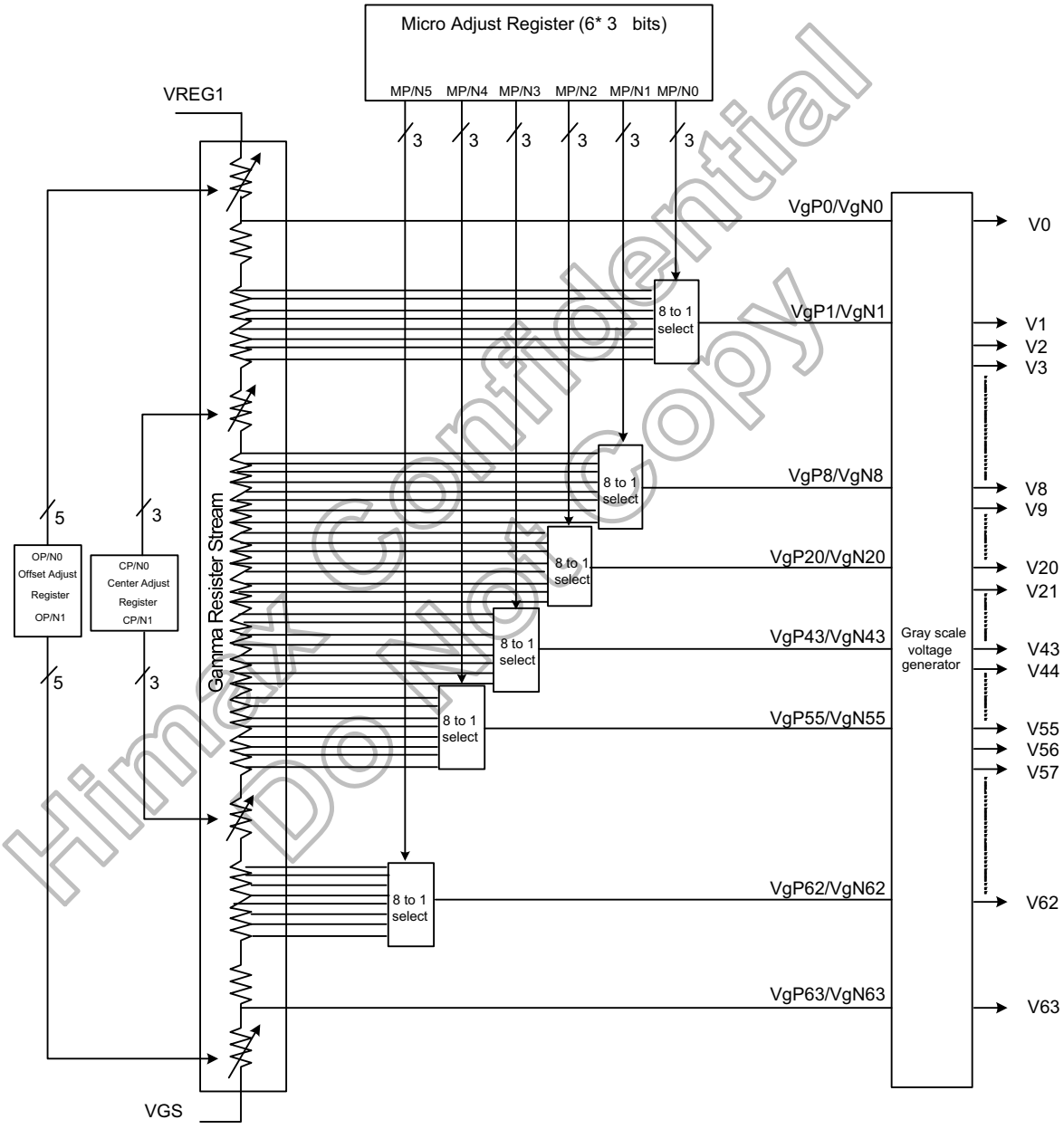



**Figure 5. 36 Structure of Grayscale Voltage Generator**

### 5.9.2 Gamma-Characteristics Adjustment Register

This HX8347-A01 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

#### 5.9.2.1 Offset Adjustment Registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

#### 5.9.2.2 Gamma Center Adjustment Registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

### 5.9.3 Gamma Macro Adjustment Registers

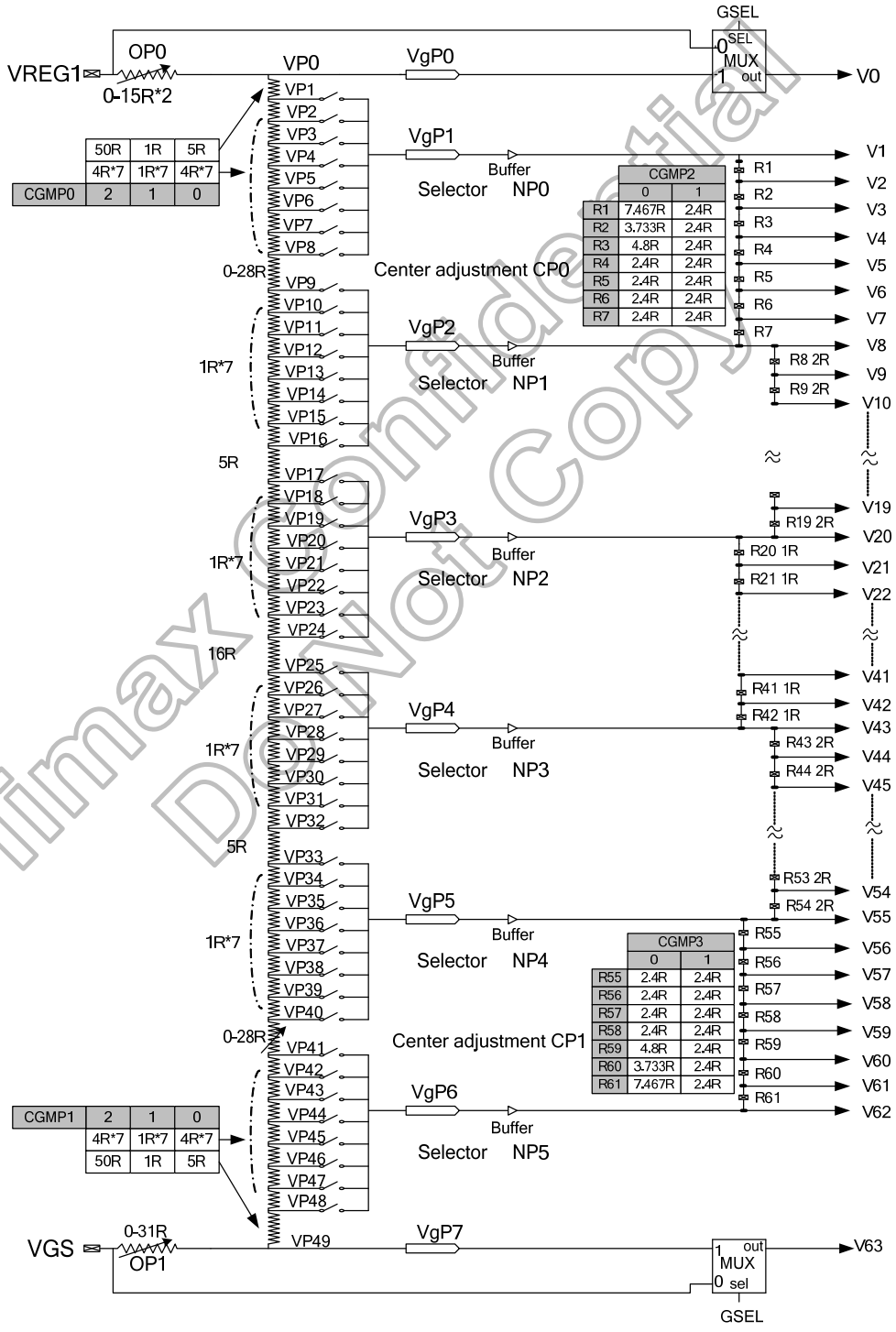
The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generates one reference voltage output (Vg(P/N)1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

| Register Groups | Positive Polarity | Negative Polarity | Description |
|---|---|---|---|
| Center Adjustment | CP0 2-0 | CN0 2-0 | Variable resistor (VRCP/N0) for center adjustment |
| | CP1 2-0 | CN1 2-0 | Variable resistor (VRCP/N1)for center adjustment |
| Macro Adjustment | MP0 2-0 | MN0 2-0 | 8-to-1 selector (voltage level of grayscale 1) |
| | MP1 2-0 | MN1 2-0 | 8-to-1 selector (voltage level of grayscale 8) |
| | MP2 2-0 | MN2 2-0 | 8-to-1 selector (voltage level of grayscale 20) |
| | MP3 2-0 | MN3 2-0 | 8-to-1 selector (voltage level of grayscale 43) |
| | MP4 2-0 | MN4 2-0 | 8-to-1 selector (voltage level of grayscale 55) |
| | MP5 2-0 | MN5 2-0 | 8-to-1 selector (voltage level of grayscale 62) |
| Offset Adjustment | OP0 3-0 | ON0 3-0 | Variable resistor (VROP/N0)for offset adjustment |
| | OP1 4-0 | ON1 4-0 | Variable resistor (VROP/N1)for offset adjustment |

**Table 5. 10 Gamma-Adjustment Registers**

### 5.9.4 Gamma Resister Stream and 8 to 1 Selector

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.



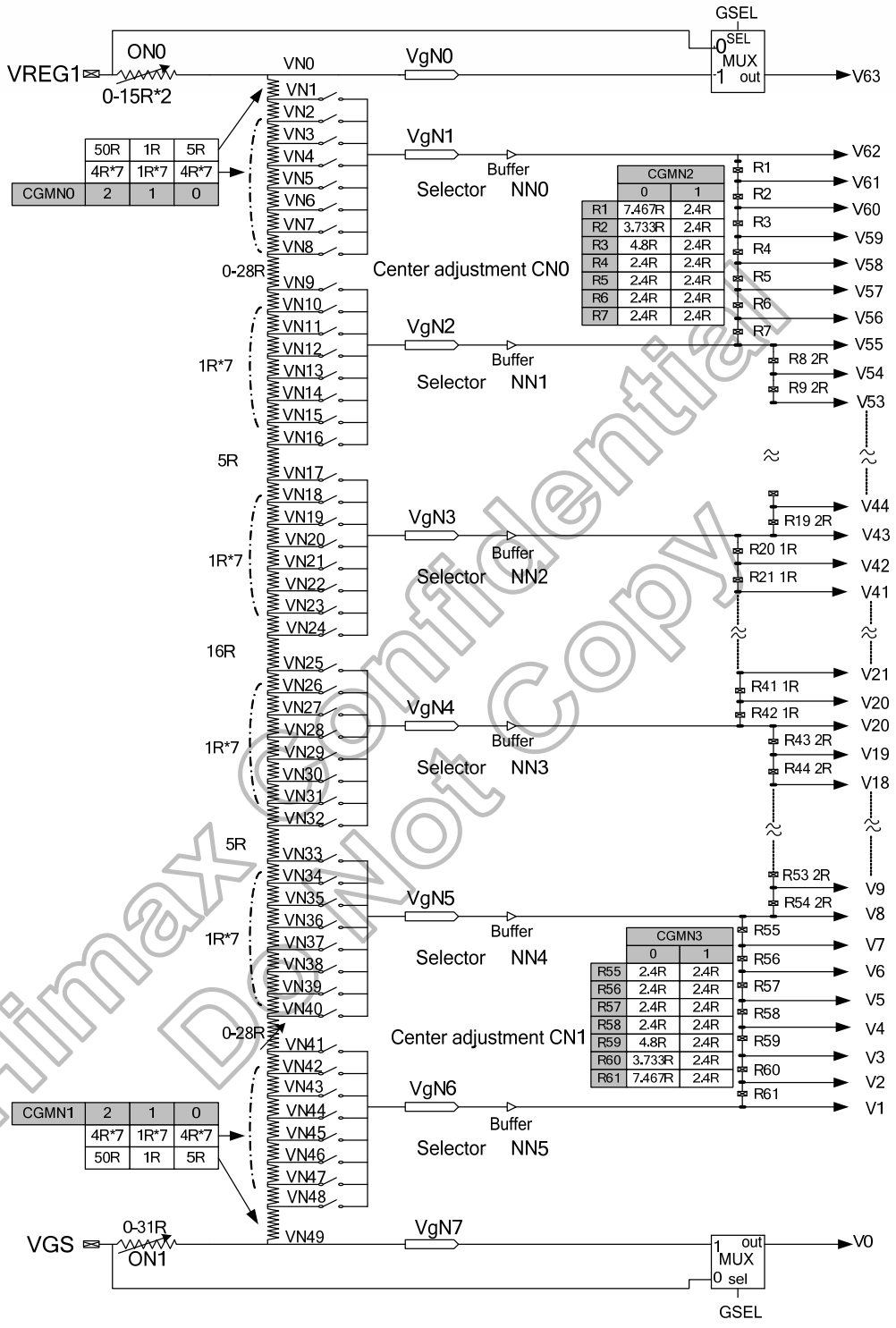



**Figure 5. 37 Gamma Resister Stream and Gamma Reference Voltage**

### 5.9.5 Variable Resister

There are two types of variable resistors, one is for center adjustment, the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

| Value in Register O(P/N)0 3-0 | Resistance VRO(P/N)0 |
|---|---|
| 0000 | 0R |
| 0001 | 2R |
| 0010 | 4R |
| • | • |
| • | • |
| 1101 | 26R |
| 1110 | 28R |
| 1111 | 30R |

Table 5. 11 Offset Adjustment 0

| Value in Register O(P/N)1 4-0 | Resistance VRO(P/N)1 |
|---|---|
| 00000 | 0R |
| 00001 | 1R |
| 00010 | 2R |
| • | • |
| • | • |
| 11101 | 29R |
| 11110 | 30R |
| 11111 | 31R |

Table 5. 12 Offset Adjustment 1

| Value in Register C(P/N)0/1 2-0 | Resistance VRC(P/N)0/1 |
|---|---|
| 000 | 0R |
| 001 | 4R |
| 010 | 8R |
| 011 | 12R |
| 100 | 16R |
| 101 | 20R |
| 110 | 24R |
| 111 | 28R |

Table 5. 13 Center Adjustment

### 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

| Value in Register | Voltage level | | | | | |
|---|---|---|---|---|---|---|
| M(P/N) 2-0 | Vg(P/N) 1 | Vg(P/N) 2 | Vg(P/N) 3 | Vg(P/N) 4 | Vg(P/N) 5 | Vg(P/N) 6 |
| 000 | VP(N)1 | VP(N)9 | VP(N)17 | VP(N)25 | VP(N)33 | VP(N)41 |
| 001 | VP(N)2 | VP(N)10 | VP(N)18 | VP(N)26 | VP(N)34 | VP(N)42 |
| 010 | VP(N)3 | VP(N)11 | VP(N)19 | VP(N)27 | VP(N)35 | VP(N)43 |
| 011 | VP(N)4 | VP(N)12 | VP(N)20 | VP(N)28 | VP(N)36 | VP(N)44 |
| 100 | VP(N)5 | VP(N)13 | VP(N)21 | VP(N)29 | VP(N)37 | VP(N)45 |
| 101 | VP(N)6 | VP(N)14 | VP(N)22 | VP(N)30 | VP(N)38 | VP(N)46 |
| 110 | VP(N)7 | VP(N)15 | VP(N)23 | VP(N)31 | VP(N)39 | VP(N)47 |
| 111 | VP(N)8 | VP(N)16 | VP(N)24 | VP(N)32 | VP(N)40 | VP(N)48 |

Table 5. 14 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas:

| Reference Voltage | Macro Adjustment Value | Formula | Pin |
|---|---|---|---|
| VgP0 | ---- | [(VREG1-VD*VROP0 /SumRP)] *GSEL +VREG1-(VREG1*GSEL) | VP0 |
| VgP1 | NP0 2-0=000 | VREG1-VD[(VROP0+(CGMP0*1R)+5R- (CGMP0*5R)] /SumRP | VP1 |
| | NP0 2-0=001 | VREG1-VD[(VROP0+(CGMP0*2R)+9R- (CGMP0*9R)] /SumRP | VP2 |
| | NP0 2-0=010 | VREG1-VD[(VROP0+(CGMP0*3R)+13R- (CGMP0*13R)] /SumRP | VP3 |
| | NP0 2-0=011 | VREG1-VD[(VROP0+(CGMP0*4R)+17R- (CGMP0*17R)] /SumRP | VP4 |
| | NP0 2-0=100 | VREG1-VD[(VROP0+(CGMP0*5R)+21R- (CGMP0*21R)] /SumRP | VP5 |
| | NP0 2-0=101 | VREG1-VD[(VROP0+(CGMP0*6R)+25R- (CGMP0*25R)] /SumRP | VP6 |
| | NP0 2-0=110 | VREG1-VD[(VROP0+(CGMP0*7R)+29R- (CGMP0*29R)] /SumRP | VP7 |
| | NP0 2-0=111 | VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R)] /SumRP | VP8 |
| VgP2 | NP1 2-0=000 | VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R) +VRCP0] /SumRP | VP9 |
| | NP1 2-0=001 | VREG1-VD[(VROP0+(CGMP0*9R)+34R- (CGMP0*34R) +VRCP0] /SumRP | VP10 |
| | NP1 2-0=010 | VREG1-VD[(VROP0+(CGMP0*10R)+35R- (CGMP0*35R) +VRCP0] /SumRP | VP11 |
| | NP1 2-0=011 | VREG1-VD[(VROP0+(CGMP0*11R)+36R- (CGMP0*36R) +VRCP0] /SumRP | VP12 |
| | NP1 2-0=100 | VREG1-VD[(VROP0+(CGMP0*12R)+37R- (CGMP0*37R) +VRCP0] /SumRP | VP13 |
| | NP1 2-0=101 | VREG1-VD[(VROP0+(CGMP0*13R)+38R- (CGMP0*38R) +VRCP0] /SumRP | VP14 |
| | NP1 2-0=110 | VREG1-VD[(VROP0+(CGMP0*14R)+39R- (CGMP0*39R) +VRCP0] /SumRP | VP15 |
| | NP1 2-0=111 | VREG1-VD[(VROP0+(CGMP0*15R)+40R- (CGMP0*40R) +VRCP0] /SumRP | VP16 |
| VgP3 | NP2 2-0=000 | VREG1-VD[(VROP0+(CGMP0*20R)+45R- (CGMP0*45R) +VRCP0] /SumRP | VP17 |
| | NP2 2-0=001 | VREG1-VD[(VROP0+(CGMP0*21R)+46R- (CGMP0*46R) +VRCP0] /SumRP | VP18 |
| | NP2 2-0=010 | VREG1-VD[(VROP0+(CGMP0*22R)+47R- (CGMP0*47R) +VRCP0] /SumRP | VP19 |
| | NP2 2-0=011 | VREG1-VD[(VROP0+(CGMP0*23R)+48R- (CGMP0*48R) +VRCP0] /SumRP | VP20 |
| | NP2 2-0=100 | VREG1-VD[(VROP0+(CGMP0*24R)+49R- (CGMP0*49R) +VRCP0] /SumRP | VP21 |
| | NP2 2-0=101 | VREG1-VD[(VROP0+(CGMP0*25R)+50R- (CGMP0*50R) +VRCP0] /SumRP | VP22 |
| | NP2 2-0=110 | VREG1-VD[(VROP0+(CGMP0*26R)+51R- (CGMP0*51R) +VRCP0] /SumRP | VP23 |
| | NP2 2-0=111 | VREG1-VD[(VROP0+(CGMP0*27R)+52R- (CGMP0*52R) +VRCP0] /SumRP | VP24 |
| VgP4 | NP3 2-0=000 | VREG1-VD[(VROP0+(CGMP0*43R)+68R- (CGMP0*68R) +VRCP0] /SumRP | VP25 |
| | NP3 2-0=001 | VREG1-VD[(VROP0+(CGMP0*44R)+69R- (CGMP0*69R) +VRCP0] /SumRP | VP26 |
| | NP3 2-0=010 | VREG1-VD[(VROP0+(CGMP0*45R)+70R- (CGMP0*70R) +VRCP0] /SumRP | VP27 |
| | NP3 2-0=011 | VREG1-VD[(VROP0+(CGMP0*46R)+71R- (CGMP0*71R) +VRCP0] /SumRP | VP28 |
| | NP3 2-0=100 | VREG1-VD[(VROP0+(CGMP0*47R)+72R- (CGMP0*72R) +VRCP0] /SumRP | VP29 |
| | NP3 2-0=101 | VREG1-VD[(VROP0+(CGMP0*48R)+73R- (CGMP0*73R) +VRCP0] /SumRP | VP30 |
| | NP3 2-0=110 | VREG1-VD[(VROP0+(CGMP0*49R)+74R- (CGMP0*74R) +VRCP0] /SumRP | VP31 |
| | NP3 2-0=111 | VREG1-VD[(VROP0+(CGMP0*50R)+75R- (CGMP0*75R) +VRCP0] /SumRP | VP32 |
| VgP5 | NP4 2-0=000 | VREG1-VD[(VROP0+(CGMP0*55R)+80R- (CGMP0*80R) +VRCP0] /SumRP | VP33 |
| | NP4 2-0=001 | VREG1-VD[(VROP0+(CGMP0*56R)+81R- (CGMP0*81R) +VRCP0] /SumRP | VP34 |
| | NP4 2-0=010 | VREG1-VD[(VROP0+(CGMP0*57R)+82R- (CGMP0*82R) +VRCP0] /SumRP | VP35 |
| | NP4 2-0=011 | VREG1-VD[(VROP0+(CGMP0*58R)+83R- (CGMP0*83R) +VRCP0] /SumRP | VP36 |
| | NP4 2-0=100 | VREG1-VD[(VROP0+(CGMP0*59R)+84R- (CGMP0*84R) +VRCP0] /SumRP | VP37 |
| | NP4 2-0=101 | VREG1-VD[(VROP0+(CGMP0*60R)+85R- (CGMP0*85R) +VRCP0] /SumRP | VP38 |
| | NP4 2-0=110 | VREG1-VD[(VROP0+(CGMP0*61R)+86R- (CGMP0*86R) +VRCP0] /SumRP | VP39 |
| | NP4 2-0=111 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0] /SumRP | VP40 |
| VgP6 | NP5 2-0=000 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1] /SumRP | VP41 |
| | NP5 2-0=001 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+4R-(4R*CGMP1)+(CGMP1*1R)] /SumRP | VP42 |
| | NP5 2-0=010 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+8R-(8R*CGMP1)+(CGMP1*2R)] /SumRP | VP43 |
| | NP5 2-0=011 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+12R-(12R*CGMP1)+(CGMP1*3R)] /SumRP | VP44 |
| | NP5 2-0=100 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+16R-(16R*CGMP1)+(CGMP1*4R)] /SumRP | VP45 |
| | NP5 2-0=101 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+20R-(20R*CGMP1)+(CGMP1*5R)] /SumRP | VP46 |
| | NP5 2-0=110 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+24R-(24R*CGMP1)+(CGMP1*6R)] /SumRP | VP47 |
| | NP5 2-0=111 | VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+28R-(28R*CGMP1)+(CGMP1*7R)] /SumRP | VP48 |
| VgP7 | ---- | { VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+33R-(33R*CGMP1)+(CGMP1*8R)] /SumRP }*GSEL+VGS-(GSEL*VGS) | VP49 |

**Note: CGMP0=1 or 0, CGMP1=1 or 0.**

**Table 5. 15 Voltage Calculation Formula (Positive Polarity)**

SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)
VD=(VREG1-VGS)

| Grayscale Voltage | Formula | Grayscale Voltage | Formula |
|---|---|---|---|
| V0 | VgP0 | V32 | VgP4+(VgP3-VgP4)*(11/23) |
| V1 | VgP1 | V33 | VgP4+(VgP3-VgP4)*(10/23) |
| V2 | VgP2+(VgP1-VgP2)*(CGMP2*14.4/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(18.133/25.6) | V34 | VgP4+(VgP3-VgP4)*(9/23) |
| V3 | VgP2+(VgP1-VgP2)*(CGMP2*12/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(4.4/25.6) | V35 | VgP4+(VgP3-VgP4)*(8/23) |
| V4 | VgP2+(VgP1-VgP2)*(CGMP2*9.6/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(9.6/25.6) | V36 | VgP4+(VgP3-VgP4)*(7/23) |
| V5 | VgP2+(VgP1-VgP2)*(CGMP2*7.2/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(7.2/25.6) | V37 | VgP4+(VgP3-VgP4)*(6/23) |
| V6 | VgP2+(VgP1-VgP2)*(CGMP2*4.8/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(4.8/25.6) | V38 | VgP4+(VgP3-VgP4)*(5/23) |
| V7 | VgP2+(VgP1-VgP2)*(CGMP2*2.4/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(2.4/25.6) | V39 | VgP4+(VgP3-VgP4)*(4/23) |
| V8 | VgP2 | V40 | VgP4+(VgP3-VgP4)*(3/23) |
| V9 | VgP3+(VgP2-VgP3)*(22/24) | V41 | VgP4+(VgP3-VgP4)*(2/23) |
| V10 | VgP3+(VgP2-VgP3)*(20/24) | V42 | VgP4+(VgP3-VgP4)*(1/23) |
| V11 | VgP3+(VgP2-VgP3)*(18/24) | V43 | VgP4 |
| V12 | VgP3+(VgP2-VgP3)*(16/24) | V44 | VgP5+(VgP4-VgP5)*(22/24) |
| V13 | VgP3+(VgP2-VgP3)*(14/24) | V45 | VgP5+(VgP4-VgP5)*(20/24) |
| V14 | VgP3+(VgP2-VgP3)*(12/24) | V46 | VgP5+(VgP4-VgP5)*(18/24) |
| V15 | VgP3+(VgP2-VgP3)*(10/24) | V47 | VgP5+(VgP4-VgP5)*(16/24) |
| V16 | VgP3+(VgP2-VgP3)*(8/24) | V48 | VgP5+(VgP4-VgP5)*(14/24) |
| V17 | VgP3+(VgP2-VgP3)*(6/24) | V49 | VgP5+(VgP4-VgP5)*(12/24) |
| V18 | VgP3+(VgP2-VgP3)*(4/24) | V50 | VgP5+(VgP4-VgP5)*(10/24) |
| V19 | VgP3+(VgP2-VgP3)*(2/24) | V51 | VgP5+(VgP4-VgP5)*(8/24) |
| V20 | VgP3 | V52 | VgP5+(VgP4-VgP5)*(6/24) |
| V21 | VgP4+(VgP3-VgP4)*(22/23) | V53 | VgP5+(VgP4-VgP5)*(4/24) |
| V22 | VgP4+(VgP3-VgP4)*(21/23) | V54 | VgP5+(VgP4-VgP5)*(2/24) |
| V23 | VgP4+(VgP3-VgP4)*(20/23) | V55 | VgP5 |
| V24 | VgP4+(VgP3-VgP4)*(19/23) | V56 | VgP6+(VgP5-VgP6)*(CGMP3*14.4/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(23.2/25.6) |
| V25 | VgP4+(VgP3-VgP4)*(18/23) | V57 | VgP6+(VgP5-VgP6)*(CGMP3*12/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(20.8/25.6) |
| V26 | VgP4+(VgP3-VgP4)*(17/23) | V58 | VgP6+(VgP5-VgP6)*(CGMP3*9.6/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(18.4/25.6) |
| V27 | VgP4+(VgP3-VgP4)*(16/23) | V59 | VgP6+(VgP5-VgP6)*(CGMP3*7.2/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(16/25.6) |
| V28 | VgP4+(VgP3-VgP4)*(15/23) | V60 | VgP6+(VgP5-VgP6)*(CGMP3*4.8/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(11.2/25.6) |
| V29 | VgP4+(VgP3-VgP4)*(14/23) | V61 | VgP6+(VgP5-VgP6)*(CGMP3*2.4/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(7.467/25.6) |
| V30 | VgP4+(VgP3-VgP4)*(13/23) | V62 | VgP6 |
| V31 | VgP4+(VgP3-VgP4)*(12/23) | V63 | VgP7 |

**Table 5. 16 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)**

| Reference Voltage | Macro Adjustment Value | Formula | Pin |
|---|---|---|---|
| VgN0 | - | [(VREG1-VD*VRON0 /SumRN)] *GSEL +VREG1-(VREG1*GSEL) | VN0 |
| VgN1 | NN0 2-0=000 | VREG1-VD[(VRON0+(CGMN0*1R)+5R- (CGMN0*5R)] /SumRN | VN1 |
| | NN0 2-0=001 | VREG1-VD[(VRON0+(CGMN0*2R)+9R- (CGMN0*9R)] /SumRN | VN2 |
| | NN0 2-0=010 | VREG1-VD[(VRON0+(CGMN0*3R)+13R- (CGMN0*13R)] /SumRN | VN3 |
| | NN0 2-0=011 | VREG1-VD[(VRON0+(CGMN0*4R)+17R- (CGMN0*17R)] /SumRN | VN4 |
| | NN0 2-0=100 | VREG1-VD[(VRON0+(CGMN0*5R)+21R- (CGMN0*21R)] /SumRN | VN5 |
| | NN0 2-0=101 | VREG1-VD[(VRON0+(CGMN0*6R)+25R- (CGMN0*25R)] /SumRN | VN6 |
| | NN0 2-0=110 | VREG1-VD[(VRON0+(CGMN0*7R)+29R- (CGMN0*29R)] /SumRN | VN7 |
| | NN0 2-0=111 | VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R)] /SumRN | VN8 |
| VgN2 | NN1 2-0=000 | VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R) +VRCN0] /SumRN | VN9 |
| | NN1 2-0=001 | VREG1-VD[(VRON0+(CGMN0*9R)+34R- (CGMN0*34R) +VRCN0] /SumRN | VN10 |
| | NN1 2-0=010 | VREG1-VD[(VRON0+(CGMN0*10R)+35R- (CGMN0*35R) +VRCN0] /SumRN | VN11 |
| | NN1 2-0=011 | VREG1-VD[(VRON0+(CGMN0*11R)+36R- (CGMN0*36R) +VRCN0] /SumRN | VN12 |
| | NN1 2-0=100 | VREG1-VD[(VRON0+(CGMN0*12R)+37R- (CGMN0*37R) +VRCN0] /SumRN | VN13 |
| | NN1 2-0=101 | VREG1-VD[(VRON0+(CGMN0*13R)+38R- (CGMN0*38R) +VRCN0] /SumRN | VN14 |
| | NN1 2-0=110 | VREG1-VD[(VRON0+(CGMN0*14R)+39R- (CGMN0*39R) +VRCN0] /SumRN | VN15 |
| | NN1 2-0=111 | VREG1-VD[(VRON0+(CGMN0*15R)+40R- (CGMN0*40R) +VRCN0] /SumRN | VN16 |
| VgN3 | NN2 2-0=000 | VREG1-VD[(VRON0+(CGMN0*20R)+45R- (CGMN0*45R) +VRCN0] /SumRN | VN17 |
| | NN2 2-0=001 | VREG1-VD[(VRON0+(CGMN0*21R)+46R- (CGMN0*46R) +VRCN0] /SumRN | VN18 |
| | NN2 2-0=010 | VREG1-VD[(VRON0+(CGMN0*22R)+47R- (CGMN0*47R) +VRCN0] /SumRN | VN19 |
| | NN2 2-0=011 | VREG1-VD[(VRON0+(CGMN0*23R)+48R- (CGMN0*48R) +VRCN0] /SumRN | VN20 |
| | NN2 2-0=100 | VREG1-VD[(VRON0+(CGMN0*24R)+49R- (CGMN0*49R) +VRCN0] /SumRN | VN21 |
| | NN2 2-0=101 | VREG1-VD[(VRON0+(CGMN0*25R)+50R- (CGMN0*50R) +VRCN0] /SumRN | VN22 |
| | NN2 2-0=110 | VREG1-VD[(VRON0+(CGMN0*26R)+51R- (CGMN0*51R) +VRCN0] /SumRN | VN23 |
| | NN2 2-0=111 | VREG1-VD[(VRON0+(CGMN0*27R)+52R- (CGMN0*52R) +VRCN0] /SumRN | VN24 |
| VgN4 | NN3 2-0=000 | VREG1-VD[(VRON0+(CGMN0*43R)+68R- (CGMN0*68R) +VRCN0] /SumRN | VN25 |
| | NN3 2-0=001 | VREG1-VD[(VRON0+(CGMN0*44R)+69R- (CGMN0*69R) +VRCN0] /SumRN | VN26 |
| | NN3 2-0=010 | VREG1-VD[(VRON0+(CGMN0*45R)+70R- (CGMN0*70R) +VRCN0] /SumRN | VN27 |
| | NN3 2-0=011 | VREG1-VD[(VRON0+(CGMN0*46R)+71R- (CGMN0*71R) +VRCN0] /SumRN | VNP8 |
| | NN3 2-0=100 | VREG1-VD[(VRON0+(CGMN0*47R)+72R- (CGMN0*72R) +VRCN0] /SumRN | VN29 |
| | NN3 2-0=101 | VREG1-VD[(VRON0+(CGMN0*48R)+73R- (CGMN0*73R) +VRCN0] /SumRN | VN30 |
| | NN3 2-0=110 | VREG1-VD[(VRON0+(CGMN0*49R)+74R- (CGMN0*74R) +VRCN0] /SumRN | VN31 |
| | NN3 2-0=111 | VREG1-VD[(VRON0+(CGMN0*50R)+75R- (CGMN0*75R) +VRCN0] /SumRN | VN32 |
| VgN5 | NN4 2-0=000 | VREG1-VD[(VRON0+(CGMN0*55R)+80R- (CGMN0*80R) +VRCN0] /SumRN | VN33 |
| | NN4 2-0=001 | VREG1-VD[(VRON0+(CGMN0*56R)+81R- (CGMN0*81R) +VRCN0] /SumRN | VN34 |
| | NN4 2-0=010 | VREG1-VD[(VRON0+(CGMN0*57R)+82R- (CGMN0*82R) +VRCN0] /SumRN | VN35 |
| | NN4 2-0=011 | VREG1-VD[(VRON0+(CGMN0*58R)+83R- (CGMN0*83R) +VRCN0] /SumRN | VN36 |
| | NN4 2-0=100 | VREG1-VD[(VRON0+(CGMN0*59R)+84R- (CGMN0*84R) +VRCN0] /SumRN | VN37 |
| | NN4 2-0=101 | VREG1-VD[(VRON0+(CGMN0*60R)+85R- (CGMN0*85R) +VRCN0] /SumRN | VN38 |
| | NN4 2-0=110 | VREG1-VD[(VRON0+(CGMN0*61R)+86R- (CGMN0*86R) +VRCN0] /SumRN | VN39 |
| | NN4 2-0=111 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0] /SumRN | VN40 |
| VgN6 | NN5 2-0=000 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1] /SumRN | VN41 |
| | NN5 2-0=001 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+4R-(4R*CGMN1)+(CGMN1*1R)] /SumRN | VN42 |
| | NN5 2-0=010 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+8R-(8R*CGMN1)+(CGMN1*2R)] /SumRN | VN43 |
| | NN5 2-0=011 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+12R-(12R*CGMN1)+(CGMN1*3R)] /SumRN | VN44 |
| | NN5 2-0=100 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+16R-(16R*CGMN1)+(CGMN1*4R)] /SumRN | VN45 |
| | NN5 2-0=101 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+20R-(20R*CGMN1)+(CGMN1*5R)] /SumRN | VN46 |
| | NN5 2-0=110 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+24R-(24R*CGMN1)+(CGMN1*6R)] /SumRN | VN47 |
| | NN5 2-0=111 | VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+28R-(28R*CGMN1)+(CGMN1*7R)] /SumRN | VN48 |
| VgN7 | - | { VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+33R-(33R*CGMN1)+(CGMN1*8R)]/SumRN } *GSEL+VGS-(GSEL*VGS) | VN49 |

**Note: CGMN0=1 or 0, CGMN1=1 or 0**

**Table 5. 17 Voltage Calculation Formula (Negative Polarity)**

SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)
VD=(VREG1-VGS)

| Grayscale Voltage | Formula |
|---|---|
| V63 | VgN0 |
| V62 | VgN1 |
| V61 | VgN2+(VgN1-VgN2)*(CGMN2*14.4/16.8) + (VgN1-VgN2)*(1-CGMN2)*(18.133/25.6) |
| V60 | VgN2+(VgN1-VgN2)*(CGMN2*12/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(14.4/25.6) |
| V59 | VgN2+(VgN1-VgN2)*(CGMN2*9.6/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(9.6/25.6) |
| V58 | VgN2+(VgN1-VgN2)*(CGMN2*7.2/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(7.2/25.6) |
| V57 | VgN2+(VgN1-VgN2)*(CGMN2*4.8/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(4.8/25.6) |
| V56 | VgN2+(VgN1-VgN2)*(CGMN2*2.4/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(2.4/25.6) |
| V55 | VgN2 |
| V54 | VgN3+(VgN2-VgN3)*(22/24) |
| V53 | VgN3+(VgN2-VgN3)*(20/24) |
| V52 | VgN3+(VgN2-VgN3)*(18/24) |
| V51 | VgN3+(VgN2-VgN3)*(16/24) |
| V50 | VgN3+(VgN2-VgN3)*(14/24) |
| V49 | VgN3+(VgN2-VgN3)*(12/24) |
| V48 | VgN3+(VgN2-VgN3)*(10/24) |
| V47 | VgN3+(VgN2-VgN3)*(8/24) |
| V46 | VgN3+(VgN2-VgN3)*(6/24) |
| V45 | VgN3+(VgN2-VgN3)*(4/24) |
| V44 | VgN3+(VgN2-VgN3)*(2/24) |
| V43 | VgN3 |
| V42 | VgN4+(VgN3-VgN4)*(22/23) |
| V41 | VgN4+(VgN3-VgN4)*(21/23) |
| V40 | VgN4+(VgN3-VgN4)*(20/23) |
| V39 | VgN4+(VgN3-VgN4)*(19/23) |
| V38 | VgN4+(VgN3-VgN4)*(18/23) |
| V37 | VgN4+(VgN3-VgN4)*(17/23) |
| V36 | VgN4+(VgN3-VgN4)*(16/23) |
| V35 | VgN4+(VgN3-VgN4)*(15/23) |
| V34 | VgN4+(VgN3-VgN4)*(14/23) |
| V33 | VgN4+(VgN3-VgN4)*(13/23) |
| V32 | VgN4+(VgN3-VgN4)*(12/23) |

| Grayscale Voltage | Formula |
|---|---|
| V31 | VgN4+(VgN3-VgN4)*(11/23) |
| V30 | VgN4+(VgN3-VgN4)*(10/23) |
| V29 | VgN4+(VgN3-VgN4)*(9/23) |
| V28 | VgN4+(VgN3-VgN4)*(8/23) |
| V27 | VgN4+(VgN3-VgN4)*(7/23) |
| V26 | VgN4+(VgN3-VgN4)*(6/23) |
| V25 | VgN4+(VgN3-VgN4)*(5/23) |
| V24 | VgN4+(VgN3-VgN4)*(4/23) |
| V23 | VgN4+(VgN3-VgN4)*(3/23) |
| V22 | VgN4+(VgN3-VgN4)*(2/23) |
| V21 | VgN4+(VgN3-VgN4)*(1/23) |
| V20 | VgN4 |
| V19 | VgN5+(VgN4-VgN5)*(22/24) |
| V18 | VgN5+(VgN4-VgN5)*(20/24) |
| V17 | VgN5+(VgN4-VgN5)*(18/24) |
| V16 | VgN5+(VgN4-VgN5)*(16/24) |
| V15 | VgN5+(VgN4-VgN5)*(14/24) |
| V14 | VgN5+(VgN4-VgN5)*(12/24) |
| V13 | VgN5+(VgN4-VgN5)*(10/24) |
| V12 | VgN5+(VgN4-VgN5)*(8/24) |
| V11 | VgN5+(VgN4-VgN5)*(6/24) |
| V10 | VgN5+(VgN4-VgN5)*(4/24) |
| V9 | VgN5+(VgN4-VgN5)*(2/24) |
| V8 | VgN5 |
| V7 | VgN6+(VgN5-VgN6)*(CGMN3*14.4/16.8) + (VgN5-VgN6)*(1-CGMN3)*(23.2/25.6) |
| V6 | VgN6+(VgN5-VgN6)*(CGMN3*12/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(20.8/25.6) |
| 5 | VgN6+(VgN5-VgN6)*(CGMN3*9.6/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(18.4/25.6) |
| V4 | VgN6+(VgN5-VgN6)*(CGMN3*7.2/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(16/25.6) |
| V3 | VgN6+(VgN5-VgN6)*(CGMN3*4.8/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(11.2/25.6) |
| V2 | VgN6+(VgN5-VgN6)*(CGMN3*2.4/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(7.467/25.6) |
| V1 | VgN6 |
| V0 | VgN7 |

**Table 5. 18 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)**

**Relationship between GRAM Data and Output Level (INVON = "0")**

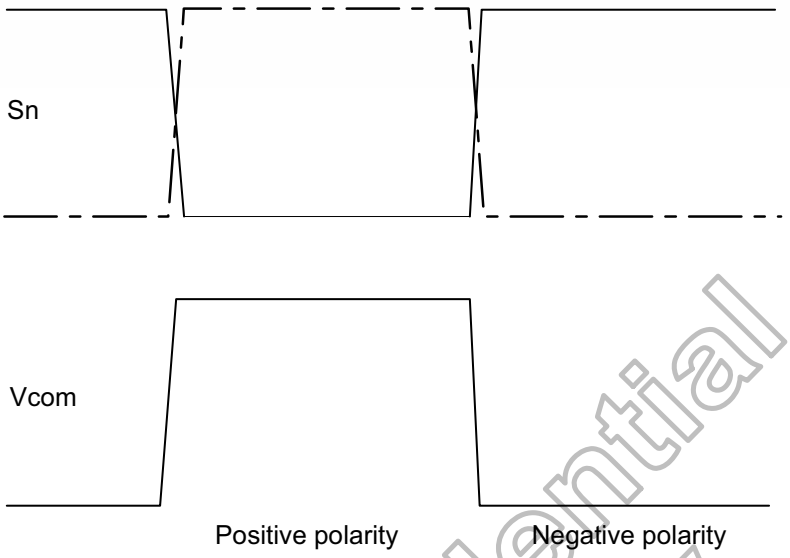
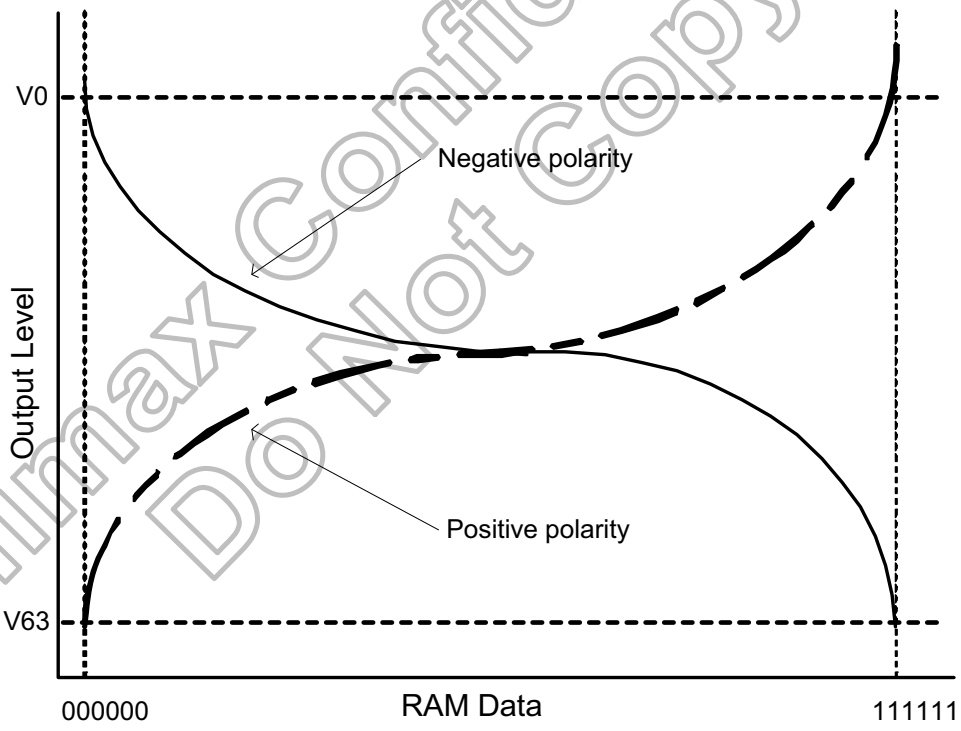



**Figure 5. 38 Relationship between Source Output and Vcom**




(Same characteristic for each RGB)

**Figure 5. 39 Relationship between GRAM Data and Output Level**

## 5.10 Scan Mode Setting

The HX8347-A01 can set internal register SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8347-A01.

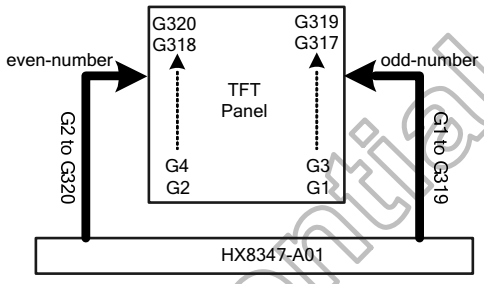
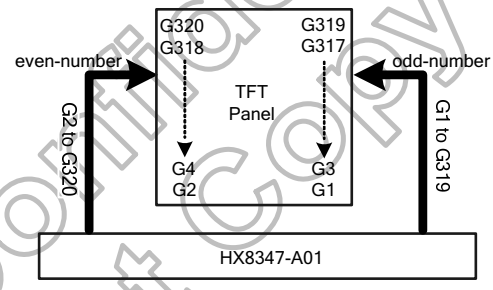
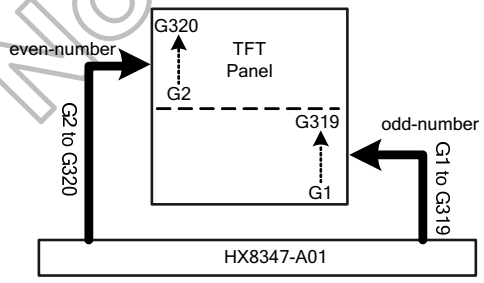
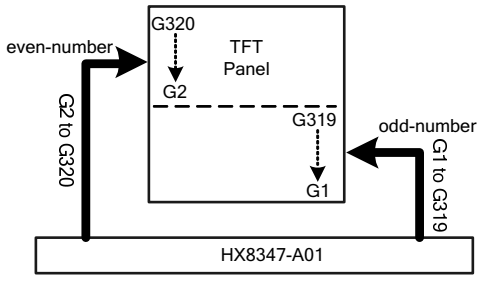
| SM | GS | Scan direction |
|---|---|---|
| 0 | 0 |  <br>G1,G2,G3,… G157,G158,… G319,G320 |
| 0 | 1 |  <br>G320,G319,G318,… G158,G157,… G2,G1 |
| 1 | 0 |  <br>G1,G3,G5,… G319,G2,G4… G318,G320 |
| 1 | 1 |  <br>G320,G318,… G2,G319,G317… G3,G1 |

**Figure 5. 40 Scan Function**

## 5.11 Oscillator

The HX8347-A01 can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the RADJ[3:0] internal register. Please refer to extended command set B0h. The default frequency is 5.5MHz.

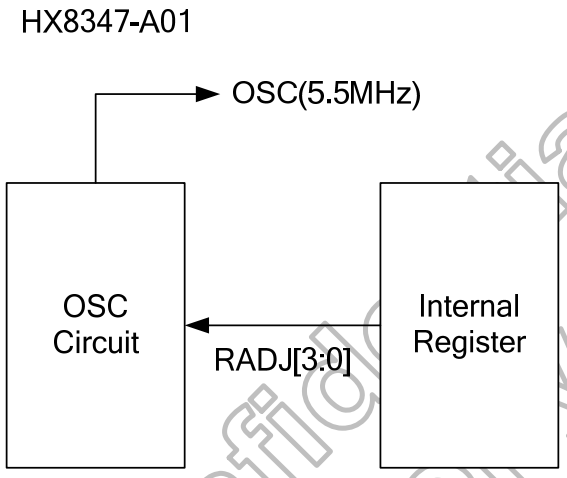



**Figure 5. 41 Oscillation Circuit**

## 5.12 Register Setting Flow (Register-Content Interface mode only)

The following are the sequences of register setting flow that applied to the HX8347-A01 driving the TFT display, when operate in Register-Content interface mode.

**Display On/Off Set flow**

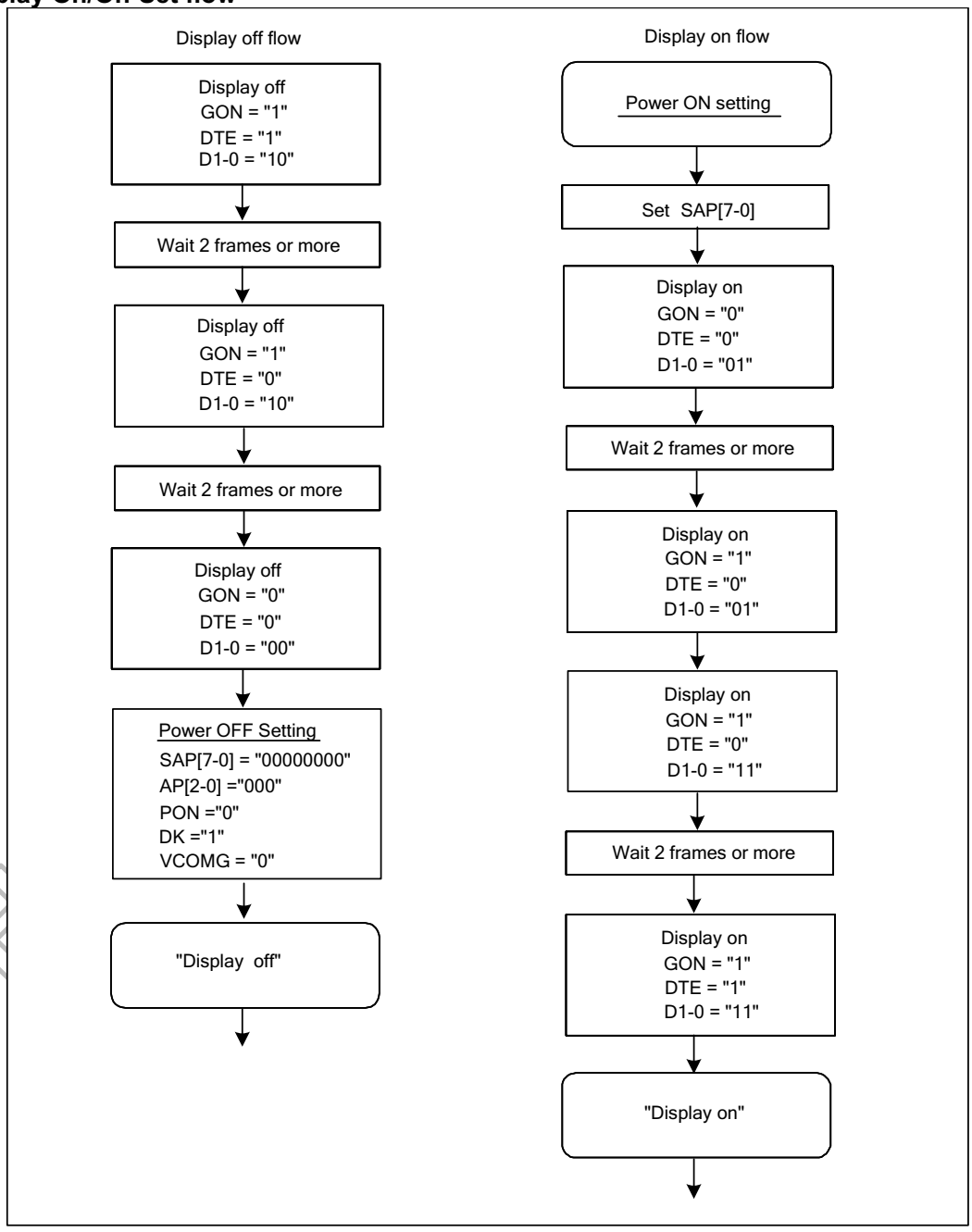
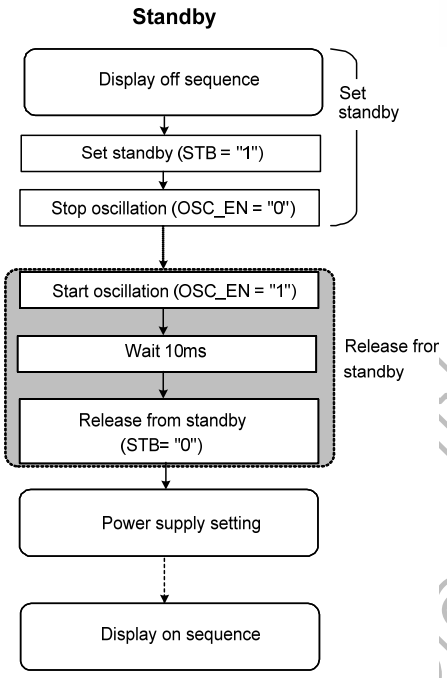



**Figure 5. 42 Display On/Off Set Sequence**

## Standby Mode Set flow




**Note:** HX8347-A01 doesn't have the Sleep mode in Register-Content interface mode.

**Figure 5. 43 Standby Mode Setting Sequence**

## 5.13 Power Supply Setting

The power supply setting sequence of the HX8347-A01 is follow as blew.

### Power Supply Setting Flow

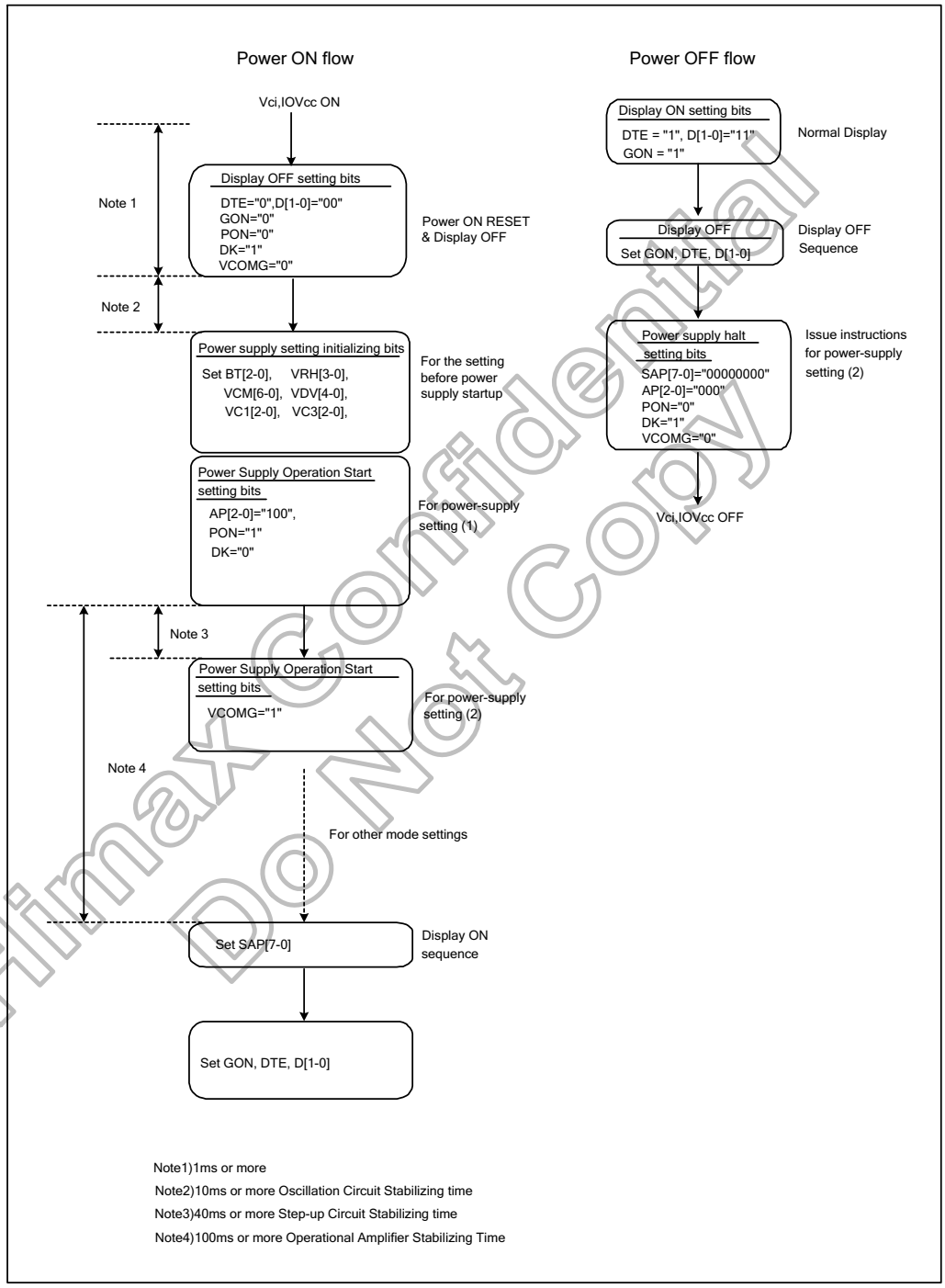



**Figure 5. 44 Power Supply Setting Flow**

## 5.14 Input / Output Pin State

### 5.14.1 Output or Bi-directional (I/O) Pins

| Output or Bi-directional pins | After Power On | After Hardware Reset | After Software Reset |
|---|---|---|---|
| TE | Low | Low | Low |
| D17 to D0 (Output driver) | High-Z (Inactive) | High-Z (Inactive) | High-Z (Inactive) |
| VSYNC | Low | Low | Low |
| TEST1 | Low | Low | Low |

**Note:** There will be no output from D17-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

**Table 5. 19 State of Output or Bi-directional (I/O) Pins**

### 5.14.2 Input Pins

| Input pins | During Power On Process | After Power On | After Hardware Reset | After Software Reset | During Power Off Process |
|---|---|---|---|---|---|
| NRESET | See Section 5.12 | Input valid | Input valid | Input valid | See Section 5.12 |
| NCS | Input valid | Input valid | Input valid | Input valid | Input valid |
| DNC_SCL | Input valid | Input valid | Input valid | Input valid | Input valid |
| NWR_RNW | Input valid | Input valid | Input valid | Input valid | Input valid |
| NRD_E | Input valid | Input valid | Input valid | Input valid | Input valid |
| D17 to D0 | Input valid | Input valid | Input valid | Input valid | Input valid |
| HSYNC | Input valid | Input valid | Input valid | Input valid | Input valid |
| VSYNC | Input valid | Input valid | Input valid | Input valid | Input valid |
| DOTCLK | Input valid | Input valid | Input valid | Input valid | Input valid |
| ENABLE | Input valid | Input valid | Input valid | Input valid | Input valid |
| OSC, BURN, P68, BS2, BS1,BS0, | Input valid | Input valid | Input valid | Input valid | Input valid |
| EXTC | Input valid | Input valid | Input valid | Input valid | Input valid |

**Table 5. 20 State of Input Pins**

## 5.15 OTP Programming

| OTP_INDEX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0x00 | Himax internal use(no open) | | | | | | | |
| 0x01 | Himax internal use(no open) | | | | | | | |
| 0x02 | Himax internal use(no open) | | | | | | | |
| 0x03 | Himax internal use(no open) | | | | | | | |
| 0x04 | Himax internal use(no open) | | | | | | | |
| 0x05 | Himax internal use(no open) | | | | | | | |
| 0x06 | Himax internal use(no open) | | | | | | | |
| 0x07 | Himax internal use(no open) | | | | | | | |
| 0x08 | BGR_PANEL | DIV_I[1:0] | | DIV_PI[1:0] | | DIV_N[1:0] | | RGB_EN |
| 0x09 | VDV[3:0] | | | | SM_PANEL | SS_PANEL | GS_PANEL | REV_PANEL |
| 0x0A | VCM[6:0] | | | | | | | VDV[4] |
| 0x0B | Himax internal use(no open) | | | | | | | |
| 0x0C | Himax internal use(no open) | | | | | | | |
| 0x0D | ID2[6:0] | | | | | | | NVALID3 |
| 0x0E | ID3[7:0] | | | | | | | |
| 0x0F | ID1[7:0] | | | | | | | |

**Note:** (1) The all OTP memory bit default value are “1”.
(2) BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL are don’t care in Register-Content Interface mode and these bit will program to “0”.
(3) If OTP_index 0x0Dh no programming, HX8347-A01 will no reload OTP value to related register.

**Table 5. 21 OTP memory table**

### Programming Flow

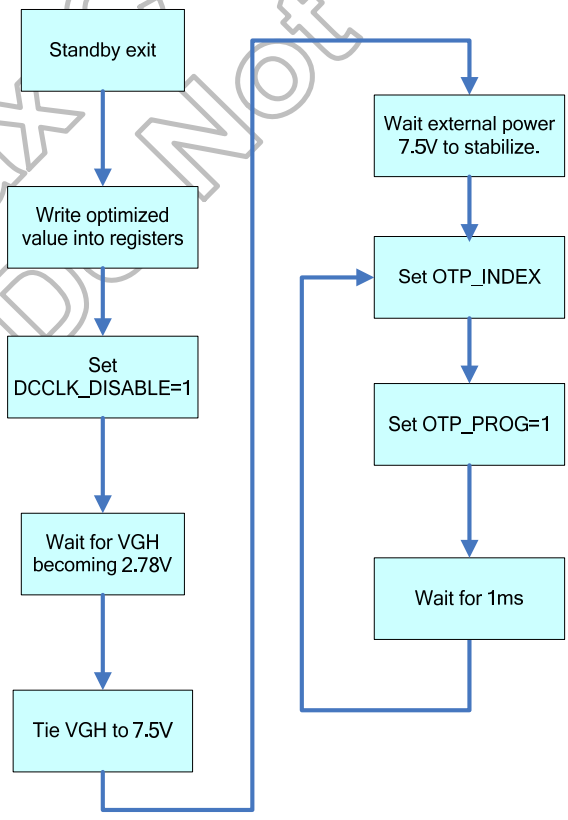
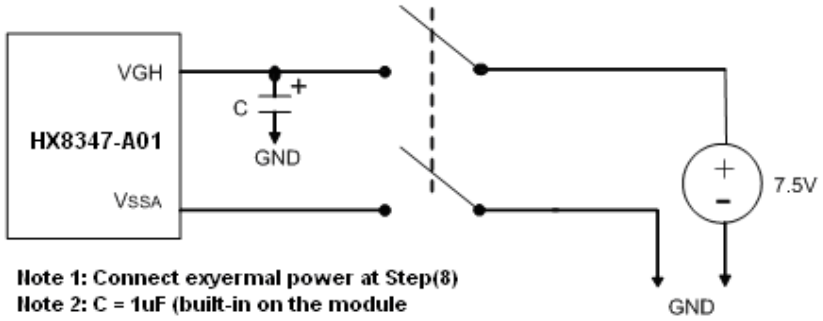



**Figure 5. 45 OTP Programming Flow**

## Programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Set OTP_LOAD_DISABLE=1, disable the auto-loading function.</td></tr>
<tr><td>3</td><td>OSC_EN=1, STB=0</td></tr>
<tr><td>4</td><td>Wait 120ms</td></tr>
<tr><td>5</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>Cycle Control4 (3Dh)</td><td>DIV_I[1:0], DIV_PI[1:0], DIV_N[1:0]</td><td>The division ratio of clocks in display mode</td></tr>
<tr><td>RGB interface control 1 (38h)</td><td>RGB_EN</td><td>RGB I/F Disable/Enable</td></tr>
<tr><td>VCOM Control2 (44h)</td><td>VCM[6:0]</td><td>VcomH voltage (High level voltage of VCOM)</td></tr>
<tr><td>VCOM Control3 (45h)</td><td>VDV[4:0]</td><td>Vcom amplitude (VcomL = VcomH – Vcom amplitude, VcomL ≥ VCL+0.5V)</td></tr>
<tr><td>Internal Use16 (64h)</td><td>ID1[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>Internal Use17 (65h)</td><td>ID2[6:0]</td><td>LCD module/driver version</td></tr>
<tr><td>Internal Use18 (66h)</td><td>ID3[7:0]</td><td>Identifies the LCD module/driver</td></tr>
</table>
Note: BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL are don’t care in Register-Content Interface mode and these bit will program to “0”.</td></tr>
<tr><td>6</td><td>Set OTP_ DCCLK_DISABLE=1, disable internal pumping clock.</td></tr>
<tr><td>7</td><td>Wait 500ms for power down</td></tr>
<tr><td>8</td><td>Connect external power 7.5V to VGH pin</td></tr>
<tr><td>9</td><td>Wait 100ms for external power 7.5V to stabilize.</td></tr>
<tr><td>10</td><td>Specify OTP_index
<table>
<tr><th>OTP_index</th><th>Parameter</th></tr>
<tr><td>0x08h</td><td>BGR_PANEL, DIV_I[1:0], DIV_PI[1:0], DIV_N[1:0], RGB_EN</td></tr>
<tr><td>0x09h</td><td>VDV[3:0], SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL</td></tr>
<tr><td>0x0Ah</td><td>VCM[6:0], VDV[4]</td></tr>
<tr><td>0x0Dh</td><td>ID2[6:0]</td></tr>
<tr><td>0x0Eh</td><td>ID3[7:0]</td></tr>
<tr><td>0x0Fh</td><td>ID1[7:0]</td></tr>
</table>
Note: BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL are don’t care in Register-Content Interface mode and these bit will program to “0”.</td></tr>
<tr><td>11</td><td>Set OTP_Mask=0x00h, programming all of the bit of one parameter.</td></tr>
<tr><td>12</td><td>Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>13</td><td>Wait 1 ms</td></tr>
<tr><td>14</td><td>Complete programming one parameter to OTP. If continue to programming other parameter, return to step (10). Otherwise, power off the module and remove the external power on VGH pin.</td></tr>
</table>

## Programming circuitry



## 5.16 Free Running Mode Specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in, it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Please note that the black and the white pattern are reversed in case of a normally black display.

| Parameter | Symbol | Description |
|---|---|---|
| Power supply pins | IOVCC, VCI | All power supply pins |
| Free running mode | BURN | BURN=1, FR-mode is enabled. |
| Reset | NRESET | Active low pulse in order to start the FR-mode. |
| Chip select(1) | NCS | This pin will be left open during FRM mode. |
| Data enable(1) | ENABLE | This pin will be left open during FRM mode. |
| Reads/not write(1) | NWR_RNW | This pin will be left open during FRM mode. |
| Data/not command(1) | DNC_SCL | This pin will be left open during FRM mode. |
| Interface select(1) | IFSEL0 | This pin will be left open during FRM mode. |
| Horizontal sync(1) | HSYNC | This pin will be left open during FRM mode. |
| Vertical sync(1) | VSYNC | This pin will be left open during FRM mode. |
| Data clock | DOTCLK | This pin will be left open during FRM mode. |
| CPU I/F Data(1) | D[0..17] | This pin will be left open during FRM mode. |
| SPI I/F Data(1) | SDI, SDO | This pin will be left open during FRM mode. |

**Note:** (1) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc, must be disabled, all mode select pins like data-not-command, interface-select etc and all data-bus pins must be set to either logic high or logic low during the FR-mode.

**Table 5. 22 Pin Information**

## Power-on Sequence

The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if it is supported by the driver specification. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP starts to load when Reset leaves low to high.

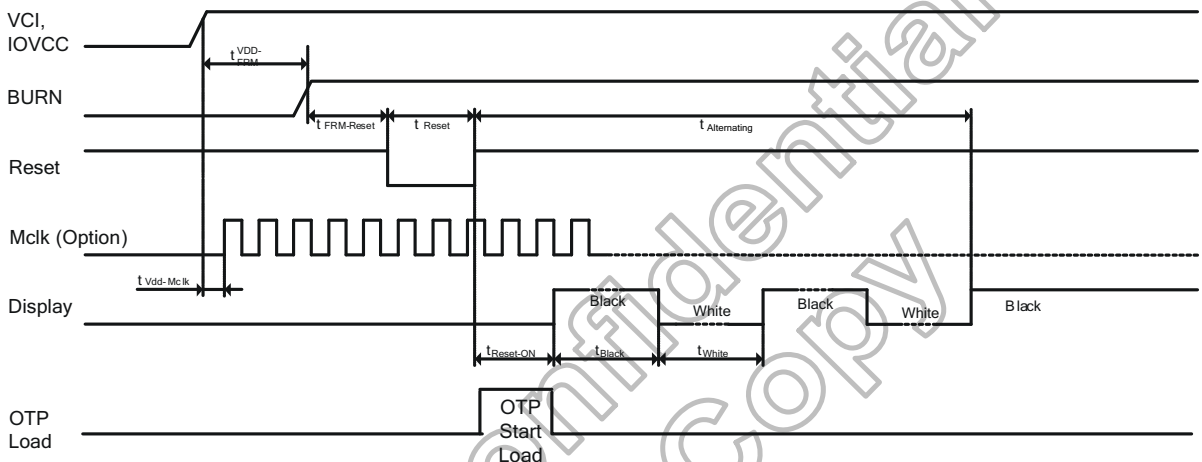



**Figure 5. 46 Power On Sequence of FR-mode (for Normally–White Panel)**

## Power off Sequence

The power supply can be switched off any time.

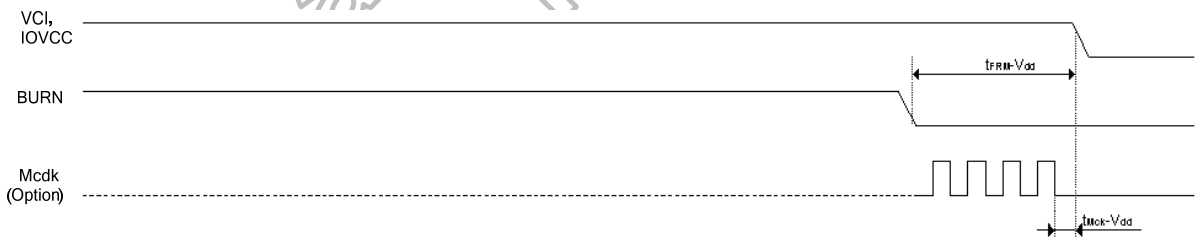



**Figure 5. 47 Power Off Sequence of FR-mode**

### Free Running Mode Display

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shell be 50%/50%. The time of the black and white pattern shell be around 1 seconds in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. The display is switched to a static black pattern after the alternating mode is finished. Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. It can be between 5 and 100Hz. The frame frequency will be set according to the parameter in the OTP.

| | | | | | |
|---|---|---|---|---|---|
| **Alternating Black and White Pattern** | $t_{Alternating}$ | - | 5 | - | min |
| **Master Clock Frequency** | $f_{Mclk}$ | - | - | 10 | MHz |

**Table 5. 23 Frequency Definition of Free Running Mode Display**

# 6. Command

## 6.1 Command Set

**Table 6. 1 List Table of Register Set**

| Register No. | Register | W/R | RS | Upper Code | Lower Code | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D[17:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| R01h | Display Mode control | W/R | 1 | * | * | * | * | * | IDMON (0) | INVON (0) | NORON (1) | PTLON(0) | |
| R02h | Column address start 2 | W/R | 1 | * | SC[15:8] (8'b0) | | | | | | | | |
| R03h | Column address start 1 | W/R | 1 | * | SC[7:0] (8'b0) | | | | | | | | |
| R04h | Column address end 2 | W/R | 1 | * | EC[15:8] (8'b0) | | | | | | | | |
| R05h | Column address end 1 | W/R | 1 | * | EC[7:0] (8'b1110_1111) | | | | | | | | |
| R06h | Row address start 2 | W/R | 1 | * | SP[15:8] (8'b0) | | | | | | | | |
| R07h | Row address start 1 | W/R | 1 | * | SP[7:0] (8'b0) | | | | | | | | |
| R08h | Row address end 2 | W/R | 1 | * | EP[15:8] (8'b0000_0001) | | | | | | | | |
| R09h | Row address end 1 | W/R | 1 | * | EP[7:0] (8'b0011_1111) | | | | | | | | |
| R0Ah | Partial area start row 2 | W/R | 1 | * | PSL[15:8] (8'b0) | | | | | | | | |
| R0Bh | Partial area start row 1 | W/R | 1 | * | PSL[7:0] (8'b0) | | | | | | | | |
| R0Ch | Partial area end row 2 | W/R | 1 | * | PEL[15:8] (8'b0000_0001) | | | | | | | | |
| R0Dh | Partial area end row 1 | W/R | 1 | * | PEL[7:0] (8'b0011_1111) | | | | | | | | |
| R0Eh | Vertical Scroll Top fixed area 2 | W/R | 1 | * | TFA[15:8] (8'b0) | | | | | | | | |
| R0Fh | Vertical Scroll Top fixed area 1 | W/R | 1 | * | TFA[7:0] (8'b0) | | | | | | | | |
| R10h | Vertical Scroll height area 2 | W/R | 1 | * | VSA[15:8] (8'b0000_0001) | | | | | | | | |
| R11h | Vertical Scroll height area 1 | W/R | 1 | * | VSA[7:0] (8'b0100_0000) | | | | | | | | |
| R12h | Vertical Scroll Button area 2 | W/R | 1 | * | BFA[15:8] (8'b0) | | | | | | | | |
| R13h | Vertical Scroll Button area 1 | W/R | 1 | * | BFA [7:0] (8'b0) | | | | | | | | |
| R14h | Vertical Scroll Start address 2 | W/R | 1 | * | VSP [15:8] (8d'0) | | | | | | | | |
| R15h | Vertical Scroll Start address 1 | W/R | 1 | * | VSP [7:0] (8d'0) | | | | | | | | |
| R16h | Memory Access control | W/R | 1 | * | MY(0) | MX(0) | MV(0) | * | BGR(0) | * | * | * | |
| R18h | Gate Scan control | W/R | 1 | * | * | * | * | * | * | * | SCROLL_ON(0) | SM(0) | |
| R19h | OSC Control 1 | W/R | 1 | * | * | CADJ[3:0] (1001) | | | CUADJ[2:0] (000) | | | OSC_EN(0) | |
| R1Ah | OSC Control 2 | W/R | 1 | * | * | * | * | * | * | * | * | OSC_TEST(0) | |
| R1Bh | Power Control 1 | W/R | 1 | * | GASENB(0) | * | * | PON(0) | DK(1) | XDK(0) | VLCD_TRI(0) | STB(1) | |
| R1Ch | Power Control 2 | W/R | 1 | * | | | | | | AP[2:0] (000) | | | |
| R1Dh | Power Control 3 | W/R | 1 | * | * | | | | * | VC1[2:0] (101) | | | |
| R1Eh | Power Control 4 | W/R | 1 | * | * | * | * | * | * | VC3[2:0] (000) | | | |
| R1Fh | Power Control 5 | | | * | * | * | * | * | VRH[3:0] (0100) | | | | |
| R20h | Power Control 6 | W/R | 1 | * | BT[3:0] (0100) | | | | * | * | * | * | |

| Register No. | Register | W/R | RS | Upper Code | Lower Code | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D[17:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| R21h | Power Control 7 | W/R | 1 | * | * | * | FS1[1:0] (01) | | * | * | FS0[1:0] (00) | | |
| R22h | SRAM Write Control | W/R | 1 | SRAM Write(1111_1111) | | | | | | | | | |
| R23h | Cycle Control 1 | W/R | 1 | * | N_DC[7:0] (1101_1100) | | | | | | | | |
| R24h | Cycle Control 2 | W/R | 1 | * | PI_DC[7:0] (1101_1100) | | | | | | | | |
| R25h | Cycle Control 3 | W/R | 1 | * | I_DC[7:0] (1101_1100) | | | | | | | | |
| R26h | Display Control 1 | W/R | 1 | * | PT[1:0] (00) | | GON(1) | DTE(0) | D[1:0] (00) | | * | * | |
| R27h | Display Control 2 | W/R | 1 | * | * | * | * | * | N_BP[3:0] (4'b0010) | | | | |
| R28h | Display Control 3 | W/R | 1 | * | * | * | * | * | N_FP[3:0] (4'b0010) | | | | |
| R29h | Display Control 4 | W/R | 1 | * | * | * | * | * | PI_BP[3;0] (4'b0010) | | | | |
| R2Ah | Display Control 5 | W/R | 1 | * | * | * | * | * | PI_FP[3:0] (4'b0010) | | | | |
| R2Bh | Power Control 11 | W/R | 1 | * | * | * | PI_PRE_REFRESH[1:0] (00) | | BLANK_DIV[3:0] (0000) | | | | |
| R2Ch | Display Control 6 | W/R | 1 | * | * | * | * | * | I_BP[3:0] (4'b0010) | | | | |
| R2Dh | Display Control 7 | W/R | 1 | * | * | * | * | * | I_FP[3:0] (4'b0010) | | | | |
| R35h | Display Control 9 | W/R | 1 | * | EQS[7:0] (0001_1001) | | | | | | | | |
| R36h | Display Control 10 | W/R | 1 | * | EQP[7:0] (0001_1001) | | | | | | | | |
| R37h | Display Control 12 | W/R | 1 | * | * | * | PTG[1:0] (10) | | ISC[3:0] (0010) | | | | |
| R38h | RGB interface control 1 | W/R | 1 | * | * | * | * | RGB_EN(0) | DPL (0) | HSPL (0) | VSPL (0) | EPL (0) | |
| R39h | RGB interface control 1 | W/R | 1 | * | DOTCLK_DIV[7:0] (0000_0000) | | | | | | | | |
| R3Ah | Cycle Control 1 | W/R | 1 | * | N_RTN[3:0] (0000) | | | | * | N_NW[2:0] (001) | | | |
| R3Bh | Cycle Control 2 | W/R | 1 | * | PI_RTN[3:0] (0000) | | | | * | PI_NW[2:0] (000) | | | |
| R3Ch | Cycle Control 3 | W/R | 1 | * | I_RTN[3:0] (0000) | | | | * | I_NW[2:0] (000) | | | |
| R3Dh | Cycle Control 4 | W/R | 1 | * | * | * | DIV_I[1:0] (00) | | DIV_PI[1:0] (00) | | DIV_N[1:0] (00) | | |
| R3Eh | Cycle Control 5 | W/R | 1 | * | SON[7:0] (8'b0001_1001) | | | | | | | | |
| R40 | Cycle Control 6 | W/R | 1 | * | GDON[7:0] (8'b0000_0011) | | | | | | | | |
| R41h | Cycle Control 7 | W/R | 1 | * | GDOF[7:0] (8'b1111_1000) | | | | | | | | |
| R42h | BGP Control | W/R | 1 | * | * | * | * | VBGP_OE(0) | BGP[3:0] (1000) | | | | |
| R43h | VCOM Control 1 | W/R | 1 | * | VCOMG (0) | * | * | * | * | * | * | * | |
| R44h | VCOM Control 2 | W/R | 1 | * | * | VCM[6:0] (101_0101) | | | | | | | |
| R45h | VCOM Control 3 | W/R | 1 | * | * | * | * | VDV[4:0] (1_0000) | | | | | |
| R46h | r Control (1) | W/R | 1 | * | GSEL(1) | CP12(0) | CP11(0) | CP10(1) | * | CP02(0) | CP01(1) | CP00(1) | |
| R47h | r Control (2) | W/R | 1 | * | * | CN12(1) | CN11(0) | CN10(0) | * | CN02(1) | CN01(1) | CN00(1) | |
| R48h | r Control (3) | W/R | 1 | * | * | NP12(1) | NP11(1) | NP10(1) | * | NP02(0) | NP01(0) | NP00(0) | |
| R49h | r Control (4) | W/R | 1 | * | * | NP32(1) | NP31(0) | NP30(1) | * | NP22(1) | NP21(1) | NP20(1) | |
| R4Ah | r Control (5) | W/R | 1 | * | * | NP52(1) | NP51(1) | NP50(0) | * | NP42(0) | NP41(0) | NP40(1) | |
| R4Bh | r Control (6) | W/R | 1 | * | * | NN12(1) | NN11(1) | NN10(1) | * | NN02(1) | NN01(1) | NN00(1) | |
| R4Ch | r Control (7) | W/R | 1 | * | * | NN32(0) | NN31(1) | NN30(0) | * | NN22(1) | NN21(0) | NN20(1) | |
| R4Dh | r Control (8) | W/R | 1 | * | * | NN52(1) | NN51(1) | NN50(1) | * | NN42(0) | NN41(1) | NN40(1) | |
| R4Eh | r Control (9) | W/R | 1 | * | CGMP11 (0) | CGMP10 (0) | CGMP01 (0) | CGMP00 (0) | OP03(0) | OP02(0) | OP01(1) | OP00(1) | |
| R4Fh | r Control (10) | W/R | 1 | * | CGMP3 (0) | CGMP2 (0) | * | OP14(1) | OP13(0) | OP12(0) | P11(1) | OP10(0) | |
| R50h | r Control (11) | W/R | 1 | * | CGMN11 (0) | CGMN10 (0) | CGMN01 (0) | CGMN00 (1) | ON03(1) | ON02(0) | ON01(0) | ON00(1) | |
| R51h | r Control (12) | W/R | 1 | * | CGMN3 (0) | CGMN2 (0) | * | ON14(0) | ON13(0) | ON12(1) | ON11(1) | ON10(1) | |
| R52h | OTP Control 1 | W/R | 1 | * | OTP_MASK[7:0] (0000_0000) | | | | | | | | |
| R53h | OTP Control 2 | W/R | 1 | * | OTP_INDEX[7:0] (0000_1101) | | | | | | | | |
| R54h | OTP Control 3 | W/R | 1 | * | OTP_LOAD_DISABLE(0) | DCCLK_DISABLE (0) | OTP_POR(0) | OTP_PWE(0) | OTP_PTM (0) | 0 | VPP_SEL (0) | OTP_PROG (0) | |
| R64h | Internal Use 16 | R | 1 | * | ID1[7:0] (8'b0) | | | | | | | | |
| R65h | Internal Use 17 | W/R | 1 | * | 1 | ID2[6:0] (7'b0) | | | | | | | |
| R66h | Internal Use 18 | W/R | 1 | * | ID3[7:0] (8'b0) | | | | | | | | |

| Register No. | Register | W/R | RS | Upper Code | Lower Code | | | | | | | | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D[17:8] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| R67h | Himax ID code | R | 1 | * | HimaxID[7:0](0100_0111) | | | | | | | | |
| R70h | Internal Use 28 | W/R | 1 | * | * | GS (0) | SS (0) | TEMODE(0) | TEON (0) | CSEL[2:0] (110) | | | |
| R72h | Data control | | | | * | * | DFM[1:0] (00) | | * | * | TRI [1:0] (00) | | |
| R90h | Display Control 8 | W/R | 1 | * | SAP[7:0] (0000_1010) | | | | | | | | |
| R91h | Display Control 11 | W/R | 1 | * | GEN_OFF[7:0] (0001_0100) | | | | | | | | |
| R93h | OSC Control 3 | W/R | 1 | * | * | * | * | * | RADJ[3:0] (1111) | | | | |
| R94h | SAP Idle mode | W/R | 1 | * | SAP_I[7:0]( 0000_0010) | | | | | | | | |
| R95h | DCCLK SYNC TO CL1 | W/R | 1 | * | * | * | * | * | * | * | * | DCCLK_SYNC (0) | |

## 6.2 Index Register

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 0 | * | * | * | * | * | * | * | * | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

**Figure 6. 1 Index Register**

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID7-0) in the range from 000000b to 1111111b in binary form.

## 6.3 Display Mode Control Register (R01h)

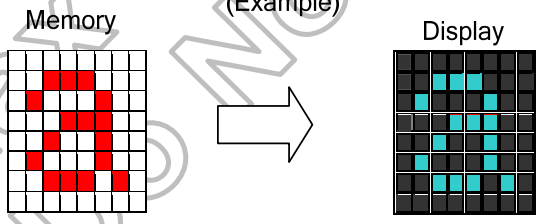
| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | IDMON (0) | INVON (0) | NORON (1) | PTLON (0) |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | IDMON (0) | INVON (0) | NORON (1) | PTLON (0) |

**Figure 6. 2 Display Mode Control Register (R01h)**

**IDMON:**
This command is used for turning on/off IDLE (8-color display) mode by setting IDMON=1/0.

**INVON:**
This command is used to enter into display inversion mode by setting INVON=1. Vise versa, it recovers from display inversion mode by setting INVON=0. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.

(Example)




**NORON:**
This command is used for turning on/off NORMAL mode by setting NORON=1/0.

**PTLON:**
This command is used for turning on/off PARTIAL mode by setting PTLON=1/0.

## 6.4 Column Address Start Register (R02~03h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SC 15 | SC 14 | SC 13 | SC 12 | SC 11 | SC 10 | SC9 | SC8 |
| R | 1 | * | * | * | * | * | * | * | * | SC 15 | SC 14 | SC 13 | SC 12 | SC 11 | SC 10 | SC9 | SC8 |

**Figure 6. 3 Column Address Start Register Upper Byte (R02h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 |
| R | 1 | * | * | * | * | * | * | * | * | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 |

**Figure 6. 4 Column Address Start Register Low Byte (R03h)**

## 6.5 Column Address End Register (R04~05h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EC 15 | EC 14 | EC 13 | EC 12 | EC 11 | EC 10 | EC9 | EC8 |
| R | 1 | * | * | * | * | * | * | * | * | EC 15 | EC 14 | EC 13 | EC 12 | EC 11 | EC 10 | EC9 | EC8 |

**Figure 6. 5 Column Address End Register Upper Byte (R04h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| R | 1 | * | * | * | * | * | * | * | * | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |

**Figure 6. 6 Column Address End Register Low Byte (R05h)**

## 6.6 Row Address Start Register (R06~07h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SP 15 | SP 14 | SP 13 | SP 12 | SP 11 | SP 10 | SP9 | SP8 |
| R | 1 | * | * | * | * | * | * | * | * | SP 15 | SP 14 | SP 13 | SP 12 | SP 11 | SP 10 | SP9 | SP8 |

**Figure 6. 7 Row Address Start Register Upper Byte (R06h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |
| R | 1 | * | * | * | * | * | * | * | * | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |

**Figure 6. 8 Row Address Start Register Low Byte (R07h)**

## 6.7 Row Address End Register (R08~09h)

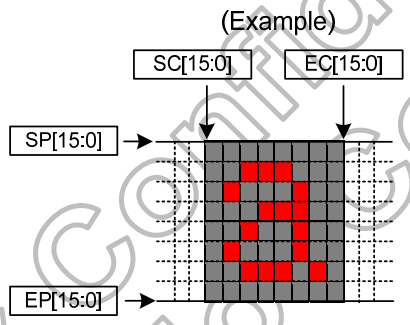
| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EP 15 | EP 14 | EP 13 | EP 12 | EP 11 | EP 10 | EP9 | EP8 |
| R | 1 | * | * | * | * | * | * | * | * | EP 15 | EP 14 | EP 13 | EP 12 | EP 11 | EP 10 | EP9 | EP8 |

**Figure 6. 9 Row Address End Register Upper Byte (R08h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 |
| R | 1 | * | * | * | * | * | * | * | * | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 |

**Figure 6. 10 Row Address End Register Low Byte (R09h)**

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. These commands make no change on the other driver status. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.




## 6.8 Partial Area Start Row Register (R0A~0Bh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PSL 15 | PSL 14 | PSL 13 | PSL 12 | PSL 11 | PSL 10 | PSL 9 | PSL 8 |
| R | 1 | * | * | * | * | * | * | * | * | PSL 15 | PSL 14 | PSL 13 | PSL 12 | PSL 11 | PSL 10 | PSL 9 | PSL 8 |

**Figure 6. 11 Partial Area Start Row Register Upper Byte (R0Ah)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PSL 7 | PSL 6 | PSL 5 | PSL 4 | PSL 3 | PSL 2 | PSL 1 | PSL 0 |
| R | 1 | * | * | * | * | * | * | * | * | PSL 7 | PSL 6 | PSL 5 | PSL 4 | PSL 3 | PSL 2 | PSL 1 | PSL 0 |

**Figure 6. 12 Partial Area Start Row Register Low Byte (R0Bh)**

## 6.9 Partial Area End Row Register (R0C~0Dh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PEL 15 | PEL 14 | PEL 13 | PEL 12 | PEL 11 | PEL 10 | PEL 9 | PEL 8 |
| R | 1 | * | * | * | * | * | * | * | * | PEL 15 | PEL 14 | PEL 13 | PEL 12 | PEL 11 | PEL 10 | PEL 9 | PEL 8 |

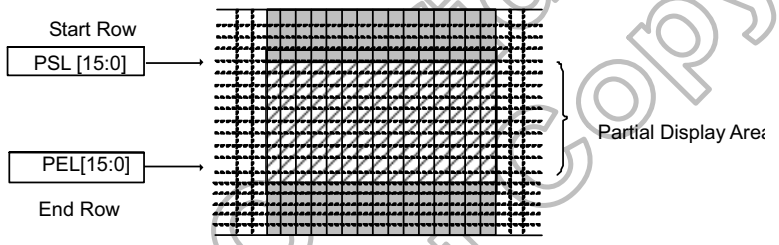
**Figure 6. 13 Partial Area End Row Register Upper Byte (R0Ch)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PEL 7 | PEL 6 | PEL 5 | PEL 4 | PEL 3 | PEL 2 | PEL 1 | PEL 0 |
| R | 1 | * | * | * | * | * | * | * | * | PEL 7 | PEL 6 | PEL 5 | PEL 4 | PEL 3 | PEL 2 | PEL 1 | PEL 0 |

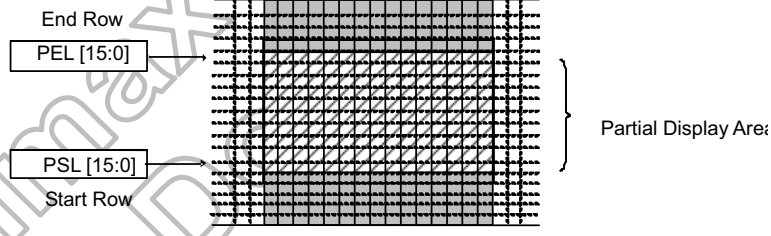
**Figure 6. 14 Partial Area End Row Register Low Byte (R0Dh)**

These commands (R0Ah~~0Dh) define the partial mode's display area. There are 4 parameters associated with this command, PSL[15:0], PEL[15:0], as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

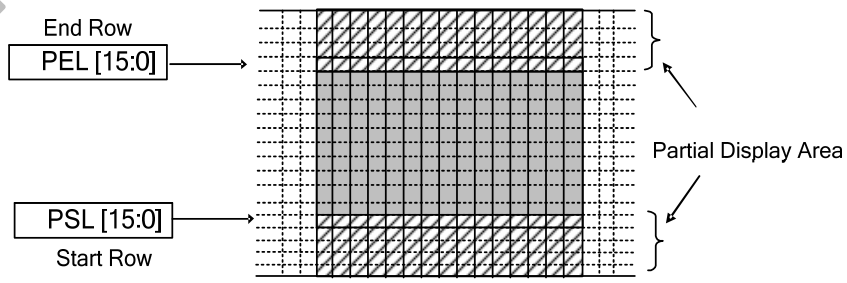
If End Row>Start Row when GS=0




If End Row>Start Row when GS=1




If End Row<Start Row when GS=0




If End Row = Start Row then the Partial Area will be one row deep.

## 6.10 Vertical Scroll Top Fixed Area Register (R0E~0Fh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | TFA 15 | TFA 14 | TFA 13 | TFA 12 | TFA 11 | TFA 10 | TFA 9 | TFA 8 |
| R | 1 | * | * | * | * | * | * | * | * | TFA 15 | TFA 14 | TFA 13 | TFA 12 | TFA 11 | TFA 10 | TFA 9 | TFA 8 |

**Figure 6. 15 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | TFA 7 | TFA 6 | TFA 5 | TFA 4 | TFA 3 | TFA 2 | TFA 1 | TFA 0 |
| R | 1 | * | * | * | * | * | * | * | * | TFA 7 | TFA 6 | TFA 5 | TFA 4 | TFA 3 | TFA 2 | TFA 1 | TFA 0 |

**Figure 6. 16 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh)**

## 6.11 Vertical Scroll Height Area Register (R10~11h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | VSA 15 | VSA 14 | VSA 13 | VSA 12 | VSA 11 | VSA 10 | VSA 9 | VSA 8 |
| R | 1 | * | * | * | * | * | * | * | * | VSA 15 | VSA 14 | VSA 13 | VSA 12 | VSA 11 | VSA 10 | VSA 9 | VSA 8 |

**Figure 6. 17 Vertical Scroll Height Area Register Upper Byte (R10h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | VSA 7 | VSA 6 | VSA 5 | VSA 4 | VSA 3 | VSA 2 | VSA 1 | VSA 0 |
| R | 1 | * | * | * | * | * | * | * | * | VSA 7 | VSA 6 | VSA 5 | VSA 4 | VSA 3 | VSA 2 | VSA 1 | VSA 0 |

**Figure 6. 18 Vertical Scroll Height Area Register Low Byte (R11h)**

## 6.12 Vertical Scroll Button Fixed Area Register (R12~13h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | BFA 15 | BFA 14 | BFA 13 | BFA 12 | BFA 11 | BFA 10 | BFA 9 | BFA 8 |
| R | 1 | * | * | * | * | * | * | * | * | BFA 15 | BFA 14 | BFA 13 | BFA 12 | BFA 11 | BFA 10 | BFA 9 | BFA 8 |

**Figure 6. 19 Vertical Scroll Button Fixed Area Register Upper Byte (R12h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | BFA 7 | BFA 6 | BFA 5 | BFA 4 | BFA 3 | BFA 2 | BFA 1 | BFA 0 |
| R | 1 | * | * | * | * | * | * | * | * | BFA 7 | BFA 6 | BFA 5 | BFA 4 | BFA 3 | BFA 2 | BFA 1 | BFA 0 |

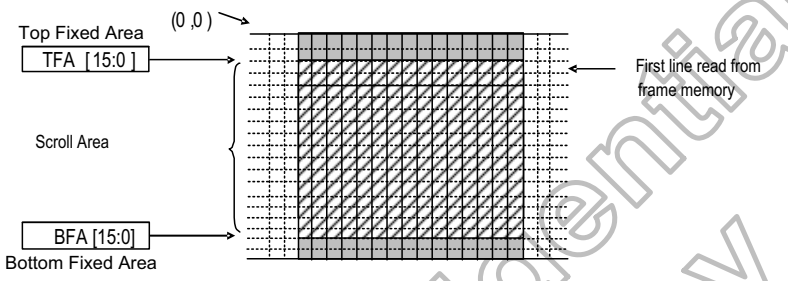
**Figure 6. 20 Vertical Scroll Button Fixed Area Register Low Byte (R13h)**

These commands (R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display. When GS=0,

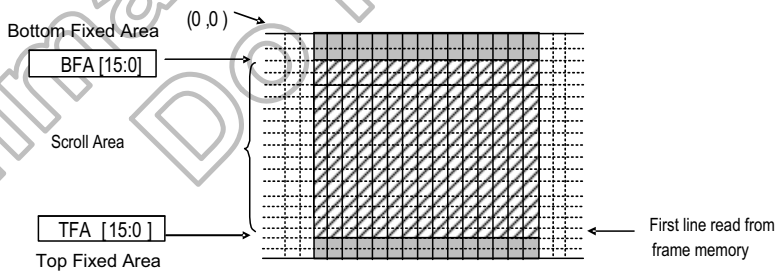
**TFA[15..0]** describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

**VSA[15..0]** describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

**BFA[15..0]** describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer.




When GS=1,
**TFA[15..0]** describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
**VSA[15..0]** describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
**BFA[15..0]** describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



## 6.13 Vertical Scroll Start Address Register (R14~15h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | VSP 15 | VSP 14 | VSP 13 | VSP 12 | VSP 11 | VSP 10 | VSP 9 | VSP 8 |
| R | 1 | * | * | * | * | * | * | * | * | VSP 15 | VSP 14 | VSP 13 | VSP 12 | VSP 11 | VSP 10 | VSP 9 | VSP 8 |

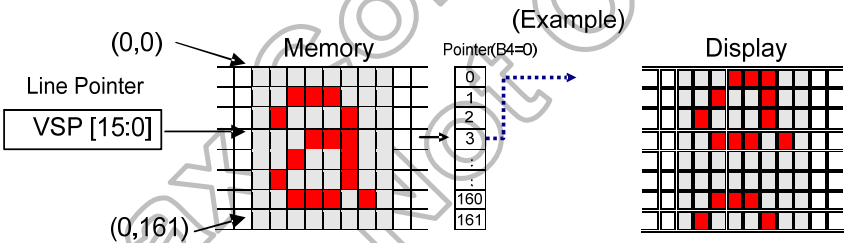
**Figure 6. 21 Vertical Scroll Start Address Register Upper Byte (R14h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | VSP 7 | VSP 6 | VSP 5 | VSP 4 | VSP 3 | VSP 2 | VSP 1 | VSP 0 |
| R | 1 | * | * | * | * | * | * | * | * | VSP 7 | VSP 6 | VSP 5 | VSP 4 | VSP 3 | VSP 2 | VSP 1 | VSP 0 |

**Figure 6. 22 Vertical Scroll Start Address Register Low Byte (R15h)**

This command is used together with Vertical Scrolling Definition (18h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When GS=0

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3




When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
VSP refers to the Frame Memory line Pointer.

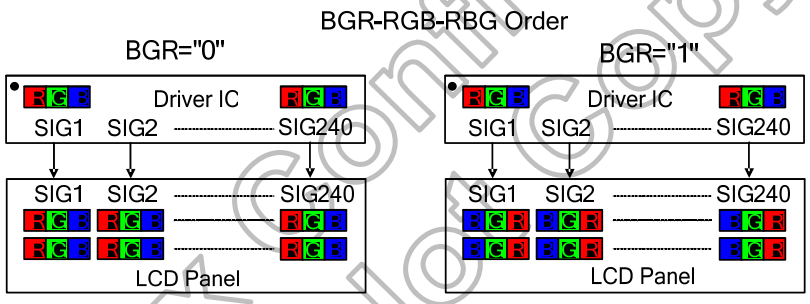
## 6.14 Memory Access Control Register (R16h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | MY | MX | MV | * | BGR | * | * | * |
| R | 1 | * | * | * | * | * | * | * | * | MY | MX | MV | * | BGR | * | * | * |

**Figure 6. 23 Memory Access Control Register (R16h)**

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

| Bit | Name | Description |
|---|---|---|
| **MY** | PAGE ADDRESS ORDER | These 3 bits controls MCU to memory write/read direction. “MCU to memory write/read direction” |
| **MX** | COLUMN ADDRESS ORDER | |
| **MV** | PAGE/COLUMN SELECTION | |
| **BGR** | RGB-BGR ORDER | Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) |



## 6.15 Gate scan Control Register (R18h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | SCROLL_ON | SM (0) |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | SCROLL_ON | SM (0) |

**Figure 6. 24 Gate Scan Control Register (R18h)**

**SCROLL_ON:** Vertical Scrolling Function enable, High active.

**SM:** Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin

## 6.16 OSC Control 1 Register (R19h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | CADJ3 | CADJ2 | CADJ1 | CADJ0 | CUADJ2 | CUADJ1 | CUADJ0 | OSC_EN |
| R | 1 | * | * | * | * | * | * | * | * | CADJ3 | CADJ2 | CADJ1 | CADJ0 | CUADJ2 | CUADJ1 | CUADJ0 | OSC_EN |

**Figure 6. 25 OSC Control 1 Register (R19h)**

This command is used to set internal oscillator related setting
**OSC_EN**: Enable internal oscillator, High active
**CADJ[3:0], CUADJ[2:0]:** Internal oscillator frequency adjust, default is 5.58MHz

| CUADJ2 | CUADJ1 | CUADJ0 | Current |
|---|---|---|---|
| 0 | 0 | 0 | 85% |
| 0 | 0 | 1 | 90% |
| 0 | 1 | 0 | 95% |
| 0 | 1 | 1 | 100% |
| 1 | 0 | 0 | 105% |
| 1 | 0 | 1 | 110% |
| 1 | 1 | 0 | 115% |
| 1 | 1 | 1 | 120% |

| CADJ3 | CADJ2 | CADJ1 | CADJ0 | CAP |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 116% |
| 0 | 0 | 0 | 1 | 114% |
| 0 | 0 | 1 | 0 | 112% |
| 0 | 0 | 1 | 1 | 110% |
| 0 | 1 | 0 | 0 | 108% |
| 0 | 1 | 0 | 1 | 106% |
| 0 | 1 | 1 | 0 | 104% |
| 0 | 1 | 1 | 1 | 102% |
| 1 | 0 | 0 | 0 | 100% |
| 1 | 0 | 0 | 1 | 98% |
| 1 | 0 | 1 | 0 | 96% |
| 1 | 0 | 1 | 1 | 94% |
| 1 | 1 | 0 | 0 | 92% |
| 1 | 1 | 0 | 1 | 90% |
| 1 | 1 | 1 | 0 | 88% |
| 1 | 1 | 1 | 1 | 86% |

## 6.17 OSC Control Register 2 (R1Ah)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | OSC_TEST |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | OSC_TEST |

**Figure 6. 26 OSC Control Register 2 (R1Ah)**

**OSC_TEST**: If OSC is fed from OSC pin, please set OSC_TEST to 1

## 6.18 Power Control 1 Register (R1Bh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | GAS ENB | * | * | PON | DK | XDK | VLCD_TRI | STB |
| R | 1 | * | * | * | * | * | * | * | * | GAS ENB | * | * | PON | DK | XDK | VLCD_TRI | STB |

**Figure 6. 27 Power Control 1 Register (R1Bh)**

**GASENB:** This stands for abnormal power-off supervisal function when the power is off. It's for monitoring power status by NISD pad when GASENB is set to 0.

**PON:** Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation. For detail, see the Power Supply Setting Sequence.

| PON | Operation of step-up circuit 2 |
|---|---|
| 0 | OFF |
| 1 | ON |

**DK:** Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

| DK | Operation of step-up circuit 1 |
|---|---|
| 0 | ON |
| 1 | OFF |

**STB:** When STB = "1", the HX8347-A01 into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

**XDK, VLCD_TRI:** Specify the ratio of step-up circuit for DDVDH voltage generation.

| VLCD_TRI | XDK | Step up circuit 1 | Capacitor connection pins |
|---|---|---|---|
| 0 | 0 | 2 x VCI | C11A, C11B |
| 0 | 1 | 2 x VCI | C11A, C11B, CX11A, CX11B |
| 1 | 0 | 3 x VCI | C11A, C11B, CX11A, CX11B |
| 1 | 1 | Setting inhabited | Setting inhabited |

## 6.19 Power Control 2 Register (R1Ch)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | AP2 | AP1 | AP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | AP2 | AP1 | AP0 |

**Figure 6. 28 Power Control 3 Register (R1Ch)**

**AP(2-0)**

Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption, AP(2-0) can be set as "000" when display is off, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

| AP2 | AP1 | AP0 | Constant Current of Operational Amplifier |
|---|---|---|---|
| 0 | 0 | 0 | Power Circuit Off |
| 0 | 0 | 1 | Ignore |
| 0 | 1 | 0 | Ignore |
| 0 | 1 | 1 | Ignore |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1.25 |
| 1 | 1 | 0 | 1.5 |
| 1 | 1 | 1 | Ignore |

## 6.20 Power Control 3 Register (R1Dh)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | VC12 | VC11 | VC10 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | VC12 | VC11 | VC10 |

**Figure 6. 29 Power Control 3 Register (R1Dh)**

**VC1(2-0):**
Specify the ratio of VBGP for DDVDH voltage adjusting.

| VC12 | VC11 | VC10 | DDVDH |
|---|---|---|---|
| 0 | 0 | 0 | VBGP * 5.47 |
| 0 | 0 | 1 | VBGP * 5.13 |
| 0 | 1 | 0 | VBGP * 4.82 |
| 0 | 1 | 1 | VBGP * 4.56 |
| 1 | 0 | 0 | VBGP * 4.32 |
| 1 | 0 | 1 | VBGP * 4.10 |
| 1 | 1 | 0 | VBGP * 3.91 |
| 1 | 1 | 1 | VBGP * 3.73 |

**Note:** 1. VBGP is the internal reference voltage equals to 1.25V
2. When VLCD_TRI=1, DDVDH ≦ ( 3xVCI - 0.5V)
3. When VLCD_TRI=0, DDVDH ≦ ( 2xVCI - 0.5V)

## 6.21 Power Control 4 Register (R1Eh)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | VC32 | VC31 | VC30 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | VC32 | VC31 | VC30 |

**Figure 6. 30 VREG3 Control Register (R1Eh)**

**VC3(2-0):**
Specify the reference voltage VREG3 (the factor of VCI) for VGL voltage adjusting

| VC32 | VC31 | VC30 | VREG3 |
|---|---|---|---|
| 0 | 0 | 0 | DDVDH |
| 0 | 0 | 1 | 2 X VCI |
| 0 | 1 | 0 | 1.92 X VCI |
| 0 | 1 | 1 | 1.84 X VCI |
| 1 | 0 | 0 | 1.76 X VCI |
| 1 | 0 | 1 | 1.68 X VCI |
| 1 | 1 | 0 | 1.60 X VCI |
| 1 | 1 | 1 | HZ |

## 6.22 Power Control 5 Register (R1Fh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | VRH 3 | VRH 2 | VRH 1 | VRH 0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | VRH 3 | VRH 2 | VRH 1 | VRH 0 |

**Figure 6. 31 Power Control 5 Register (R1Fh)**

**VRH(3-0):**
Set the magnification of amplification for VREG1 voltage for gamma voltage setting. It allows magnify the amplification of VBGP from 2.8 to 4.8 times.

| VRH3 | VRH2 | VRH1 | VRH0 | VREG1 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VBGPx 2.8 |
| 0 | 0 | 0 | 1 | VBGP x 3.0 |
| 0 | 0 | 1 | 0 | VBGP x 3.2 |
| 0 | 0 | 1 | 1 | VBGP x 3.3 |
| 0 | 1 | 0 | 0 | VBGP x 3.4 |
| 0 | 1 | 0 | 1 | VBGP x 3.5 |
| • • | • • | • • | • • | • • |
| 1 | 0 | 0 | 1 | VBGP x 3.9 |
| 1 | 0 | 1 | 0 | VBGPx 4.0 |
| 1 | 0 | 1 | 1 | VBGPx 4.2 |
| 1 | 1 | 0 | 0 | VBGPx 4.4 |
| 1 | 1 | 0 | 1 | VBGPx 4.6 |
| 1 | 1 | 1 | 0 | VBGPx 4.8 |
| 1 | 1 | 1 | 1 | Inhibited |

**Note:** 1. VBGP is the internal reference voltage equals to 1.25V
2. VREG1 ≦ (DDVDH – 0.5V).

## 6.23 Power Control 6 Register (R20h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | BT3 | BT2 | BT1 | BT0 | * | * | * | * |
| R | 1 | * | * | * | * | * | * | * | * | BT3 | BT2 | BT1 | BT0 | * | * | * | * |

**Figure 6. 32 Power Control 6 Register (R20h)**

**BT(3-0):**
Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

| BT3 | BT2 | BT1 | BT0 | VCL | VGH | VGL | | Capacitor Connection Pins |
|---|---|---|---|---|---|---|---|---|
| | | | | | | VCOMG=1 | VCOMG=0 | |
| 0 | 0 | 0 | 0 | -1 x VCI | VREG3X3 [x 6] | -(VREG3X2)+VCL [x -5] | -(VREG3X2) [x -4] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 0 | 0 | 1 | -1 x VCI | VREG3X3 [x 6] | -(VREG3X2) [x -4] | -(VREG3X2) [x -4] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 0 | 1 | 0 | -1 x VCI | VREG3X3 [x 6] | -(VREG3x2)+VCI [x -3] | -(VREG3x2)+VCI [x -3] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 0 | 1 | 1 | -1 x VCI | VREG3X2+VCI [x 5] | -(VREG3X2)+VCL [x -5] | -(VREG3X2) [x -4] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 1 | 0 | 0 | -1 x VCI | VREG3X2+VCI [x 5] | -(VREG3X2) [x -4] | -(VREG3X2) [x -4] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 1 | 0 | 1 | -1 x VCI | VREG3X2+VCI [x 5] | -(VREG3x2)+VCI [x -3] | -(VREG3x2)+VCI [x -3] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| 0 | 1 | 1 | 0 | -1 x VCI | VREG3X2 [x 4] | -(VREG3X2) [x -4] | -(VREG3X2) [x -4] | VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B |
| Other setting | | | | Inhibited | | | | |

**Note:** 1. The conditions of VLCD ≦ 6V, VCL ≦ -3.3V, VGH-VGL ≦ 32V must be satisfied.
2. If VCOMG=0, VCL output is float.

## 6.24 Power Control 7 Register (R21h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | | FS11 | FS10 | * | | FS01 | FS00 |
| R | 1 | * | * | * | * | * | * | * | * | * | | FS11 | FS10 | * | | FS01 | FS00 |

**Figure 6. 33 Power Control 7 Register (R21h)**

**FS0(1-0):**

Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

| FS01 | FS0 | Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1 |
|---|---|---|
| 0 | 0 | DCDCf / 1 |
| 0 | 1 | DCDCf / 2 |
| 1 | 0 | DCDCf / 4 |
| 1 | 1 | DCDCf / 8 |

**FS1(1-0):**

Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL, VCL voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

| FS11 | FS10 | Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3 |
|---|---|---|
| 0 | 0 | DCDCf / 1 |
| 0 | 1 | DCDCf / 2 |
| 1 | 0 | DCDCf / 4 |
| 1 | 1 | DCDCf / 8 |

**Note:** Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

## 6.25 Read Data Register (R22h)

| R/W | RS | RB17 | RB16 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 1 | RD17 | RD16 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 |

**Figure 6. 34 Read Data Register (R22h)**

**RD17-0:** Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

### Write Data Register (R22h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | WD15 | WD14 | WD13 | WD12 | WD11 | WD10 | WD9 | WD8 | WD7 | WD6 | WD5 | WD4 | WD3 | WD2 | WD1 | WD0 |

**Figure 6. 35 Write Data Register (R22h)**

**WD[15:0] :** Transforms the data into 16-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

## 6.26 Cycle Control 1~3 Register (R23~25h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | N_DC7 | N_DC6 | N_DC5 | N_DC4 | N_DC3 | N_DC2 | N_DC1 | N_DC0 |
| R | 1 | * | * | * | * | * | * | * | * | N_DC7 | N_DC6 | N_DC5 | N_DC4 | N_DC3 | N_DC2 | N_DC1 | N_DC0 |

**Figure 6. 36 Cycle Control 1 Register (R23h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PI_DC7 | PI_DC6 | PI_DC5 | PI_DC4 | PI_DC3 | PI_DC2 | PI_DC1 | PI_DC0 |
| R | 1 | * | * | * | * | * | * | * | * | PI_DC7 | PI_DC6 | PI_DC5 | PI_DC4 | PI_DC3 | PI_DC2 | PI_DC1 | PI_DC0 |

**Figure 6. 37 Cycle Control 2 Register (R24h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | I_DC7 | I_DC6 | I_DC5 | I_DC4 | I_DC3 | I_DC2 | I_DC1 | I_DC0 |
| R | 1 | * | * | * | * | * | * | * | * | I_DC7 | I_DC6 | I_DC5 | I_DC4 | I_DC3 | I_DC2 | I_DC1 | I_DC0 |

**Figure 6. 38 Cycle Control 3 Register (R25h)**

**N_DC:** Normal mode
**PI_DC:** Partial mode + Idle mode
**I_DC:** Idle mode

**DC(7-0):** specify the clock frequency for DC/DC converter operating.

fosc = R-C oscillation frequency

| DC7 | DC6 | DC5 | DC4 | DC3 | DC2 | DC1 | DC0 | DCDCf |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Inhibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | fosc |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | fosc/ 2 |
| | | | | • | | | | • |
| | | | | • | | | | • |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | fosc/ 254 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | fosc / 255 |

**Note:** It is recommended to set DC(7-0) as "20"h, which means one charge bump clock periodis 32 internal oscillation clocks.

## 6.27 Display Control 1 Register (R26h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PT1 | PT0 | GON | DTE | D1 | D0 | * | * |
| R | 1 | * | * | * | * | * | * | * | * | PT1 | PT0 | GON | DTE | D1 | D0 | * | * |

**Figure 6. 39 Display Control 1 Register (R26h)**

**D[1:0]:** When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8347-A01 can control the charging current for the LCD with AC driving. When D1–0 = 01, the internal display of the HX8347-A01 is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

**GON, DTE:**

| GON | DTE | Gate Output |
|---|---|---|
| 0 | X | VGH |
| 1 | 0 | VGL |
| 1 | 1 | VGH/VGL |

**PT[1:0] :** Non-display area source output control see follow table

| INVON /REV_PANEL | GRAM Data | Source Output Level | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Display area | | Non-display Area | | | | | |
| | | | | PT1-0=(0,*) | | PT1-0=(1,0) | | PT1-0=(1,1) | |
| | | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" | VCOM = "L" | VCOM = "H" |
| 0 | 18'h00000<br>.<br>.<br>18'h3FFFF | V63<br>.<br>.<br>V0 | V0<br>.<br>.<br>V63 | V63 | V0 | VSSD | VSSD | Hi-z | Hi-z |
| 1 | 18'h00000<br>.<br>.<br>18'h3FFFF | V0<br>.<br>.<br>V63 | V63<br>.<br>.<br>V0 | V63 | V0 | VSSD | VSSD | Hi-z | Hi-z |

## 6.28 Display Control 2~7 Register (R27h~R2Ah, R2Ch, R2Dh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | N_BP3 | N_BP2 | N_BP1 | N_BP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | N_BP3 | N_BP2 | N_BP1 | N_BP0 |

Figure 6. 40 Display Control 2 Register (R27h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | N_BP3 | N_BP2 | N_BP1 | N_BP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | N_BP3 | N_BP2 | N_BP1 | N_BP0 |

Figure 6. 41 Display Control 3 Register (R28h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | PI_BP3 | PI_BP2 | PI_BP1 | PI_BP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | PI_BP3 | PI_BP2 | PI_BP1 | PI_BP0 |

Figure 6. 42 Display Control 4 Register (R29h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | PI_FP3 | PI_FP2 | PI_FP1 | PI_FP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | PI_FP3 | PI_FP2 | PI_FP1 | PI_FP0 |

Figure 6. 43 Display Control 5 Register (R2Ah)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | I_BP3 | I_BP2 | I_BP1 | I_BP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | I_BP3 | I_BP2 | I_BP1 | I_BP0 |

Figure 6. 44 Display Control 6 Register (R2Ch)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | I_FP3 | I_FP2 | I_FP1 | I_FP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | I_FP3 | I_FP2 | I_FP1 | I_FP0 |

Figure 6. 45 Display Control 7 Register (R2Dh)

**N_BP, N_FP:** Back Porch and Front Porch setting in Normal mode
**PI_BP, PI_FP:** Back Porch and Front Porch setting in Partial mode + Idle mode
**I_BP, P_FP:** Back Porch and Front Porch setting in Idle mode

**FP[3:0]:** Specify the amount of scan line for front porch (FP).
**BP[3:0]:** Specify the amount of scan line for back porch (BP).

| FP3 | FP2 | FP1 | FP0 | Number of FP Line | Number of BP Line |
|---|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | | |
| 0 | 0 | 0 | 0 | Ignore | |
| 0 | 0 | 0 | 1 | Ignore | |
| 0 | 0 | 1 | 0 | 2 lines | |
| 0 | 0 | 1 | 1 | 3 lines | |
| 0 | 1 | 0 | 0 | 4 lines | |
| 0 | 1 | 0 | 1 | 5 lines | |
| 0 | 1 | 1 | 0 | 6 lines | |
| 0 | 1 | 1 | 1 | 7 lines | |
| 1 | 0 | 0 | 0 | 8 lines | |
| 1 | 0 | 0 | 1 | 9 lines | |
| 1 | 0 | 1 | 0 | 10 lines | |
| 1 | 0 | 1 | 1 | 11 lines | |
| 1 | 1 | 0 | 0 | 12 lines | |
| 1 | 1 | 0 | 1 | 13 lines | |
| 1 | 1 | 1 | 0 | 14 lines | |
| 1 | 1 | 1 | 1 | Ignore | |

| Operation Mode | BP | FP | BP + FP |
|---|---|---|---|
| **System Interface** | ≥2 lines | ≥2 lines | ≤ 16 lines |

## 6.29 Power Control 11 Register (R2Bh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | PI_PRE_REFRESH1 | PI_PRE_REFRESH0 | BLANK_DIV3 | BLANK_DIV2 | BLANK_DIV1 | BLANK_DIV0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | PI_PRE_REFRESH1 | PI_PRE_REFRESH0 | BLANK_DIV3 | BLANK_DIV2 | BLANK_DIV1 | BLANK_DIV0 |

**Figure 6. 46 Power Control 11 Register (R2Bh)**

**PI_PRE_PEFRESH:** Internal used, not open.

**BLANK_DIV:** Internal used, not open.

## 6.30 Display Control 9 Register (R35h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EQS 7 | EQS 6 | EQS 5 | EQS 4 | EQS 3 | EQS 2 | EQS 1 | EQS 0 |
| R | 1 | * | * | * | * | * | * | * | * | EQS 7 | EQS 6 | EQS 5 | EQS 4 | EQS 3 | EQS 2 | EQS 1 | EQS 0 |

**Figure 6. 47 Display Control 9 Register (R35h)**

**EQS[7:0] :** Internal used and Not open.

## 6.31 Display Control 10 Register (R36h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | EQP 7 | EQP 6 | EQP 5 | EQP 4 | EQP 3 | EQP 2 | EQP 1 | EQP 0 |
| R | 1 | * | * | * | * | * | * | * | * | EQP 7 | EQP 6 | EQP 5 | EQP 4 | EQP 3 | EQP 2 | EQP 1 | EQP 0 |

**Figure 6. 48 Display Control 9 Register (R36h)**

**EQP[7:0] :** Internal used and Not open.

## 6.32 Display Control 12 Register (R37h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | PTG 1 | PTG 0 | ISC 3 | ISC 2 | ISC 1 | ISC 0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | PTG 1 | PTG 0 | ISC 3 | ISC 2 | ISC 1 | ISC 0 |

**Figure 6. 49 Display Control 6 Register (R37h)**

**PTG[1:0]:** Specify the scan mode of gate driver in non-display area.

| PTG1 | PTG0 | Gate Outputs in Non-display Area |
|---|---|---|
| 0 | 0 | Normal Drive |
| 0 | 1 | Fixed VGL |
| 1 | 0 | Interval scan |
| 1 | 1 | Ignore |

**ISC[3:0] :**Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

| ISC3 | ISC2 | ISC1 | ISC0 | Scan Cycle | $f_{FLM}$ = 70Hz |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 frame | - |
| 0 | 0 | 0 | 1 | 3 frames | 50 ms |
| 0 | 0 | 1 | 0 | 5 frames | 84 ms |
| 0 | 0 | 1 | 1 | 7 frames | 117 ms |
| 0 | 1 | 0 | 0 | 9 frames | 150 ms |
| 0 | 1 | 0 | 1 | 11 frames | 184 ms |
| 0 | 1 | 1 | 0 | 13 frames | 217 ms |
| 0 | 1 | 1 | 1 | 15 frames | 251 ms |
| 1 | 0 | 0 | 0 | 17 frames | 284 ms |
| 1 | 0 | 0 | 1 | 19 frames | 317 ms |
| 1 | 0 | 1 | 0 | 21 frames | 351 ms |
| 1 | 0 | 1 | 1 | 23 frames | 384 ms |
| 1 | 1 | 0 | 0 | 25 frames | 418 ms |
| 1 | 1 | 0 | 1 | 27 frames | 451 ms |
| 1 | 1 | 1 | 0 | 29 frames | 484 ms |
| 1 | 1 | 1 | 1 | 31 frames | 518 ms |

## 6.33 RGB Interface Control 1 Register (R38h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | RGB_EN | DPL | HSPL | VSPL | EPL |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | RGB_EN | DPL | HSPL | VSPL | EPL |

**Figure 6. 50 RGB Interface Control 1 Register (R38h)**

This command is used to set RGB interface related register

**EPL:** Specify the polarity of Enable pin in RGB interface mode. EPL=0, the Enable is High active; EPL=1, the Enable is Low active

**VSPL:** The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

**HSPL:** The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

**DPL:** The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

## 6.34 RGB Interface Control 2 Register (R39h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | DOTCLK_DIV7 | DOTCLK_DIV6 | DOTCLK_DIV5 | DOTCLK_DIV4 | DOTCLK_DIV3 | DOTCLK_DIV2 | DOTCLK_DIV1 | DOTCLK_DIV0 |
| R | 1 | * | * | * | * | * | * | * | * | DOTCLK_DIV7 | DOTCLK_DIV6 | DOTCLK_DIV5 | DOTCLK_DIV4 | DOTCLK_DIV3 | DOTCLK_DIV2 | DOTCLK_DIV1 | DOTCLK_DIV0 |

**Figure 6. 51 RGB Interface Control 2 Register (R39h)**

**DOTCLK_DIV[7:0]:** Internal used, not open.

## 6.35 Cycle Control 1~3 Register (R3A~3Ch)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | N_RTN3 | N_RTN2 | N_RTN1 | N_RTN0 | * | N_NW2 | N_NW1 | N_NW0 |
| R | 1 | * | * | * | * | * | * | * | * | N_RTN3 | N_RTN2 | N_RTN1 | N_RTN0 | * | N_NW2 | N_NW1 | N_NW0 |

**Figure 6. 52 Cycle Control 1 Register (R3Ah)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | PI_RTN3 | PI_RTN2 | PI_RTN1 | PI_RTN0 | * | PI_NW2 | PI_NW1 | PI_NW0 |
| R | 1 | * | * | * | * | * | * | * | * | PI_RTN3 | PI_RTN2 | PI_RTN1 | PI_RTN0 | * | PI_NW2 | PI_NW1 | PI_NW0 |

**Figure 6. 53 Cycle Control 2 Register (R3Bh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | I_RTN3 | I_RTN2 | I_RTN1 | I_RTN0 | * | I_NW2 | I_NW1 | I_NW0 |
| R | 1 | * | * | * | * | * | * | * | * | I_RTN3 | I_RTN2 | I_RTN1 | I_RTN0 | * | I_NW2 | I_NW1 | I_NW0 |

**Figure 6. 54 Cycle Control 3 Register (R3Ch)**

The driver IC support individual inversion type and clock per line for Normal display mode, Partial display mode and Idle (8-color) display mode. The resultant NW and RTN will be selected automatically according display mode.
**N_ NW, N_ RTN:** Normal mode
**PI_ NW , PI_ RTN:** Partial mode + Idle mode
**I_ NW, I_ RTN:** Idle mode

**NW[2:0]**: Frame Inversion and N-line inversion control for normal display mode.

| NW[2:0] | Inversion Type |
|---|---|
| 0 | Frame inversion |
| 1 | 1-line inversion |
| 2 | 2-line inversion |
| 3 | 3-line inversion |
| .. | .. |
| 7 | 7-line inversion |

**RTN[3:0]:** Set the 1-line period in a clock unit for normal display mode.

Clock cycles=1/internal operation clock frequency

| RTN[3:0] | Clock Cycles per Line |
|---|---|
| 4'b0000 | 245 |
| 4'b0001 | 246 |
| 4'b0010 | 247 |
| 4'b0011 | 248 |
| …. | …. |
| 4'b1110 | 259 |
| 4'b1111 | 260 |

## 6.36 Cycle Control 4 Register (R3Dh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | DIV_I1 | DIV_I0 | DIV_PI1 | DIV_PI0 | DIV 1 | DIV 0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | DIV_1 | DIV_I0 | DIV_PI1 | DIV_PI0 | DIV 1 | DIV 0 |

**Figure 6. 55 Cycle Control 4 Register (R3Dh)**

**DIV_N1-0:**The division ratio of clocks for Normal mode internal operation (DIV_N1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_N1-0. Frame frequency can be adjusted along with the 1H period (RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

**DIV_PI1-0:**The division ratio of clocks for Partial mode + Idle mode internal operation (DIV_PI1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_PI1-0. Frame frequency can be adjusted along with the 1H period (PI_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

**DIV_I1-0:**The division ratio of clocks for Idle mode internal operation (DIV_I1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_I1-0. Frame frequency can be adjusted along with the 1H period (I_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

| DIV_N1 / DIV_PI1 / DIV_I1 | DIV_N0 / DIV_PI0 / DIV_I0 | Division Ratio | Internal Operation Clock Frequency |
|---|---|---|---|
| 0 | 0 | 1 | fosc / 1 |
| 0 | 1 | 2 | fosc / 2 |
| 1 | 0 | 4 | fosc / 4 |
| 1 | 1 | 8 | fosc / 8 |

**Formula for the Frame Frequency:**
Frame frequency = fosc/( RTN × DIV × (NL+BP+FP) ) [HZ]
fosc: RC oscillation frequency
NL: 320 lines.

## 6.37 Cycle Control 5 Register (R3Eh)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SON 7 | SON 6 | SON 5 | SON 4 | SON 3 | SON 2 | SON 1 | SON 0 |
| R | 1 | * | * | * | * | * | * | * | * | SON 7 | SON 6 | SON 5 | SON 4 | SON 3 | SON 2 | SON 1 | SON 0 |

**Figure 6. 56 Display Control 5 Register (R3Eh)**

## 6.38 Cycle Control 6 Register (R40h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | GDON 7 | GDON 6 | GDON 5 | GDON 4 | GDON 3 | GDON 2 | GDON 1 | GDON 0 |
| R | 1 | * | * | * | * | * | * | * | * | GDON 7 | GDON 6 | GDON 5 | GDON 4 | GDON 3 | GDON 2 | GDON 1 | GDON 0 |

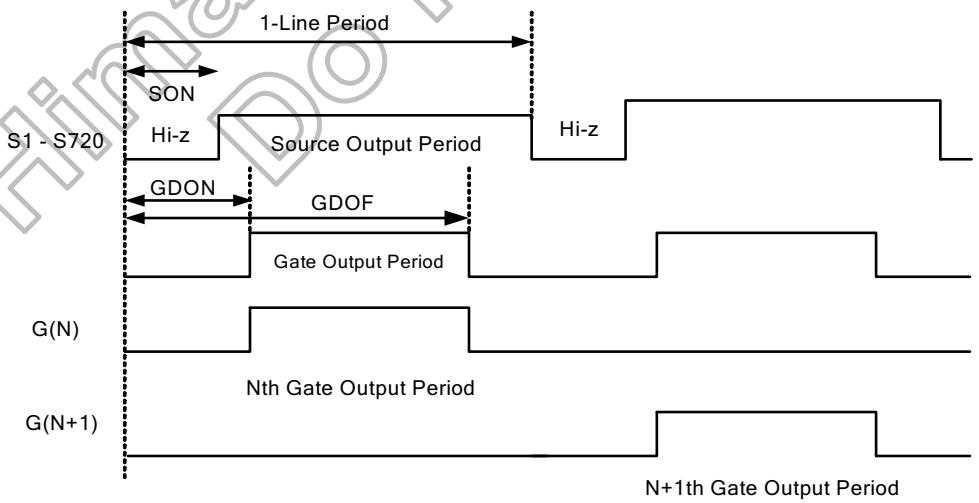
**Figure 6. 57 Display Control 6 Register (R40h)**

## 6.39 Display Control 14 Register (R41h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | GDOF 7 | GDOF 6 | GDOF 5 | GDOF 4 | GDOF 3 | GDOF 2 | GDOF 1 | GDOF 0 |
| R | 1 | * | * | * | * | * | * | * | * | GDOF 7 | GDOF 6 | GDOF 5 | GDOF 4 | GDOF 3 | GDOF 2 | GDOF 1 | GDOF 0 |

**Figure 6. 58 Display Control 3 Register (R41h)**

The HX8347-A01 can control the display operation period time for LCD panel driving as follow:



**SON7-0**: Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number. (Please note that the setting “00h” and “01h” is inhibited).

**GDON7-0**: Specify the valid gate output start time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the setting “00h”,“01h”, “02h” is inhibited).

**GDOF7-0**: Specify the gate output end time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the GDOF7-0 ≤ HCK-1).

## 6.40 BGP Control Register (R42h)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB 9 | RB 8 | RB 7 | RB 6 | RB 5 | RB 4 | RB 3 | RB 2 | RB 1 | RB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | VBG P_OE | BGP3 | BGP2 | BGP1 | BGP0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | VBG P_OE | BGP3 | BGP2 | BGP1 | BGP0 |

**Figure 6. 59 BGP Control 1 Register (R42h)**

**BGP[3:0]:** band gap voltage control

| BGP[3:0] | VBGP Otput |
|---|---|
| 4’b0000 | X 0.936 |
| 4’b0001 | X 0.944 |
| 4’b0010 | X 0.952 |
| 4’b0011 | X 0.96 |
| 4’b0100 | X 0.968 |
| 4’b0101 | X 0.976 |
| 4’b0110 | X 0.984 |
| 4’b0111 | X 0.992 |
| **4’b1000** | **X 1.000** |
| 4’b1001 | X 1.008 |
| 4’b1010 | X 1.016 |
| 4’b1011 | X 1.024 |
| 4’b1100 | X 1.032 |
| 4’b1101 | X 1.040 |
| 4’b1110 | X 1.048 |
| 4’b1111 | X 1.056 |

**BGP_OE:** If VBGP_OE=1, HX8347-A01 outputs the band gap voltage to VBGP pin.

## 6.41 Vcom Control 1 Register (R43h)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB 9 | RB 8 | RB 7 | RB 6 | RB 5 | RB 4 | RB 3 | RB 2 | RB 1 | RB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | VCOMG | * | * | * | * | * | * | * |
| R | 1 | * | * | * | * | * | * | * | * | VCOMG | * | * | * | * | * | * | * |

**Figure 6. 60 Vcom Control 1 Register (R43h)**

**VCOMG:**
When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ VCL+0.3V). When VCOMG = 0, VCOML outputs VSSA and VDV(4-0) setting are invalid. Then, low power consumption is accomplished.

## 6.42 Vcom Control 2 Register (R44h)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB 9 | RB 8 | RB 7 | RB 6 | RB 5 | RB 4 | RB 3 | RB 2 | RB 1 | RB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | VCM6 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 |
| R | 1 | * | * | * | * | * | * | * | * | * | VCM6 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 |

**Figure 6. 61 Vcom Control 2 Register**

**VCM(6-0):**
Set the VCOMH voltage (High level voltage of VCOM) It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage.

| VCM6 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 | VCOMH |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.405 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.41 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.415 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.42 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.425 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.43 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.435 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.44 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.445 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.45 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.455 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.46 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.465 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.47 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.475 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.48 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.485 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.49 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.495 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.5 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.505 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.51 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.515 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.52 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.525 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.53 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.535 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.54 |

| VCM6 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 | VCOMH |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.545 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.55 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | VREG1 * 0.555 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.56 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.565 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.57 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.575 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.58 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.585 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.59 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.595 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.6 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.605 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.61 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.615 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.62 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.625 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.63 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.635 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.64 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.645 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.65 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.655 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.66 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.665 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.67 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.675 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.68 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.685 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.69 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.695 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.7 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.705 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.71 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | VCOMH can be adjusted from VCOMR with a external VR (variable resister), |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.715 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.72 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.725 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.73 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.735 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.74 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.745 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.75 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.755 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.76 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.765 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.77 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.78 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.785 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.79 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.795 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.8 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.805 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.81 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.815 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.82 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | VREG1 * 0.825 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | VREG1 * 0.83 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | VREG1 * 0.835 |

| VCM6 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 | VCOMH |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | VREG1 * 0.84 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | VREG1 * 0.845 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | VREG1 * 0.85 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | VREG1 * 0.855 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | VREG1 * 0.86 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | VREG1 * 0.865 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | VREG1 * 0.87 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | VREG1 * 0.875 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | VREG1 * 0.88 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | VREG1 * 0.885 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | VREG1 * 0.89 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | VREG1 * 0.895 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | VREG1 * 0.9 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | VREG1 * 0.905 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | VREG1 * 0.91 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | VREG1 * 0.915 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | VREG1 * 0.92 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | VREG1 * 0.925 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | VREG1 * 0.93 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | VREG1 * 0.935 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | VREG1 * 0.94 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | VREG1 * 0.945 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | VREG1 * 0.95 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | VREG1 * 0.955 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | VREG1 * 0.96 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | VREG1 * 0.965 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | VREG1 * 0.97 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | VREG1 * 0.975 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | VREG1 * 0.98 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | inhibit |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | VCOMH can be adjusted from VCOMR with a external VR (variable resister) |

## 6.43 Vcom Control 3 Register (R45h)

| R/W | RS | RB 15 | RB 14 | RB 13 | RB 12 | RB 11 | RB 10 | RB 9 | RB 8 | RB 7 | RB 6 | RB 5 | RB 4 | RB 3 | RB 2 | RB 1 | RB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | VDV4 | VDV3 | VDV2 | VDV1 | VDV0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | VDV4 | VDV3 | VDV2 | VDV1 | VDV0 |

**Figure 6. 62 Vcom Control 3 Register (R45h)**

**VDV(4-0):**
Specify the VCOM amplitude factors for panel common driving (VCOML = VCOMH – VCOM amplitude, VCOML ≥ VCL+0.3V). It is possible to setup from 0.6 to 1.23 times of VREG1. When VCOMG = 0, the VDV(4-0) setup is invalid and VCOML is output VSSA

| VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | VCOM Amplitude |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | VREG1*0.6 |
| 0 | 0 | 0 | 0 | 1 | VREG1*0.63 |
| 0 | 0 | 0 | 1 | 0 | VREG1*0.66 |
| 0 | 0 | 0 | 1 | 1 | VREG1*0.69 |
| 0 | 0 | 1 | 0 | 0 | VREG1*0.72 |
| 0 | 0 | 1 | 0 | 1 | VREG1*0.75 |
| 0 | 0 | 1 | 1 | 0 | VREG1*0.78 |
| 0 | 0 | 1 | 1 | 1 | VREG1*0.81 |
| 0 | 1 | 0 | 0 | 0 | VREG1*0.84 |
| 0 | 1 | 0 | 0 | 1 | VREG1*0.87 |
| 0 | 1 | 0 | 1 | 0 | VREG1*0.9 |
| 0 | 1 | 0 | 1 | 1 | VREG1*0.93 |
| 0 | 1 | 1 | 0 | 0 | VREG1*0.96 |
| 0 | 1 | 1 | 0 | 1 | VREG1*0.99 |
| 0 | 1 | 1 | 1 | 0 | VREG1*1.02 |
| 0 | 1 | 1 | 1 | 1 | Inhibit |
| 1 | 0 | 0 | 0 | 0 | VREG1*1.05 |
| 1 | 0 | 0 | 0 | 1 | VREG1*1.08 |
| 1 | 0 | 0 | 1 | 0 | VREG1*1.11 |
| 1 | 0 | 0 | 1 | 1 | VREG1*1.14 |
| 1 | 0 | 1 | 0 | 0 | VREG1*1.17 |
| 1 | 0 | 1 | 0 | 1 | VREG1*1.2 |
| 1 | 0 | 1 | 1 | 0 | VREG1*1.23 |
| 1 | 0 | 1 | 1 | 1 | Inhibit |
| 1 | 1 | 0 | 0 | 0 | Inhibit |
| 1 | 1 | 0 | 0 | 1 | Inhibit |
| 1 | 1 | 0 | 1 | 0 | Inhibit |
| 1 | 1 | 0 | 1 | 1 | Inhibit |
| 1 | 1 | 1 | 0 | 0 | Inhibit |
| 1 | 1 | 1 | 0 | 1 | Inhibit |
| 1 | 1 | 1 | 1 | 0 | Inhibit |
| 1 | 1 | 1 | 1 | 1 | Inhibit |

**Note: VCOML >= (VCL + 0.3), VCOMH <= (DDVDH - 0.3) when set VDV[4:0]**

## 6.44 GAMMA Control 1~12 Register (R46~51h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | GSEL | CP12 | CP11 | CP10 | * | CP02 | CP01 | CP00 |
| R | 1 | * | * | * | * | * | * | * | * | GSEL | CP12 | CP11 | CP10 | * | CP02 | CP01 | CP00 |

**Figure 6. 63 GAMMA Control 1 Register (R46h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | CN12 | CN11 | CN10 | * | CN02 | CN01 | CN00 |
| R | 1 | * | * | * | * | * | * | * | * | * | CN12 | CN11 | CN10 | * | CN02 | CN01 | CN00 |

**Figure 6. 64 GAMMA Control 2 Register (R47h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NP12 | NP11 | NP10 | * | NP02 | NP01 | NP00 |
| R | 1 | * | * | * | * | * | * | * | * | * | NP12 | NP11 | NP10 | * | NP02 | NP01 | NP00 |

**Figure 6. 65 GAMMA Control 3 Register (R48h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NP32 | NP31 | NP30 | * | NP22 | NP21 | NP20 |
| R | 1 | * | * | * | * | * | * | * | * | * | NP32 | NP31 | NP30 | * | NP22 | NP21 | NP20 |

**Figure 6. 66 GAMMA Control 4 Register (R49h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NP52 | NP51 | NP50 | * | NP42 | NP41 | NP40 |
| R | 1 | * | * | * | * | * | * | * | * | * | NP52 | NP51 | NP50 | * | NP42 | NP41 | NP40 |

**Figure 6. 67 GAMMA Control 5 Register (R4Ah)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NN12 | NN11 | NN10 | * | NN02 | NN01 | NN00 |
| R | 1 | * | * | * | * | * | * | * | * | * | NN12 | NN11 | NN10 | * | NN02 | NN01 | NN00 |

**Figure 6. 68 GAMMA Control 6 Register (R4Bh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NN32 | NN31 | NN30 | * | NN22 | NN21 | NN20 |
| R | 1 | * | * | * | * | * | * | * | * | * | NN32 | NN31 | NN30 | * | NN22 | NN21 | NN20 |

**Figure 6. 69 GAMMA Control 7 Register (R4Ch)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | NN52 | NN51 | NN50 | * | NN52 | NN51 | NN50 |
| R | 1 | * | * | * | * | * | * | * | * | * | NN52 | NN51 | NN50 | * | NN52 | NN51 | NN50 |

**Figure 6. 70 GAMMA Control8 Register (R4Dh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | CGM P11 | CGM P10 | CGM P01 | CGMP 00 | OP03 | OP02 | OP01 | OP00 |
| R | 1 | * | * | * | * | * | * | * | * | CGM P11 | CGM P10 | CGM P01 | CGMP 00 | OP03 | OP02 | OP01 | OP00 |

**Figure 6. 71 GAMMA Control 9 Register (R4Eh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | CGM P3 | CGM P2 | * | OP14 | OP13 | OP12 | OP11 | OP10 |
| R | 1 | * | * | * | * | * | * | * | * | CGM P3 | CGM P2 | * | OP14 | OP13 | OP12 | OP11 | OP10 |

**Figure 6. 72 GAMMA Control 10 Register (R4Fh)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | CGMN 10 | CGMN 10 | CGMN 01 | CGMN 00 | ON03 | ON02 | ON01 | ON00 |
| R | 1 | * | * | * | * | * | * | * | * | CGMN 10 | CGMN 10 | CGMN 01 | CGMN 00 | ON03 | ON02 | ON01 | ON00 |

**Figure 6. 73 GAMMA Control 11 Register (R50h)**

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | CGM N3 | CGMN2 | * | ON14 | ON13 | ON12 | ON11 | ON10 |
| R | 1 | * | * | * | * | * | * | * | * | CGM N3 | CGMN2 | * | ON14 | ON13 | ON12 | ON11 | ON10 |

**Figure 6. 74 GAMMA Control 12 Register (R51h)**

**CP1-0 [2:0]:** Gamma Center Adjustment registers for positive polarity output
**CN1-0 [2:0]:** Gamma Center Adjustment registers for negative polarity output
**NP5-0 [2:0]:** Gamma Macro Adjustment registers for positive polarity output
**NN5-0 [2:0]:** Gamma Macro Adjustment registers for negative polarity output
**OP0 [3:0]/OP1 [4:0]:** Gamma Offset Adjustment register for positive polarity output
**ON0 [3:0]/ON1 [4:0]:** Gamma Offset Adjustment register for negative polarity output
**CGMP0[1:0], CGMP1[1:0]:** Gamma Tap Adjustment register for positive polarity output
**CGMN0[1:0], CGMN1[1:0]:** Gamma Tap Adjustment register for negative polarity output

**CGMP2, CGMP3:** Gamma Harmony adjustment register for positive polarity output
**CGMN2, CGMN3:** Gamma Harmony adjustment register for negative polarity output
**GSEL:** V0, V256 reference voltage selection. GSEL=1, V0=VgP/N0, V63= VgP/N7; If GSEL=0, V0=VREG1, V63= VGS. For details, please refer to 5.9.4 Gamma resister stream and 8 to 1 Selector.

This command is used to set Gamma Curve Related Setting

| Register Groups | Positive Polarity | Negative Polarity | Description |
|---|---|---|---|
| Center Adjustment | CP0 2-0 | CN0 2-0 | Variable resistor (VRCP/N0) for center adjustment |
| | CP1 2-0 | CN1 2-0 | Variable resistor (VRCP/N1)for center adjustment |
| Macro Adjustment | NP0 2-0 | NN0 2-0 | 8-to-1 selector (voltage level of grayscale 1) |
| | NP1 2-0 | NN1 2-0 | 8-to-1 selector (voltage level of grayscale 8) |
| | NP2 2-0 | NN2 2-0 | 8-to-1 selector (voltage level of grayscale 20) |
| | NP3 2-0 | NN3 2-0 | 8-to-1 selector (voltage level of grayscale 43) |
| | NP4 2-0 | NN4 2-0 | 8-to-1 selector (voltage level of grayscale 55) |
| | NP5 2-0 | NN5 2-0 | 8-to-1 selector (voltage level of grayscale 62) |
| Offset Adjustment | OP0 3-0 | ON0 3-0 | Variable resistor (VROP/N0)for offset adjustment |
| | OP1 4-0 | ON1 4-0 | Variable resistor (VROP/N1)for offset adjustment |

## 6.45 Internal Use 16 (R64h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 |
| R | 1 | * | * | * | * | * | * | * | * | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 |

**Figure 6. 75 Internal Use 16 (R64h)**

For internal use and not open.

## 6.46 Internal Use 17 (R65h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | 0 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 |
| R | 1 | * | * | * | * | * | * | * | * | 0 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 |

**Figure 6. 76 Internal Use 17 (R65h)**

For internal use and not open.

## 6.47 Internal Use 18 (R66h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 |
| R | 1 | * | * | * | * | * | * | * | * | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 |

**Figure 6. 77 Internal Use 18 (R66h)**

For internal use and not open.

## 6.48 Himax ID code (R67h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | Himax ID7 | Himax ID6 | Himax ID5 | Himax ID4 | Himax ID3 | Himax ID2 | Himax ID1 | Himax ID0 |
| R | 1 | * | * | * | * | * | * | * | * | Himax ID7 | Himax ID6 | Himax ID5 | Himax ID4 | Himax ID3 | Himax ID2 | Himax ID1 | Himax ID0 |

**Figure 6. 78 Himax ID code (R676h)**

**HimaxID[7:0]:** The value is 0x47h of HX8347-A01.

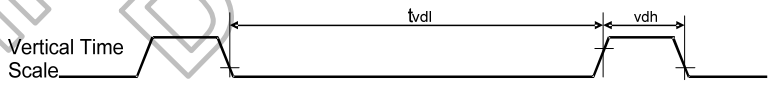
## 6.49 Internal Use 28 (R70h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | GS | SS | TEMODE | TEON | CSEL 2 | CSEL 1 | CSEL 0 |
| R | 1 | * | * | * | * | * | * | * | * | * | GS | SS | TEMODE | TEON | CSEL 2 | CSEL 1 | CSEL 0 |

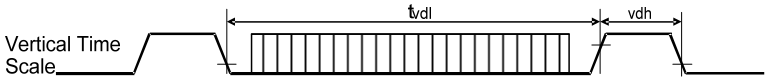
**Figure 6. 79 Internal Use 28 (R70h)**

**TEMODE:** Specify the Tearing-Effect mode.

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only.




When TEMODE =1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information




**Note:** During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin active low

**TEON:**
This command is used to turn ON the Tearing Effect output signal from the TE signal line.

**CSEL[2:0]:**
This command is used to define the format of RGB picture data, which is to be transferred via the RGB Interface. The formats are shown in the table:

| Interface Format | CSEL2 | CSEL1 | CSEL0 |
|---|---|---|---|
| Not Defined | 0 | 0 | 0 |
| Not Defined | 0 | 0 | 1 |
| Not Defined | 0 | 1 | 0 |
| Not Defined | 0 | 1 | 1 |
| Not Defined | 1 | 0 | 0 |
| 16 Bit/Pixel | 1 | 0 | 1 |
| 18 Bit/Pixel | 1 | 1 | 0 |

**SS:** The source driver output shift direction selected. When SS=0, the shift direction from S1 to S720. When SS = 1, the shift direction from S720 to S1.

**GS:** The gate driver output shift direction selected. When GS=0, the shift direction from G1 to S320. When SS = 1, the shift direction from S320 to S1.

## 6.50 Data control register (R72h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | DFM1 | DFM0 | * | * | TRI1 | TRI0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | DFM1 | DFM0 | * | * | TRI1 | TRI0 |

**Figure 6. 80 Serial Bus Interface Control Register (R72h)**

| TRI[1:0] | GRAM |
|---|---|
| 00 | 16 bit-color/per pixel data |
| 01 | 18 bit-color/per pixel data |
| 1X | 18 bit-color/per pixel data |

For details, please refer to serial bus system interface.

## 6.51 Display Control 8 (R90h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SAP[7:0] | | | | | | | |
| R | 1 | * | * | * | * | * | * | * | * | SAP[7:0] | | | | | | | |

**Figure 6. 81 Display Control 8 (R90h)**

**SAP [7:0]:** Adjust the amount of fixed current from the fixed current source for the source driver operational amplifier in the Normal display .

## 6.52 Display Control 11 (R91h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | GEN_OFF[7:0] | | | | | | | |
| R | 1 | * | * | * | * | * | * | * | * | GEN_OFF[7:0] | | | | | | | |

**Figure 6. 82 Display Control 11 (R91h)**

For internal use and not open.

## 6.53 OSC Control 3 (R93h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | RADJ 3 | RADJ 2 | RADJ 1 | RADJ 0 |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | RADJ 3 | RADJ 2 | RADJ 1 | RADJ 0 |

**Figure 6. 83 OSC Control 3 (R93h)**

**RADJ[4:0]:** Internal oscillator frequency adjust, default is 5.58MHz.

| RADJ3 | RADJ2 | RADJ1 | RADJ0 | Internal Oscillator Frequency |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 175% |
| 0 | 0 | 0 | 1 | 170% |
| 0 | 0 | 1 | 0 | 165% |
| 0 | 0 | 1 | 1 | 160% |
| 0 | 1 | 0 | 0 | 155% |
| 0 | 1 | 0 | 1 | 150% |
| 0 | 1 | 1 | 0 | 145% |
| 0 | 1 | 1 | 1 | 140% |
| 1 | 0 | 0 | 0 | 135% |
| 1 | 0 | 0 | 1 | 130% |
| 1 | 0 | 1 | 0 | 125% |
| 1 | 0 | 1 | 1 | 120% |
| 1 | 1 | 0 | 0 | 115% |
| 1 | 1 | 0 | 1 | 110% |
| 1 | 1 | 1 | 0 | 105% |
| 1 | 1 | 1 | 1 | 100% |

## 6.54 SAP Idle Mode (R94h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | SAP_I[7:0] | | | | | | | |
| R | 1 | * | * | * | * | * | * | * | * | SAP_I[7:0] | | | | | | | |

**Figure 6. 84 SAP Idle Mode (R94h)**

**SAP_I[7:0]:** Adjust the amount of fixed current from the fixed current source for the source driver operational amplifier in the Idle display mode.

## 6.55 DCCLK SYNC TO CL1 (R95h)

| R/W | RS | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | DCCLK_SYNC |
| R | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | DCCLK_SYNC |

**Figure 6. 85 DCCLK SYNC TO CL1 (R95h)**

For internal use and not open.

# 7. Electrical Characteristic

## 7.1 Absolute Maximum Ratings

($V_{SS}$ = 0V)

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage 1 | $IOV_{CC}$ | -0.3 ~ +4.6 | V |
| Supply Voltage 2 | $V_{CI}$ | -0.3 ~ +4.6 | V |
| Supply Voltage 3 | DDVDH | -0.3 ~ +9 | V |
| Supply Voltage 4 | VCL | -4.6 ~ +0.3 | V |
| Supply Voltage 5 | VGH | -0.3 ~ +18.5 | V |
| Supply Voltage 6 | VGL | -18.5 ~ +0.3 | V |
| Input Voltage Range | $V_{IN}$ | -0.3 ~ VCI+0.3 | V |
| Operating Temperature Range | $T_{OPR}$ | -40 ~ +85 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 ~ +110 | °C |

## 7.2 ESD Protection Level

| Mode | Test Condition | Protection Level | Unit |
|---|---|---|---|
| Human Body Model | C = 100 pF, R = 1.5 kΩ | ±2.0K | V |
| Machine Model | C = 200 pF, R = 0.0 Ω | ±200 | V |

**Table 7. 1**

## 7.3 Latch-Up Protection Level

TBD

## 7.4 Light Sensitivity

TBD

## 7.5 Maximum Series Resistance

| Name | Type | Maximum Series Resistance | Unit |
|---|---|---|---|
| IOVCC | Power supply | 10 | Ω |
| VCI | Power supply | 10 | Ω |
| VSSA | Power supply | 10 | Ω |
| VSSD | Power supply | 10 | Ω |
| OSC | Input | 100 | Ω |
| P68, BS[2:0], EXTC, IFSEL0, BURN, REGVDD, | Input | 100 | Ω |
| NRD_E, NWR_RNW, DNC_SCL, NCS, SDI | Input | 100 | Ω |
| NRESET | Input | 100 | Ω |
| D[17:0], DOTCLK, ENABLE, VSYNC, HSYNC | Input | 100 | Ω |
| VGH | Capacitor connection | 10 | Ω |
| VGL | Capacitor connection | 10 | Ω |
| VCL | Capacitor connection | 10 | Ω |
| DDVDH | Capacitor connection | 10 | Ω |
| VDDD | Capacitor connection | 10 | Ω |
| VREG1 | Capacitor connection | 30 | Ω |
| VREG3 | Capacitor connection | 20 | Ω |
| VCOMH, VCOML | Capacitor connection | 20 | Ω |
| C11A, C11B, CX11A, CX11B | Capacitor connection | 10 | Ω |
| C12A, C12B | Capacitor connection | 10 | Ω |
| C21A, C21B | Capacitor connection | 15 | Ω |
| C22A, C22B | Capacitor connection | 15 | Ω |
| VCOMR | Input | 100 | Ω |
| VGS | Input | 30 | Ω |
| TEST[3:1] | Input | 100 | Ω |
| VBGP, SDO | Output | 100 | Ω |

**Table 7. 2**

## 7.6 DC Characteristics

**(Vci = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C)**

| Item | Symbol | Unit | Test Condition | Min. | Typ. | Max. | Note |
|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | V | IOVcc= 1.65 ~ 3.3V | 0.7xIOVcc | - | IOVcc | - |
| Input low voltage | $V_{IL}$ | V | IOVcc= 1.65 ~ 3.3V | -0.3V | - | 0.3xIOVcc | - |
| Output high voltage ( D0-17 Pins) | $V_{OH1}$ | V | $I_{OH}$ = -0.1 mA | 0.8xIOVcc | - | - | - |
| Output low voltage ( D0-17 Pins) | $V_{OL1}$ | V | IOVcc= 1.65 ~ 3.3V $I_{OL}$ = 0.1mA | - | - | 0.2xIOVcc | - |
| I/O leakage current | $I_{Li}$ | µA | Vin = 0 ~ Vcc | -1 | - | 1 | - |
| Current consumption during normal operation (IOVcc-VSSD) | $I_{OP(IOVcc)}$ | µA | Vci =2.8V ,IOVcc=2.8V Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=01111111, AP=100, FS0=00, FS1=11, BT=0100, VC1=111, VC3=000 VRH=0100, VCM=0100000,VDV=01110, VCOMG=1 No panel load | - | 400 | 600 | - |
| Current consumption during normal operation ( Vci – VSSD ) | $I_{OP(Vci)}$ | mA | | - | 2.7 | 3.0 | - |
| Current consumption during standby mode (IOVcc-VSSD) | $I_{ST(IOVcc)}$ | µA | IOVcc=2.8V , Ta=25°C | - | 5 | 20 | - |
| Current consumption during standby mode ( Vci – VSSD ) | $I_{ST(Vci)}$ | µA | | | 0.5 | 1 | |
| Output voltage deviation | - | mV | - | - | 5 | - | - |
| Dispersion of the Average Output Voltage | V | mV | - | - | - | 35 | - |

**Table 7. 3 DC Characteristic**

## 7.7 AC CHARACTERISTICS

### 7.7.1 Parallel Interface Characteristics (8080-series MPU)

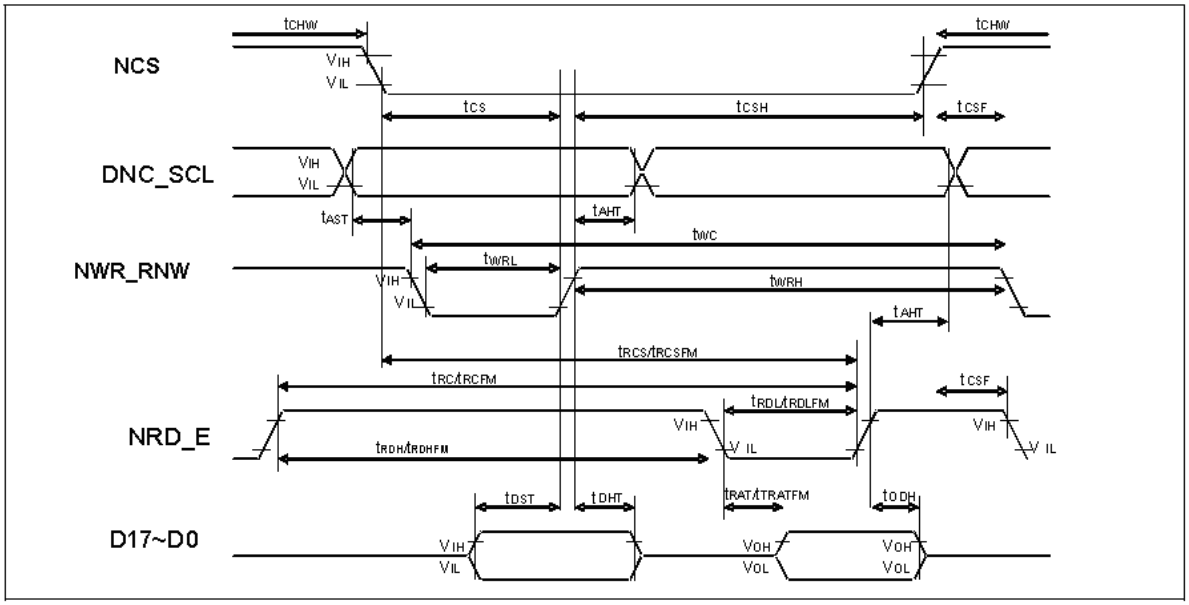


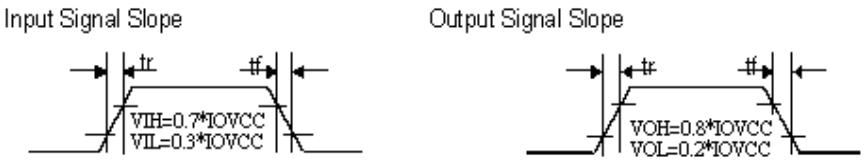

**Figure 7. 1 Parallel Interface Characteristics (8080-series MPU)**

**(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)**

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| DNC_SCL | $t_{AST}$ | Address setup time | 10 | - | ns | - |
| | $t_{AHT}$ | Address hold time (Write/Read) | 10 | - | | |
| NCS | $t_{CHW}$ | Chip select "H" pulse width | 0 | - | ns | - |
| | $t_{CS}$ | Chip select setup time (Write) | 35 | - | | |
| | $t_{RCSFM}$ | Chip select setup time | 180 | - | | |
| | $t_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | | |
| | $t_{CSH}$ | Chip select hold time | 10 | - | | |
| NWR_RNW | $t_{WC}$ | Write cycle | 100 | - | ns | - |
| | $t_{WRH}$ | Control pulse "H" duration | 15 | - | | |
| | $t_{WRL}$ | Control pulse "L" duration | 20 | - | | |
| NRD_E | $t_{RCFM}$ | Read cycle | 250 | - | ns | When read from GRAM |
| | $t_{RDHFM}$ | Control pulse "H" duration | 15 | - | | |
| | $t_{RDLFM}$ | Control pulse "L" duration | 180 | - | | |
| D17 to D0 | $t_{DST}$ | Data setup time | 10 | - | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| | $t_{DHT}$ | Data hold time | 10 | - | | |
| | $t_{RAT}$ | Read access time (ID) | - | 180 | | |
| | $t_{RATFM}$ | Read access time (FM) | - | 340 | | |
| | $t_{ODH}$ | Output disable time | 20 | 80 | | |

**Note**: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

**Table 7. 4 AC Characteristic of 8080-series Interface**



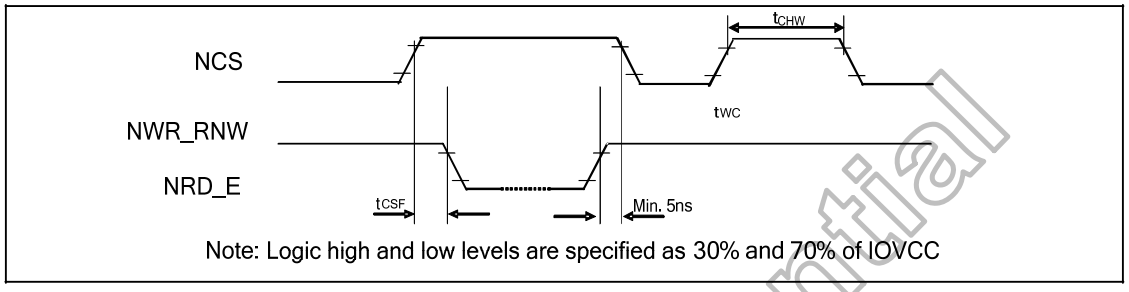




**Figure 7. 2 Chip Select Timing**

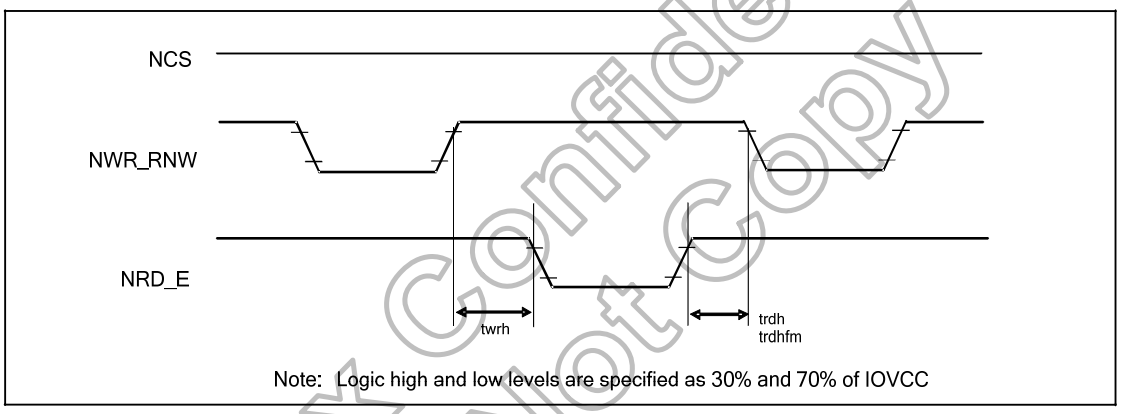



**Figure 7. 3 Write to Read and Read to Write Timing**

### 7.7.2 Parallel Interface Characteristics (6800-series MPU)

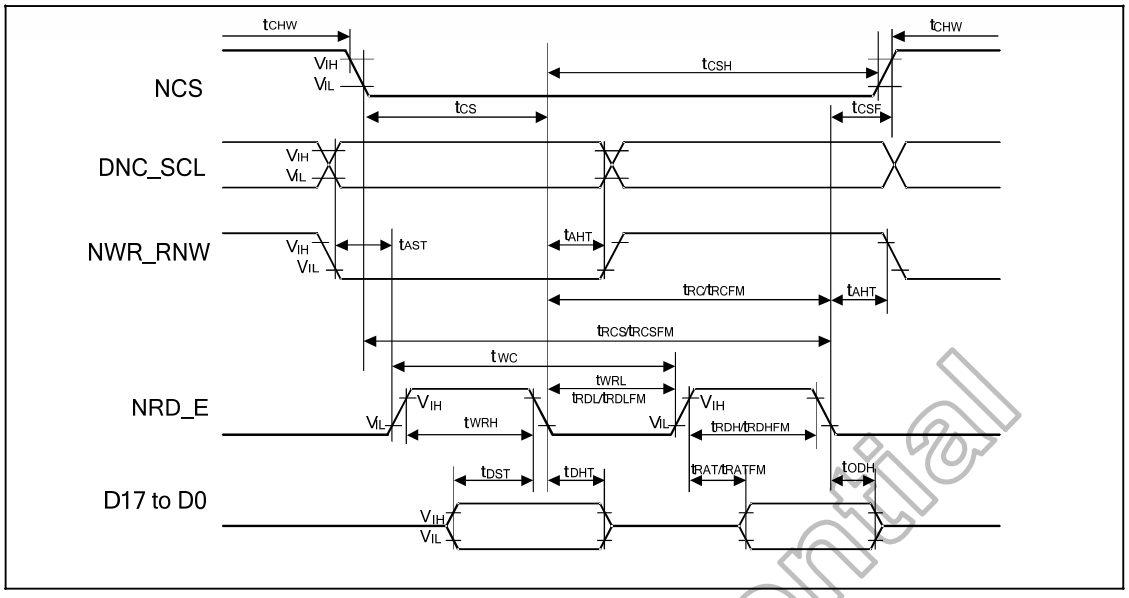



**Figure 7. 4 Parallel Interface Characteristics (6800-series MPU)**

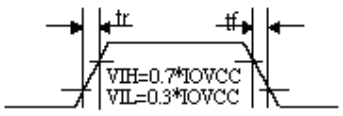
**(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)**

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| DNC_SCL | $t_{AST}$ | Address setup time | 10 | - | ns | - |
| | $t_{AHT}$ | Address hold time (Write/Read) | 10 | - | | |
| NCS | $t_{CHW}$ | Chip select "H" pulse width | 0 | - | ns | - |
| | $t_{CS}$ | Chip select setup time (Write) | 35 | - | | |
| | $t_{RCSFM}$ | Chip select setup time | 150 | - | | |
| | $t_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | | |
| | $t_{CSH}$ | Chip select hold time | 10 | - | | |
| NWR_RNW | $t_{WC}$ | Write cycle | 100 | - | ns | - |
| | $t_{WRH}$ | Control pulse "H" duration | 35 | - | | |
| | $t_{WRL}$ | Control pulse "L" duration | 35 | - | | |
| NRD_E | $t_{RCFM}$ | Read cycle | 450 | - | ns | When read from GRAM |
| | $t_{RDHFM}$ | Control pulse "H" duration | 90 | - | | |
| | $t_{RDLFM}$ | Control pulse "L" duration | 355 | - | | |
| D17 to D0 | $T_{dst}$ | Data setup time | 10 | - | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| | $t_{DHT}$ | Data hold time | 10 | - | | |
| | $t_{RAT}$ | Read access time (ID) | - | 180 | | |
| | $t_{RATFM}$ | Read access time (FM) | - | 340 | | |
| | $t_{ODH}$ | Output disable time | 20 | 80 | | |

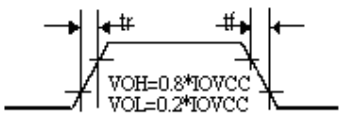
**Table 7. 5 AC Characteristic of 6800-series Interface**

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope




Output Signal Slope



### 7.7.3 Serial Interface Characteristics

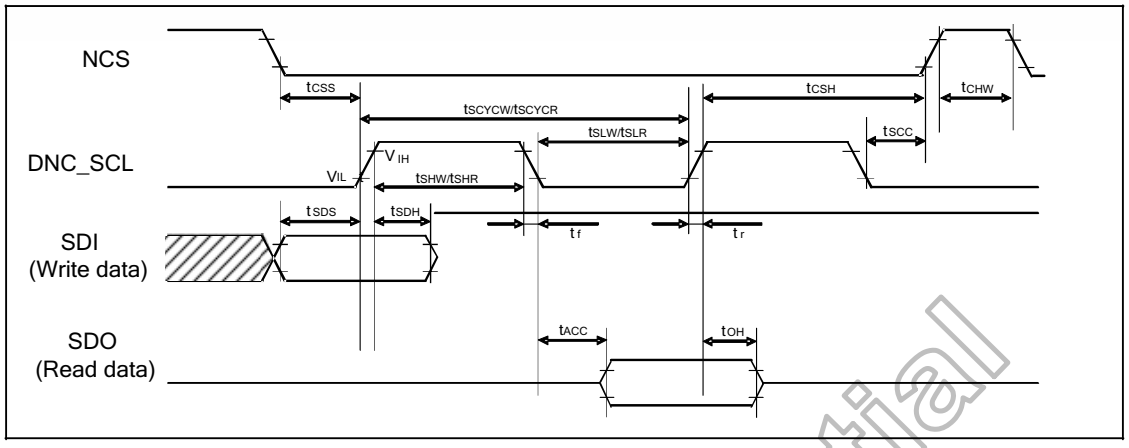



**Figure 7. 5 Serial Interface Characteristics**

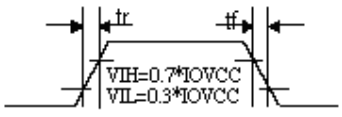
**(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)**

| Parameter | Symbol | Conditions | Min. | Typ. | Maz. | Unit |
|---|---|---|---|---|---|---|
| Serial clock cycle (Write)<br>DNC_SCL "H" pulse width (Write)<br>DNC_SCL "L" pulse width (Write) | $t_{SCYCW}$<br>$t_{SHW}$<br>$t_{SLW}$ | DNC_SCL | 100<br>35<br>35 | -<br>-<br>- | -<br>-<br>- | ns |
| Data setup time (Write)<br>Data hold time (Write) | $t_{SDS}$<br>$t_{SDH}$ | SDI | 30<br>30 | -<br>- | -<br>- | ns |
| Serial clock cycle (Read)<br>DNC_SCL "H" pulse width (Read)<br>DNC_SCL "L" pulse width (Read) | $t_{SCYCR}$<br>$t_{SHR}$<br>$t_{SLR}$ | DNC_SCL | 150<br>60<br>100 | -<br>-<br>- | -<br>-<br>- | ns |
| Access Time | $t_{ACC}$ | SDO for maximum $C_L$=30pF<br>For minimum $C_L$=8pF | 10 | - | 100 | ns |
| Output disable time | $t_{OH}$ | SDO For maximum $C_L$=30pF<br>For minimum $C_L$=8pF | 15 | - | 100 | ns |
| DNC_SCL to Chip select | $t_{SCC}$ | DNC_SCL, NCS | 50 | - | - | ns |
| NCS "H" pulse width | $t_{CHW}$ | NCS | 45 | - | - | ns |
| Chip select setup time<br>Chip select hold time | $t_{CSS}$<br>$t_{CSH}$ | NCS | 60<br>80 | -<br>- | -<br>- | ns |

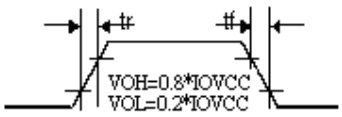
**Table 7. 6 AC Characteristic of SPI Interface**

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope




Output Signal Slope



### 7.7.4 RGB Interface Characteristics

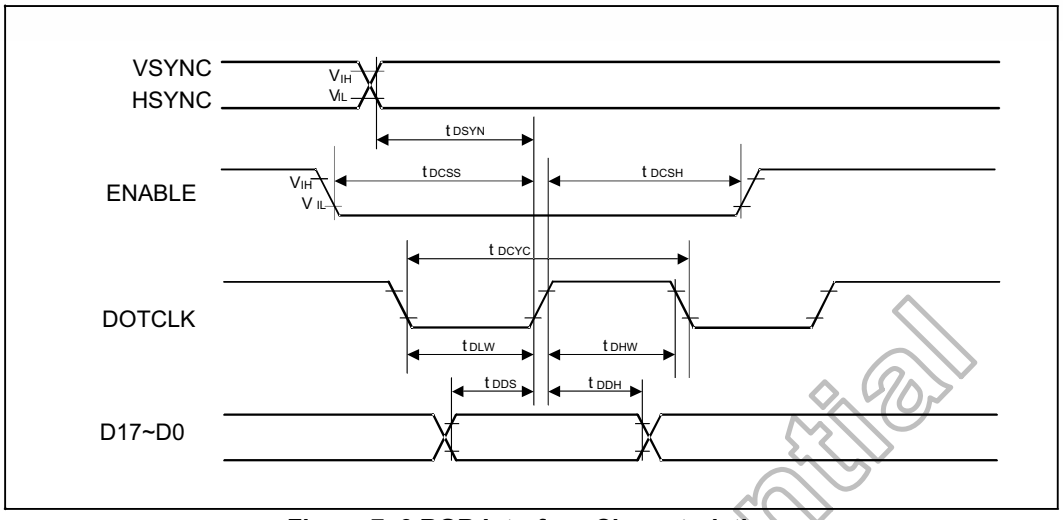


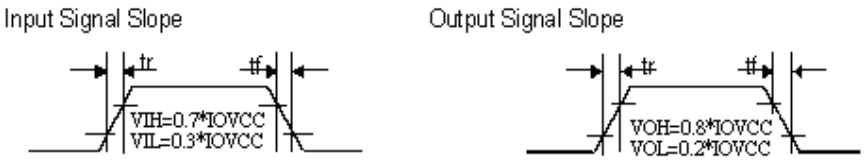

**Figure 7. 6 RGB Interface Characteristics**

**(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,Ta = -30 to 70° C)**

| Symbol | Parameter | Conditions | Related Pins | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{DCYC}$ | DOTCLK cycle time | VRR = Min . 50 Hz Max. 65 Hz | DOTCLK | 100 (note2) | - | 226 (note3) | ns |
| $t_{DLW}$<br>$t_{CHW}$ | DOTCLK Low time<br>DOTCLK High time | - | | 50<br>15 | - | -<br>- | ns |
| $t_{DDS}$<br>$t_{DDH}$ | RGB Data setup time<br>RGB Data hold time | - | DOTCLK, D17-D0 | 15<br>15 | -<br>- | -<br>- | ns |
| $t_{DCSS}$<br>$t_{DCSH}$ | ENABLE setup time<br>ENABLE hold Time | - | ENABLE | 15<br>15 | - | - | ns |
| $t_{DSYN}$ | SYNC setup time | - | DOTCLK, HSYNC, VSYNC | 15 | - | - | ns |

**Table 7. 7 AC Characteristic of RGB Interface**

**Note:** (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) 16.6 MHz
(3) 4.4MHz



### 7.7.5 Reset Input Timing

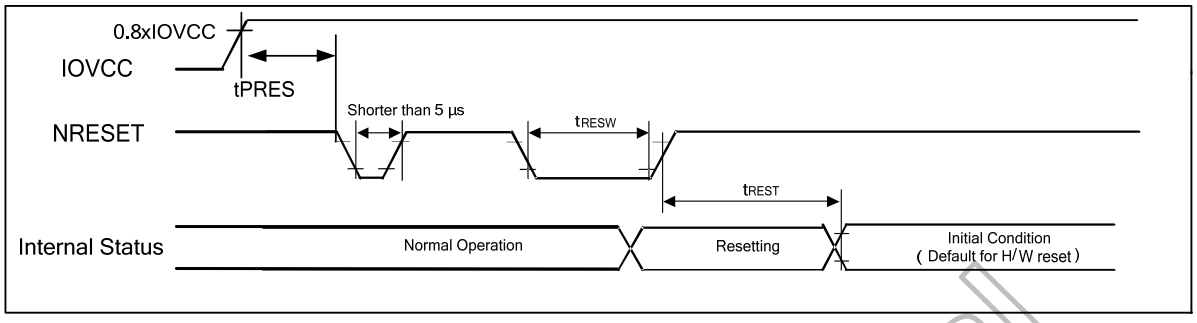



**Figure 7. 7 Reset input timing**

| Symbol | Parameter | Related Pins | Min. | Typ. | Max. | Note | Unit |
|---|---|---|---|---|---|---|---|
| tRESW | Reset low pulse width(1) | NRESET | 10 | - | - | - | µs |
| tREST | Reset complete time(2) | - | - | - | 5 | When reset applied during STB mode | ms |
| | | - | | - | 120 | When reset applied during STB mode | ms |
| tPRES | Reset goes high level after Power on time | NRESET & IOVCC | 1 | - | - | Reset goes high level after Power on | ms |

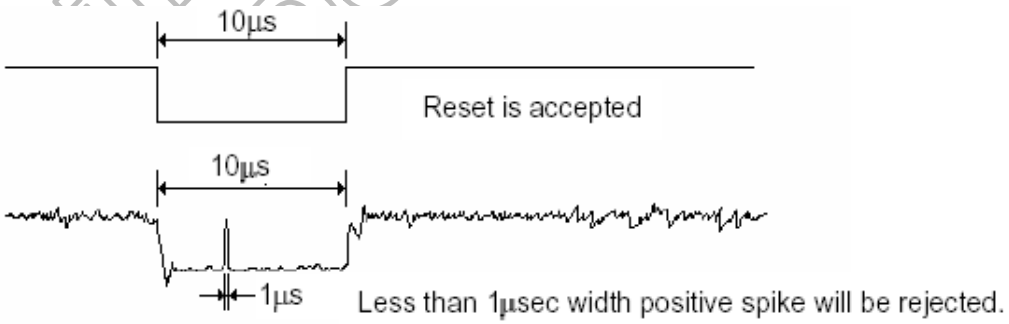
**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

| NRESET Pulse | Action |
|---|---|
| Shorter than 5 µ | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

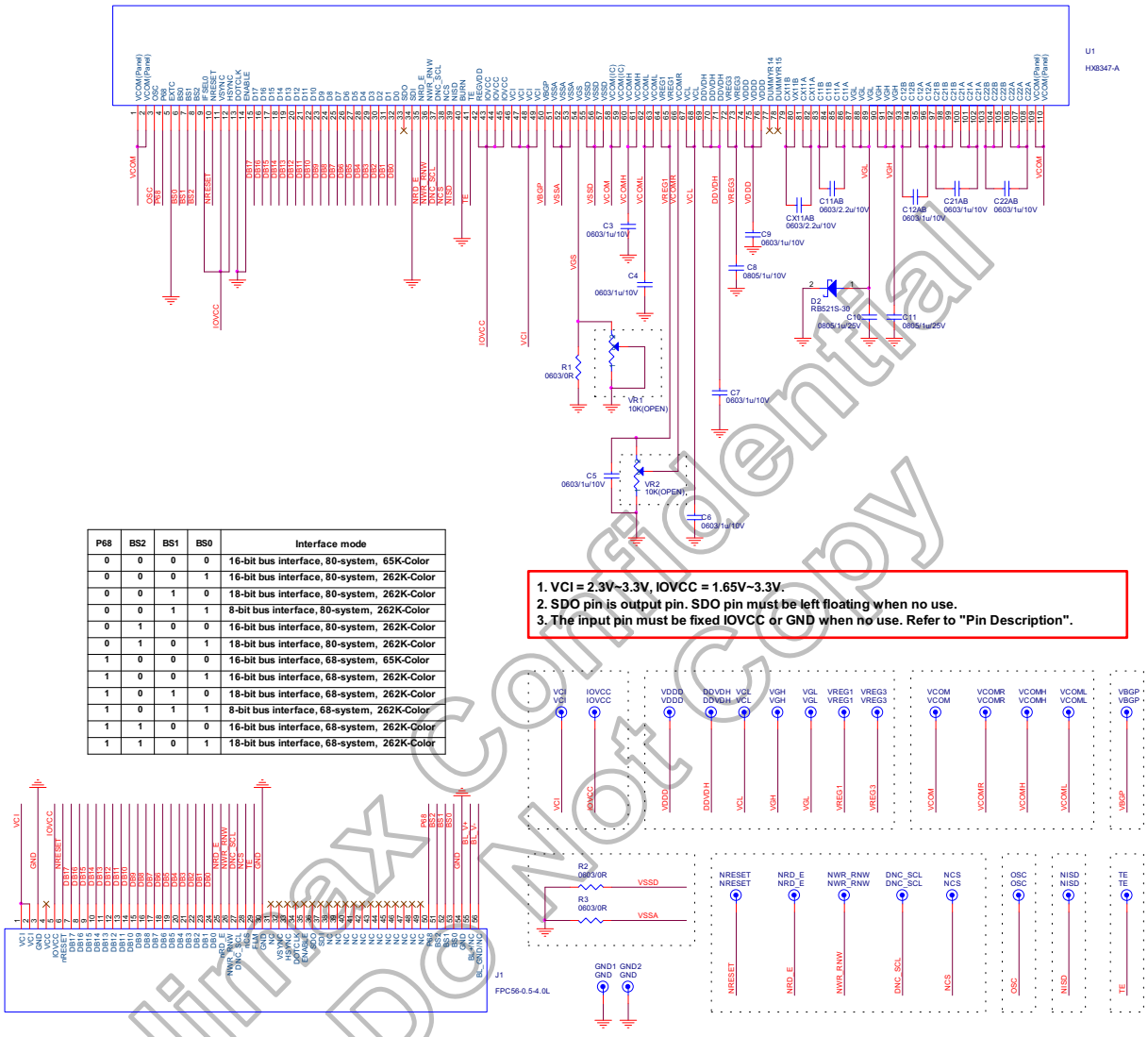
(4) Spike Rejection also applies during a valid reset pulse as shown below:




(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out command cannot be sent for 120msec.

# 8. Reference Applications

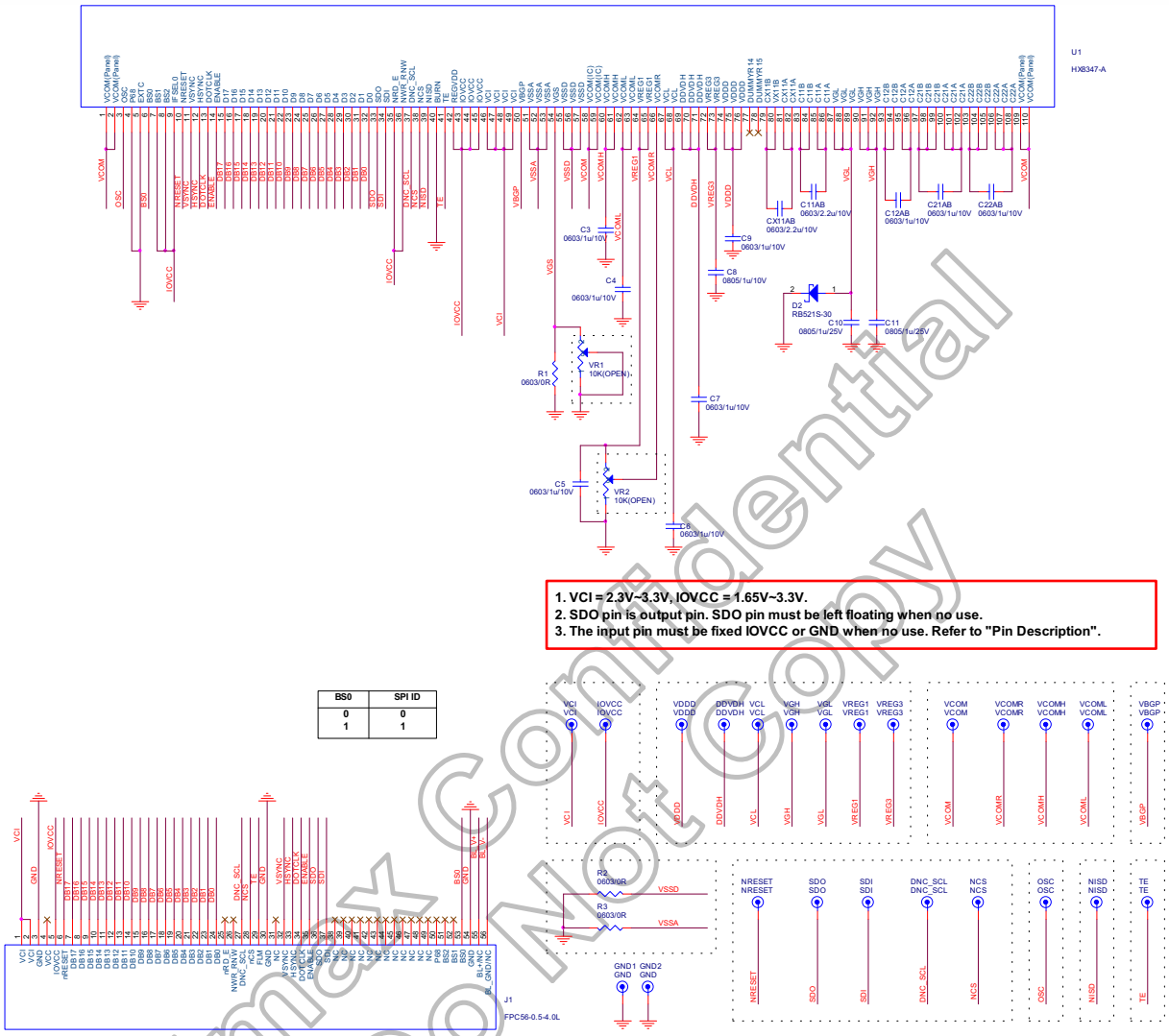
## 8.1 Parallel Interface of Register-Content Mode (For CMO Panel)



| P68 | BS2 | BS1 | BS0 | Interface mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 16-bit bus interface, 80-system, 65K-Color |
| 0 | 0 | 0 | 1 | 16-bit bus interface, 80-system, 262K-Color |
| 0 | 0 | 1 | 0 | 18-bit bus interface, 80-system, 262K-Color |
| 0 | 0 | 1 | 1 | 8-bit bus interface, 80-system, 262K-Color |
| 0 | 1 | 0 | 0 | 16-bit bus interface, 80-system, 262K-Color |
| 0 | 1 | 0 | 1 | 18-bit bus interface, 80-system, 262K-Color |
| 1 | 0 | 0 | 0 | 16-bit bus interface, 68-system, 65K-Color |
| 1 | 0 | 0 | 1 | 16-bit bus interface, 68-system, 262K-Color |
| 1 | 0 | 1 | 0 | 18-bit bus interface, 68-system, 262K-Color |
| 1 | 0 | 1 | 1 | 8-bit bus interface, 68-system, 262K-Color |
| 1 | 1 | 0 | 0 | 16-bit bus interface, 68-system, 262K-Color |
| 1 | 1 | 0 | 1 | 18-bit bus interface, 68-system, 262K-Color |

1. VCI = 2.3V~3.3V, IOVCC = 1.65V~3.3V.
2. SDO pin is output pin. SDO pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

## 8.2 RGB + SPI Interface of Register-Content Mode (For CMO Panel)



## 8.3 External Components Connection

| Pad Name | Connection | Component Spec |
|---|---|---|
| VCOMH | Connect to Capacitor (Max 6V): VCOMH---(+)----\| \|--- (-)------ VSSA | 1.0 uF |
| VCOML | Connect to Capacitor (Max 3V): VCOML ---(-)----\| \|--- (+)----- VSSA | 1.0 uF |
| VGL | Connect to Capacitor (Max 16V): VGL ---(-)----\| \|--- (+)----- VSSA | 1.0 uF |
| VGH | Connect to Capacitor (Max 21V): VGH ---(+)----\| \|--- (-)----- VSSA | 1.0 uF |
| VCL | Connect to Capacitor (Max 5V): VCL ---(-)----\| \|--- (+)----- VSSA | 1.0 uF |
| C22A - C22B | Connect to Capacitor (Max 7V): C22A ---(+)----\| \|--- (-)-----C22B | 1.0 uF |
| C21A - C21B | Connect to Capacitor (Max 7V): C21A ---(+)----\| \|--- (-)-----C21B | 1.0 uF |
| CX11A - CX11B | Connect to Capacitor (Max 7V): CX11A ---(+)----\| \|--- (-)-----CX11B | 2.2 uF |
| C11A - C11B | Connect to Capacitor (Max 5V): C11A ---(+)----\| \|--- (-)-----C11B | 2.2 uF |
| C12A - C12B | Connect to Capacitor (Max 6V): C12A ---(+)----\| \|--- (-)-----C12B | 1.0 uF |
| VREG1 | Connect to Capacitor (Max 6V): VREG1 ---(+)----\| \|--- (-)-----VSSA | 1.0 uF |
| VREG3 | Connect to Capacitor (Max 6V): VREG3 ---(+)----\| \|--- (-)-----VSSA | 1.0 uF |
| VDDD | Connect to Capacitor (Max 6V): VDDD ---(+)----\| \|--- (-)-----VSSA | 1.0 uF |
| DDVDH | Connect to Capacitor (Max 6V): DDVDH ---(+)----\| \|--- (-)-----VSSA | 1.0 uF |
| VGL - GND | Connect to Schottky Diode | VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30) |

**Table 8. 1 External component table**

# 9. Ordering Information

| Part No. | Package |
|---|---|
| **HX8347-A010 PDxxx-E** | PD : mean COG<br>xxx : mean chip thickness (μm), (default: 300 μm) |

# 10. Revision History

| Version | Date | Description of Changes |
|---|---|---|
| 01 | 2007/06/29 | 1. New setup(HX8347-A01Datasheet) |
| | 2007/07/02 | 1. Modify Figure 5.24~25 of TE mode output.(P.46) |
| | 2007/07/20 | 1. Update Gamma formula.(P.59~P.62)<br>2. Modify Figure 5.37 Gamma Resister Stream and Gamma Reference Voltage.(P.57)<br>3. Update 5.14 Output Voltage of 8 to 1 Selector.(P.58) |
| | 2007/07/23 | 1. Update chip thickness (300 μm).(P.16) |
| | 2007/08/03 | 1. Modify NISD pin description (P.13) |
| | 2007/08/24 | 1. Update 5.15 OTP programming.(P.70)<br>2. Add RGB+SPI interface circuit.(P.127)<br>3. Modify D17-D0 pin description.(P.14) |
| | 2007/09/04 | 1. Update AC timing.(P.120~P.124) |
| V02 | 2007/10/13 | 1. Update Table5.7 EPL Bit Setting and Valid Enable Signal. (P.39)<br>2. Modify 6.33 RGB Interface Control 1 Register - EPL bit setting description.(P.99) |
| | 2007/11/07 | 1. Modify state of Data bus unused pins.(P.14)<br>2. Modify Figure 5.11~12 and 5.15.(P.34~P.35)<br>3. Add tRAT timing in Table 7. 4 AC Characteristic of 8080-series Interface.(P.120)<br>4. Upfate Ordering Information(P.129) |
| | 2008/02/13 | 1. Modify Figure 5. 40 Scan Function.(P.64) |
| | 2008/03/18 | 1. Remove Schottky Diode(D1, D3) and Capacitor(C1, C2) in 8. Reference Applications.(P.126~P.128) |