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JD9165A-A

Rev. 0.0.1

PRELIMINARY DATA SHEET

1538CH TFT LCD Single Chip Driver with TCON

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1. GENERAL DESCRIPTION 4
2. FEATURES 5
3. BLOCK DIAGRAM 6
3.1 Function block diagram 6
3.2 Power structure 7
3.3 DC/DC circuit reference design 7
4. PIN DESCRIPTION 8
4.1 Pin description 8
5. FUNCTION DESCRIPTION 12
5.1 Power On Sequence 12
5.2 Power Off Sequence 12
5.3 Panel structure 13
5.3.1 Dual Gage Panel Configuration 13
5.3.2 Dual Gage + Zig-zag Panel Configuration 14
5.3.3 Single Gage Panel Configuration 16
5.4 Gamma correction 17
5.4.1 Gamma structure 17
5.5 BIST function 20
5.6 GAS function 21
6. MIPI INTERFACE 23
6.1 DSI protocol 23
6.2 Processor to peripheral (forward direction) packets data types 26
8.3 Nokia command 33
6.3.1 NOP (00h) 34
6.3.2 SWRESET (01h) 35
6.3.3 RDDIDIF (04h) 36
6.3.4 RDNUMPE (05h) 37
6.3.5 REDRD (06h) 38
6.3.6 REDGREEN (07h) 39
6.3.7 REDBLUE (08h) 40
6.3.8 RDDST (09h) 41
6.3.9 RDDPM (0Ah) 43
6.3.10 RDDMATCDL (0Bh) 44
6.3.11 RDDIM (0Dh) 45
6.3.12 RDDSM (0Eh) 46
6.3.13 RDDSDR (0Fh) 47
6.3.14 SLPIN (10h) 48
6.3.15 SLPOUT (11h) 49
6.3.16 INVOFF (20h) 50
6.3.17 INVON (21h) 51
6.3.18 ALLPOFF (22h) 52
6.3.19 ALLPOON (23h) 53
6.3.20 DISPOFF (28h) 54
6.3.21 DISPON (29h) 55
6.3.22 TEOFF (34h) 56
6.3.23 TEOFF (35h) 57
6.3.24 DISPON (36h) 58
6.3.25 IDMOFF (38h) 60
6.3.26 IDMON (39h) 61
6.3.27 TESL (44h) 62
6.3.28 GETTSCAN (45h) 63
6.3.29 WRIMC (80h) 64
6.3.30 RDRIMC (81h) 65
6.4 MIPI video input timing 66
6.4.1 MIPI transmission packet sequences 67
6.5 MIPI timing characteristic 71
6.6 MIPI DC characteristic 72
6.7 MIPI AC characteristic 73
6.7.1 LP Transmitter AC Specification 73
6.7.2 Turnaround Procedure 74
6.7.3 High Speed Clock and Data Transmission Procedure 75

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7. SPI FORMAT 77
7.1 3-wire SPI format 77
7.1.1 3-wire SPI interface Ⅰ 77
7.1.2 3-wire SPI interface Ⅱ 79
7.2 3-wire interface characteristics 81
8. I2C FORMAT 82
8.1 Register write sequence of I^2C interface 82
8.2 Register read sequence of I^2C interface 83
9. DC CHARACTERISTICS 84
9.1 Absolute maximum ratings 84
9.2 Typical operating condition 84
9.3 VDD power on slew time 85
9.4 Timing requirements for RESX 85
10. REVISION HISTORY 86

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1. General Description

JD9165 is a one-chip solution for Amorphous Si TFT LCD panel. The source driver integrates 1538 source channels, a timing controller, and supports GOA control circuits for the middle size panel application. In addition, the chip also provides Gamma reference voltage and VCOM voltage.

JD9165 also supports various types of peripheral interface such as MIPI interface without frame memory and provide 60Hz frame rate. The serial communication interface is also embedded for function setting.

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2. Features

- Single chip solution for Amorphous Si TFT LCD display
- Integrated 1538 channel source driver
- Support panel resolution (HxV):
  - 1024RGBx768, (256RGB+4*n)xV
- Embedded GOA circuit, support 22 GOUT pins each on R-side/L-side
- Panel type:
  - Single chip: Dual gate panel/Dual gate+Zig-zag panel/Single gate panel
- Inversion architecture:
  - Column inversion
  - 1+2 dot inversion
  - 2 dot inversion
  - Dot inversion
- Support Normally black and white panel
- Provide total 26 register value for gamma correction adjustment
- Support BIST mode
- Support GAS function for abnormal power off
- Support SPI/I2C interface
- Source driver output with 8-bit DAC
- OTP memory to store initialization register settings
  - OTP for GOA setting
  - OTP for Gamma setting
  - 6 times OTP for VCOM setting
- Input power supply:
  - VDD=1.71V to 2.0V / 2.5V to 3.3V **(power supply for digital circuit)**
  - AVDD=9V to 11V **(power supply for analog circuit)**
  - VCOM=2.7V to 4.94V **(power supply for analog circuit)**
  - VGH=15V to 20V **(power supply for GOA circuit)**
  - VGL= -6V to -12V **(power supply for GOA circuit)**
- Support MIPI DSI version 1.02
- Support MIPI D-PHY version 1.00
- Support MIPI 1port interface
- COG package
- Operating temperature **(T_A)**: -20℃ to +85℃
- Storage temperature **(T_{STG})**: -55℃ to +125℃

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3. BLOCK DIAGRAM

3.1 Function block diagram

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3.2 Power structure

3.3 DC/DC circuit reference design

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4. PIN DESCRIPTION

4.1 Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">MIPI interface pins</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>In</td><td>MIPI data input pin.
If not used, please float this pin.</td></tr>
<tr><td>CKP/CKN</td><td>In</td><td>MIPI clock input pin.
If not used, please float this pin.</td></tr>
<tr><td colspan="3">Global pins</td></tr>
<tr><td>RESX
(VDD)</td><td>In</td><td>Global reset pin, active low. (Default pull High)</td></tr>
<tr><td>STBYB
(VDD)</td><td>In</td><td>Standby mode selection.(Default pull High)
STBYB=H, Normal mode.
STBYB=L, Standby mode.</td></tr>
<tr><td>DSWAP[1:0]
(VDD)</td><td></td><td>These pins must be connected to VDD or VSSD. DSWAP[1:0] are used for the combination of data lane swap of DSI. (Default DSWAP[1:0]=11b)
<table>
<tr><th rowspan="2">DSWAP[1:0]</th><th>DP0</th><th>DN0</th><th>DP1</th><th>DN1</th><th>CKP</th><th>CKN</th><th>DP2</th><th>DN2</th><th>DP3</th><th>DN3</th></tr>
<tr><th colspan="10">MIPI lanes mapping table</th></tr>
<tr><td>00</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>CKP</td><td>CKN</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td></tr>
<tr><td>01</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>CKP</td><td>CKN</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
<tr><td>10</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>CKP</td><td>CKN</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td></tr>
<tr><td>11</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>CKP</td><td>CKN</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
</table></td></tr>
<tr><td>PNSWAP
(VDD)</td><td>In</td><td>MIPI polarity selection. (Default pull Low)
<table>
<tr><th rowspan="2">PNSWAP</th><th>D0P/N</th><th>D1P/N</th><th>CKP/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><th colspan="5">MIPI lanes mapping table</th></tr>
<tr><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
</table></td></tr>
<tr><td>LANSEL[1:0]
(VDD)</td><td>In</td><td>MIPI lane number configuration. (Default LANSEL[1:0]=11b)
<table>
<tr><th>LANSEL[1:0]</th><th>MIPI lane number</th></tr>
<tr><td>00</td><td>1 lane</td></tr>
<tr><td>01</td><td>2 lanes</td></tr>
<tr><td>10</td><td>3 lanes</td></tr>
<tr><td>11</td><td>4 lanes</td></tr>
</table></td></tr>
<tr><td>IFSEL[1:0]
(VDD)</td><td>In</td><td>Interface selection. (Default IFSEL[1:0]=00b)
<table>
<tr><th>IFSEL[1:0]</th><th>Interface</th></tr>
<tr><td>00</td><td>T.B.D.</td></tr>
<tr><td>01</td><td>MIPI</td></tr>
<tr><td>10</td><td>T.B.D.</td></tr>
<tr><td>11</td><td>T.B.D.</td></tr>
</table></td></tr>
<tr><td>BIST_EN
(VDD)</td><td>In</td><td>BIST mode enable, high active. (Default pull Low)</td></tr>
<tr><td>SHLR
(VDD)</td><td>In</td><td>Horizontal scan direction. (Default pull Low)
<table>
<tr><th>SHLR</th><th>Function</th></tr>
<tr><td>1</td><td>S1537→S1536→.....S1→S0</td></tr>
<tr><td>0</td><td>S0→S1→.....S1536→S1537</td></tr>
</table></td></tr>
</table>

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UPDN (VDD)	In	Vertical scan direction. **(Default pull Low)** UPDN: 1 — Bottom → Top UPDN: 0 — Top → Bottom
ZIGZAG_ENB (VDD)	In	Dual gata or Zig-zag panel setting. **(Default pull High)** ZIGZAG_ENB: 1 — Dual gate panel ZIGZAG_ENB: 0 — Dual gate+Zig-zag panel
PTYPE[1:0] (VDD)	In	Panel layout type selection. **(Default PTYPE[1:0]=00b)** PTYPE[1:0]: 00 — Dual gate panel: Dual gate layout type1; Zig-zag panel: Zig-zag layout type1 PTYPE[1:0]: 01 — Dual gate panel: Dual gate layout type1; Zig-zag panel: Zig-zag layout type2 PTYPE[1:0]: 10 — Dual gate panel: Dual gate layout type2; Zig-zag panel: Zig-zag layout type3 PTYPE[1:0]: 11 — Dual gate panel: Dual gate layout type2; Zig-zag panel: Zig-zag layout type4
INVSEL (VDD)	In	Inversion type selection. **(Default pull High)** (only for dual gate panel, single gate panel = dummy function) INVSEL: 1 — 1+2dot INVSEL: 0 — 2 dot
NBW (VDD)	In	Normally black or normally white setting. **(Default pull Low)** NBW: 1 — Normally white panel NBW: 0 — Normally black panel
CMD_SEL[1:0] (VDD)	In	Command interface selection. **(Default CMD_SEL[1:0]=00b)**. CMD_SEL1: 0, CMD_SEL0: 0 — 3-wire SPI Ⅰ CMD_SEL1: 0, CMD_SEL0: 1 — 3-wire SPI Ⅱ CMD_SEL1: 1, CMD_SEL0: X — I2C MIPI and SPI/I2C command can't receive at the same time.
VCOMIN_SEL (VDD)	In	Internal/External VCOM selection.**(Default pull Low)** VCOMIN_SEL: 1 — External VCOM VCOMIN_SEL: 0 — Internal VCOM
VCOM_EN (VDD)	In	VCOM buffer selection. **(Default pull High)** VCOM_EN: 1 — VCOM buffer enable VCOM_EN: 0 — VCOM buffer disable
VMIDOP_EN (VDD)	In	Internal/external VMIDOP selection.**(Default pull Low)** VMIDOP_EN: 1 — VMIDOP Enable VMIDOP_EN: 0 — VMIDOP Disable
VDD18V_BPS (VDD)	In	VDD bypass mode selection.**(Default pull Low)** VDD18V_BPS: 1 — Enable VDD18V_BPS: 0 — Disable
LEDPWM	Out	This pin is connected to the external LED driver. PWM type control signal for brightness of the LED backlight. If not used, please float this pin.
Panel control pins		

S[1537:0]	Out	Source Driver output signals. **(If not used, let it open).**
GOUT_L[22:1]	Out	GOA control signal at left side. **(If not used, let it open).**
GOUT_R[22:1]	Out	GOA control signal at right side. **(If not used, let it open).**
Power pins		
VDD_R/VDD_L	In	Power supply for digital circuits. VDD=1.71V to 2.0V / 2.5V to 3.3V
VDDIO	In	Power supply for I/O circuits. VDDIO=1.71V to 2.0V / 2.5V to 3.3V
AVDD	In	Power supply for analog circuits. AVDD=9V to 11V.
VGH_R/VGH_L	In	Power supply for GOA circuits. VGH=15V to 20V.
VGL	In	Power supply for GOA circuits. VGL= -6V to -12V.
VDD_18V	Out	Internal power supply for logic circuits. Connect to a stabilizing capacitor.
VDD_18V_IF	Out	Internal power supply for interface circuits. Connect to a stabilizing capacitor.
VDD_12V_IF	Out	VDDLP LDO output for MIPI LP mode TX use. VDDLP LDO enable on MIPI interface. (IFSEL[1:0]=01b)
VREF	Out	Internal reference voltage.
VMID_R[1:0] VMID_L[1:0]	I/O	Power supply for analog circuits (VMID=1/2*AVDD).
VMID_OP	Out	VMID OP output (VMID=1/2*AVDD).
VQHI_R/VQHI_L	Out	Internal source reference voltage (7V to 7.5V).
VQLI_R/VQLI_L	Out	Internal source reference voltage (2.5V to 3V).
VQHO	Out	Internal source reference voltage (0.7AVDD).
VQLO	Out	Internal source reference voltage (0.2AVDD).
VCOMIN	In	VCOM buffer in.
VCOM_OP	Out	VCOM buffer out (2.7V to 4.94V).
VOTP	In	External OTP voltage input pin and operates at 7.75V. **(If not used, let it open).**
VPP_REN	Out	Internal high voltage pin used in OTP mode and operates at 7.75V. **(If not used, let it open).**
VSS	In	GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.

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VSSA	In	Analog ground. VSS=0V. When using the COG method, connect to VSS on the FPC to prevent noise.
VSS_IF	In	Ground for interface, connect to VSS.
Shielding_VSSA	In	Internal shielding ground pin. connect to VSSA.
Serial interface pins		
CSB (VDD)	In	Serial Interface chip enable signal for SPI interface. SPI_CSB=0: Selected (Accessible). SPI_CSB=1: Not selected (Inaccessible).
SCL (VDD)	In	Serial interface clock input for SPI interface.
SDI (VDD)	I/O	Serial interface address and data input/output for SPI interface.
SDO (VDD)	I/O	Serial interface data output for SPI interface.
SDA_I2C (VDD)	I/O	Serial interface address and data input/output for I2C interface. (I2C interface need external pull high resistance.)
SCL_I2C (VDD)	In	Serial interface clock input for I2C interface. (I2C interface need external pull high resistance.)
Test pins		
TEST_I[25:0]	In	Internal test pins. **Please let it open.**
TEST_O[19:0]	Out	Internal test pins. **Please let it open.**
TEST_VDD[0]	In	Internal test pins. **Please let it open.**
TEST_HV_I[1:0]	In	Internal test pins. **Please let it open.**
TEST_MV_I[1:0]	In	Internal test pins. **Please let it open.**
TEST_HV_O[1:0]	Out	Internal test pins. **Please let it open.**
TEST_MV_O[1:0]	Out	Internal test pins. **Please let it open.**
Dummy pins		
DUMMY[1]/[36]	In	Dummy pins. **Please let it open.**

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5. FUNCTION DESCRIPTION

5.1 Power On Sequence

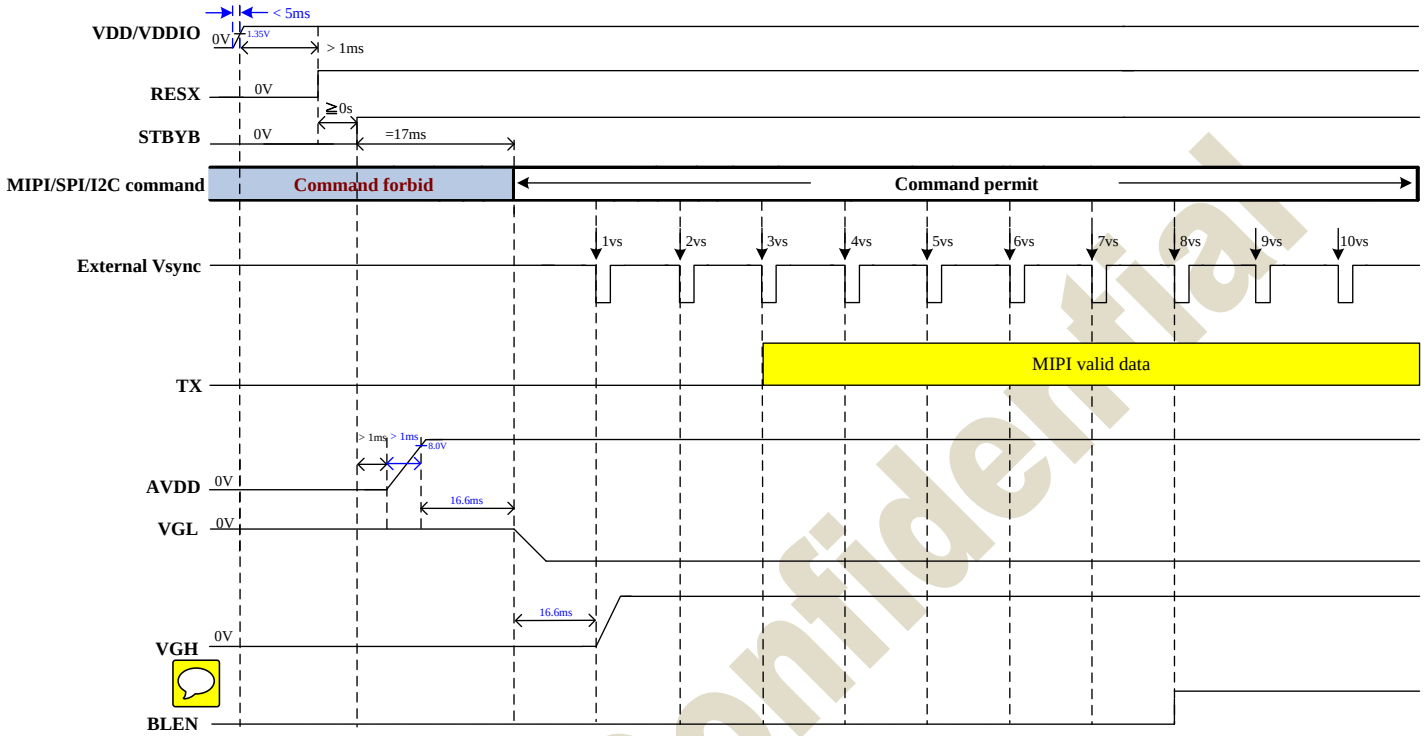

Figure 5.1: Power On timing chart

5.2 Power Off Sequence

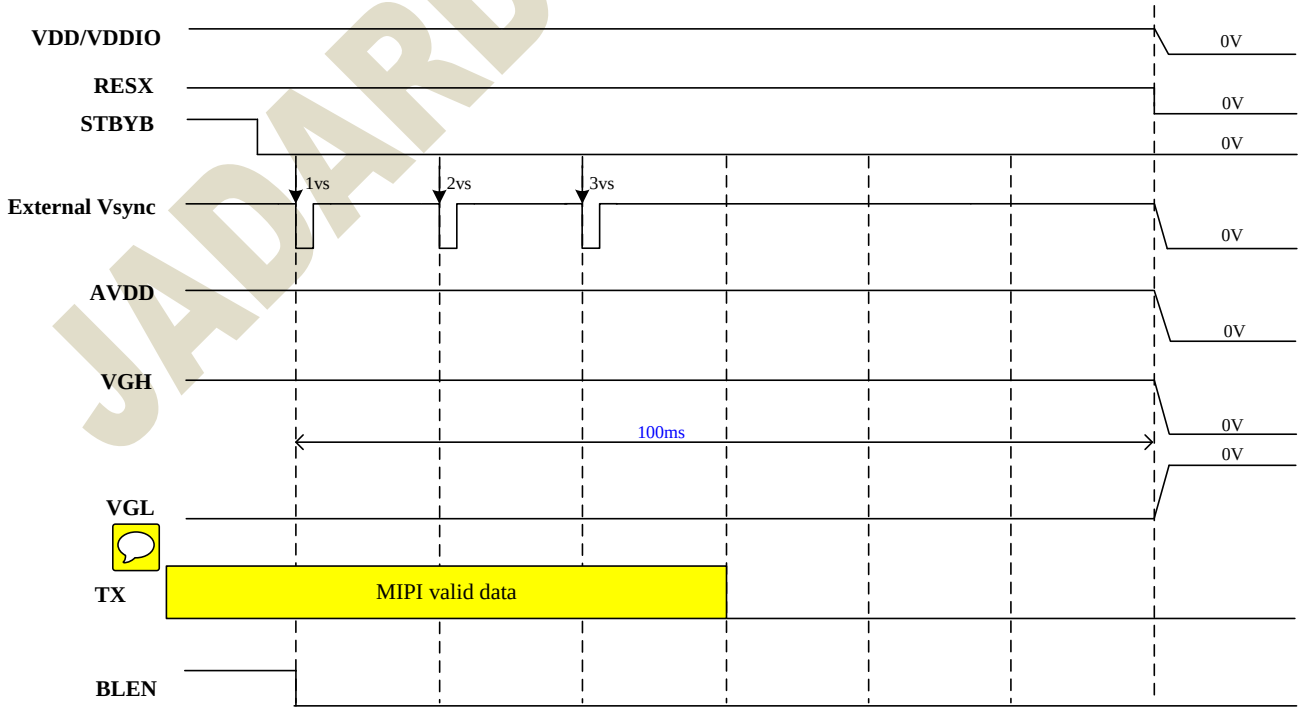

Figure 5.2: Power Off timing chart

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5.3 Panel structure

JD9165 can support 3 types of driving method – Dual gate panel, Dual gate+Zig-Zag, and Single gate driving.

5.3.1 Dual Gage Panel Configuration

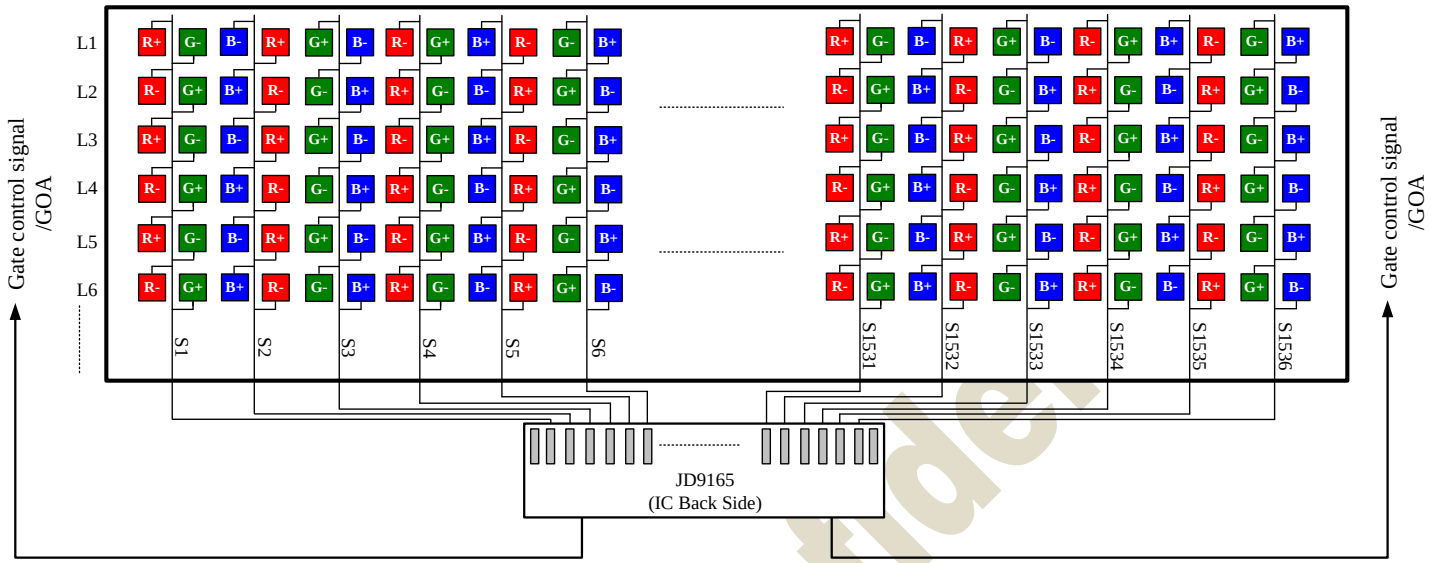

Figure 5.3: Dual gate type1 panel structure

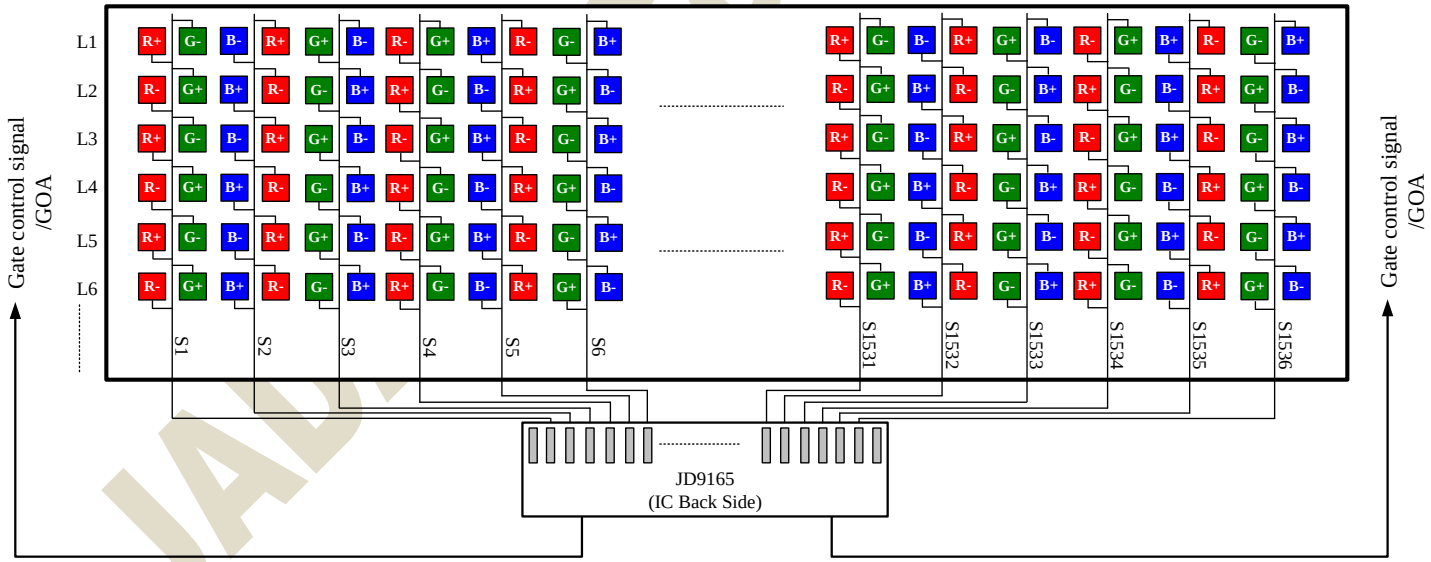

Figure 5.4: Dual gate type2 panel structure

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5.3.2 Dual Gage + Zig-zag Panel Configuration

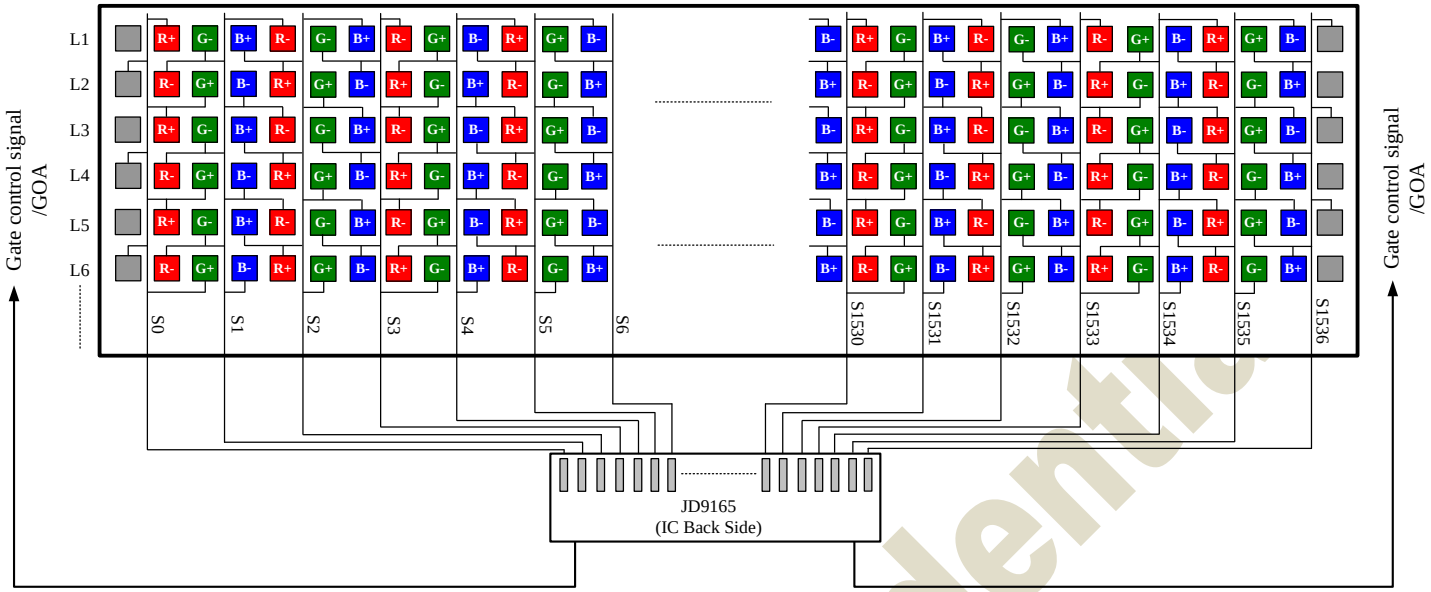

Figure 5.5: Dual gate+Zig-zag type1 panel structure

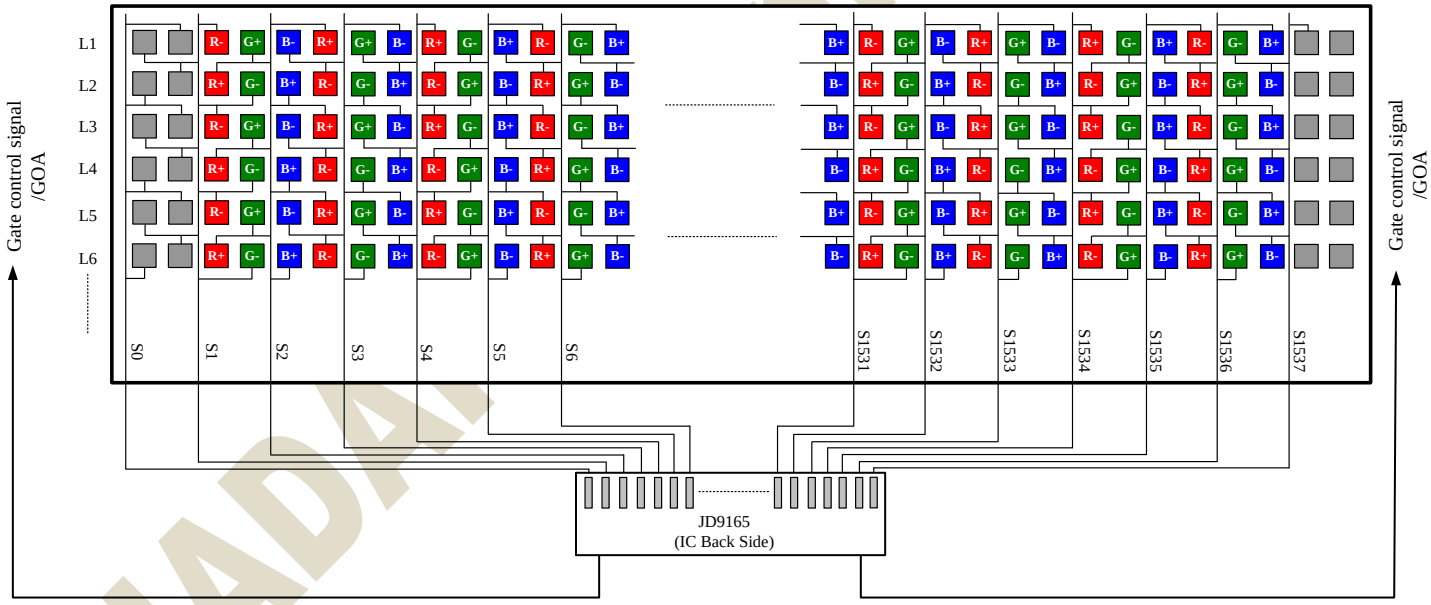

Figure 5.6: Dual gate+Zig-zag type2 panel structure

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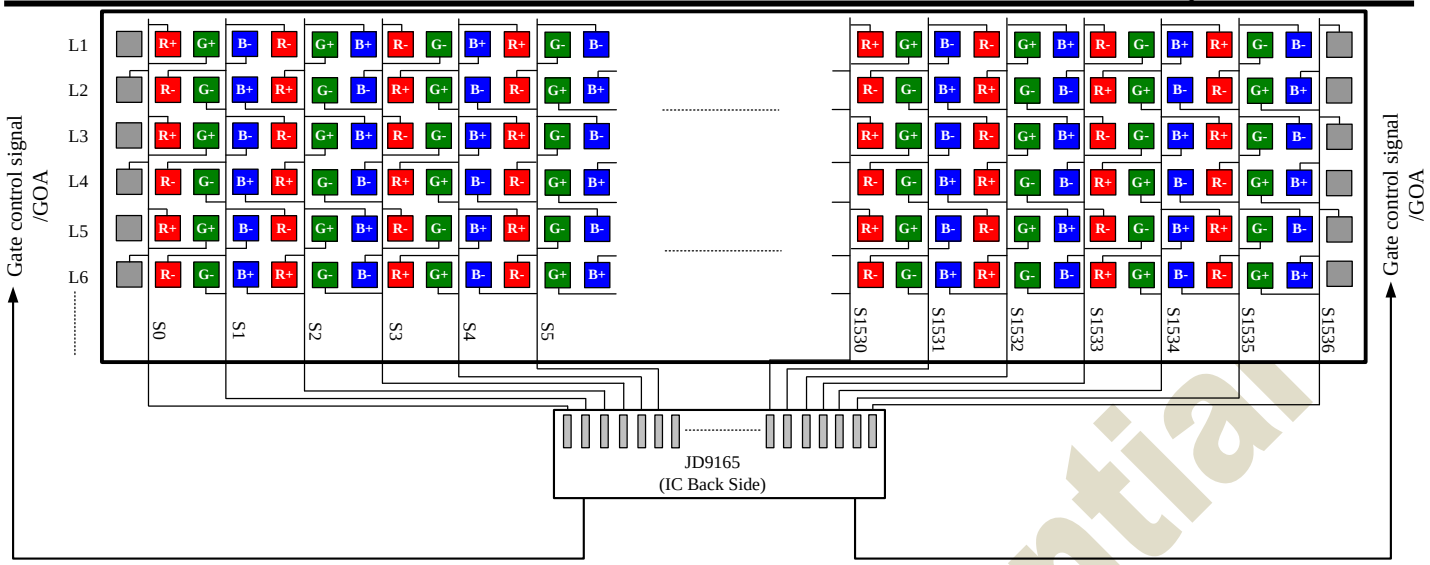

Figure 5.7: Dual gate+Zig-zag type3 panel structure

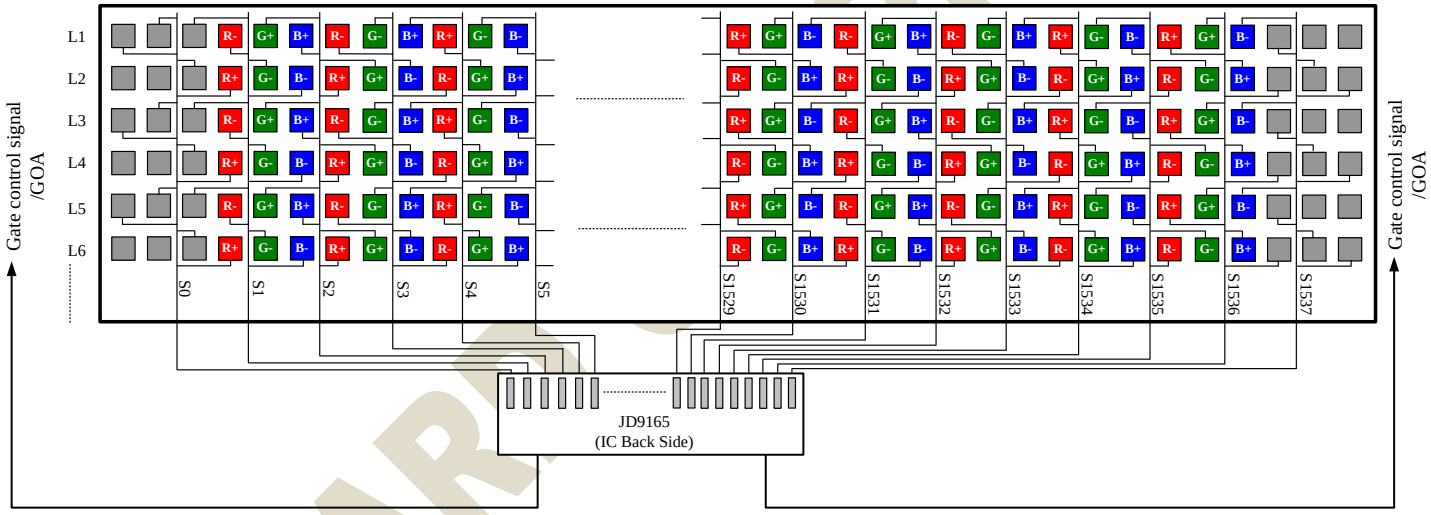

Figure 5.8: Dual gate+Zig-zag type4 panel structure

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5.3.3 Single Gage Panel Configuration

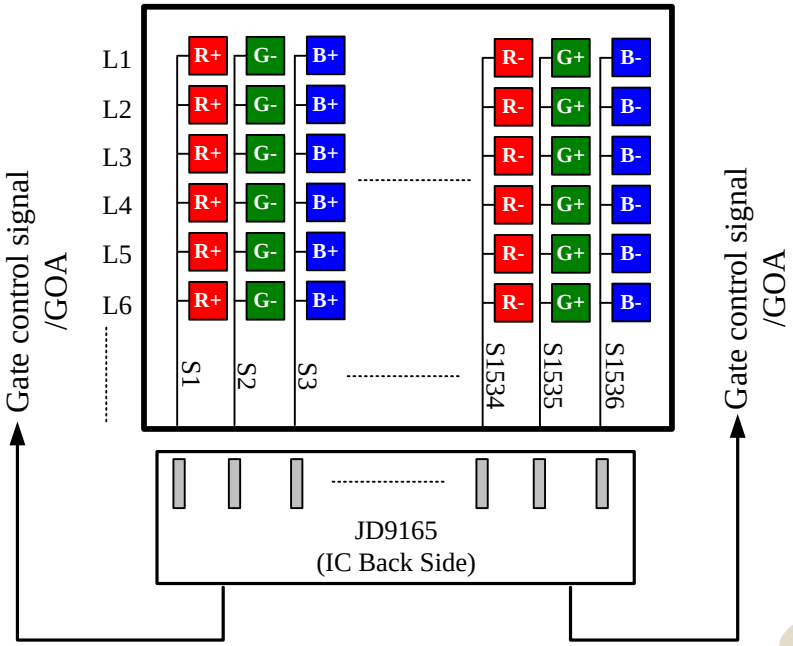

Figure 5.9: Single gate panel structure

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5.4 Gamma correction

JD9165 gamma correction are done by 13-segment piecewise linear interpolation. The 13 segments are defined with 14 register values for level 0, 4, 8, 14, 22, 47, 143, 175, 207, 232, 240, 246, 251, 255.These gamma register stream has 128-1 selector to adjust voltage.

5.4.1 Gamma structure

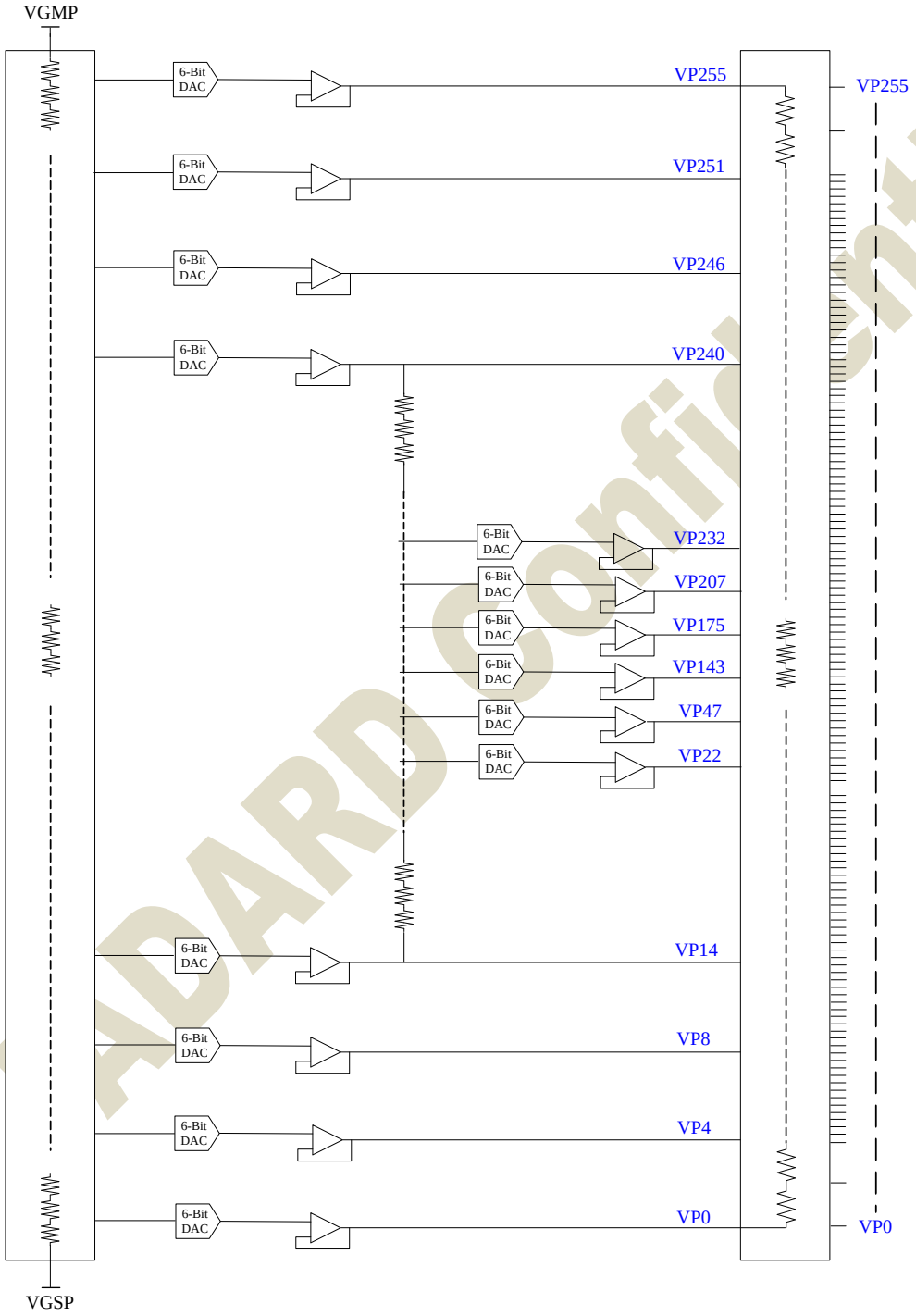

Figure 5.10: Positive analog gamma structure

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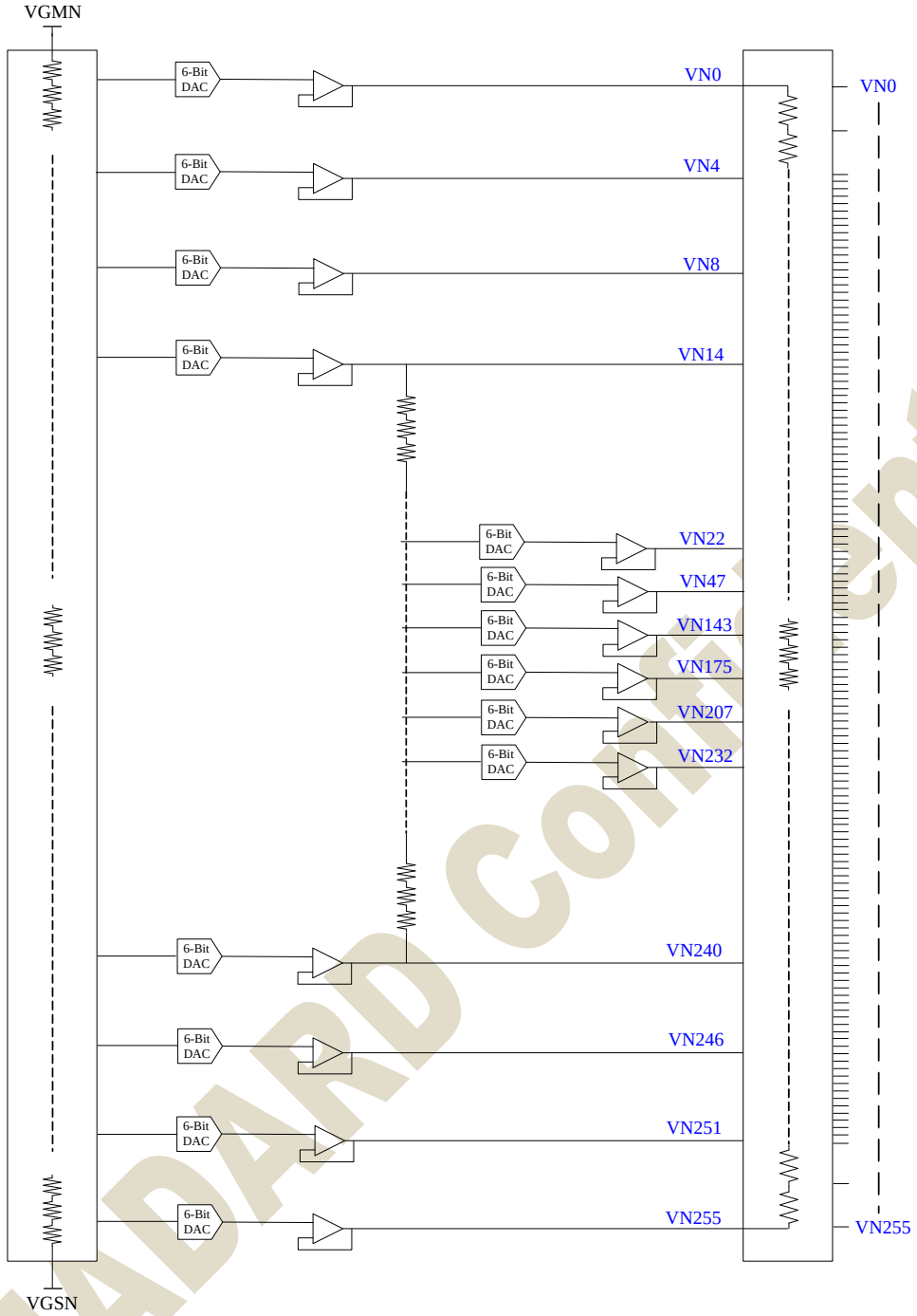

Figure 5.11: Negative analog gamma structure

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5.4.2 Gamma voltage reference table

The reference voltages can be set by registers, as described in the following table.

Setting for positive gamma voltage

Gamma code	Reference voltage
VP0	VGSP + (1/200)*(VP0[5:0])*(VGMP-VGSP)
VP4	VGSP + (1/200)*(VP4[5:0]+1)*(VGMP-VGSP)
VP8	VGSP + (1/200)*(VP8[5:0]+4)*(VGMP-VGSP)
VP14	VGSP + (1/200)*(VP14[5:0]+6)*(VGMP-VGSP)
VP22	VP14+ (1/600)*(VP22[5:0]+4)*(VP240-VP14)
VP47	VP14+ (1/600)*(VP47[5:0]+60)*(VP240-VP14)
VP143	VP14+ (1/600)*(VP143[5:0]+150)*(VP240-VP14)
VP175	VP14+ (1/600)*(VP175[5:0]+180)*(VP240-VP14)
VP207	VP14+ (1/600)*(VP207[5:0]+420)*(VP240-VP14)
VP232	VP14+ (1/600)*(VP232[5:0]+520)*(VP240-VP14)
VP240	VGSP + (1/200)*(VP246[5:0]+134)*(VGMP-VGSP)
VP246	VGSP + (1/200)*(VP246[5:0]+134)*(VGMP-VGSP)
VP251	VGSP + (1/200)*(VP251[5:0]+136)*(VGMP-VGSP)
VP255	VGSP + (1/200)*(VP255[5:0]+137)*(VGMP-VGSP)

Setting for negative voltage

Gamma code	Reference voltage
VN0	VGSN + (1/200)*(VN0[5:0])*(VGMN–VGSN)
VN4	VGSN + (1/200)*(VN4[5:0]+ 1)*(VGMN–VGSN)
VN8	VGSN + (1/200)*(VN8[5:0]+ 4)*(VGMN–VGSN)
VN14	VGSN + (1/200)*(VN14[5:0]+ 6)*(VGMN–VGSN)
VN22	VN14 + (1/600)*(VN22[5:0] + 4)*(VN240– VN14)
VN47	VN14 + (1/600)*(VN47[5:0] + 60)*(VN240– VN14)
VN143	VN14 + (1/600)*(VN143[5:0] + 150)*(VN240– VN14)
VN175	VN14 + (1/600)*(VN175[5:0] + 180)*(VN240– VN14)
VN207	VN14 + (1/600)*(VN207[5:0] + 420)*(VN240– VN14)
VN232	VN14 + (1/600)*(VN232[5:0] + 520)*(VN240– VN14)
VN240	VGSN + (1/200)*(VN240[5:0] + 128)*(VGMN–VGSN)
VN246	VGSN + (1/200)*(VN246[5:0] + 134)*(VGMN–VGSN)
VN251	VGSN + (1/200)*(VN251[5:0] + 136)*(VGMN–VGSN)
VN255	VGSN + (1/200)*(VN255[5:0] + 137)*(VGMN–VGSN)

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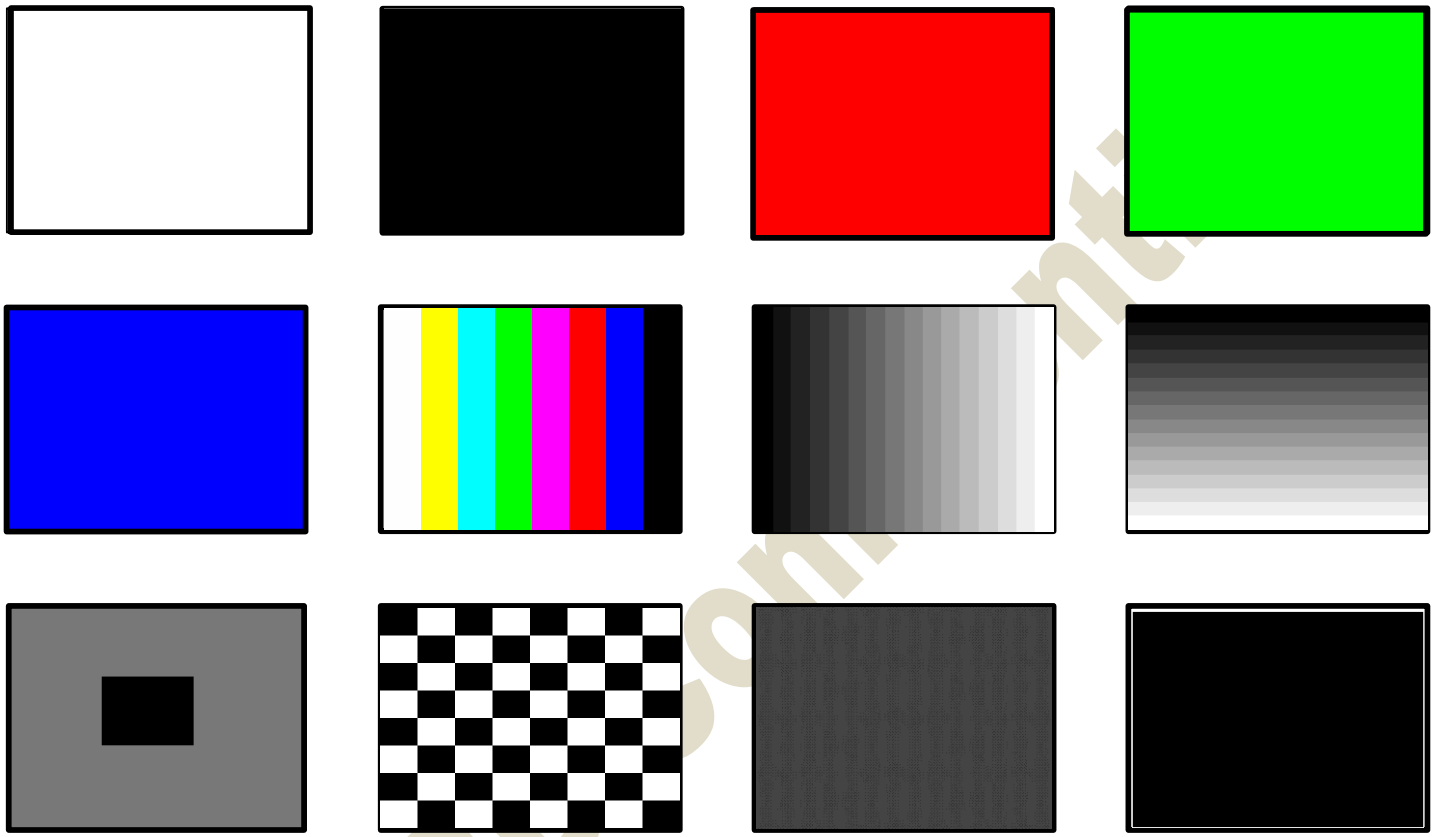
5.5 BIST function

When BIST is trigger to high, then JD9165 will leave normal operation mode and starts to generate the BIST pattern to LCD panel without TX input signals.

5.5.1 BIST pattern



White→Black→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Gray128→Black background with white out frame

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5.6 GAS function

When battery is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS function can speed the process that image disappears.

The GAS function is a voltage detector. By GAS circuit, JD9165 can detect voltage of VDD/AVDD/VGH and sent ideal GAS signal to discharge residual potential in LCD panel and removes image. The detect voltage could be selected by register setting.

When VDD recovers, power on procedure must be done to return normal mode.

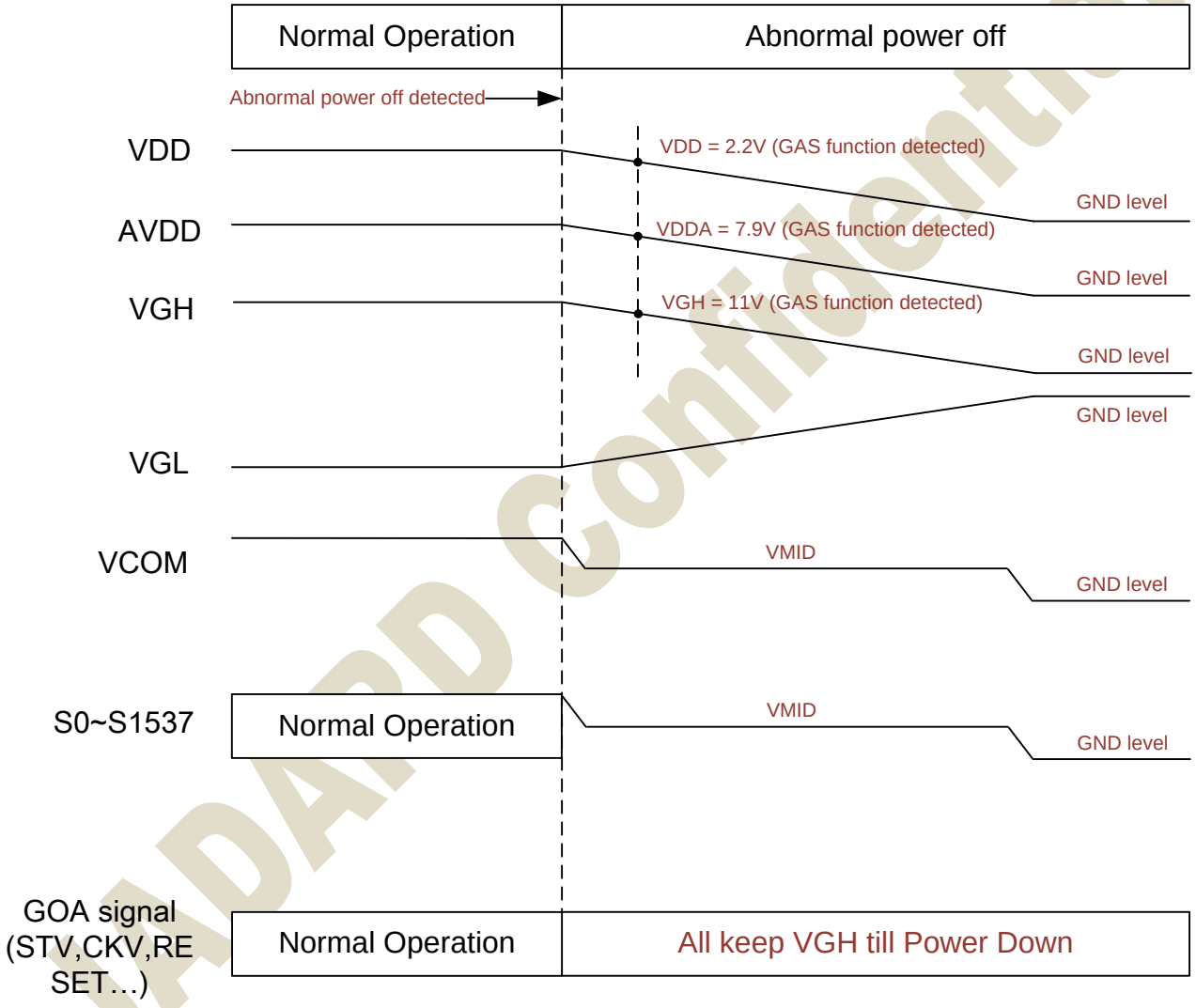

Figure 5.12: GAS discharge timing

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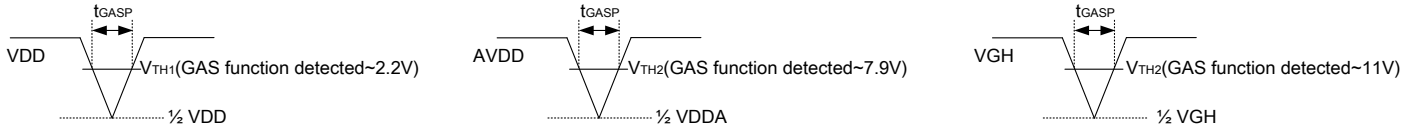

Figure 5.13: GAS V.S. VDD/AVDD/VGH

Parameter	Symbol	Step	Spec			Unit
			Min	Typ	Max	
VDD/AVDD power drop noise filter period.	T_{GASP}	-	100	-	-	ns
GAS function detection threshold voltage. VDD lower than V_{TH1}, IC will execute GAS function	V_{TH1}	0.1	1.6	2.2	3.0	V
GAS function detection threshold voltage. AVDD lower than V_{TH2}, IC will execute GAS function	V_{TH2}	0.5	7.11	7.9	8.3	V
GAS function detection threshold voltage. VGH lower than V_{TH3}, IC will execute GAS function	V_{TH3}	0.5	11	11	15	V

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6. MIPI INTERFACE

6.1 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure is illustrates multiple HS Transmission packets.

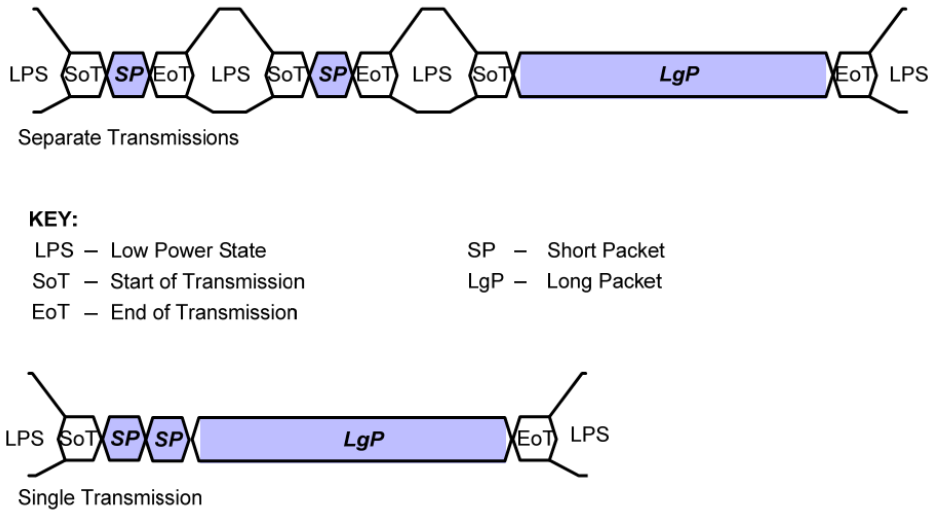
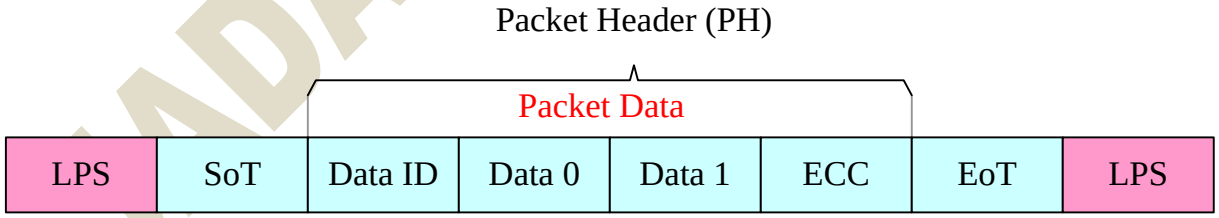


Figure 6.1: Multiple packets transmission

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier **(DI)**, includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

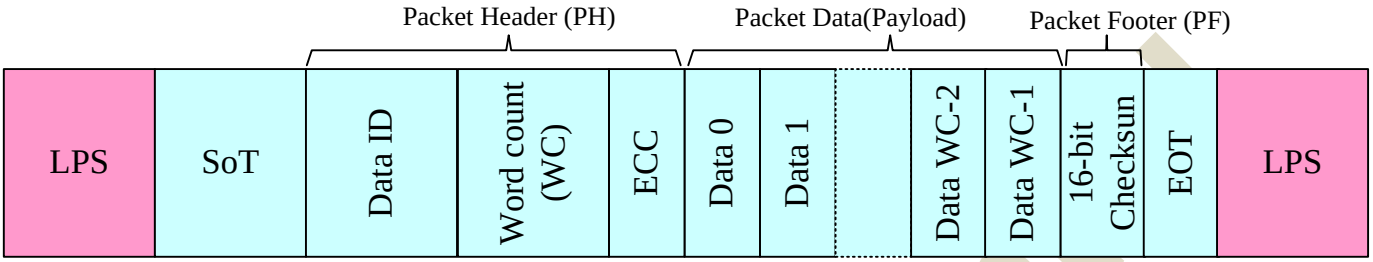


Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

Figure 6.2: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,535 bytes in length. Thus Long packets permit

transmission of large blocks of pixel or other data. Figure 7.3 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = 4 bytes PH + (2_{16}-1) bytes Payload + 2 bytes PF



Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
WC **(Word Count)**: The receiver uses WC to determine the packet end.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF **(Packet Footer)**: Mean 16-bit Checksum.

Figure 6.3: Structure of the long packet

According to packet form, basic elements include DI and ECC. Below Table is shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		**DT (Data Type)**					

Note: (1) DI[7:6]_These two bits identify the data as directed to one of four virtual channels.
DI[5:0]_These six bits specify the Data Type, which specifies the size, format, and in some case, the interpretation of the packet contents.

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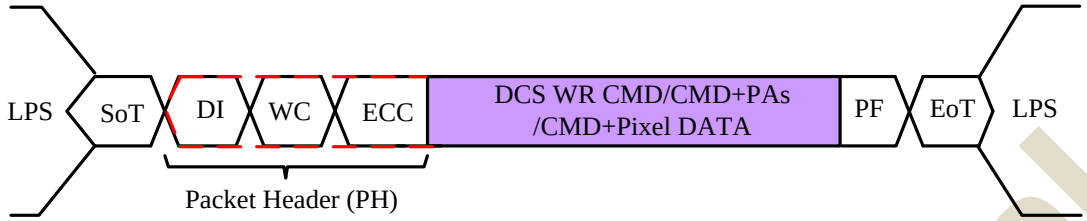
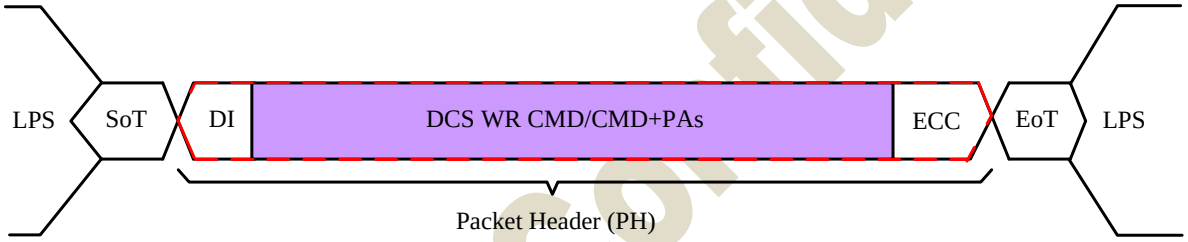
Due to Data Type **(DT)** mean format of transmission type. Below Figure 7.5 is shows short / long-packet transmission command sequence. Long packet writes command / parameters / pixel Data



Note: (1) DI: Write suitable Data type.
WC: Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD+PAs write, WC setting as number of **(CMD+PAs)**.
CMD+DATA write, WC setting as number of **(CMD+Pixel DATA)**.

Figure 6.4: Long packet writes command / parameters



Note: (1) D I: Write suitable Data type.
Ex: One CMD write, DI+DCS WR CMD
CMD+PAs write, DI+DCS WR CMD+PAs.

Figure 6.5: Show short-packet / long-packet transmission command sequence

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6.2 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 8.1 Data Types for Processor-sourced Packets.

Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Size
0	0	0	0	0	1	01	Sync Event, V Sync Start	Short
0	1	0	0	0	1	11	Sync Event, V Sync End	Short
1	0	0	0	0	1	21	Sync Event, H Sync Start	Short
1	1	0	0	0	1	31	Sync Event, H Sync End	Short
0	0	1	0	0	0	08	End of Transmission Packet (EoTP)	Short
0	0	0	0	1	1	03	Generic Short WRITE, no parameters	Short
0	1	0	0	1	1	13	Generic Short WRITE, 1 parameters	Short
1	0	0	0	1	1	23	Generic Short WRITE, 2 parameters	Short
0	0	0	1	0	0	04	Generic Short READ, no parameters	Short
0	1	0	1	0	0	14	Generic Short READ, 1 parameters	Short
1	0	0	1	0	0	24	Generic Short READ, 2 parameters	Short
0	0	0	1	0	1	05	DCS Write, No Parameter	Short
0	1	0	1	0	1	15	DCS Write, 1 Parameter	Short
0	0	0	1	1	0	06	DCS Read, No Parameter	Short
1	1	0	1	1	1	37	Set Maximum Return Packet Size	Short
0	0	1	0	0	1	09	Null Packet, No Data,	Long
0	1	1	0	0	1	19	Blanking Packet, no data	Long
1	0	1	0	0	1	29	Generic Long Write	Long
1	1	1	0	0	1	39	DCS Write Long	Long
1	0	1	1	1	0	2C	Packed Pixel Stream, 16-bit YCbCr, 4:2:2 Format	Long
0	0	1	1	1	0	0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0	1	1	1	1	0	1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
1	0	1	1	1	0	2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
1	1	1	1	1	0	3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x x	x x	0 1	0 1	0 1	0 1	x0 xF	DO NOT USE All unspecified codes are reserved	--

Table 6.1: Data Types for Processor-sourced Packets

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Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type (Hex)	**Function description**	**Number of byte**
01h	V Sync start, Start of VSA pulse.	4 bytes **(DI+00h+00h+ECC)**
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	

Note: (1) V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.

End of Transmission packet (EoT)		
Data type (Hex)	**Function description**	**Number of byte**
08h	End of Transmission packet **(EoTp)**.	4 bytes **(DI+00h+00h+ECC)**

Display status (shutdown command, turn-on command)		
Data type (Hex)	**Function description**	**Number of byte**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes **(DI+00h+00h+ECC)**
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	

Note: (1) When use shutdown command; interface shall remain powered in order to receive the turn-on, or wake-up, command.

Generic Short WRITE Packet with 0,1,2 parameter		
Data type (Hex)	**Function description**	**Number of byte**
03h	Generic Short WRITE, no parameter.	**(DI+00h+00h+ECC)**
13h	Generic Short WRITE, 1 parameter.	**(DI+P1+00h+ECC)**
23h	Generic Short WRITE, 2 parameter.	**(DI+P1+P2+ECC)**

Note: (1) P1=parameter1, P2=parameter2

Generic READ Request with 0,1,2 parameter		
Data type (Hex)	**Function description**	**Number of byte**
04h	Generic READ no parameter.	**(DI+00h+00h+ECC)**
14h	Generic READ 1 parameter.	**(DI+P1+00h+ECC)**
24h	Generic READ 2 parameter.	**(DI+P1+P2+ECC)**

Note: (1) Note: MIPI read only support MIPI 4 lane application.

DCS Short WRITE Command with 0,1 parameter		
Data type (Hex)	**Function description**	**Number of byte**
05h	DCS Short WRITE, no parameter.	**(DI+DCS+00h+ECC)**
15h	DCS Short WRITE, 1 parameter.	**(DI+DCS+P1+ECC)**

Note: (1) P1=parameter1, DCS=DCS Command

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DCS command setting		
Data type (Hex)	**Function description**	**Number of byte**
06h	DCS Read command, the returned data may be of Short or Long packet format.	4 bytes **(DI+DCS CMD+00h+ECC)**
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD +Payload DATA+PF**

Note: (1) For write part, If DCS Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission **(Host _ Slave)**. Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

(2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

- If an error was detected and corrected in Packet Header field by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- If no error was detected by the peripheral, it shall send the requested READ packet **(Short or Long)** with appropriate ECC and Checksum, if either or both features are enabled.

(4) One byte <= Length of payload DATA <= 2_{16}-1

(5) MIPI read only support MIPI 4 lane application.

Return packet size setting		
Data type (Hex)	**Function description**	**Number of byte**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes **(DI+Maximum Return Packet Size+ECC)**

Note: (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

Variable data packet		
Data type (Hex)	**Function description**	**Number of byte**
09h	Null Packet is a mechanism for keeping the serial Data Lane**(s)** in High-Speed mode while sending dummy data.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA +PF)**
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.

(2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display.

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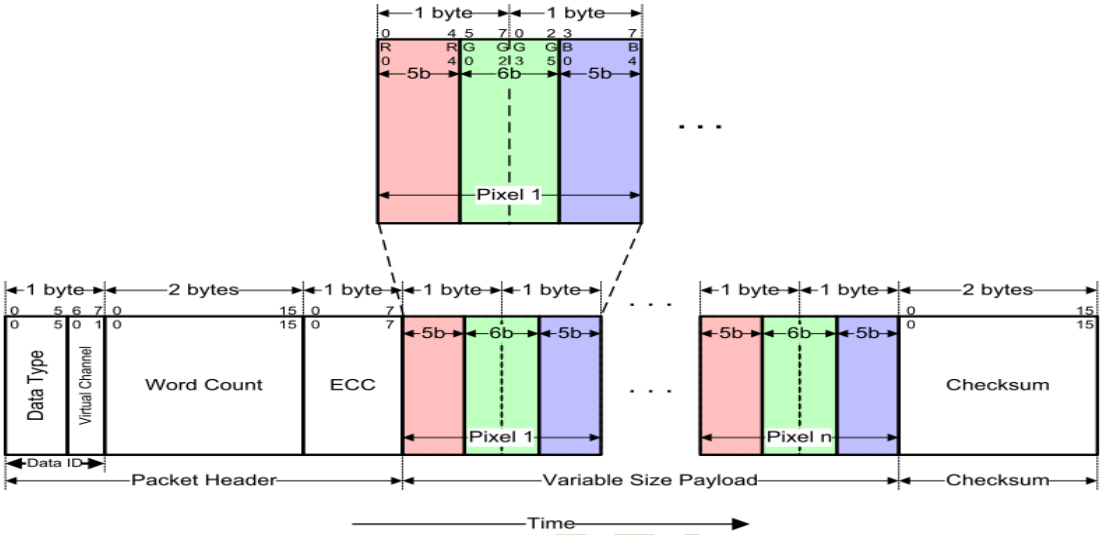
Data stream format – 16bit Format		
Data type (Hex)	**Function description**	**Number of byte**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "**(5-bit)** red, **(6-bit)** green and **(5-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+ PF)**



Note: (1) Within a color component, the "LSB is sent first, the MSB last ".

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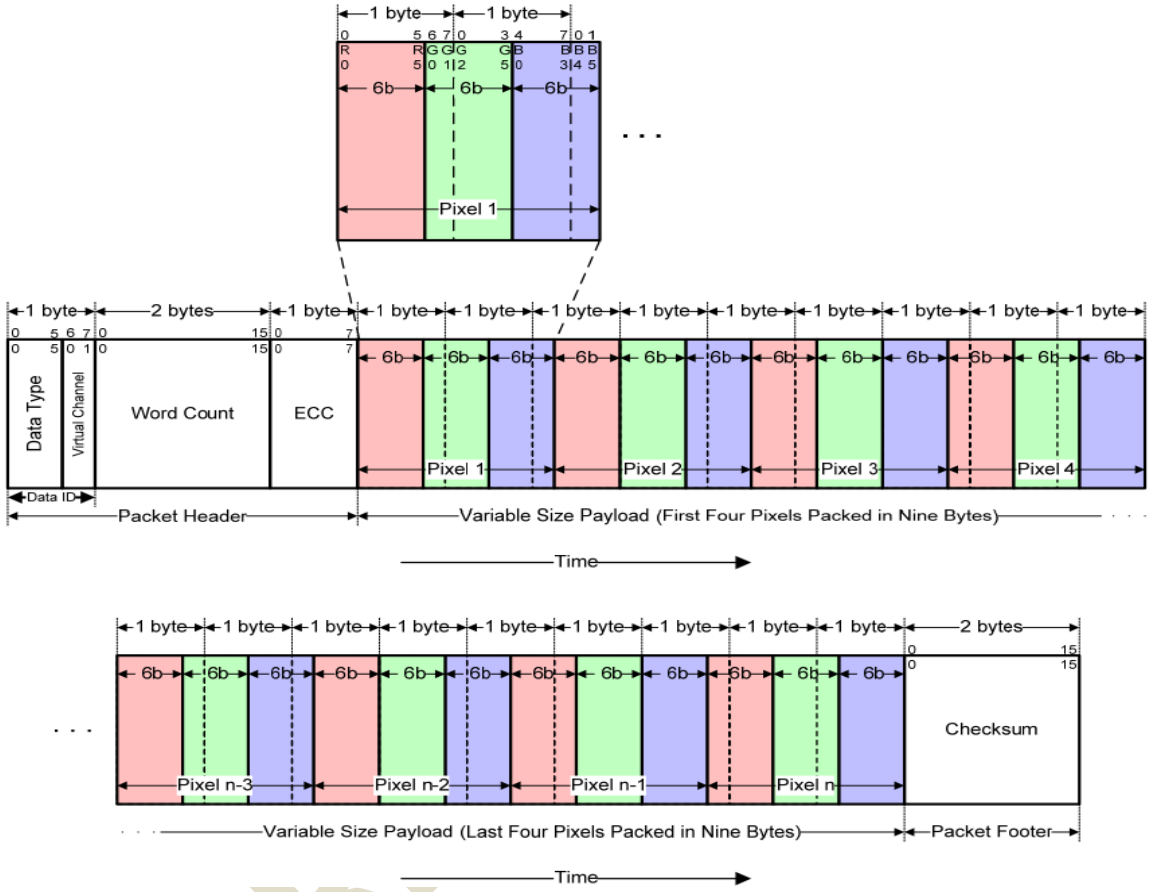
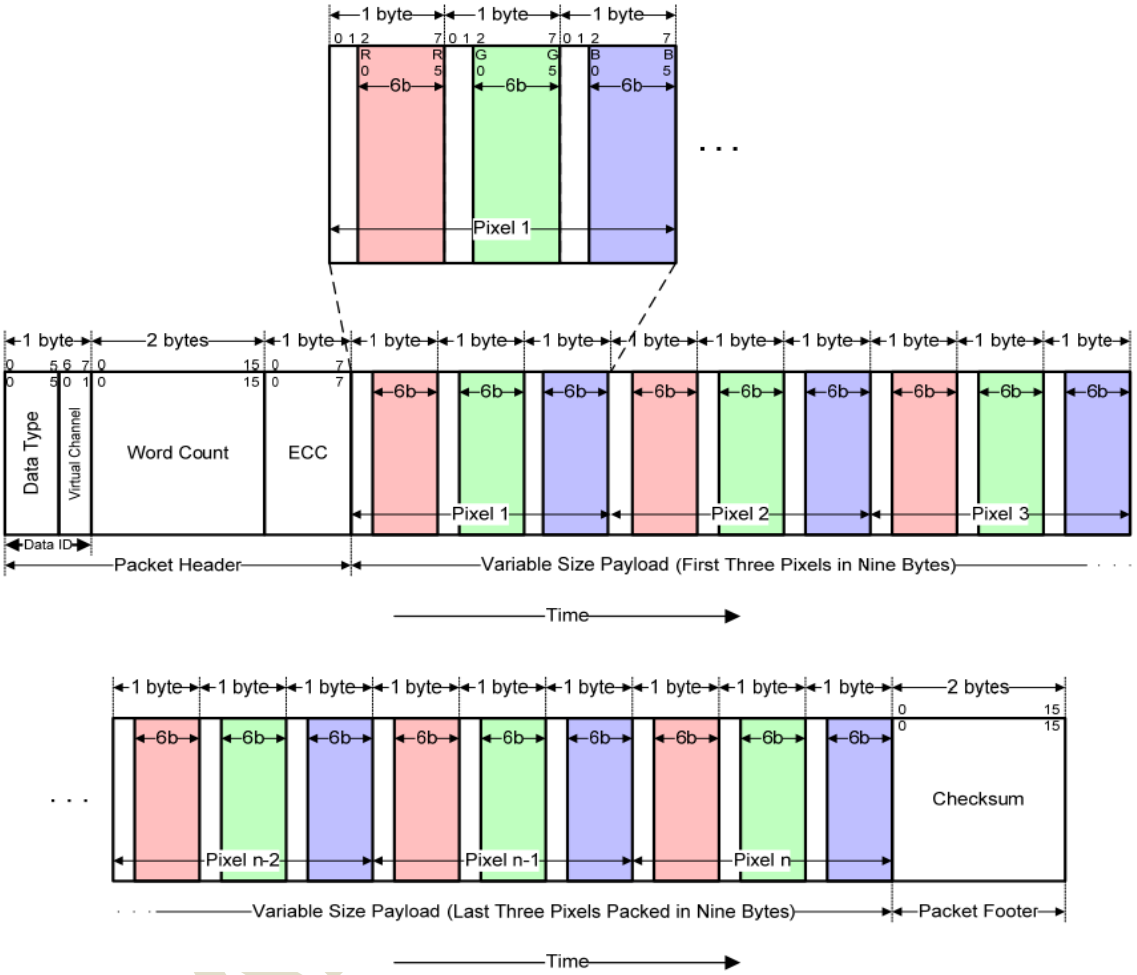
Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of byte**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



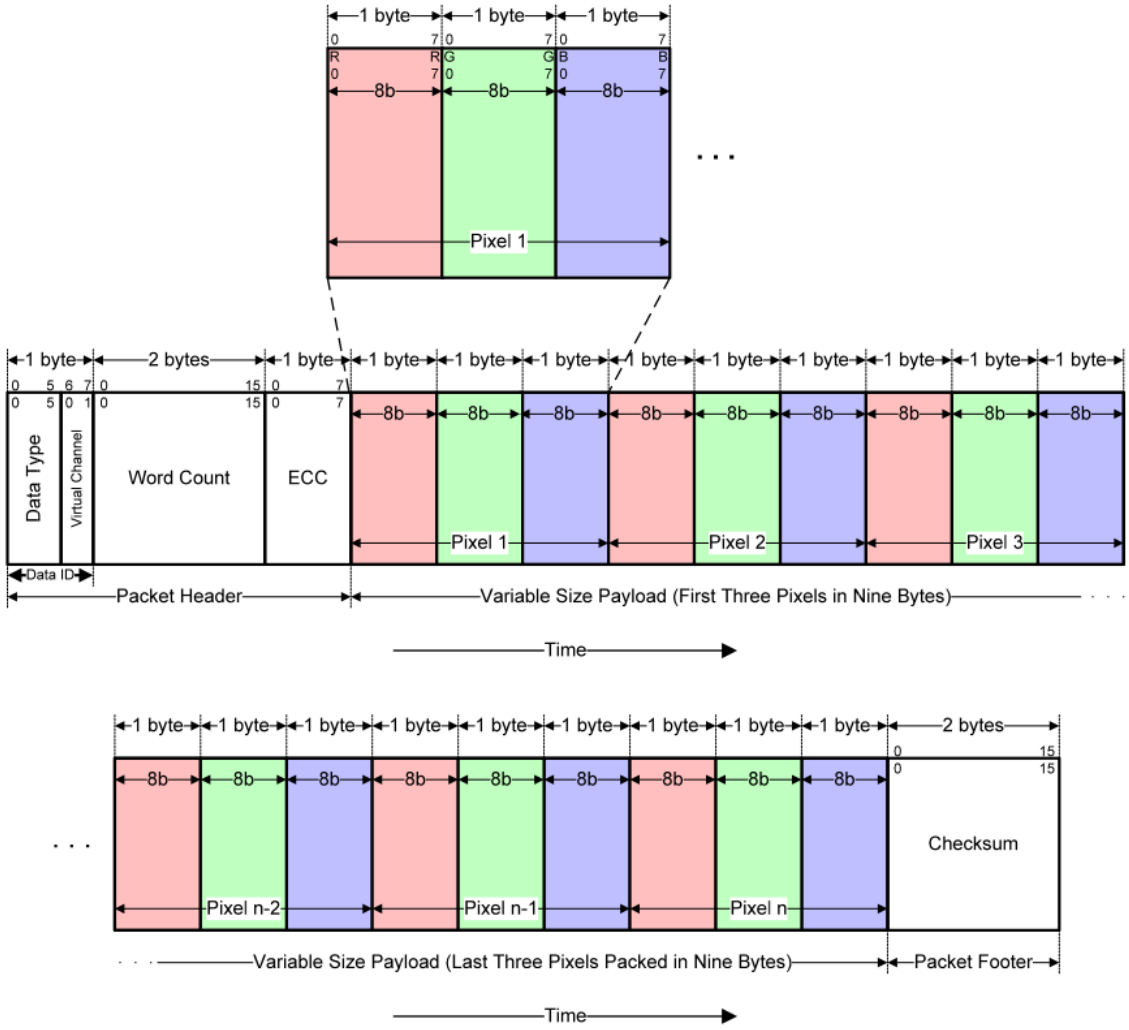
Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels **(nine bytes)**. Preferably, display modules employing this format have a horizontal extent **(width in pixels)** evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of byte**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream forma – 24bit Format		
Data type (Hex)	**Function description**	**Number of byte**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is **(8-bit)** red, **(8-bit)** green and **(8-bit)** blue.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD +Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

8.3 Nokia command

Command	R/W	Hex	Description	Number of Parameters
NOP	W	00h	No operation.	0
SWRESET	W	01h	Software reset.	0
RDDIDIF	R	04h	Read display identification information.	3
RDNUMPE	R	05h	Read number of the parity errors.	1
REDRD	R	06h	Read red color.	1
REDGREEN	R	07h	Read green color.	1
REDBLUE	R	08h	Read blue color.	1
RDDST	R	09h	Read display status.	1
RDDPM	R	0Ah	Read display power mode.	1
RDDMATCDL	R	0Bh	Read display MADCTL.	1
RDDIM	R	0Dh	Read display image mode.	1
RDDSM	R	0Eh	Read display signal mode.	1
RDDSDR	R	0Fh	Read display self-diagnostic result.	1
SLPIN	W	10h	Sleep In.	0
SLPOUT	W	11h	Sleep out.	0
INVOFF	W	20h	Display inversion off.	0
INVON	W	21h	Display inversion on.	0
ALLPOFF	W	22h	All pixel off.	0
ALLPOON	W	23h	All pixel on.	0
DISPOFF	W	28h	Display off.	0
DISPON	W	29h	Display on.	0
TEOFF	W	34h	Tearing effect line off.	0
TEON	W	35h	Tearing effect line on.	1
MADCTL	W	36h	Memory access control.	1
IDMOFF	W	38h	Idle mode off.	0
IDMON	W	39h	Idle mode on.	0
TESL	W	44h	Set tear effect scan lines.	2
GETSCAN	R	45h	Return the current scan line.	2
WRIMC	W	80h	Color selection.	1
RDRIMC	R	81h	Read color selection.	1

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6.3.1 NOP (00h)

00H	**NOP (No Operation)**									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	0	0	0	0	00
Parameter	No Parameter									
Description	- This command is empty command. It does have effect on the display module									
Restriction	-									
Flow Chart	-									

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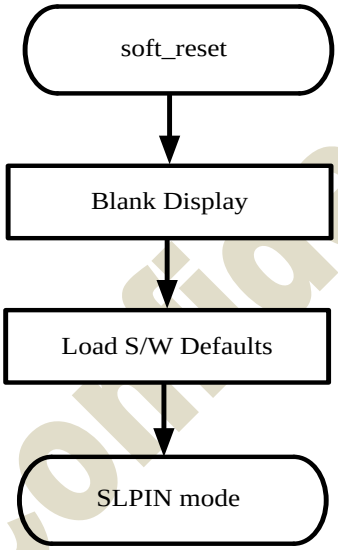
6.3.2 SWRESET (01h)

01H	SWRESET									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	0	0	1	01
Parameter	No Parameter									
Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description)									
Restriction	- It will be necessary to wait 5msec before sending new command following software reset. - The display module loads all display supplier's factory default values to the registers during 5msec. - If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. - Software Reset command cannot be sent during Sleep Out sequence.									
Flow Chart										

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6.3.3 RDDIDIF (04h)

04H	RDDIDIF									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	0	1	0	0	04
Parameter 1	R	ID1[7:0]								
Parameter 2	R	ID2[7:0]								
Parameter 3	R	ID3[7:0]								

Description

- This read byte returns 24-bit display identification information.
- The 1st Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.
- The 2nd Parameter has 2 purposes. Bit7(MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Color). Bits 6~0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specification. See Table:

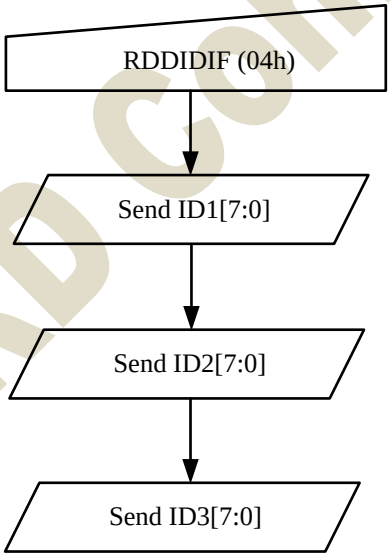
ID Byte Value V[7:0]	Version	Changes
80h		
81h		
82h		
83h		
84h		
85h		

- The 3rd parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.

Restriction

-

Flow Chart



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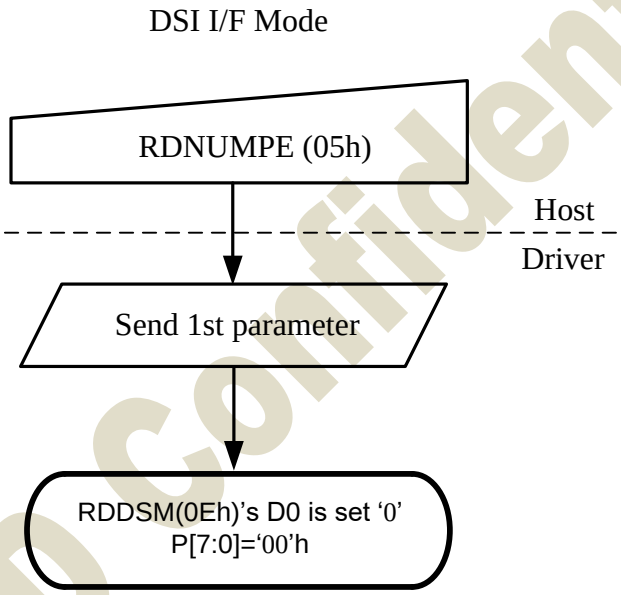
6.3.4 RDNUMPE (05h)

05H	RDNUMPE									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	0	1	0	1	05
Parameter 1	R	P7	P6	P5	P4	P3	P2	P1	P0	
Description	- The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. - P[6:0] bits are telling a number of the errors. - P[7] is set to ‘1’ if there is overflow with P[6..0] bits. - P[7:0] bits are set to ‘0’s (as well as RDDSM(0Eh)’s D0 is set ‘0’ at the same time) after there is sent the second parameter information (=The read function is completed).									
Restriction	-									
Flow Chart										

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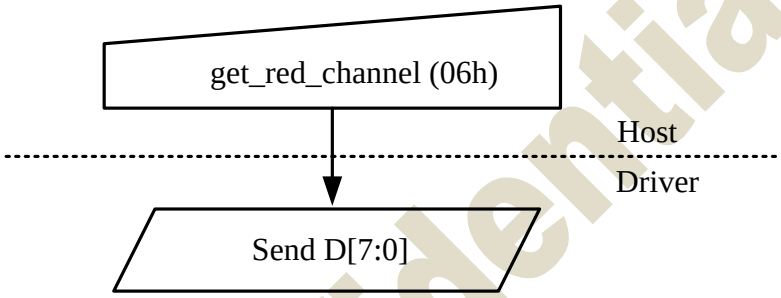
6.3.5 REDRD (06h)

06H	REDRD										
	R/W	**D15-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	-	0	0	0	0	0	1	1	0	06
Parameter 1	R	-	R7	R6	R5	R4	R3	R2	R1	R0	
Description	- The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to ‘0’. - 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to ‘0’. - 24 bit format: R7 is MSB and R0 is LSB. All bits are used.										
Restriction	-										
Flow Chart											

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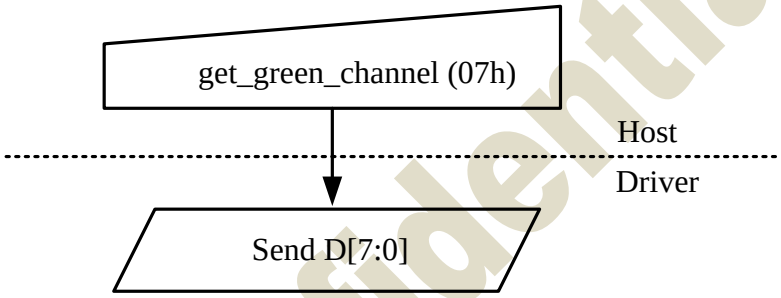
6.3.6 REDGREEN (07h)

07H	REDGREEN									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	0	1	1	1	07
Parameter 1	R	G7	G6	G5	G4	G3	G2	G1	G0	
Description	- The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to ‘0’. - 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to ‘0’. - 24 bit format: G7 is MSB and G0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

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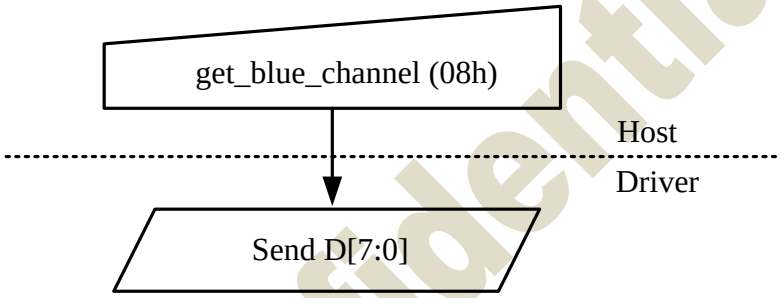
6.3.7 REDBLUE (08h)

08H	REDBLUE									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	0	0	0	08
Parameter 1	R	B7	B6	B5	B4	B3	B2	B1	B0	
Description	- The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and BR0 are set to ‘0’. - 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to ‘0’. - 24 bit format: B7 is MSB and B0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

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6.3.8 RDDST (09h)

09H	RDDST									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	1	0	0	1	09
Parameter 1	R	D[31:24]								
Parameter 2	R	D[23:16]								
Parameter 3	R	D[15:8]								
Parameter 4	R	D[7:0]								

Description

-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D31	Booster voltage status	‘0’ = booster off ‘1’ = booster on
D30	Not defined	Set to ‘0’
D29	Not defined	Set to ‘0’
D28	Not defined	Set to ‘0’
D27	Not defined	Set to ‘0’
D26	RGB/BGR order	‘0’ = RGB (MADCTL B4=‘0’) ‘1’ = BGR (MADCTL B4=‘1’)
D25	Not defined	Set to ‘0’
D24	Source scan sequence	‘0’ = Source output Left to Right (MADCTL B1=‘0’) ‘1’ = Source output Right to Left (MADCTL B1=‘1’)
D23	Gate scan sequence	‘0’ = Gate output Top to Bottom (MADCTL B0=‘0’) ‘1’ = Gate output Bottom to Top (MADCTL B0=‘1’)
D22	Not defined	Set to ‘0’
D21	Not defined	Set to ‘0’
D20	Not defined	Set to ‘0’
D19	Idle mode on/off	‘0’ = Idle mode off. ‘1’ = Idle mode on.
D18	Partial mode on/off	‘0’ = Partial mode off. ‘1’ = Partial mode on.
D17	Sleep in/out	‘0’ = Sleep in mode. ‘1’ = Sleep out mode.
D16	Not defined	Set to ‘1’
D13	Not defined	Set to ‘0’
D12	Not defined	Set to ‘0’
D11	Not defined	Set to ‘0’
D10	Display on/off	‘0’ = Display is off. ‘1’ = Display is on.
D9	Not defined	Set to ‘0’
D8	Not defined	Set to ‘0’
D7	Not defined	Set to ‘0’
D6	Not defined	Set to ‘0’

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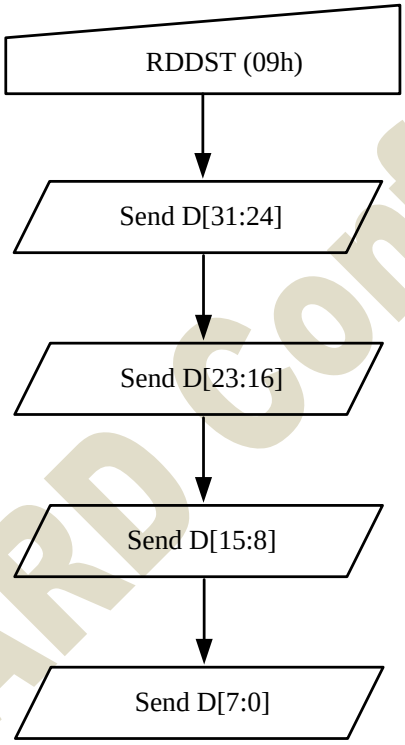
D5	Not defined	Set to ‘0’
D4	Not defined	Set to ‘0’
D3	Not defined	Set to ‘0’
D2	Not defined	Set to ‘0’
D1	Not defined	Set to ‘0’
D0	Parity error on DSI	‘0’ = No Parity Error. ‘1’ = Parity Error.

Restriction	-
Flow Chart	

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6.3.9 RDDPM (0Ah)

0AH	**RDDPM**									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	1	0	1	0	0A
Parameter 1	R	D7	D6	D5	D4	D3	D2	0	0	

Description

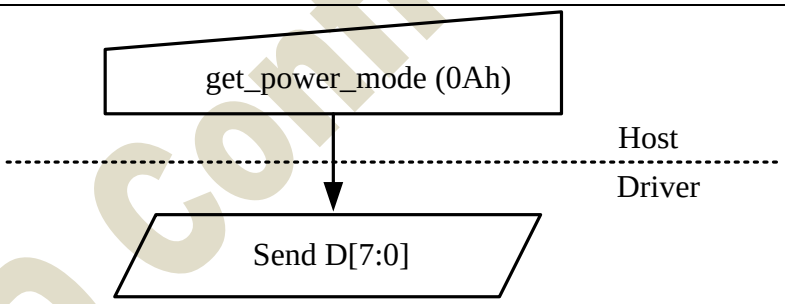
-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Defined	Set to ‘0’ or ‘1’
D6	Not Defined	Set to ‘0’
D5	Not Defined	Set to ‘0’
D4	Sleep in/out	‘0’ = sleep in mode ‘1’ = sleep out mode
D3	Not Defined	Set to ‘1’
D2	Display on/off	‘0’ = display is off ‘1’ = display is on
D1	Not defined	Set to ‘0’
D0	ESD detect	‘0’ = ESD detect off ‘1’ = ESD detect on

Restriction

-

Flow Chart



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6.3.10 RDDMATCDL (0Bh)

0BH	RDDMATCDL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	0	1	1	0B
Parameter 1	R	0	0	0	0	0	0	D1	D0	

Description

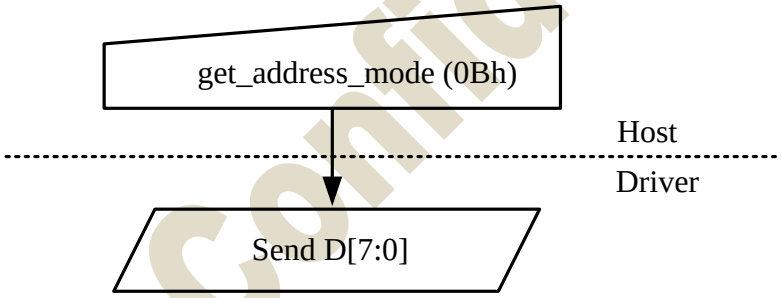
-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D1	Source scan sequence	‘0’ = left to right (when MADCTL B1=’0’) ‘1’ = right to left (when MADCTL B1=’1’)
D0	Gate scan sequence	‘0’ = top to bottom (when MADCTL B0=’0’) ‘1’ = bottom to top (when MADCTL B0=’1’)

Restriction

-

Flow Chart



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6.3.11 RDDIM (0Dh)

0DH	RDDIM									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	1	0	1	0D
Parameter 1	R	0	D6	D5	0	0	0	0	0	

Description

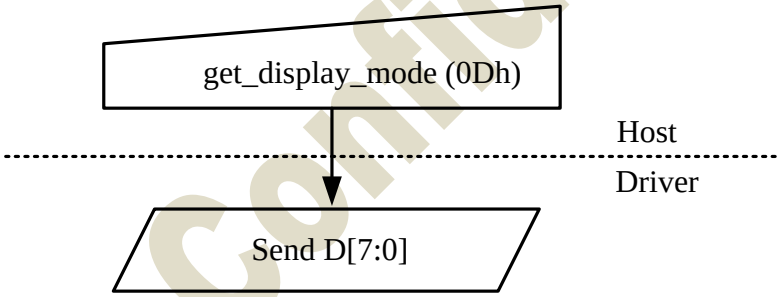
-This is command indicates the current status of the display as described in the table below.

Bit	Description	Value
D6	Horizontal Scrolling Status	This bit is not applicable for this project, set it to ‘0’
D5	Inversion On/Off	‘0’ = Inversion is Off. ‘1’ = Inversion is On.

Restriction

-

Flow Chart



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6.3.12 RDDSM (0Eh)

0EH	RDDSM									
	R/W	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	W	0	0	0	0	1	1	1	0	0E
Parameter 1	R	D7	D6	0	0	0	0	0	0	

Description

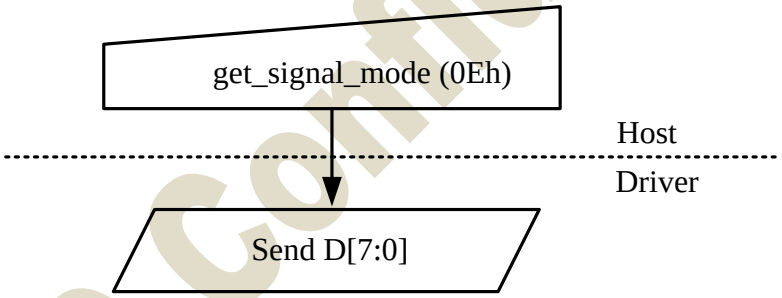
-This command indicates the current status of the display as described in the table below.

Bit	Description	Value
D7	Tearing Effect Line On/Off	‘0’ = Tearing Effect Line Off. ‘1’ = Tearing Effect On.
D6	Tearing Effect Line Output Mode	‘0’ = Mode 1. ‘1’ = Mode 2.

Restriction

-

Flow Chart



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6.3.13 RDDSDR (0Fh)

0FH	RDDSDR									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	1	1	1	0F
Parameter 1	R	D7	D6	D5	D4	0	0	0	0	

Description

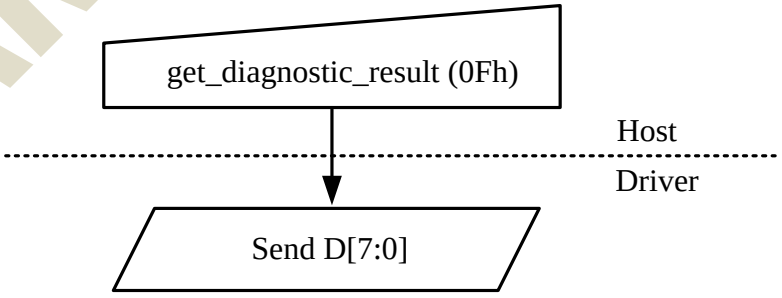
-The display module returns the self-diagnostic results following a SLPOUT command.

Bit	Description	Value
D7	Register Loading Detection	See section “Sleep Out –command and self-diagnostic functions of the display module”
D6	Functionality Detection	
D5	Reserved	Set to ‘0’.
D4		Set to ‘0’.
D3		Set to ‘0’.
D2		Set to ‘0’.
D1		Set to ‘0’.
D0	ESD detect	‘0’ = ESD detect off ‘1’ = ESD detect on

Restriction

-

Flow Chart



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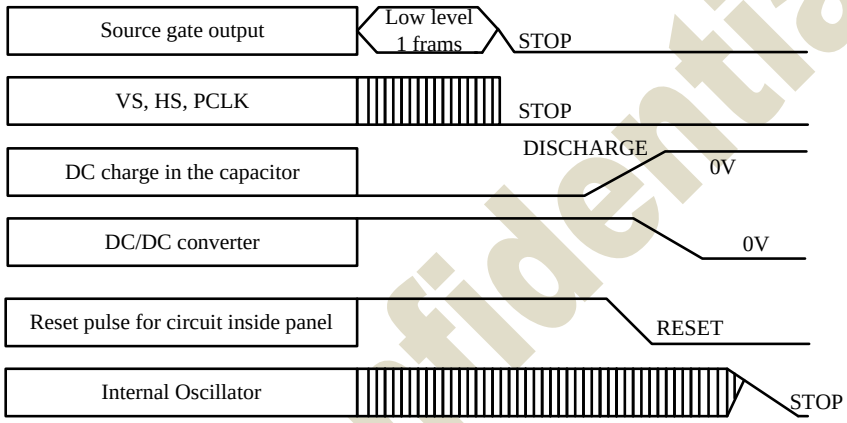
6.3.14 SLPIN (10h)

10H	SLPIN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	0	10

Description

- This command causes the LCD module to enter the minimum power consumption mode.
In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports.

DBI or DSI Command Mode remains operational and the line buffer maintains its contents. The host processor continues to send PCLK, HS and VS information to DPI IF for two frames after this command is sent when the display module is in Normal mode.
In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.

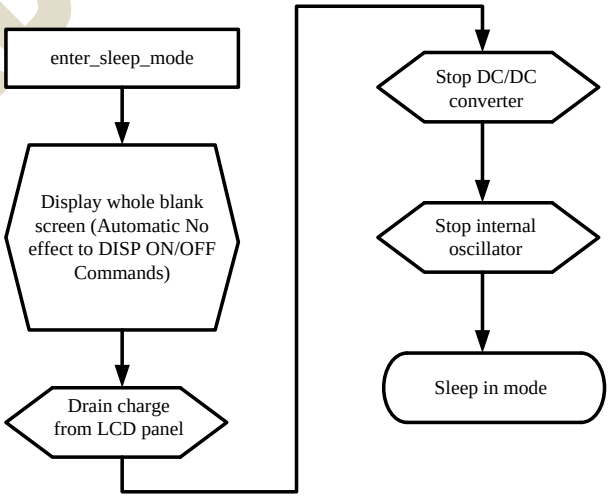


Restriction

- This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



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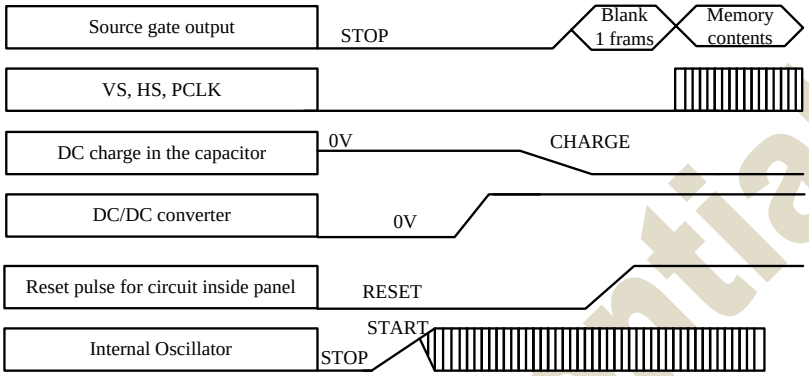
6.3.15 SLPOUT (11h)

11H	SLPOUT									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	1	11

Description

This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started



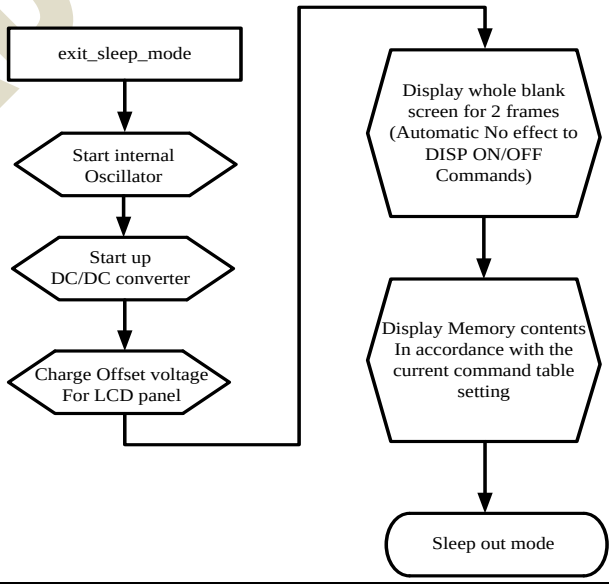
User can start to send PCLK, HS and VS information on DPI IF before Sleep Out command and this information is valid at least 1 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.

Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.
The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



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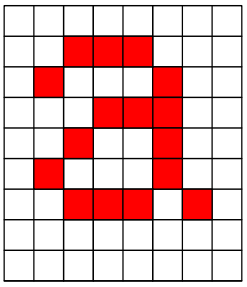
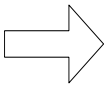
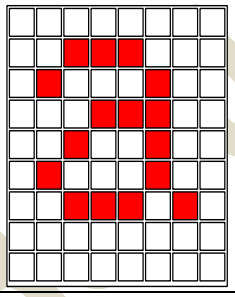
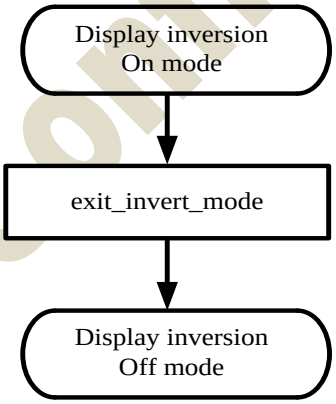
6.3.16 INVOFF (20h)

20H	INVOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	0	20
Description	This command is used to recover from display inversion mode. This command makes no change of contents of line buffer. This command does not change any other status. (Example) Memory   Display Panel 									
Restriction	This command has no effect when module is already in inversion off mode.									
Flow Chart										

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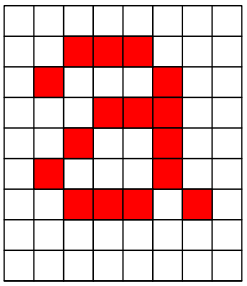
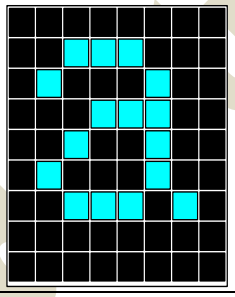
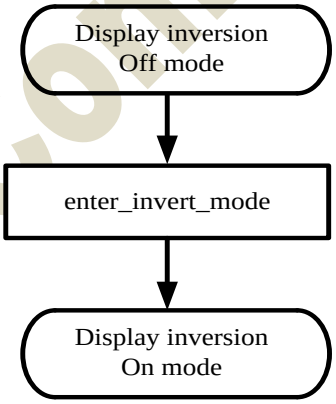
6.3.17 INVON (21h)

21H	INVON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	1	21
Description	This command is used to enter into display inversion mode. This command makes no change of contents of line buffer. Every bit is inverted from the line buffer to the display. This command does not change any other status. (Example) Memory  Display Panel 									
Restriction	This command has no effect when module is already in inversion on mode.									
Flow Chart										

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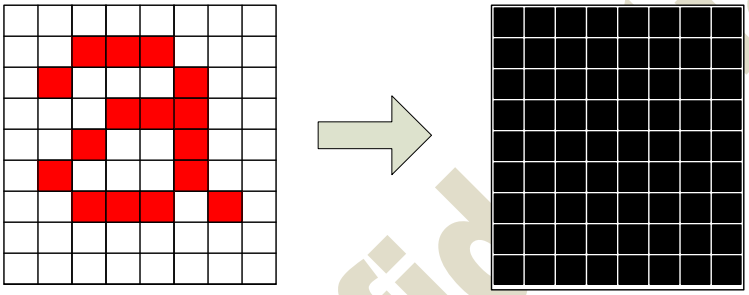
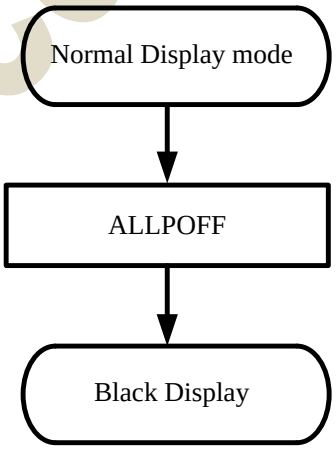
6.3.18 ALLPOFF (22h)

22H	ALLPOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	1	0	22
Description	This command turns the display panel black in ‘Sleep Out’ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’. This command makes no change of contents of line buffer. This command does not change any other status. (Example) Memory Display Panel  ‘All Pixels On’, ‘Normal Display Mode On’ or ‘Partial Mode On’ – commands are used to leave this mode. The display panel is showing the contect of the line buffer after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands.									
Restriction	This command has no effect when module is already in All Pixel Off mode.									
Flow Chart										

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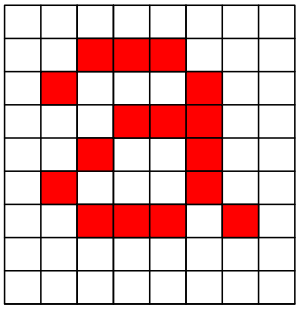
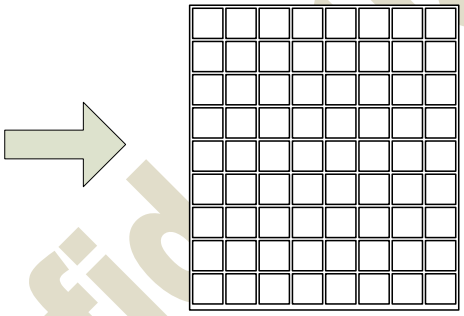
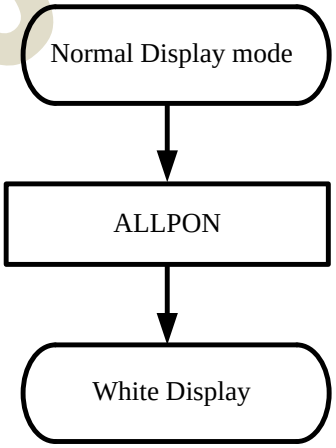
6.3.19 ALLPOON (23h)

23H	ALLPOON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	1	1	23
Description	This command turns the display panel white in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of line buffer. This command does not change any other status. (Example) Memory  Display Panel  'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the contect of the line buffer after 'Normal Display Mode On' and 'Partial Mode On' –commands.									
Restriction	This command has no effect when module is already in All Pixel Off mode.									
Flow Chart										

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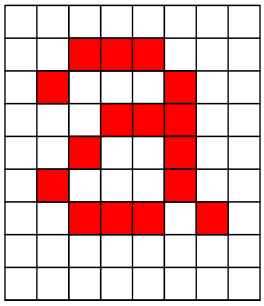
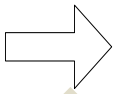
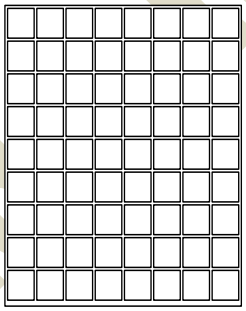
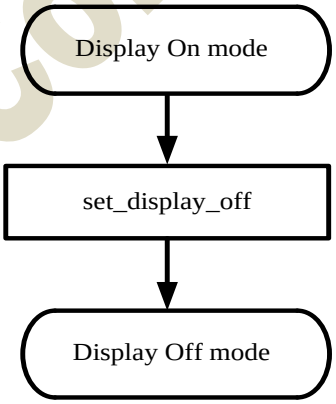
6.3.20 DISPOFF (28h)

28H	DISPOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	0	28
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Line Buffer is disabled and blank page inserted. This command makes no change of contents of line buffer. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Memory   Display Panel 									
Restriction	It will be necessary to wait 40msec and send Sleep In command for power off sequence.									
Flow Chart										

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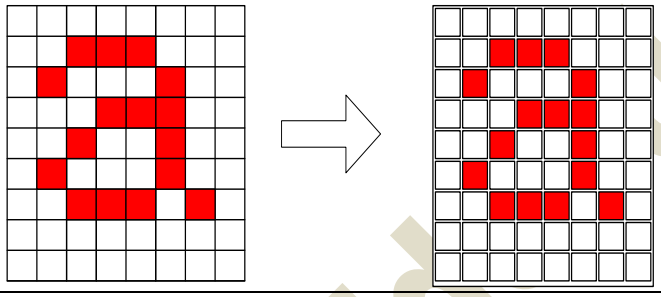
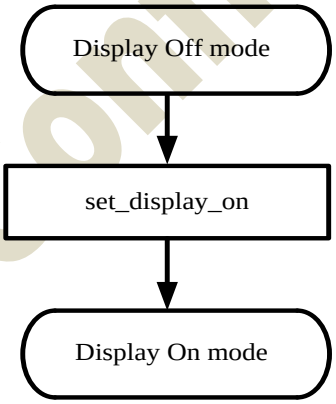
6.3.21 DISPON (29h)

29H	DISPON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	1	29
Description	This command is used to recover from DISPLAY OFF mode. Output from the Line Buffer is enabled. This command makes no change of contents of line buffer. This command does not change any other status. (Example) Memory  Display Panel									
Restriction	This command has no effect when module is already in display on mode.									
Flow Chart										

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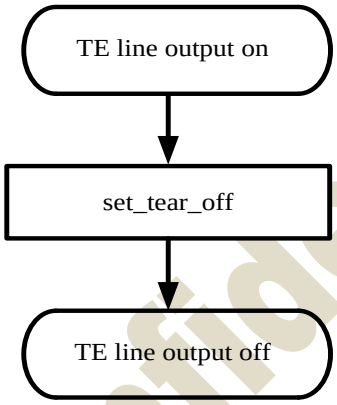
6.3.22 TEOFF (34h)

34H	TEOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	0	0	34
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Flow Chart										

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6.3.23 TEOFF (35h)

35H	TEON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	0	1	35
Parameter 1	W	X	X	X	X	X	X	X	M	

Description

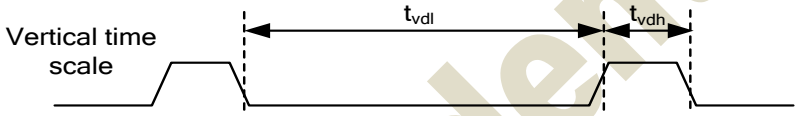
This command is used to turn ON the Tearing Effect output signal from the TE signal line.

This output is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

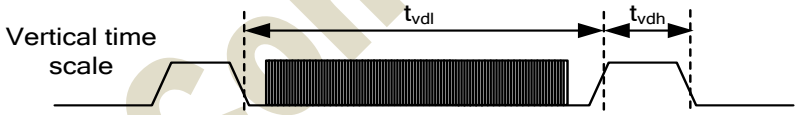
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

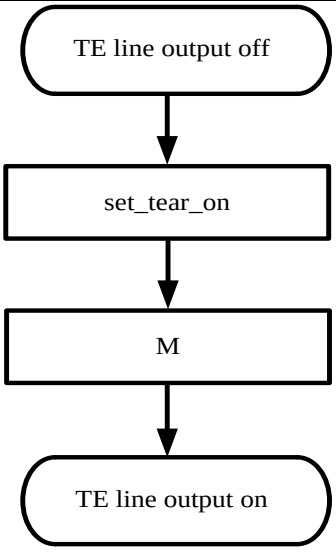


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

Flow Chart



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6.3.24 DISPON (36h)

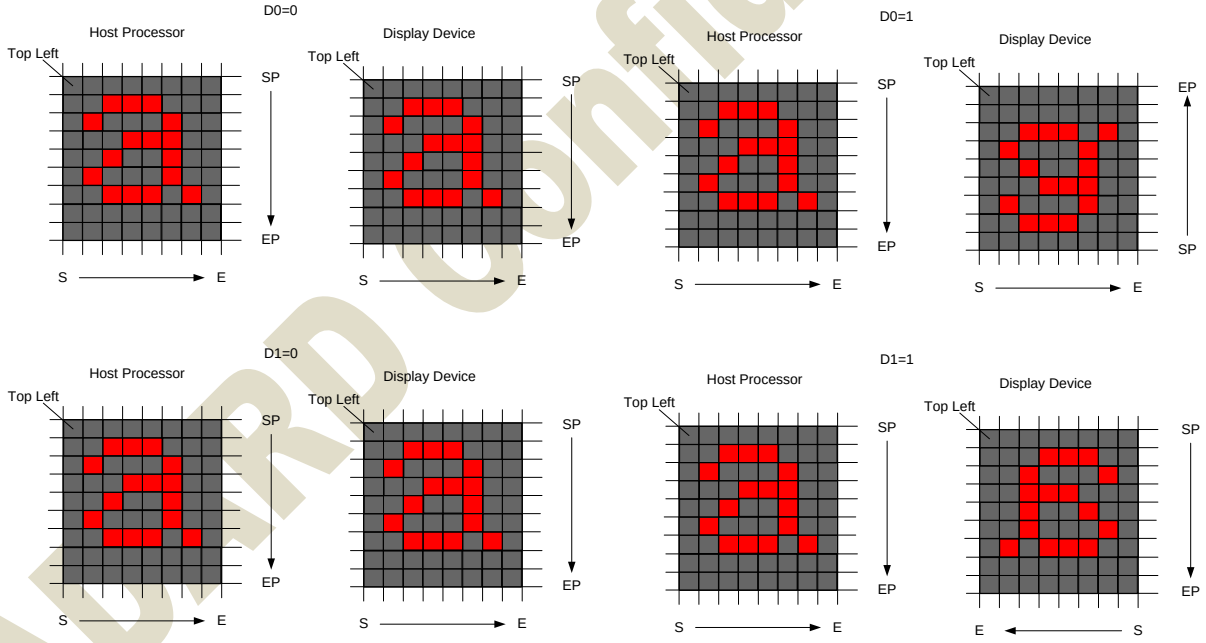
36H	MADCTL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	1	0	36
Parameter 1	W	0	0	0	0	D3	0	D1	D0	

Description

This command defines read/write scanning direction of line buffer.

This command makes no change on the other driver status.

Bit	Description	Value
D3	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
D1	Source scan sequence	Horizontal scan 0=Left to right 1=Right to left
D0	Gate scan sequence	Vertical scan 0=Top to bottom 1=Bottom to top



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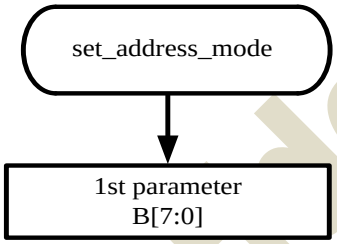
Restriction	
Flow Chart	

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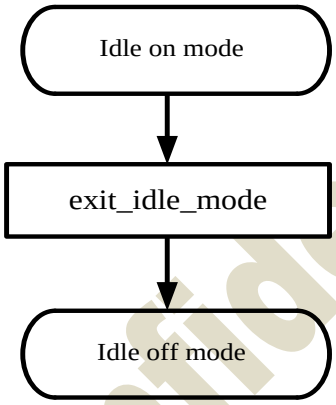
6.3.25 IDMOFF (38h)

38H	IDMOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	1	0	0	0	38
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in idle off mode.									
Flow Chart										

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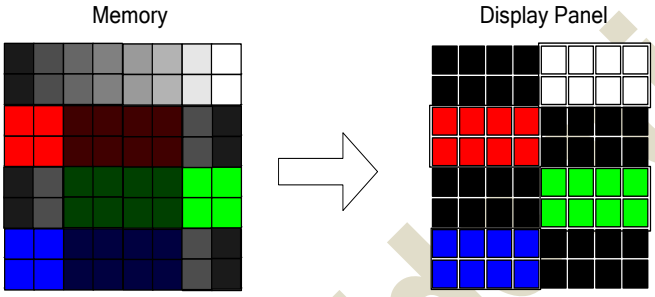
6.3.26 IDMON (39h)

39H	IDMON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	1	0	0	1	39

Description

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the line buffer, 8 color depth data is displayed.

(Example)



Memory contents vs. Display Color

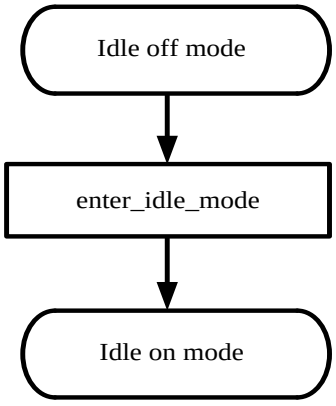
	R7 – R0	G7 – G0	B7 – B0
Black	0XXXXX	0 XXXXX	0 XXXXX
Blue	0 XXXXX	0 XXXXX	1 XXXXX
Red	1 XXXXX	0 XXXXX	0 XXXXX
Magent	1 XXXXX	0 XXXXX	1 XXXXX
Green	0 XXXXX	1 XXXXX	0 XXXXX
Cyan	0 XXXXX	1 XXXXX	1 XXXXX
Yellow	1 XXXXX	1 XXXXX	0 XXXXX
White	1 XXXXX	1 XXXXX	1 XXXXX

X=don’t care

Restriction

This command has no effect when module is already in idle on mode.

Flow Chart



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6.3.27 TESL (44h)

44H	TESL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	1	0	0	0	1	0	0	44
Parameter 1	W	TELINE[15:8]								
Parameter 2	W	TELINE[7:0]								

Description

This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

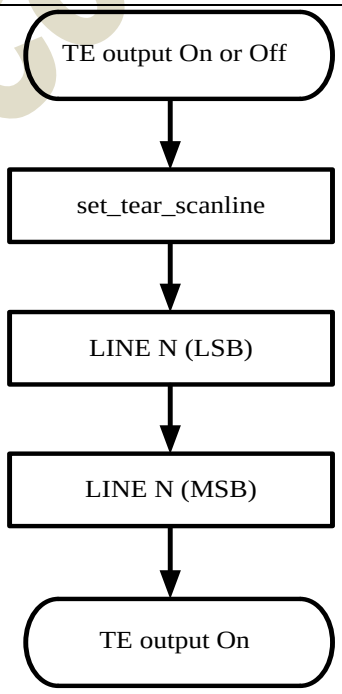
The Tearing Effect Output line consists of V-Blanking information only:

Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.

Restriction

The command has no effect when Tearing Effect output is already ON.

Flow Chart



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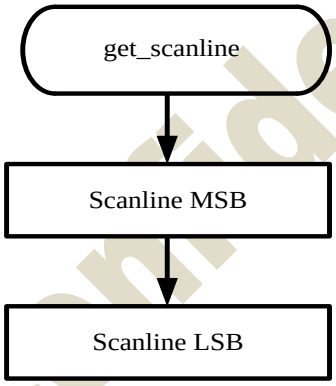
6.3.28 GETTSCAN (45h)

45H	GETSCAN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	1	0	0	0	1	0	1	45
Parameter 1	R	SLIN[15:8](8'b0)								
Parameter 2	R	SLIN[7:0](8'b0)								
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined									
Restriction										
Flow Chart										

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6.3.29 WRIMC (80h)

80H	WRIMC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	0	0	0	0	0	0	80
Parameter 1	W	X	X	X	X	X	R	G	B	

Description

This command is used to select color for 1bpp Idle Mode. Color selection is configured with bits [D2:D0].

D2: R Component

D1: G Component

D0: B Component

Color selection is defined in following table:

1bpp Idle Mode Color Selection	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

X = Don’t care.

Restriction	-This command is only applicable to 1bpp Compression in Idle Mode.
Flow Chart	-

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6.3.30 RDRIMC (81h)

81H	RDRIMC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	0	0	0	0	0	1	81
Parameter 1	R	X	X	X	X	X	R	G	B	

Description

This command returns the current color selection of 1bpp Idle Mode which color selection is configured with bits [D2:D0].

D2: R Component

D1: G Component

D0: B Component

Color selection is defined in following table:

1bpp Idle Mode Color Selection	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

X = Don’t care.

Restriction

-This command is only applicable to 1bpp Compression in Idle Mode.

Flow Chart

-

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6.4 MIPI video input timing

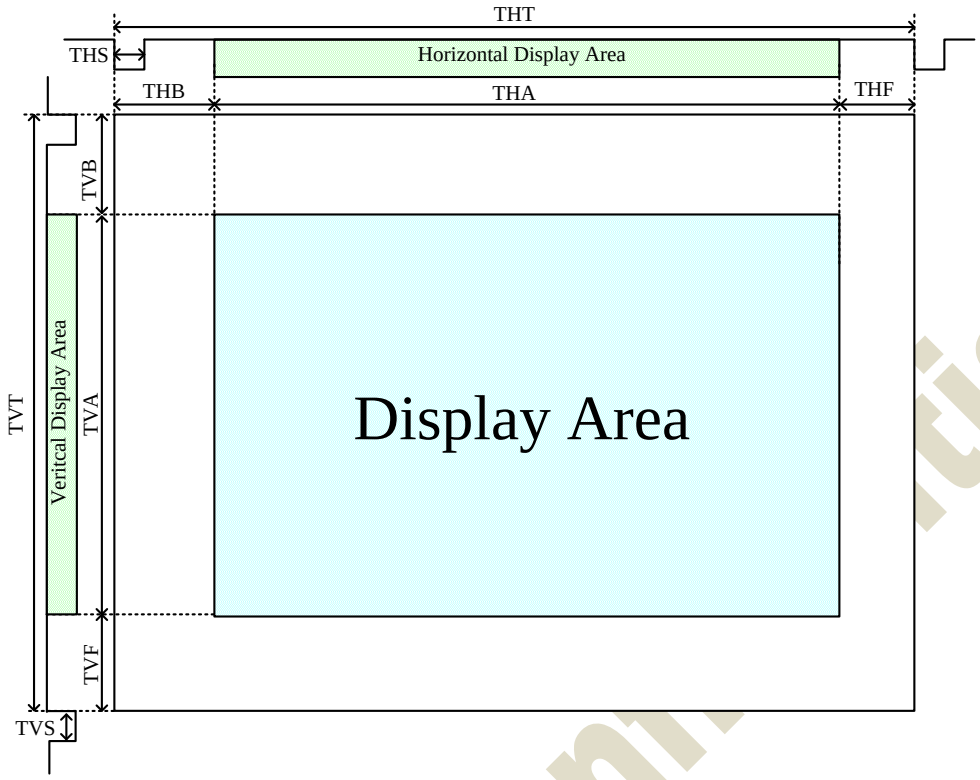

Figure 6.6: MIPI video input timing

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6.4.1 MIPI transmission packet sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

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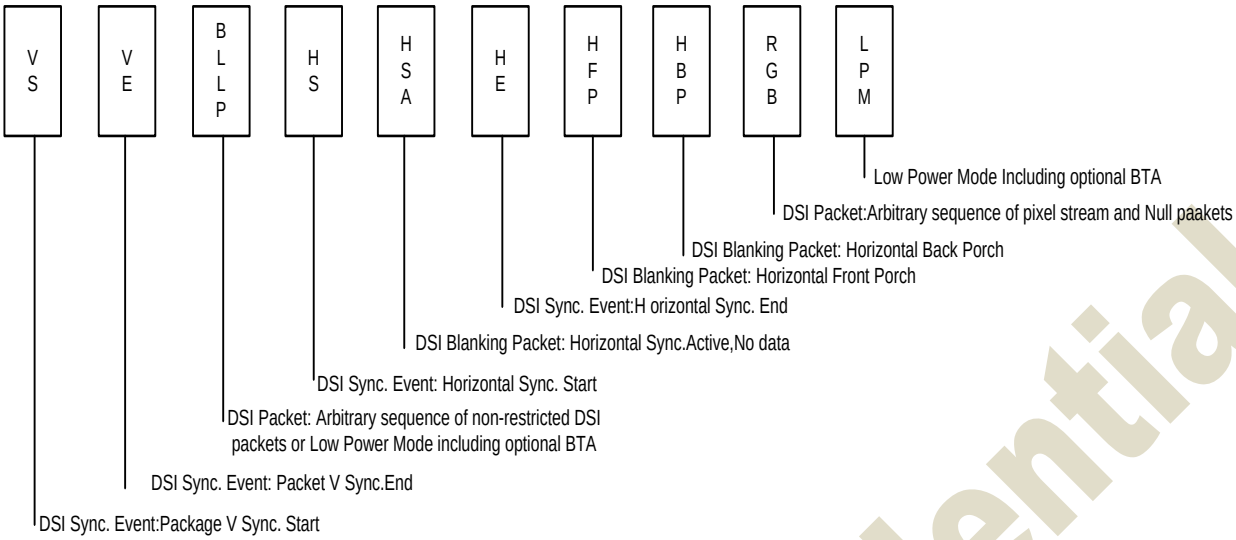
Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

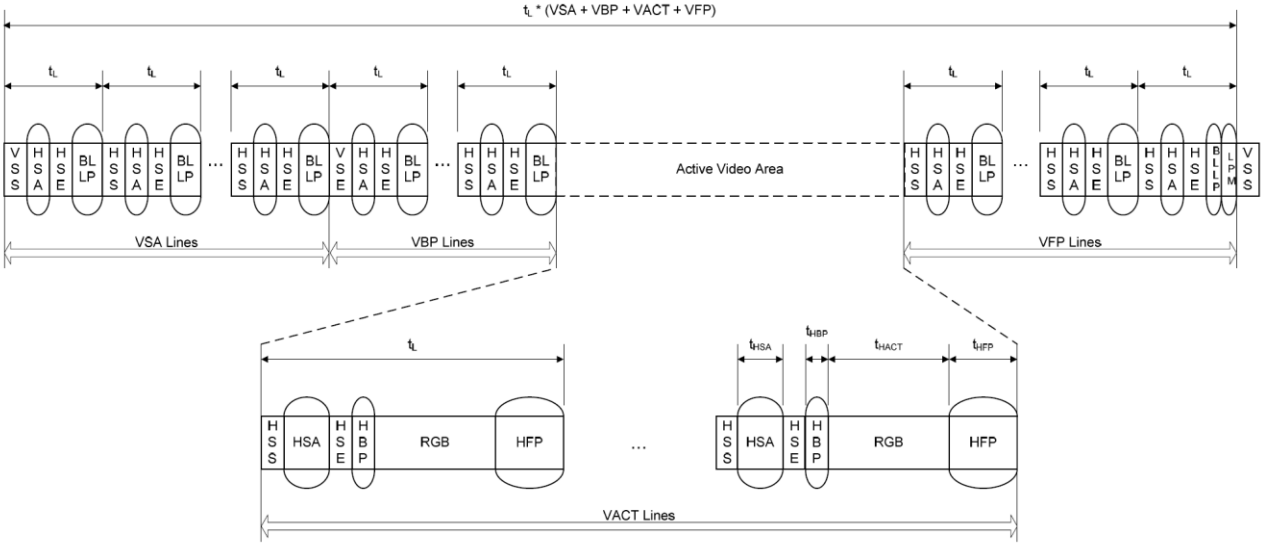
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

●Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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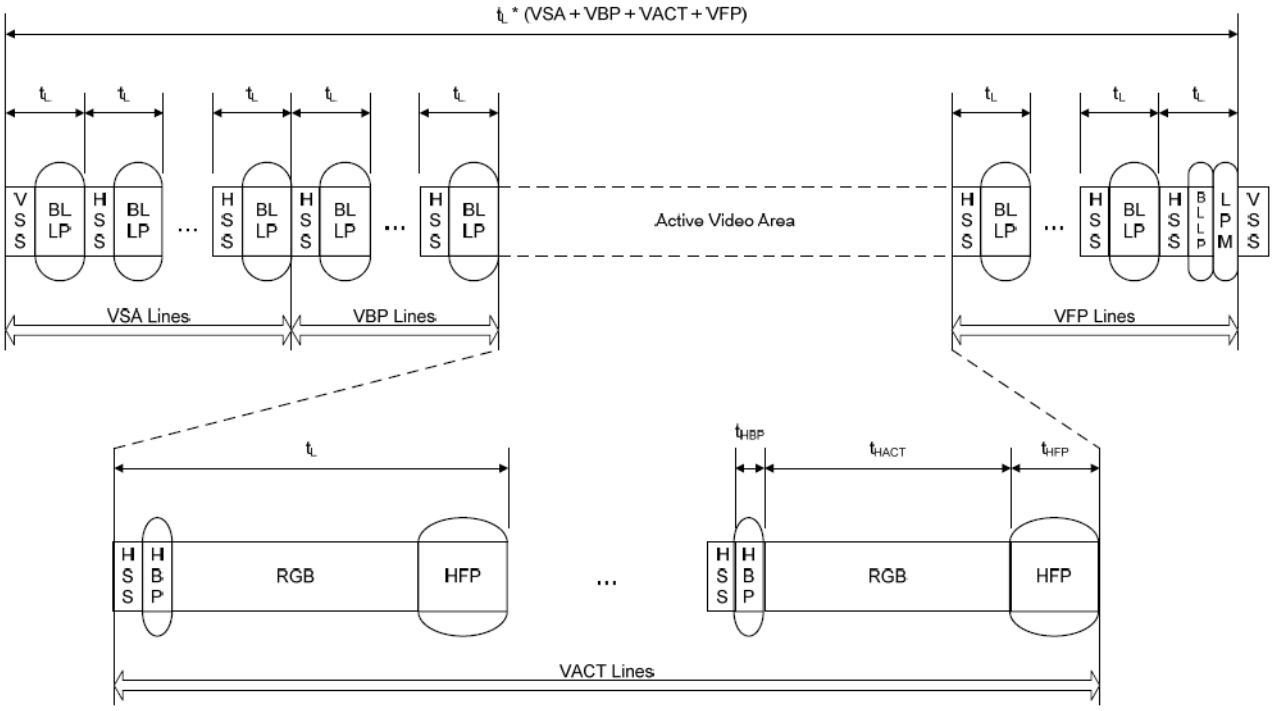
●Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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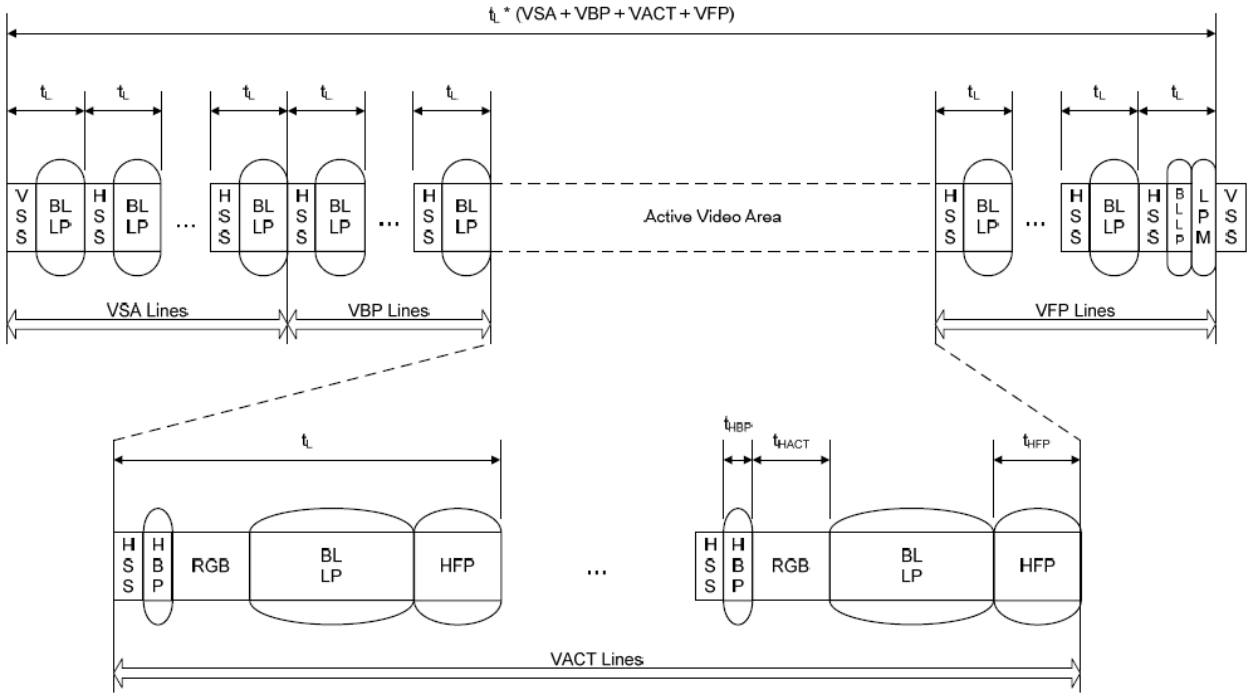
- **Burst Mode**

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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6.5 MIPI timing characteristic

MIPI Input Timing	Symbol	1024RGBx768			1024RGBx600			800RGBx600			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI 24-bit RGB@ 2 lane Operating Frequency	-	100	-	750	100	-	750	100	-	750	Mbps
MIPI 24-bit RGB@ 4 lane Operating Frequency	-	100	-	500	100	-	500	100	-	500	Mbps
Horizontal Total	tht	1114	1344	1400	1114	1344	1400	890	1000	1300	DCLK
Hsync Pulse width	ths	1	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	60	160	160	60	160	160	60	88	250	DCLK
Horizontal Valid Data	thd		1024			1024			800		DCLK
Horizontal Front Porch	thfp	30	160	216	30	160	216	30	112	250	DCLK
Vertical Total	tvt	778	806	845	610	635	800	610	660	800	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	33	8	23	100	8	39	100	THT
Vertical Valid Data	tvd		768			600			600		THT
Vertical Front Porch	tvfp	2	15	44	2	12	100	2	21	100	THT

MIPI Input Timing	Symbol	640RGBx480			480RGBx272			Unit
		Min	Typ	Max	Min	Typ	Max	
MIPI 24-bit RGB@ 2 lane Operating Frequency	-	100	-	750	100	-	750	Mbps
MIPI 24-bit RGB@ 4 lane Operating Frequency	-	100	-	500	100	-	500	Mbps
Horizontal Total	tht	890	1000	1114	830	890	950	DCLK
Hsync Pulse width	ths	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	140	88	220	180	210	240	DCLK
Horizontal Valid Data	thd		640			480		DCLK
Horizontal Front Porch	thfp	110	272	254	170	200	230	DCLK
Vertical Total	tvt	610	660	800	498	610	660	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	28	39	160	126	180	210	THT
Vertical Valid Data	tvd		480			272		THT
Vertical Front Porch	tvfp	102	141	160	100	158	178	THT

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6.6 MIPI DC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	120	ohm
HS transmit differential voltage(V_{OD}=V_{DP}-V_{DN})	|V_{OD}|	100	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	1000	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	110			ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 1 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV
MIPI Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA
MIPI Digital Stand-by Current	I_{STMIPI}	-	-	250	uA

Note: MIPI Digital Operating and Stand-by Current is at RT 25℃ condition.

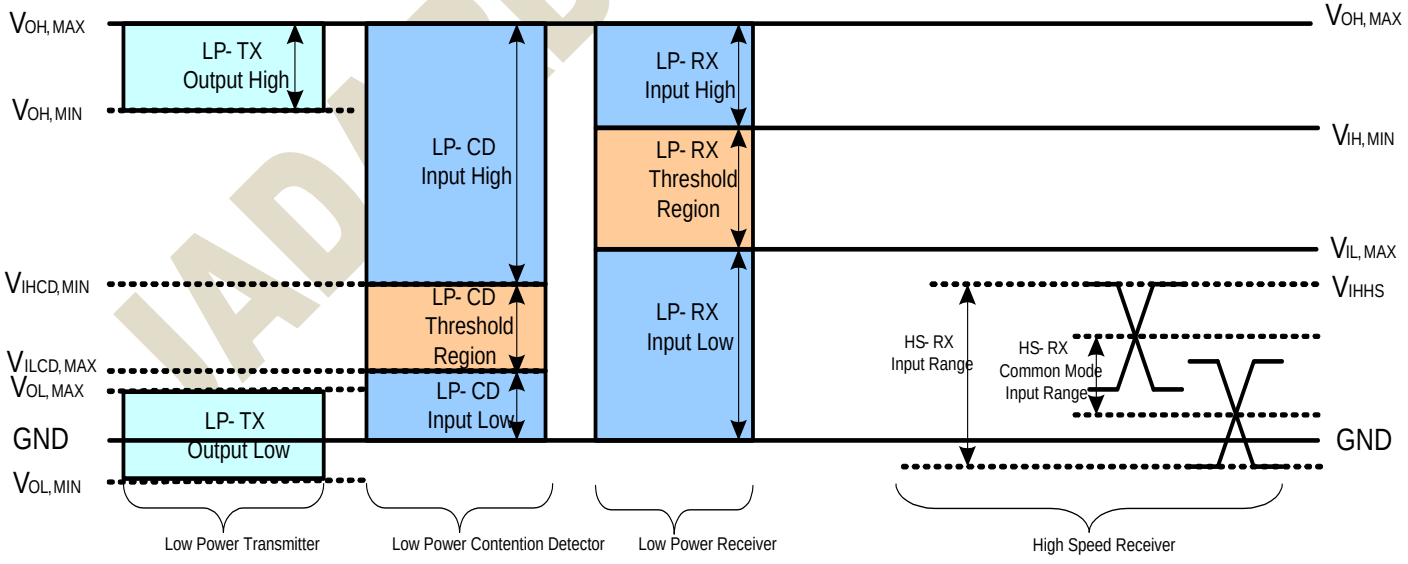

Figure 6.7: MIPI signaling and contention voltage levels

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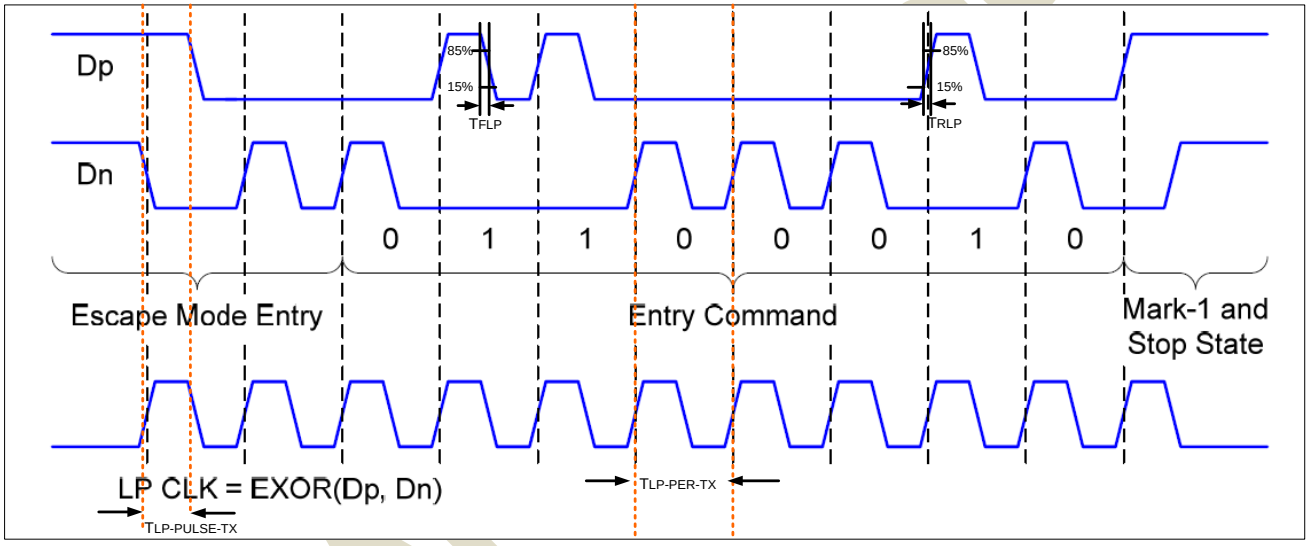
6.7 MIPI AC characteristic

6.7.1 LP Transmitter AC Specification

Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP\text{-}PULSE\text{-}TX}$	100	-	-	ns	-
	All other pulses		100	-	-	ns	-
Period of the LP EXOR clock(LP Speed)		$T_{LP\text{-}PER\text{-}TX}$	200	-	-	ns	-
Slew Rate @CLOAD =0pF		δ V/δ t_{SR}	20	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			20	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			20	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			20	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



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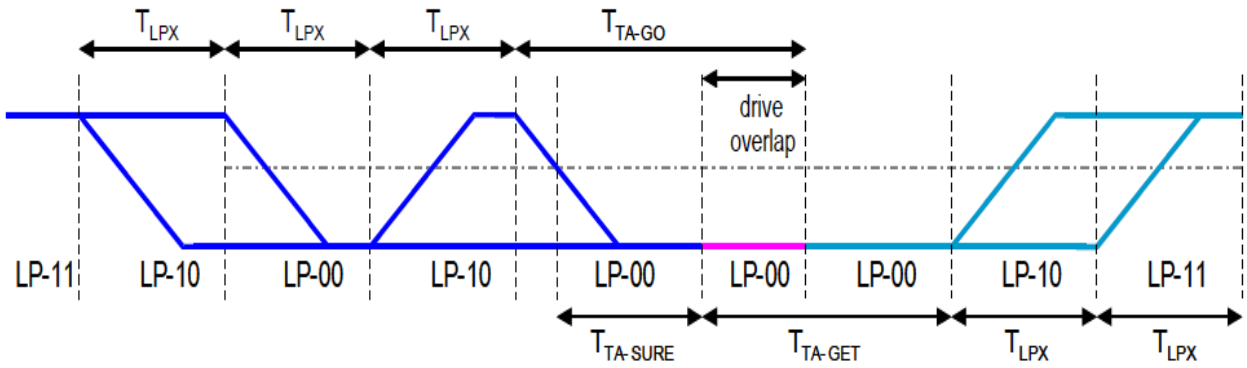
6.7.2 Turnaround Procedure

●Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period	T_{LPX}	100	-	-	ns
Time-out before new TX side start driving	$T_{TA\text{-}Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	$T_{TA\text{-}GET}$	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	$T_{TA\text{-}GO}$	-	$4T_{LPX}$	-	ns



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6.7.3 High Speed Clock and Data Transmission Procedure

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		UI
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+n*12*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	100	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For $T_{CLK-POST}$ example:
$T_{CLK-POST}$ min value =164UI when MIPI max frequency per lane = 0.5Gbps.
$T_{CLK-POST}$ min value =112UI when MIPI max frequency per lane = 1Gbps
(2) For T_{EOT}:
When n = 1 for Forward-direction HS mode and n=4 for Reverse-direction HS mode.

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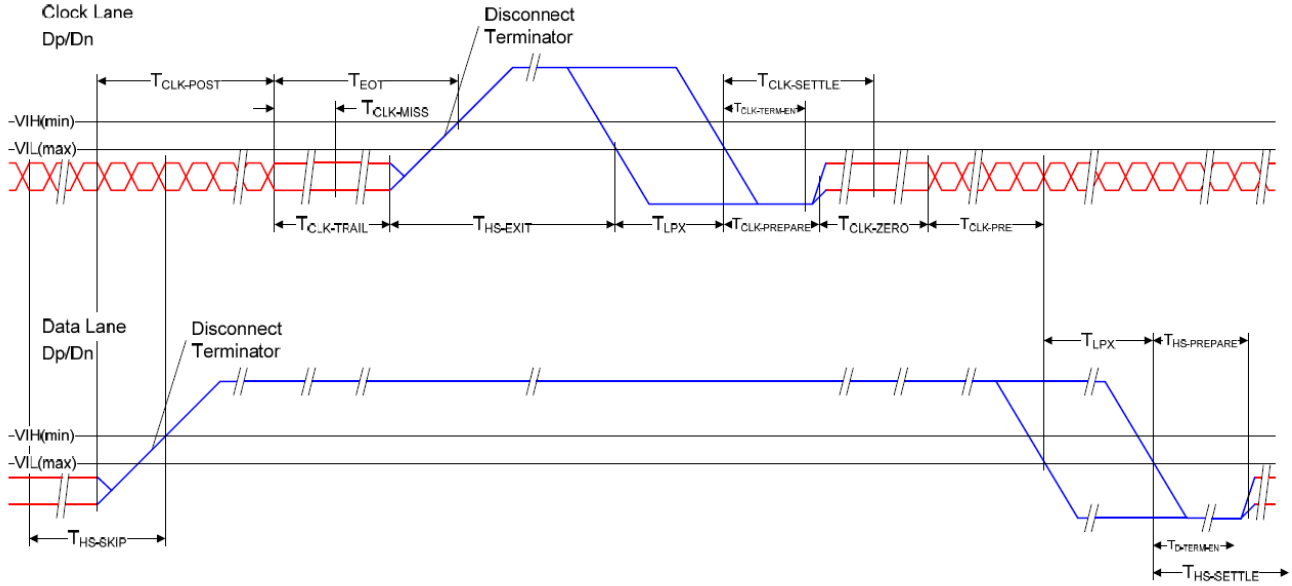

Figure 6.8: Switching the clock lane between clock transmission and low-power mode

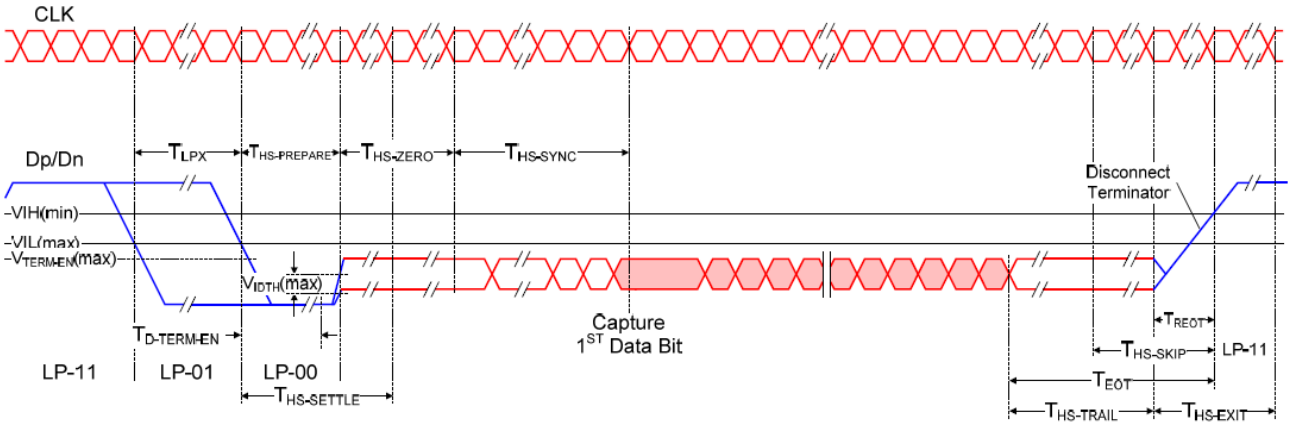

Figure 6.9: Timing of high-speed data transmission in bursts

7. SPI FORMAT

7.1 3-wire SPI format

The JD9165 supports the 3-wire serial peripheral interface **(SPI)** to set internal register. The basic operation of SPI interface is shown below. The Host asserts the CSB when it wants to initiate a read or write transaction. This is followed by the Host sending 9 pulses on the SPI clock **(SCL)**. The 1th bit of SCL pulses is defined to write command or parameter. **(0=command , 1=parameter)**. The Host de-asserts the CSB to indicate end of transfer.

7.1.1 3-wire SPI interface Ⅰ

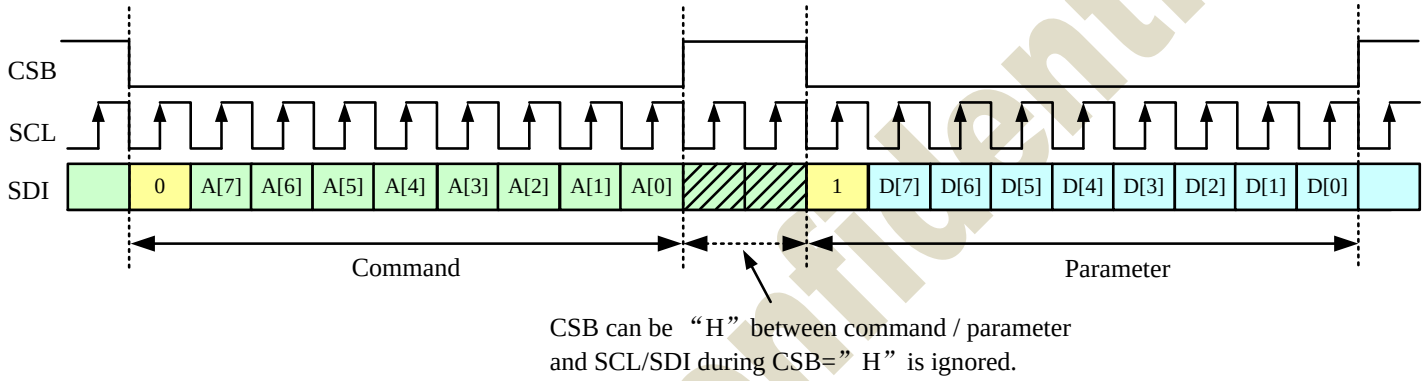

Figure 7.1: 3-wire SPI Ⅰ single write operation

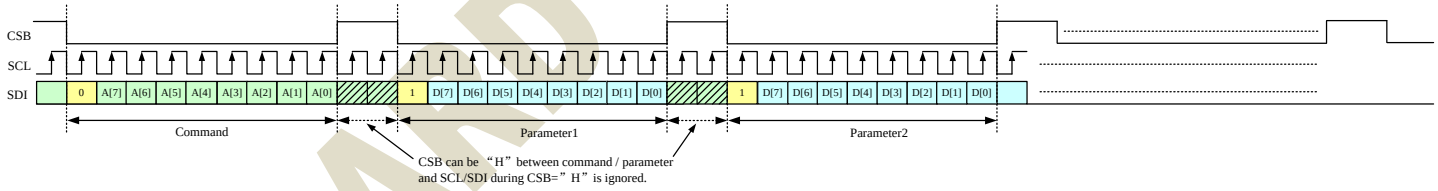

Figure 7.2: 3-wire SPI Ⅰ multi write operation

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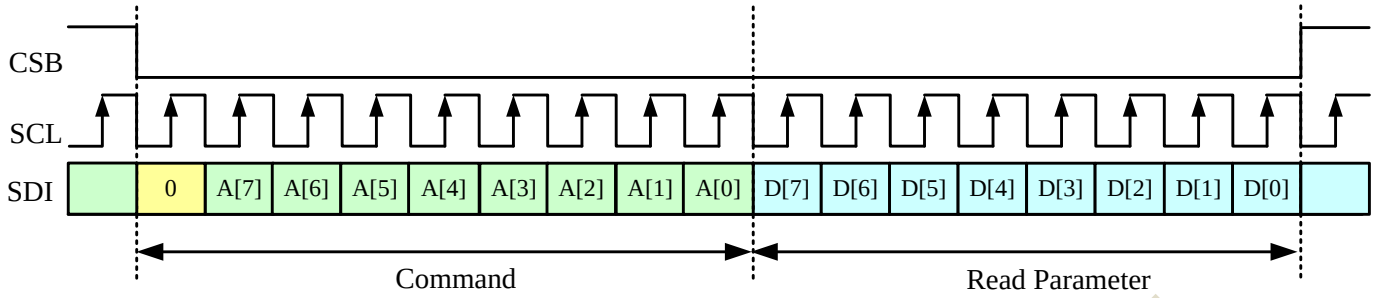

Figure 7.3: 3-wire SPI I single read operation

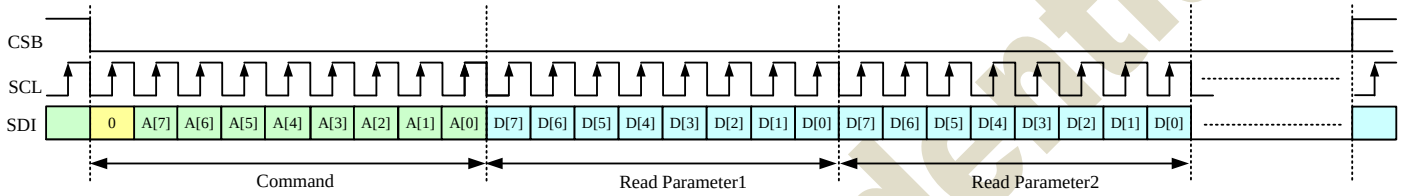

Figure 7.4: 3-wire SPI I multi read operation

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7.1.2 3-wire SPI interface Ⅱ

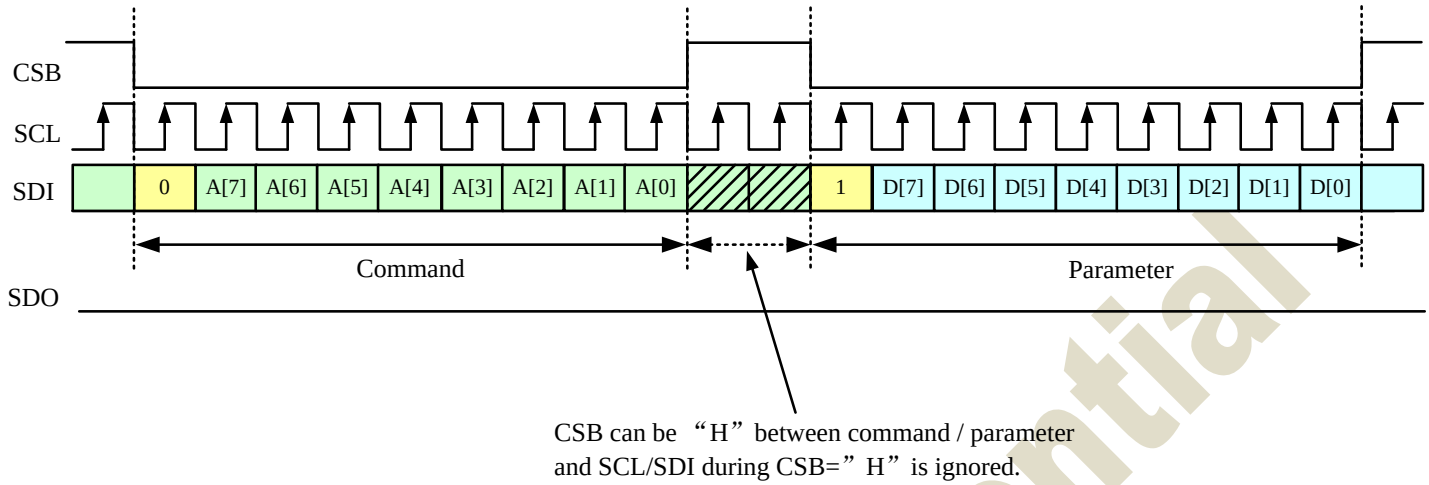

Figure 7.5: 3-wire SPI Ⅱ single write operation

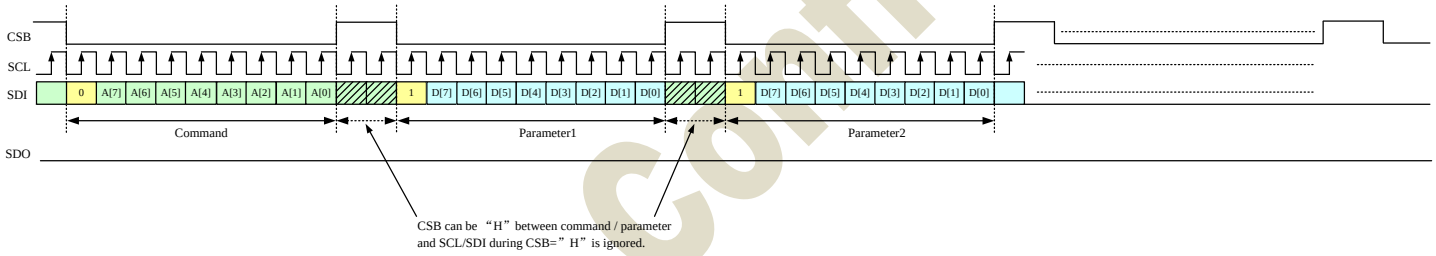

Figure 7.6: 3-wire SPI Ⅱ multi write operation

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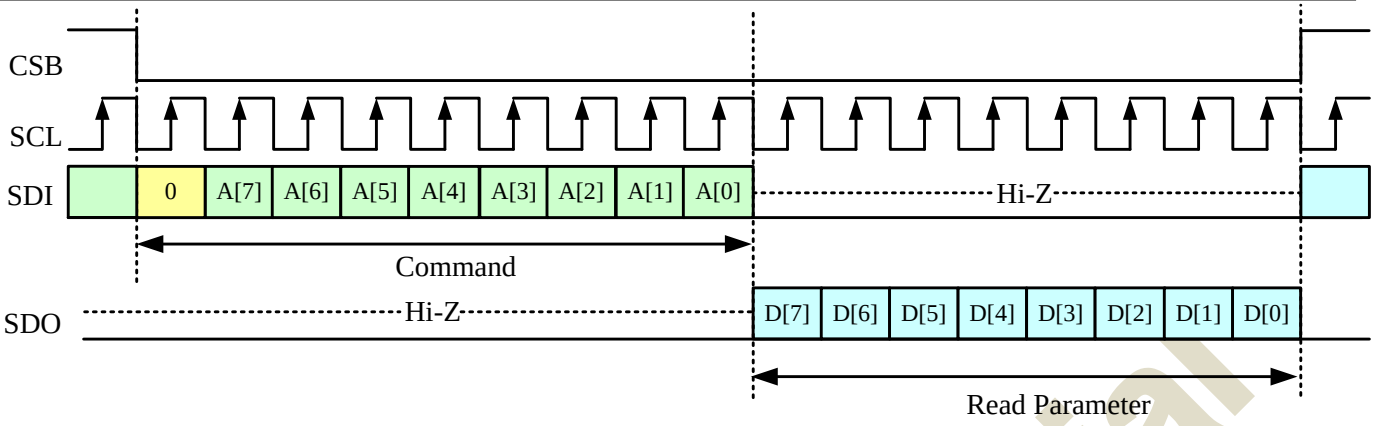

Figure 7.7: 3-wire SPI Ⅱ single read operation

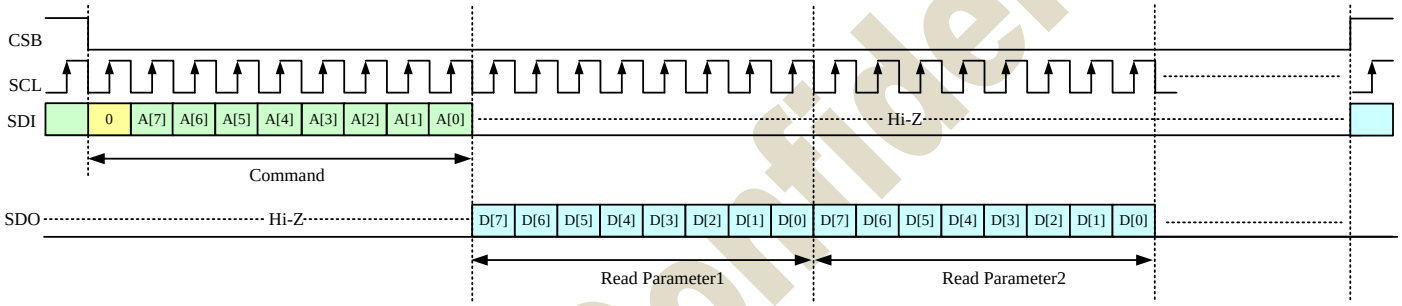

Figure 7.8: 3-wire SPI Ⅱ multi read operation

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7.2 3-wire interface characteristics

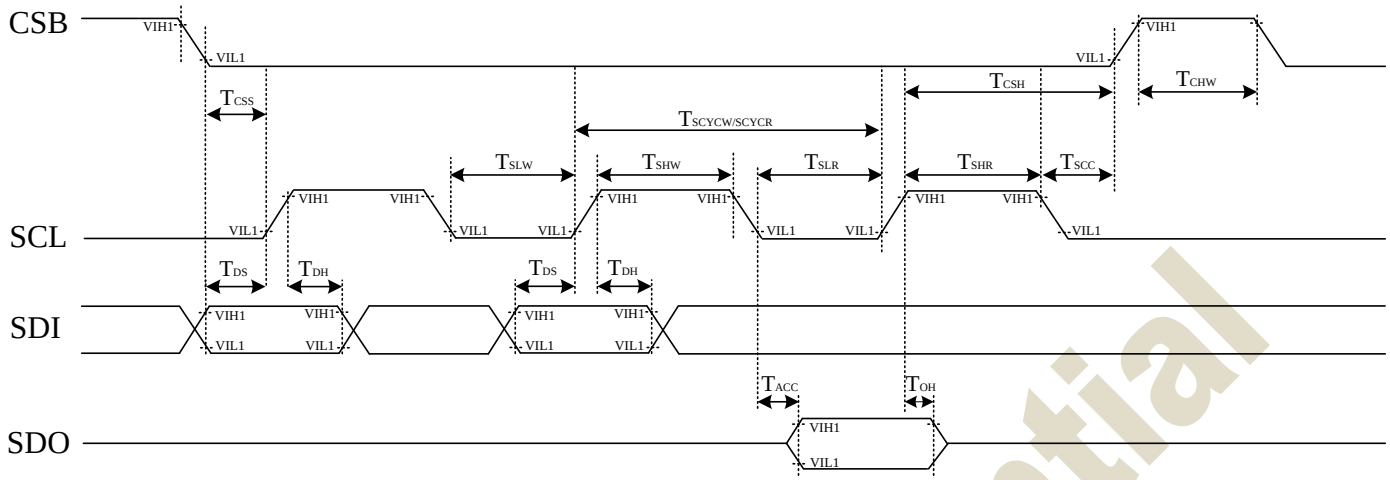

Figure 7.9: 3-wire SPI interface characteristics

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max	
Chip select setup time	T_{CSS}	120	-	-	ns
Chip select hold time	T_{CSH}	220	-	-	ns
Chip select setup time	T_{SCC}	120	-	-	ns
Chip select high width	T_{CHW}	100	-	-	ns
Serial clock cycle (Write)	T_{SCYCW}	74	-	-	ns
SCL “H” pulse width (Write)	T_{SHW}	37	-	-	ns
SCL “L” pulse width (Write)	T_{SLW}	37	-	-	ns
Serial clock cycle (Read)	T_{SCYCR}	200	-	-	ns
SCL “H” pulse width (Read)	T_{SHR}	100	-	-	ns
SCL “L” pulse width (Read)	T_{SHL}	100	-	-	ns
Data setup time	T_{SDS}	18	-	-	ns
Data hold time	T_{SDH}	18	-	-	ns
Access time	T_{ACC}	10	-	75	ns
Output disable time	T_{OH}	10	-	75	ns

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8. I2C FORMAT

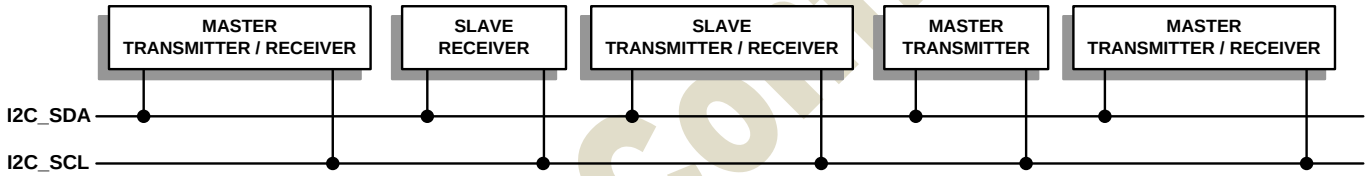
The I^2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I^2C_SDA) and the Serial Clock Line (I^2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I^2C-Bus Protocol:

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

(b) Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



8.1 Register write sequence of I^2C interface

JD9165 supports register write sequence via I^2C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) JD9165 DA[6:0]=110_1000

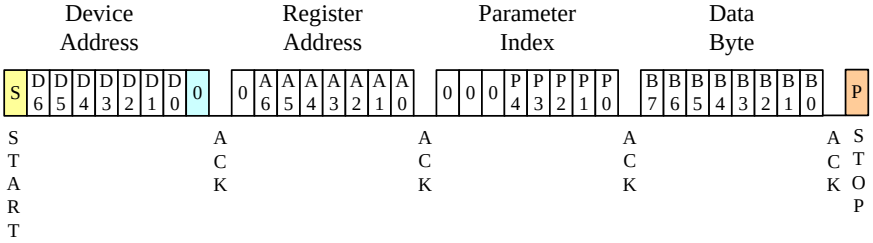


Figure 8.1: Single Register Writing Timing

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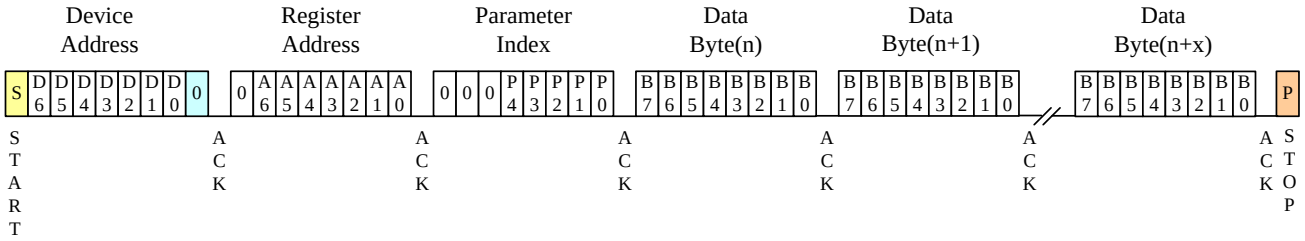

Figure 8.2: Multi Register Writing Timing

8.2 Register read sequence of I^{2}C interface

JD9165 supports register read sequence via I^{2}C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.

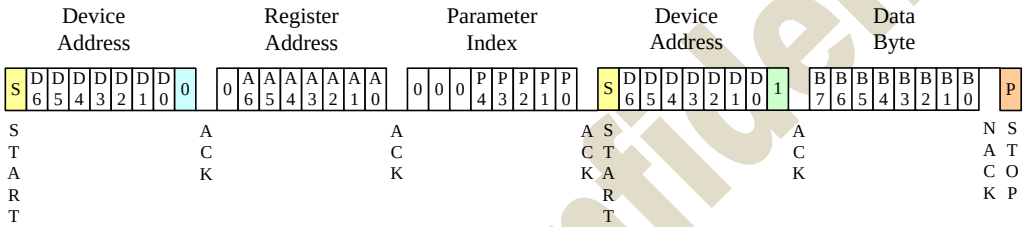

Figure 8.3: Single Register Reading Timing

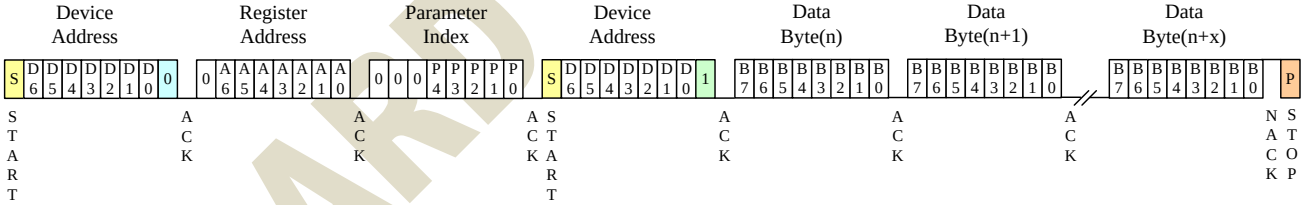

Figure 8.4: Multi Register Reading Timing

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9. DC CHARACTERISTICS

9.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	-0.30	-	3.96	V	
IO supply voltage	VDDIO	-0.30		3.96	V	
AVDD voltage	AVDD	-0.30	-	12	V	
VGH voltage	VGH	-0.30	-	VGL+32V	V	
VGL voltage	VGL	VGH-32V	-	0.30	V	
VMID voltage	VMID	-0.30	-	6.6	V	
VCOM voltage	VCOM_OP	-0.30	-	5.43	V	
VOTP **(OTP power)**	VOTP	-	-	9	V	
Operating Temperature	T_{OPR}	-20	-	+85	℃	
Storage temperature	T_{STG}	-55	-	125	℃	

9.2 Typical operating condition

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	1.71	1.8	2.0	V	MIPI mode condition1
I/O power voltage	VDDIO	1.71	1.8	2.0	V	
Supply power voltage	VDD	2.5	3.0	3.3	V	MIPI mode condition2
I/O power voltage	VDDIO	2.5	3.0	3.3	V	
AVDD voltage	AVDD	9	10	11	V	
VGH voltage	VGH	15	18	20	V	
VGL voltage	VGL	-12	-8	-6	V	
VMID voltage	VMID	4.5	5	5.5	V	
VMID_OP voltage	VMID_OP	4.5	5	5.5	V	
VQHO voltage	VQHO	-	0.7AVDD	-	V	
VQLO voltage	VQLO	-	0.3AVDD	-	V	
VCOM voltage	VCOM_OP	2.7	3.8	4.94	V	
VOTP	VOTP	7.5	7.75	8	V	

Note: VDD operation voltage range must depend on FPC circuit.

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9.3 VDD power on slew time

Be sure that VDD input can't result automatically in power on sequence.

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
VDD power on skew time	T_{POR}	From 0V to 1.35V	0.05	-	5	ms

9.4 Timing requirements for RESX

When RESX of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDD=1.71V to 2.0V / 2.5V to 3.3V , VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		6	-	-	µs

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10. Revision History

Reversion	Content	Date
0.0.0	New SPEC	2021/11/05
0.0.1	Modify VMIDOP_EN definition(p10)	2022/06/21

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