NOVATEK 聯詠科技

Data Sheet

NT35532

One-chip RAM-less Driver IC
for 16.77M colors Full-HD a-Si GOA TFT LCD with MIPI/SPI/I2C Interface

Version 4.0
2014/07/04

Index

Reversion History

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Preliminary Version	Steve Chiang	Charley Chou		2013/04/12
0.01	1. Modify Source driver output (page 7.) 2. Modify ENPWRP/ENPWRN to digital output (page 16.) 3. Modify CGOUTL[18:1] and CGOUTR[18:1] to CGOUTL[20:1] and CGOUTR[20:1] (page 17.) 4. Add Block diagram (page 10.) 5. Add HBM mode in 0x5300 (page 184.) 6. Add 0xE1h IDLE MODE BL Control (page 214.) 7. Add 0xBAh DSI mode selection(page.202.) 8. Add Output Voltage Level(page.9)	Aaron Tan	Charley Chou		2012/09/17
0.02	1. Add CGTEST3, CGTEST4 (page. 19) 2. Add HBP and HFP application restriction (page. 207) 3. Modify VP_HSSI, VDD typical voltage level (page.231, 233) 4. Modify parameters of table “Required Peripheral Timing” (P.133)	Aaron Tan Steve Chiang	Charley Chou		2013/03/28
0.03	1. Modify “Block Diagram” (page.10) 2. ”TOP_PATEN”, “TOP_COM”, ”BOTM_PATEN”, ”BOTM_COM” pin description move to “Panel Test Pins” block. (page.20) 3. Modify “Required Peripheral Timing” Table. (page.133) 4. Modify OSC spec: 14MHz -> 14.66MHz (page.134) 5. Modify VDDAM range : 1.65 ~ 3.6V (page.8,11,229,231,241-244) 6. Remove 3D function (include BCh command) description. (page.8,9,67,154,188,204) 7. Modify VBP/VFP/HBP/HFP constraints. (page.206) 8. Add current consumption data. (page.230)	Steve Chiang	Chris Chen	Charley Chou	2013/06/07
1.0	1.Modify Block diagram. (page.10) 2.Modify Display Module Pin Configuration for DSI.(page.39,40)	Steve Chiang	Chris Chen	Charley Chou	2013/07/19
1.1	1.Modify LEDPWM frequency. (page.36) 2.Modify MIPI DSI mode selection.(page.202) 3.Modify HBP unit. (page.206)	Steve Chiang	Chris Chen	Charley Chou	2013/08/16
1.2	1.Modify the formula of LEDPWM frequency. (page.36) 2.Modify power ramp up spec. (page.144, 145) 3.Add the constraint of “page setting command” at MIPI I/F. (page.150) 4.Modify the typo: 80MHz → 80Mbps.(page.232)	Steve Chiang	Chris Chen	Charley Chou	2013/11/21
2.0	1.Modify Power Supply On/Off setting sequence. (page.141-143)	Steve Chiang	Chris Chen	Charley Chou	2014/01/06
3.0	1.Modify the pin description of VCI pad (When 2-2 & 3-PWR mode, do not need VCI stabilize cap). (page.11) 2.Modify the pin description of IDLE_ON, LED_BOOST pad. (page.19)	Steve Chiang	Chris Chen	Charley Chou	2014/02/10
4.0	1.Modify the pin description of VSOUT,HSOUT pad. (page.19) 2.Remove Section5.2 “Display Data PATH”. 3.Modify the typo of 0xD9h EXCK_CTRL register. (page.208) 4.Modify the typo of Gamma reference voltage spec. (page.229)	Steve Chiang	Chris Chen	Max Tang	2014/07/04

1. General Description

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35532. IC designers, testing engineers and application engineers should refer to these specifications for circuits design, quality/performance control, and IC applications for customer.

1.2 General Description

The NT35532 device is a single-chip RAM-less solution for a-Si GOA TFT LCD that incorporates gate drivers, a timing controller with glass interface level-shifters, a VCOM driver and a glass power supply circuit.

The NT35532 can support MIPI, SPI and I2C interface. The source resolution can be adjusted from 720RGB to 1080RGB, and the gate resolution also can be set from 1024 lines to 1920 lines. Regarding the detailed resolution setting, please refer to NT35532 Application Note.

The NT35532 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC includes internal boosters that generate the LCD driving voltage, breeder resistance and voltage follower circuit for the LCD driver. A deep standby mode is also supported for lower power consumption.

The NT35532 also supports CABC function for the backlight control. It's able to reduce the total power consumption of display module significantly.

This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA.

2. Features

- **Single-chip Full-HD a-Si GOA Controller / Driver.**
- **Principal Display Resolution**
  - 1080RGB x 1920 (1:1 Multiplexer for source driver, Source output from S1 to S1620, and S1621 to S3240)
  - 1050RGB x 1680 (1:1 Multiplexer for source driver, Source output from S1 to S1575, and S1666 to S3240)
  - 1050RGB x 1400 (1:1 Multiplexer for source driver, Source output from S1 to S1575, and S1666 to S3240)
  - 1024RGB x 1280 (1:1 Multiplexer for source driver, Source output from S1 to S1536, and S1705 to S3240)
  - 1000RGB x 1600 (1:1 Multiplexer for source driver, Source output from S1 to S1500 and S1741 to S3240)
  - 960RGB x 1440 (1:1 Multiplexer for source driver, Source output from S1 to S1440, and S1801 to S3240)
  - 960RGB x 1280 (1:1 Multiplexer for source driver, Source output from S1 to S1440, and S1801 to S3240)
  - 900RGB x 1600 (1:1 Multiplexer for source driver, Source output from S1 to S1350, and S1891 to S3240)
  - 900RGB x 1440 (1:1 Multiplexer for source driver, Source output from S1 to S1350, and S1891 to S3240)
  - 850RGB x 1360 (1:1 Multiplexer for source driver, Source output from S1 to S1275, and S1966 to S3240)
  - 810RGB x 1440 (1:1 Multiplexer for source driver, Source output from S1 to S1215, and S2026 to S3240)
  - 800RGB x 1280 (1:1 Multiplexer for source driver, Source output from S1 to S1200, and S2041 to S3240)
  - 768RGB x 1366 (1:1 Multiplexer for source driver, Source output from S1 to S1152, and S2089 to S3240)
  - 720RGB x 1280 (1:1 Multiplexer for source driver, Source output from S1 to S1080, and S2161 to S3240)
- **Display Modes**
  - Full Color Mode: 16.77M-colors
  - Reduced Color Mode: 262K-colors
  - Reduced Color Mode: 65K-colors
  - Only supported Normal Display Mode
- **Interface**
  - MIPI DSI Interface (D-PHY: V1.1 , DSI:1.01.00, DCS:1.01.00)

    MIPI I/F Supported 2, 3 or 4 data lanes (Lane number is selected by register Bah of CMD1 in MIPI LP mode, and this register can be programmed by MTP)
  - I2C Interface
  - SPI Interface
  - Multi-interface (MIPI + SPI (8/9-bits) or MIPI + I2C by HW pin or register setting)
- **Display Features**
  - Individual gamma correction setting for RGB dots
  - Deep standby function

- **On Chip Function**
  - DC/DC converter
  - VCOM voltage generator
  - Supports control signals (CGOUTR1~R20, CGOUTL1~L20) to gate driver in the LCD panel
  - Provide OTP (1 time) to store related Power, a-Si setting, and gamma setting
  - Provide MTP (3 times) to store VCOM, ID1, ID2, ID3 and DDB calibration
  - Oscillator for display clock generation
  - On module checksum checking
  - Image enhancement technology

- **Content Adaptive Backlight Control (CABC) Function**
  - Histogram analysis & data process
  - Dimming control
  - Only supported in full display mode

- **Supply Voltage Range**
  - Analog supply voltage range VCI to AVSS: 2.5V to 4.8V
  - I/O supply voltage range for VDDI to VSS: 1.65V to 3.6V
  - MIPI DSI supply voltage range for VDDAM to VSS: 1.65V to 3.6V
    (VDDAM can connect to VDDI or VCI if its operation voltage is available)
  - Analog supply voltage range for AVDD to AVSS: 4.5V to 6V
  - Analog supply voltage range for AVEE to AVSS: -4.5V to -6V

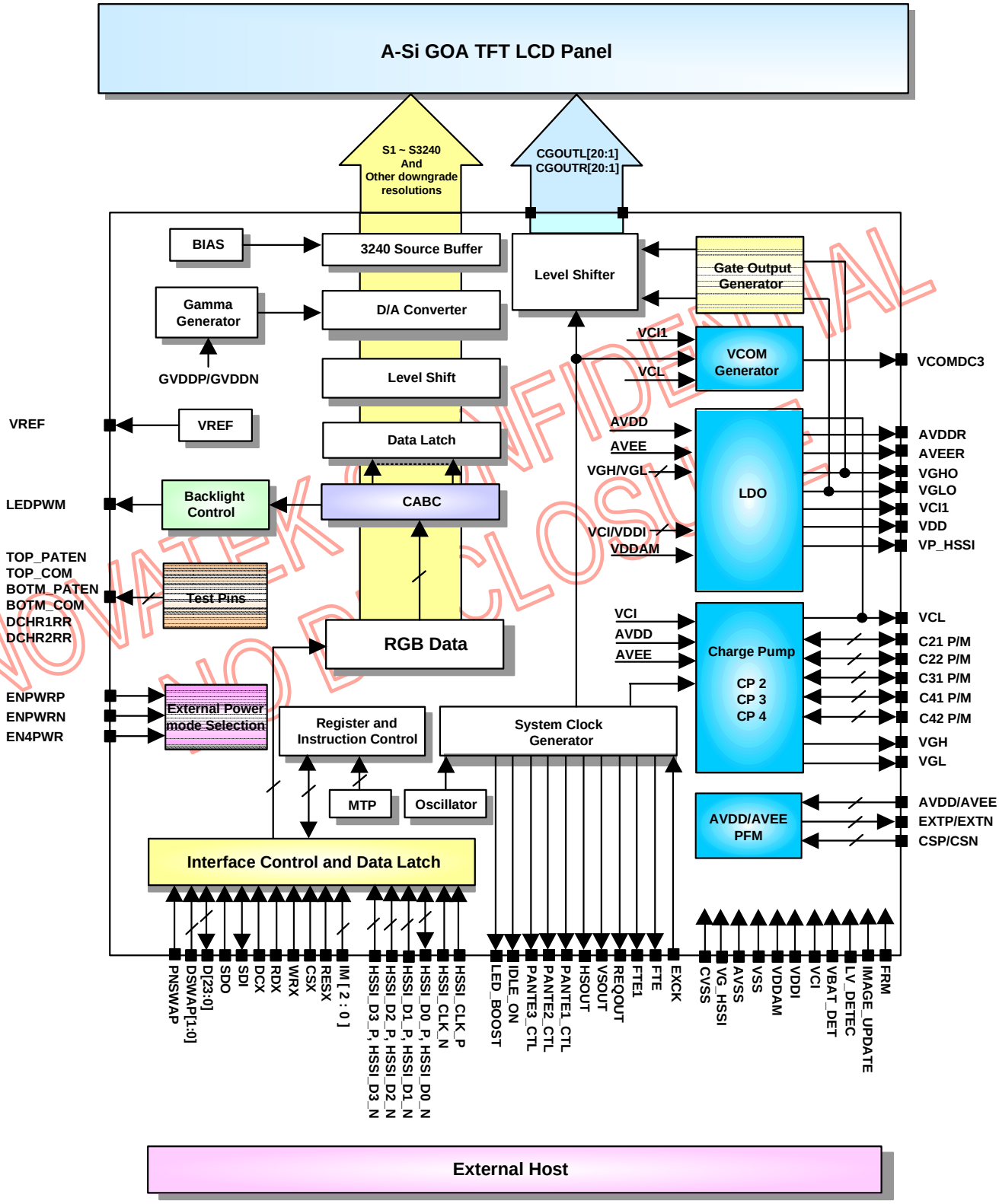
- **Output Voltage Level**
  - Source output voltage level: (GVDDP ~ +0.2V) and (-0.2V ~ GVDDN)
  - Gamma voltage range: GVDDP = 3.5V ~ 5.5V (10mV/step)

    GVDDN = -3.5V ~ -5.5V (10mV/step)
  - Positive gate driver output voltage level: VGH to AVSS = 2 x AVDD, 2 x AVDD – VCL, 2 x AVDD – AVEE, 3 x AVDD – VCL, 3 x AVDD - AVEE

    VGHO = +7V ~ +20V (100mV/step)
  - Negative gate driver output voltage level: VGL to AVSS = AVEE – VCI1, 2 x AVEE, 2 x AVEE – VCI1, 2 x AVEE - AVDD

    VGLO= -4V ~ -18V (100mV/step)
  - Common electrode output voltage level: VCOMDC3 = -4V to +1V (10mV/step)

3. Block Diagram



4. Pin Description

4.1 Pins for Power Input

Symbol	Pad Type	Description
VCI	Power Supply	- Power supply to the liquid crystal power supply analog circuit. Connect VCI to an external power supply with 2-1PWR and 4 PWR modes (VCI = 2.5V to 4.8V). - In 2-2PWR and 3 PWR modes, VCI will be a LDO output.
VDDI	Power Supply	- Power supply to the I/O. - VDDI = 1.65V to 3.6V
VDDI_DC	Power Supply	- Connect to VDDI for preventing noise.
VDDAM	Power Supply	- Power supply for MIPI interface. - VDDAM = 1.65V ~ 3.6V
VSS	Power Ground	- Ground for digital logic. VSS = 0V.
AVSS AVSS_DC	Power Ground	- Ground for the analog unit (regulator, liquid crystal power supply circuit). AVSS = 0V. - In case of COG, connect AVSS to VSS on the FPC to prevent noise.
CVSS	Power Ground	- Ground for the charge pump. CVSS = 0V. - In case of COG, connect CVSS to VSS on the FPC to prevent noise.
VG_HSSI	Power Ground	- Ground for the High Speed Interface regulator. VG_HSSI= 0V. - In case of COG, connect VG_HSSI to VSS on the FPC to prevent noise.
AVDD	Power Input	- Positive input analog power for driver IC use. - It can be generated by “Internal PFM” or supported by “external PMIC”.
AVEE	Power Input	- Negative input analog power for driver IC use. - It can be generated by “Internal PFM” or supported by “external PMIC”.
VBAT	Powe input (AVDD-VSS)	- Battery voltage detection input signal. - If not used, please tie it to VSS.
VCI_DET	Powe input (VCI-VSS)	- Battery voltage detection input signal. - It is used to connect to VCI.
EXTP	Output	- Control output for gate of NMOS in positive internal PFM converter when ENPWRP = AVSS. - If not used, please let this pin open.
EXTN	Output	- Control output for gate of PMOS in negative internal PFM converter when ENPWRN = AVSS. - If not used, please let this pin open.
CSP	Analog Input	- Voltage signal for sensing external inductor current in positive Internal PFM converter when ENPWRP = AVSS. - If not used, please let this pin open.
CSN	Analog Input	- Voltage signal for sensing external inductor current in negative Internal PFM converter when ENPWRN = AVSS. - If not used, please let this pin open.

4.2 Pins for MIPI Interface

Symbol	Pad Type	Description
HSSI_CLK_P/N	**MIPI Input**	- DSI_CLK positive/ negative in MIPI interface. - HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the – COG resistance is less than 10 ohm. - For MIPI I/F, if deep standby mode is used, please pull HSSI_CLK_P/N to VSS after issuing deep standby command - If not used, please tie to VSS.
HSSI_D0_P/N	**MIPI I/O**	- MIPI positive/negative data signal line. - HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. - For MIPI I/F, if deep standby mode is used, please pull HSSI_D0_P/N to VSS after issuing deep standby command - If not used, please tie to VSS.
HSSI_D1_P/N	**MIPI Input**	- MIPI positive/ negative data signal line. - HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. - For MIPI I/F, if deep standby mode is used, please pull HSSI_D1_P/N to VSS after issuing deep standby command - If not used, please tie to VSS.
HSSI_D2_P/N	**MIPI Input**	- MIPI positive/ negative data signal line. - HSSI_D2_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. - For MIPI I/F, if deep standby mode is used, please pull HSSI_D2_P/N to VSS after issuing deep standby command - If not used, please tie to VSS.
HSSI_D3_P/N	**MIPI Input**	- MIPI positive/ negative data signal line. - HSSI_D3_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. - For MIPI I/F, if deep standby mode is used, please pull HSSI_D3_P/N to VSS after issuing deep standby command. - If not used, please tie to VSS.

4.3 Pins for SPI / I2C Interface

Symbol	Pad Type	Description
CSX	**Digital Input (VDDI – VSS)**	- Chip select input pin of NT35532. CSX = “0” (VSS): Selected (accessible) CSX = “1” (VDDI): Unselected (not accessible) - If not used, please pull it to VDDI.
DCX	**Input**	- This pin is used for SPI 8-bits I/F. - If not used, please tie this pin to VDDI.
WRX (SCL/ I2C_SCL)	**Digital Input (VDDI – VSS)**	- WRX: Novatek engineering mode. - SCL: A synchronous clock signal in serial interface (SPI) operation. - I2C_SCL: Serial input / output clock in I2C interface operation. - If not used, please pull it to VDDI.
SDI (I2C_SDA)	**Digital I/O (VDDI – VSS)**	- SDI: Serial data input pin (SDI) in serial interface (SPI) operation. - I2C_SDA: Serial input/output data in I2C-Bus interface operation. - If not used, please pull it to VSS.
SDO	**Digital Output (VDDI – VSS)**	- Serial data output pin (SDO) in serial interface operation. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together. - If not used, please let it floating. - If user wants to save one trace of glass and system can support SDI/SDO share one wire, you can let SDO tie to SDI together on glass.

4.4 Pins for CABC

Symbol	Pad Type	Description
LEDPWM	**Digital Output (VDDI – VSS)**	- This pin is used to connect to the external LED driver of panel backlight control. - PWM type control signal for determining brightness of the LED backlight. - The duty width of this LEDPWM signal is set by an 8-bits value to determine the duty from 0% (Low) and 100% (High). - If not used, please open this pin.

4.5 Pins for Interface Control

<table>
<tr><th>Symbol</th><th>Pad Type</th><th>Description</th></tr>
<tr><td>IM2 – 0</td><td>Digital Input
(VDDI – VSS)</td><td>Selects the interface to MPU (VDDI –VSS amplitude signal).
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Selection</th><th>Data Pins</th><th>Available Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MIPI + I2C</td><td>MIPI : HSSI_D0_P/N ~ HSSI_D3_P/N
I2C : I2C_SDA</td><td>65k, 262k, 16.77M</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MIPI + SPI (9-bits)
(SCL rising edge trigger)</td><td>MIPI : HSSI_D0_P/N ~ HSSI_D3_P/N
SPI : SDI, SDO</td><td>65k, 262k, 16.77M</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MIPI + SPI (8-bits)
(SCL rising edge trigger)</td><td>MIPI :HSSI_D0_P/N ~ HSSI_D3_P/N
SPI : SDI, SDO</td><td>65k, 262k, 16.77M</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI Interface</td><td>HSSI_D0_P/N, HSSI_D1_P/N
HSSI_D2_P/N, HSSI_D3_P/N</td><td>65k, 262k, 16.7M</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note: 1. When user set IM[2:0] = 000b/010b/011b and do not use MIPI I/F, please tie MIPI Clock Lane and Data Lane to VP_HSSI.
2. When user set IM[2:0]=110b, multi-interface function also can be set by CMD1 register F3h.</td></tr>
</table>

4.6 Pins for Logic Function Control

<table>
<tr><th>Symbol</th><th>Pad Type</th><th>Description</th></tr>
<tr><td>RESX</td><td>Digital Input
(VDDI – VSS)</td><td>- This signal will reset the device and must be applied to properly initialize the chip. Signal is active Low.
- There is no internal pull high resistor for this pin.</td></tr>
<tr><td>EXCK</td><td>Digital Input
(VDDI – VSS)</td><td>- External Clock Source to Driver IC.
- This external clock frequency range is 9MHz to 40MHz.
- If not used, please tie it to VSS.</td></tr>
<tr><td>FTE</td><td>Digital Output
(VDDI – VSS)</td><td>- Frame head pulse signal. Utilize this signal when synchronizing RAM data write operations.
- The output voltage level of FTE pin is determined by VDDI.
- If not used, please let this pin floating.</td></tr>
<tr><td>FTE1</td><td>Digital Output
(VDDI – VSS)</td><td>- This signal is used for noise sensing of TP (Generating a pulse output per scan line from NT35532).
- The output voltage level of FTE1 pin is determined by VDDI.
- If not used, please let this pin floating.</td></tr>
<tr><td>REQOUT</td><td>Digital Output
(VDDI – VSS)</td><td>- This signal is used to notice Host to input frame data in interval driving mode.
- The output voltage level of REQOUT pin is determined by VDDI.
- If not used, please let this pin floating.</td></tr>
<tr><td>PNSWAP
DSWAP[1:0]</td><td>Digital Input
(VDDI – VSS)</td><td>- PNSWAP and DSWAP are used for the combination of polarity swap and data lane swap of MIPI.
- If not used, please assigned default state as PNSWAP=1b, DSWAP[1:0]=11b.
<table>
<tr><th>PNSWAP</th><th>DSWAP [1:0]</th><th>D2+</th><th>D2-</th><th>D1+</th><th>D1-</th><th>CLK+</th><th>CLK-</th><th>D0+</th><th>D0-</th><th>D3+</th><th>D3-</th></tr>
<tr><td rowspan="4">0</td><td>00b</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>01b</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>10b</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>11b</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td rowspan="4">1</td><td>00b</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>01b</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><td>10b</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>11b</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
</table>
</td></tr>
<tr><td>EN4PWR</td><td>Digital Input
(VDDI – VSS)</td><td>- Enable or Disable 4PWR mode selection.
- If not used, please tie it to VSS.</td></tr>
</table>

<table>
<tr>
<td>ENPWRP/
ENPWRN</td>
<td>Digital Input
(VDDI – VSS)</td>
<td>- ENPWRP and ENPWRN are used to select four kind power modes for AVDD and AVEE.
<table>
<tr><th>EN4PWR</th><th>ENPWRP,
ENPWRN</th><th>Power Mode</th><th>Input Power</th><th>AVDD</th><th>AVEE</th></tr>
<tr><td rowspan="2">N.A.</td><td>00</td><td>2-1PWR</td><td>VDDI, VCI</td><td>Internal PFM</td><td>Internal PFM</td></tr>
<tr><td>10</td><td>2-2PWR</td><td>VDDI, AVDD</td><td>External AVDD</td><td>Internal PFM</td></tr>
<tr><td>0</td><td>11</td><td>3PWR</td><td>VDDI, AVDD, AVEE</td><td>External AVDD</td><td>External AVEE</td></tr>
<tr><td>1</td><td>11</td><td>4PWR</td><td>VDDI, VCI, AVDD, AVEE</td><td>External AVDD</td><td>External AVEE</td></tr>
</table>
Note: For more detail application circuits, please refer to NT35532 Application Note.</td>
</tr>
</table>

4.7 Analog Output for Display Driving

Symbol	Pad Type	Description
VCOMDC3	Analog Output	- VCOMDC3 signal output for panel usage.
S1 to S3240 and SL1/SR1	Analog Output	- Liquid crystal application voltage output lines. - If source output number less than 3240, please let non-used source pins open. - SR1 and SL1 are dummy sources.

4.8 Panel Control Signals

Symbol	Pad Type	Description
CGOUTL[20:1] CGOUTR[20:1]	Digital Output (VGHO – VGLO)	- These pins are used for a-Si GOA control signal. - Please let non-used pins floating.

4.9 Power Supply Pins

Symbol	Pad Type	Description
VDD	LDO output	- Power supply to the internal logic regulator circuit. - Connect a capacitor to stabilize output voltage.
AVDDR	LDO Output	- Positive LDO output for Driver IC usage. - Connect a capacitor to stabilize output voltage.
AVEER	LDO Output	- Negative LDO output for Driver IC usage. - Connect a capacitor to stabilize output voltage.
GVDDP	LDO Output	- Positive LDO output for gamma circuit.
GVDDN	LDO Output	- Negative LDO output for gamma circuit.
VREF	LDO Output	- Reference voltage output from the internal reference voltage generating circuit.
VP_HSSI	LDO Output	- Internal logic regulator output for MIPI high speed / low power mode use. - Connect a capacitor for stabilization.
VGH	Charge Pump Output	- Output voltage from the step-up circuit, and generate from AVDD, AVEE and VCL. - Connect a capacitor to stabilize output voltage.
C21P/C21M/ C22P/C22M	Analog Output	- Capacitor connection pins for the step-up circuit which generate VGH. - If not used, please let these pins floating.
VGL VGLOUT	Charge Pump Output	- Output voltage from the step-up circuit, and generated from AVEE and VCI. - Please tie VGL with VGLOUT together. - Connect a capacitor to stabilize output voltage.
C31P/C31M	Analog Output	- Capacitor connection pins for the step-up circuit which generate VGL. - If not used, please let these pins open.
VGHO	LDO Output	- Positive LDO output for a-Si power generator. - Connect a capacitor to stabilize output voltage.
VGLO	LDO Output	- Negative LDO output for a-Si power generator. - Connect a capacitor to stabilize output voltage.
VCL	Charge Pump Output Or LDO Output	- Output voltage from the step-up circuit or LDO circuit, and generated from AVEE or VCI1. - Connect a capacitor to stabilize output voltage.
C41P/C41M C42P/C42M	Analog Output	- Capacitor connection pins for the step-up circuit which generate VCL. - If not used, please let these pins floating.
VCI1	Charge Pump Output Or LDO Output	- Output voltage from the step-up circuit or LDO circuit, and generated from AVDD or VCI. - Connect a capacitor to stabilize output voltage.

4.10 Test and Dummy Pins

Symbol	Pad Type	Description
DUMMY	DUMMY	- These pins are dummy (possess no function inside), and are not accessible to user. - Please open these test pins.
COGTEST1~4	Output	- Dummy pins to measure contact resistance. COGTEST1~4 pins are internal short.
TEST[12:0]	Input/Output	- Novatek internal test pins. - Please let these pins open.
FRM	Input	- This pin is used for Novatek engineering mode. - If not use, please tie this pin to VSS. FRM: Low – Free Running Mode: Disable; High – Enable
VDDIO	Power Output (VDDI – VSS)	- This pin output a VDDI level for fixed level logic pin used. - If not used, please let it open.
VSOUT	Output	- The VSOUT pin can select to output signal type via register setting. About the detail illustration, please refer to the application notes. *(CMD2 Page4, D6h ~ D8h)* - If not use, please let this pin open.
HSOUT	Output	- The HSOUT pin can select to output signal type via register setting. About the detail illustration, please refer to the application notes. *(CMD2 Page4, D6h ~ D8h)* - If not use, please let this pin open.
IDLE_ON	Digital Output (VDDI – VSS)	- This pin is used for connected to the external LED driver circuit. - It is a control signal to decrease backlight DC current in IDLE LPM mode. - If not used, please let this pin open.
LED_BOOST	Digital Output (VDDI – VSS)	- This pin is used for connected to the external LED driver circuit. - It is a control signal to increase backlight DC current in high brightness mode. - If not used, please let this pin open.
PANTE1_CTL	Digital Output (VDDI – VSS)	- Touch panel noise reduction output signal 1. - If not used, please let this pin open.
PANTE2_CTL	Digital Output (VDDI – VSS)	- Touch panel noise reduction output signal 2. - If not used, please let this pin open.
PANTE3_CTL	Digital Oleutput (VDDI – VSS)	- Touch panel noise reduction output signal 3. - If not used, please let this pin open.
VGH1 VGH2	Power Input (VGHO-VSS)	- This pin is used to discharge function. - If not used, please let this pin short to VGHO.
VS	Digital Input (VDDI – VSS)	- Novatek test mode. - If not used, please pull it to VSS.
HS	Digital Input (VDDI – VSS)	- Novatek test mode. - If not used, please pull it to VSS.
PCLK	Digital Input (VDDI – VSS)	- Novatek test mode. - if not used, please pull it to VSS.
DE	Digital Input (VDDI – VSS)	- Novatek test mode. - If not used, please pull it to VSS.
RDX	Digital Input	- Novatek test mode. - Please tie this pin to VDDI.

	(VDDI – VSS)	
D[23:0]	Digital I/O (VDDI – VSS)	- Novatek test mode. - If not used, please let these pins floating.

4.11 Panel Test Pins

Symbol	Pad Type	Description
TOP_PATEN	Output	- Please let this pin open.
TOP_COM	Output	- Please let this pin open.
BOTM_PATEN	Output	- Please let this pin open.
BOTM_COM	Output	- Please let this pin open.
DCHR1RR	Analog ouput (VGH-VSS)	- For gate signal (Group 1) slope control usage. If user wants to use, please connect a resister. - If not used, please tie it to VSS.
DCHR2RR	Analog ouput (VGH-VSS)	- For gate signal (Group 2) slope control usage. If user wants to use, please connect a resister. - If not used, please tie it to VSS.
IMAGE_UPDATE	Digital Input (VDDI – VSS)	- Image update detection input signal. - If not used, please tie it to VSS.
LV_DETEC	Digital Input (VDDI – VSS)	- Low voltage detection input signal. - If not used, please tie it to VSS.

5. Function Descriptions

5.1 Interfaces (SPI/I2C/MIPI)

The NT35532 provides MIPI DSI, MIPI DSI + SPI (8/9-bits) and MIPI DSI + I2C interface. The interface can be determined by hardware pins (IM[2:0]). When MIPI DSI + SPI (8/9-bits) and MIPI DSI + I2C interface, SPI (8/9-bits) and I2C only support register access. Besides, user also can read and write registers via MIPI interface. But NT35532 doesn't support these two I/F to access register simultaneously. NT35532 also provides another multi-interface selection by register setting (CMD1 F3h), It is only available when IM[2:0] = 110b.

IM2	IM1	IM0	System Interface	Data Pins	Available Colors
0	0	0	MIPI DSI + I2C	MIPI : HSSI_D0_P/N ~ HSSI_D3_P/N I2C : I2C_SDA	65k, 262k, 16.77M
0	0	1	Reserved	Reserved	Reserved
0	1	0	MIPI DSI + SPI (9-bits Type) (SCL rising edge trigger)	MIPI : HSSI_D0_P/N ~ HSSI_D3_P/N SPI : SDI, SDO	65k, 262k, 16.77M
0	1	1	MIPI DSI + SPI (8-bits Type) (SCL rising edge trigger)	MIPI : HSSI_D0_P/N ~ HSSI_D3_P/N SPI : SDI, SDO	65k, 262k, 16.77M
1	0	0	Reserved	Reserved	Reserved
1	0	1	Reserved	Reserved	Reserved
1	1	0	MIPI DSI Interface	HSSI_D0_P/N, HSSI_D1_P/N HSSI_D2_P/N, HSSI_D3_P/N	65k, 262k, 16.7M
1	1	1	Reserved	Reserved	Reserved

Interface Selection of NT35532

5.1.1 SPI Interface

5.1.1.1 General Description for LoSSI

The Module uses a 9-bits serial interface (LoSSI). The chip-select CSX (active low) enables and disables the serial interface. RESX (active low) is an external reset signal. SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDI in the sequence D/CX, D7 to D0. The Graphics Controller Chip reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are command parameters. When D/CX = "0" D7 to D0 bits are commands.

SCL is not a continuous clock and it can be stopped by the host CPU when SCL is low or high after a rising edge of SCL for D0 in the writing mode.

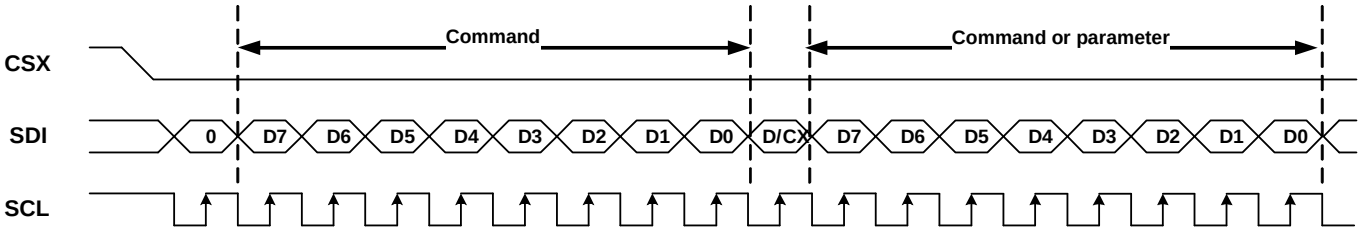
SCL and SDI can be high or low when there is a falling or rising edge of the CSX.

The 8bits serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL), serial data Input (SDI) and serial output data (SDO) for data transmission. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

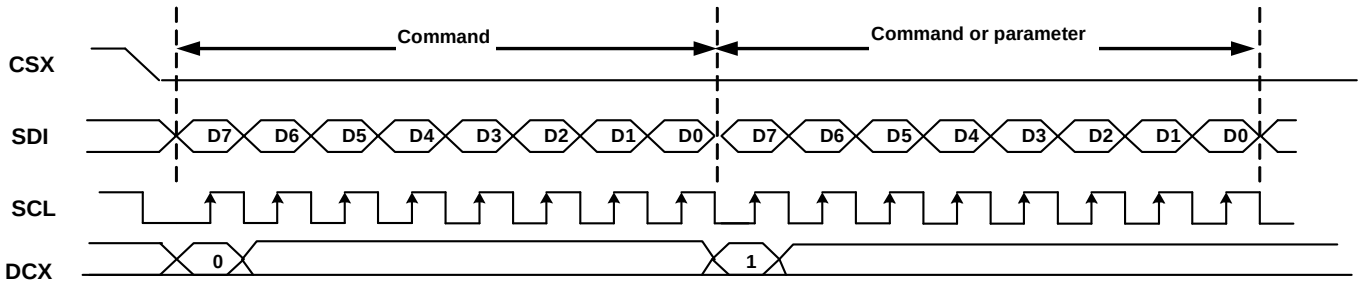
Note: If user wants to save trace of FPC and system can support SDI and SDO share same wire, you can tie SDO to SDI together on glass.

5.1.1.2 Command Write for LoSSI

The host CPU drives the CSX pin low and starts by setting the D/CX-bit on SDI. The bit is read by the display on the first rising edge of SCL. On the next falling edge of SCL the MSB data bit (D7) is set on SDA by the CPU. On the next falling edge of SCL the next bit (D6) is set on SDI. This continues until all 8 Data bits have been transmitted as shown in below figures: Command Write.



Command Write for 9-bits SPI

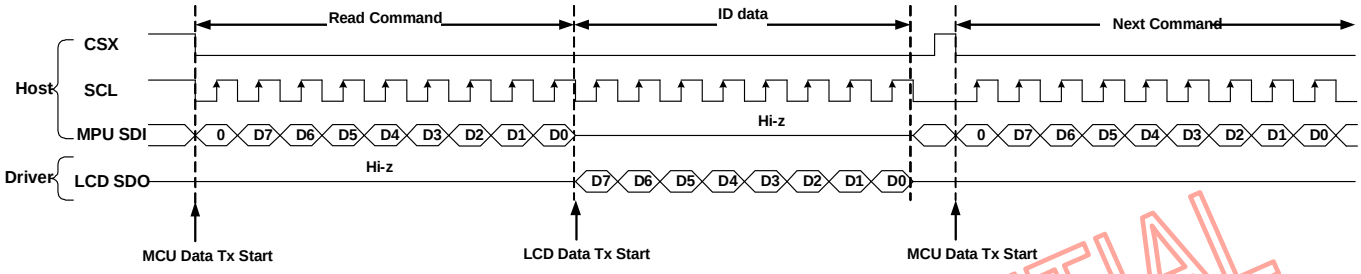


Command Write for 8-bits SPI

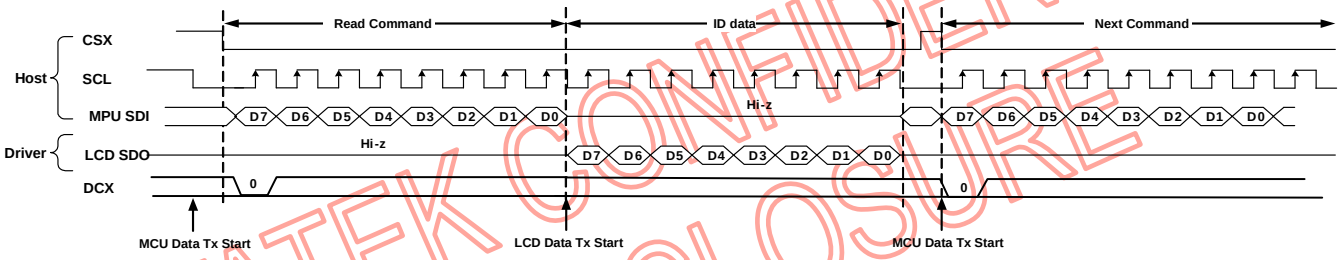
5.1.1.3 Read Functions for LoSSI

8-bits Reading Function without including dummy clock cycle

Reading commands 05h, 0Ah, 0Bh, 0Dh, 0Eh, 0Fh, DAh, DBh, DCh, FEh, 52h, 54h, 56h, 5Fh, AAh, AFh, F4h



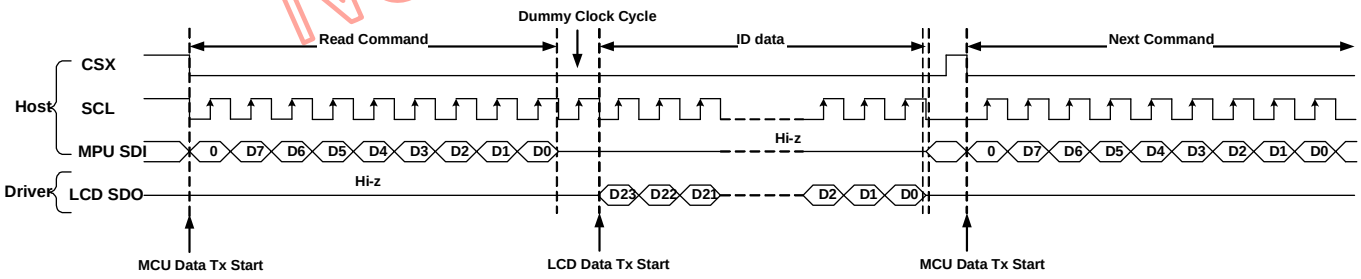
Command Read for 9-bits SPI



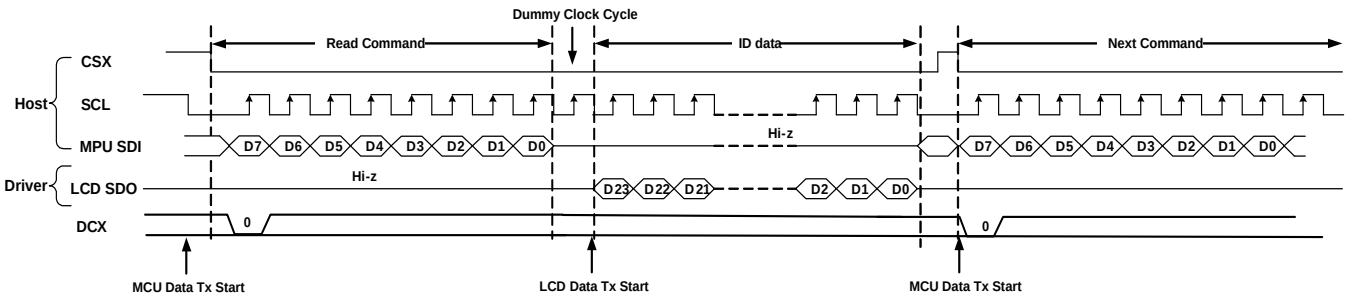
Command Read for 8-bits SPI

24-bits reading function with including dummy clock cycle

Reading command 04h, 46h, A1h, A8h



Command Read for 9-bits SPI

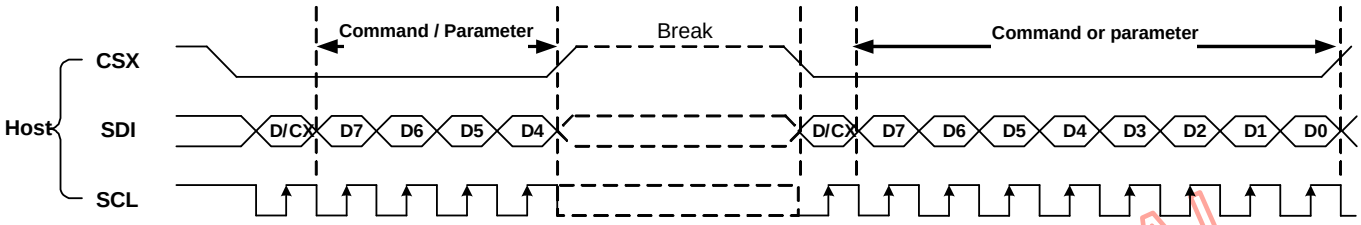


Command Read for 8-bits SPI

Note: In above figure is an ID Data length 24bits example (MSB first and parameter 1 first).

5.1.1.4 Display Module Data Transfer Recovery (example for LoSSI)

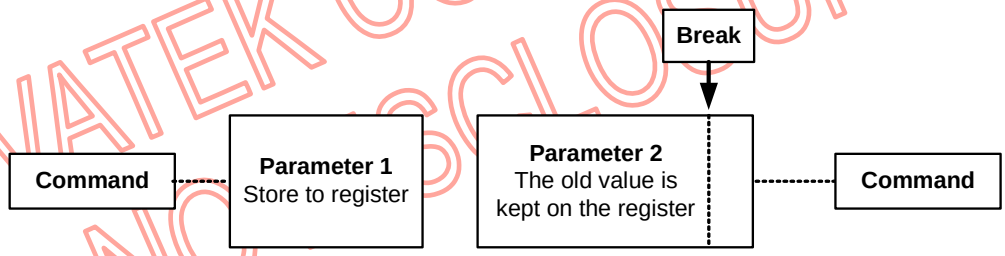
If there is a break in data transmission while transferring command or Multiple Parameter command Data, before a whole byte has been completed, then the Display Module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example:



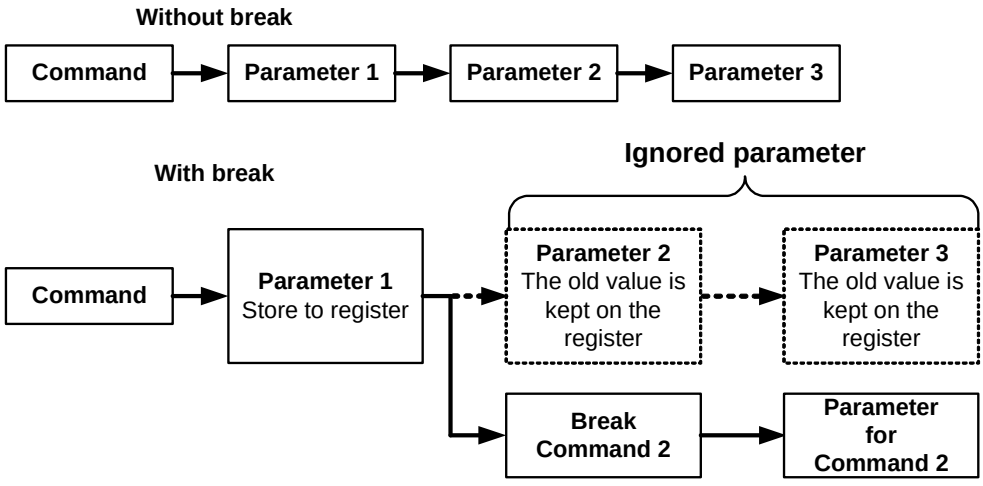
LoSSI and Break

If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

1. Middle of frame



2. Between frames



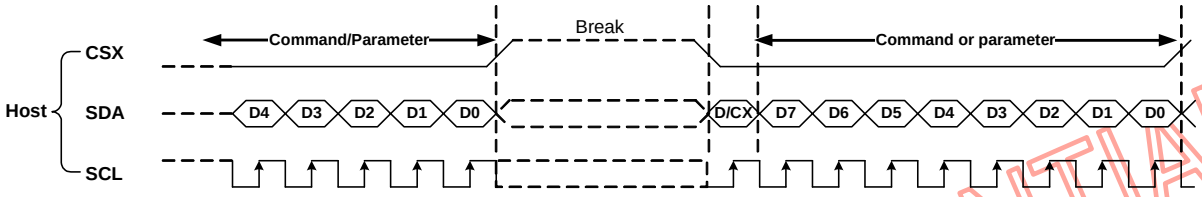
LoSSI and break during parameter

Note: Break can be e.g. another command or noise pulse.

5.1.1.5 Display Module Data Transfer Pause (example for LoSSI)

It will be possible when transferring Command or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of Frame Memory Data, Command or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Command or Parameter Data Transmission from the point where it was

paused as shown below:



LoSSI and Pause

There are 4 cases where there is possible to see this kind of pause:

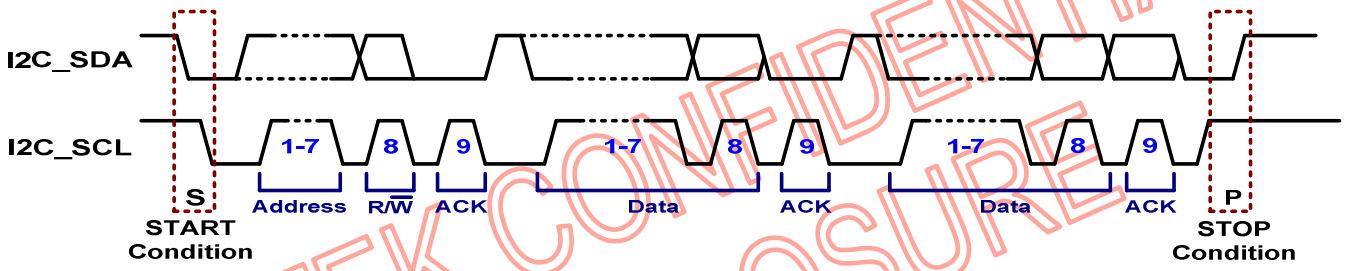
1) Command – Pause – Command
2) Command – Pause – Parameter
3) Parameter – Pause – Command
4) Parameter – Pause – Parameter

5.1.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

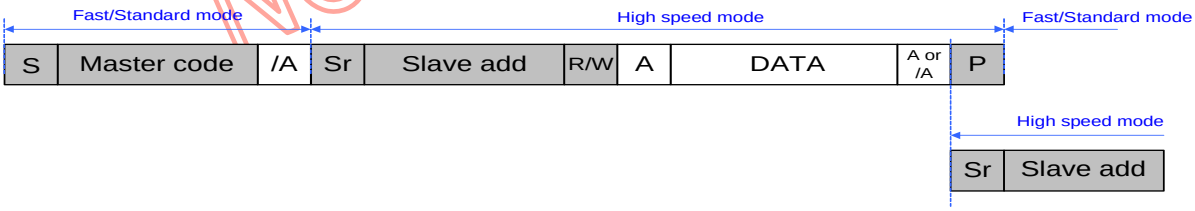
(a) I2C-Bus Protocol:

Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.



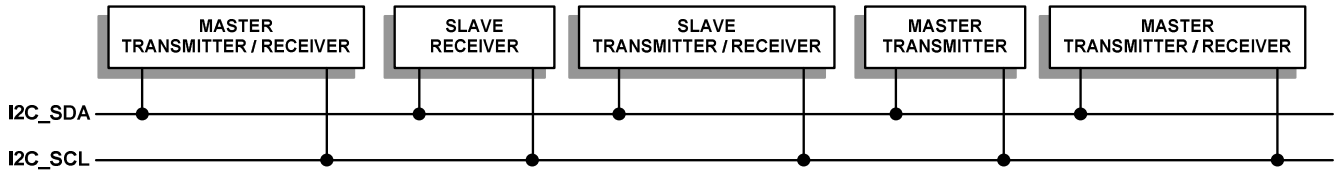
Definition of I2C-Bus Protocol

NT35532 I²C-bus supports high speed mode transfer r(3.4MHz). I²C master must transfer 8 bits “Master codes”, which are not used for slave addressing or other purposes. This master code is binary code “0000_1xxx”. Next diagram shows the sequence from fast/standard mode to high mode and high speed mode to fast/standard mode.



(b) Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



System Configuration

5.1.2.1 Slave Address of I2C

NT35532 supports many slave addresses after the START procedure via I2C bus for MCU usage. A register (CMD1 register F8h) bit I2C_SLAVE_ADDR[6:0] to set the user's desired slave address. And 000_0xxxb and 111_1xxxb except 000_0000h has been reversed. The slave address selection is described as the following table. The I2C interface address is decided by external MPU. 000_0000h is a global address that always can access register of NT35532.

I2C_SLAVE_ADDR[6:0]	Slave Address	Notes
000_0000b	000_000b	000_0xxxb and 111_1xxxb: Reversed excepted 000_0000b
:	:	
111_0110b	111_0110b	
111_0111b	111_0111b	

Selection Table of Slave Address

5.1.2.2 Register Write Sequence of I2C Interface

NT35532 supports register write sequence via I2C-bus transfer. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.

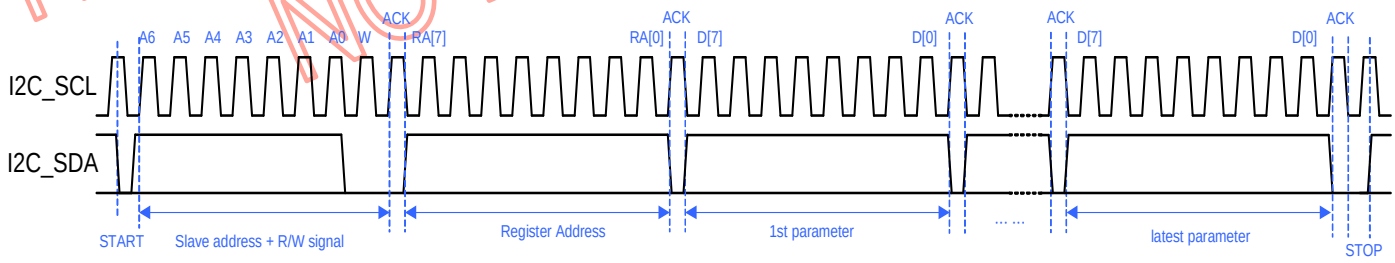
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "zero" for WRITE.

(3) The slave issues an ACK to master.

(4) 8-bits register high byte address transfer first. Then transfer the register low byte address.

(5) 8-bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter.

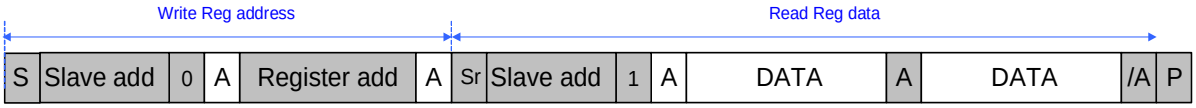
(6) A data transfer is always terminated by a STOP condition.



Register Writing Timing

5.1.2.3 Register Read Sequence of I2C Interface

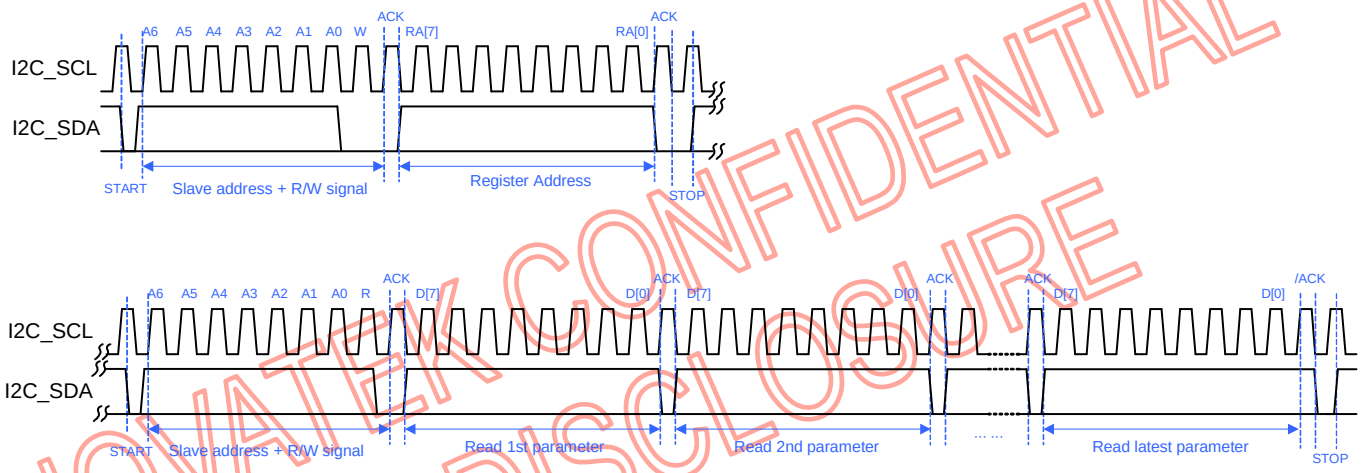
NT35532 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in below.



S: Start condition
P: Stop condition
Sr: Restart condition
A: Acknowledge
/A: No-acknowledge

Master to Slave

Slave to Master



Register Reading Timing of I2C Interface

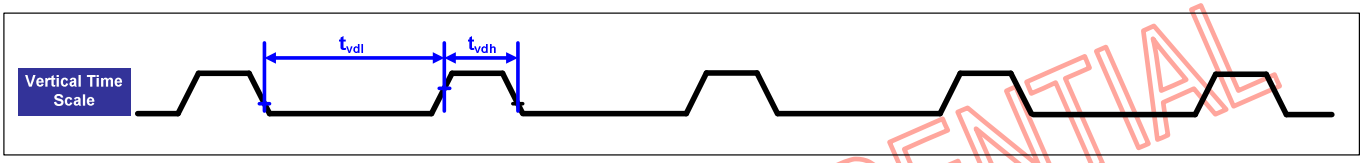
5.2 Frame Tearing Effect Interface

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off and on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.1 Tearing Effect Line Modes

Mode A

The Tearing Effect Output signal consists of V-Blanking Information only：

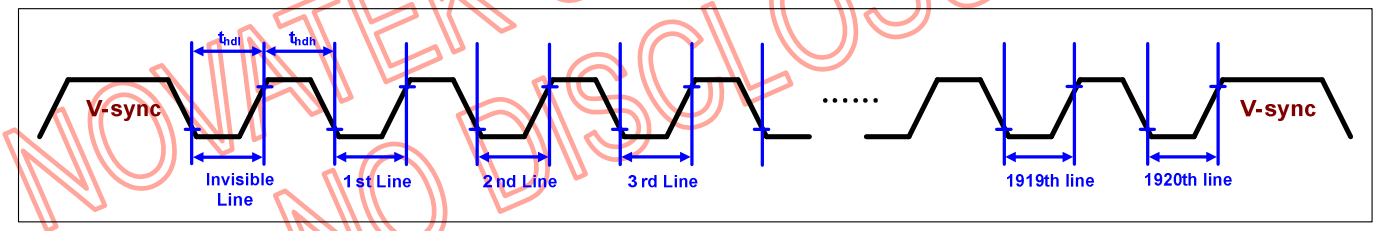


tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode B

The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one Mode" A" TE and 1920H-sync pulses per field.

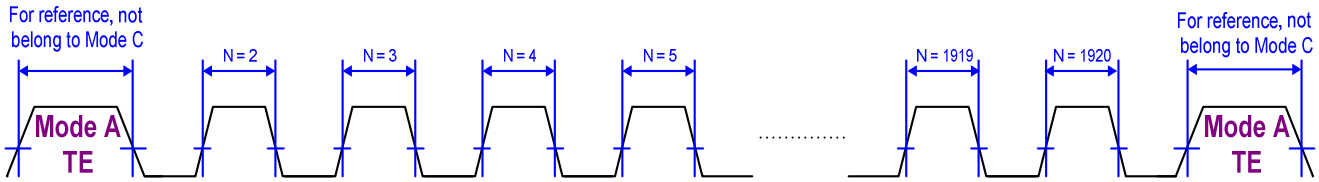


t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

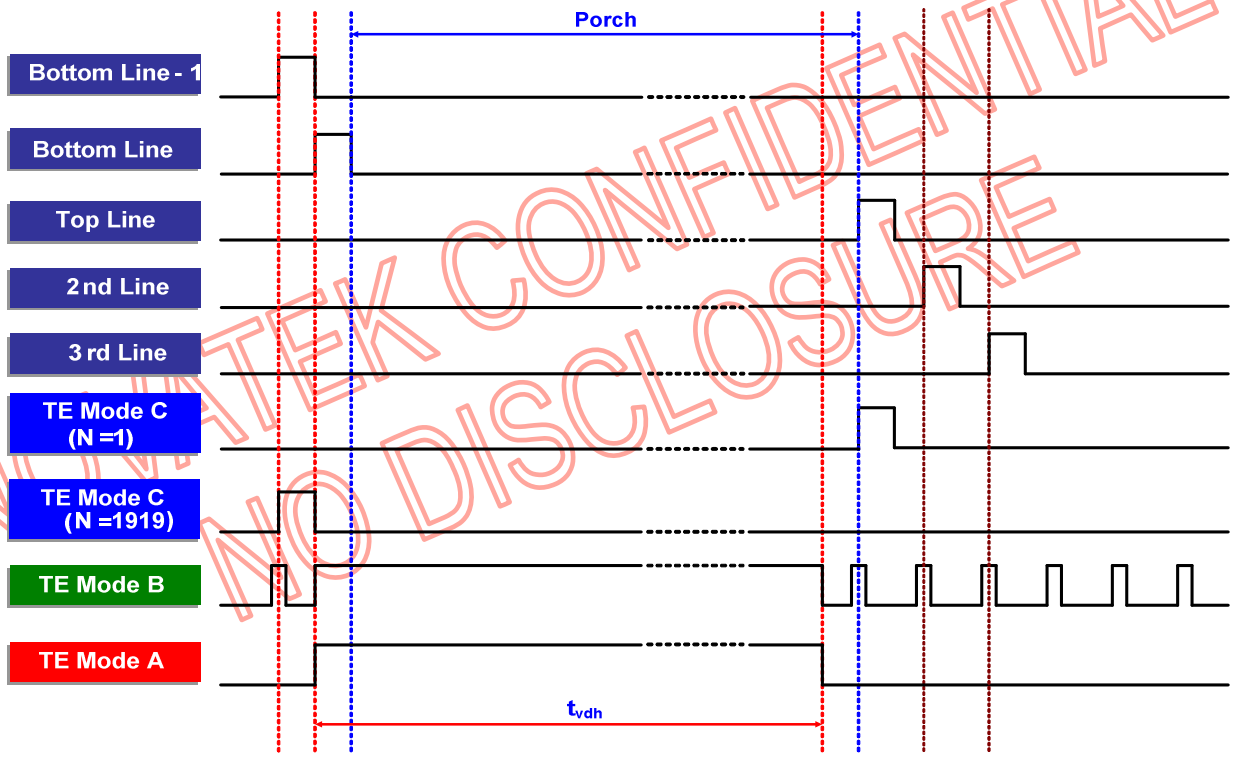
Mode C

This mode turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. In below figure, it shows that TE only output one line period pulse that can be selected from 2nd line to 1920th line by register 4400h and 4401h.



Register 3500h	Register 4400h	TE Output
M	N	
0	0	TE high in V-porch region (A)
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

Where Mode A, Mode B, and Mode C timing chart is shown in below:

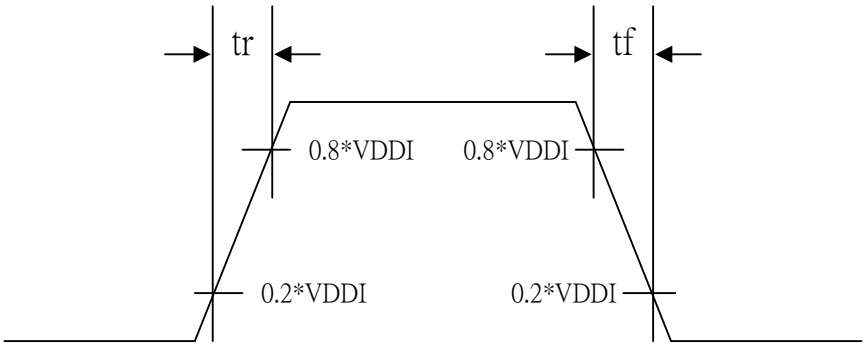


Notes 1: During sleep-in mode, the Tearing Output pin is active Low

Notes 2: N ≧"Horizontal line number" will be ignore in TE mode C. "Horizontal line number" is decided by bit GM[1:0] of 00h (CMD2 Page0).

AC characteristics of Tearing Effect Signal (FTE)

FTE's rising-time and falling-time (tr, tf) are stipulated to equal to or less than 15ns when maximum loading is 30pF.



5.2.2 FTE Output Position Setting

The FTE pulse of “Mode C” is output to the line determined by N[10:0]. The FTE signal can be adopted as the trigger signal for writing image data in synchronization with display operation by detecting the RAM address where data is read out for display.

N[10 : 0]	FTE Output Line
0000h	FTE high only in VBP Region
0001h	2nd lines
0002h	3rd lines
0003h	4th lines
:	:
077Dh	1918th lines
077Eh	1919th lines
077Fh	1920th lines

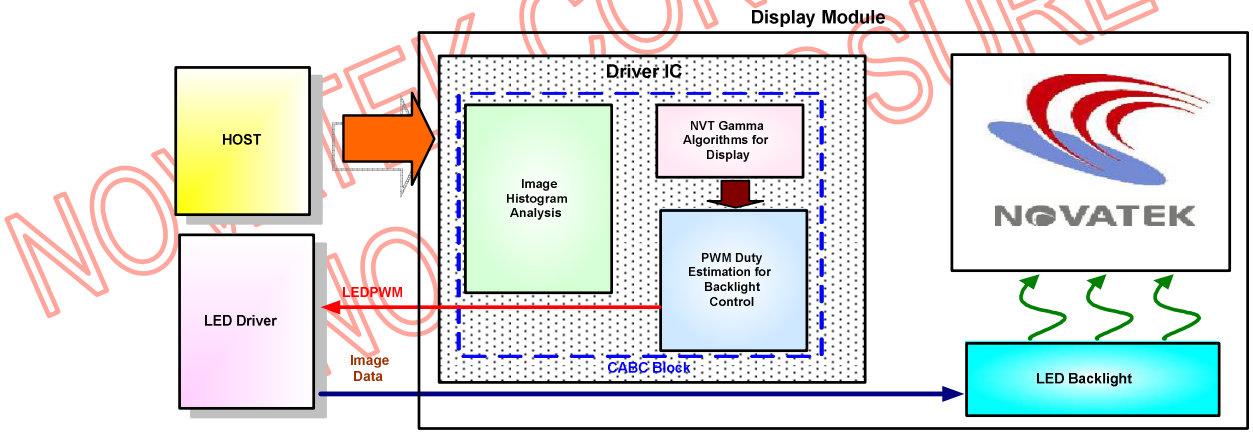
FTE Output Line

5.3 Dynamic Backlight Control Function

The NT35532 supports Backlight-Control function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power consumption and minimize the effect of reduced power on the display image. The display image is dynamically controlled by CABC (Contents Adaptive Backlight Control) block. The availability of this function ranges from moving picture such as TV image to still picture such as menu. However, in order to gain a better display quality and reduce the power consumption of the backlight, the NT35532 internally uses NVT gamma algorithm to produce an optimal backlight control based on different image contents. Therefore, the power consumption of the backlight can be reduced without changing display image. The Backlight-Control function of the NT35532 supports two architectures as shown in below:

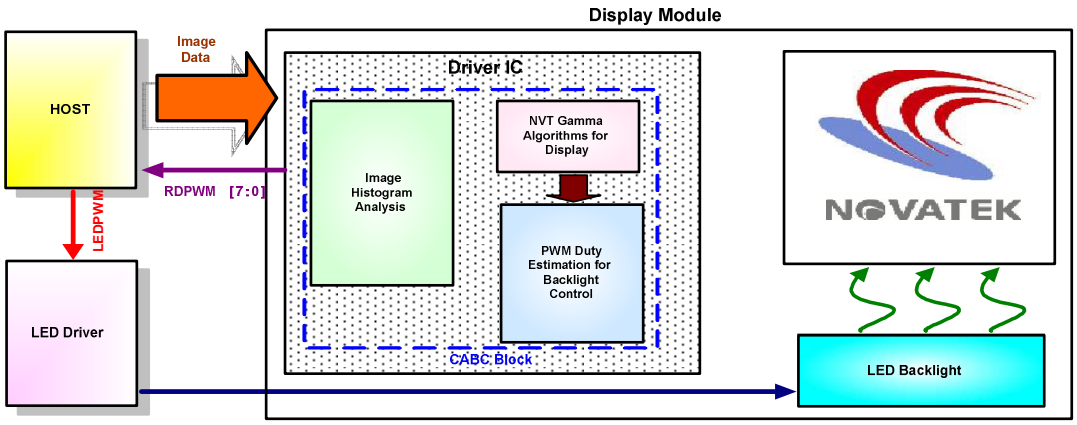
Architecture 1:

The brightness of backlight can directly be controlled by CABC block of the NT35532. The NT35532 will output the PWM duty via "LEDPWM" pin. The PWM duty is determined by CABC processed results based on different image contents. As for this application, user also can set/clear the bit "BL" of CMD1 register 53h to turn on/off the backlight. Besides, the user can control the brightness of the backlight by forcing a specified PWM duty. The CMD2 Page3 register 00h and 2Fh (include of FORCE_CABC_DUTY[7:0] and FORCE_CABC_PWM) is used to forcing the PWM duty.



Architecture 2:

The brightness of the backlight is controlled by the external host processor. In this application, the CABC block of the NT35532 also works and estimates a better gamma setting for improving the brightness of display image, the determined PWM duty information can be read from CMD2 Page3 Register 10h (RDPWM) of the NT35532. Because the backlight is controlled by host processor, user can clear the bit "BL" of the register 5300h for keeping the "LEDPWM" pins as ground level.



5.3.1 Content Adaptive Backlight Control (CABC)

A Content Adaptive Brightness Control (CABC) function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously decreasing brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. The NVT CABC algorithm can adjust the brightness of each gray level without changing the original image contents.

The NVT CABC function provides three operation modes, and these modes can be selected by the CMD1 register 55h. See command "Write Content Adaptive Brightness Control (55h)" (CABC_COND[1:0]) for more information. These three modes are described as:

- Off Mode:

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, the NT35532 will use the original Gamma 2.2 registers setting for display. And if the function of "forced PWM duty" is turn-off (i.e. "FORCE_CABC_PWM" is set as '0'), the PWM duty of the "LEDPWM" pin is 100%.

- UI [User interface] Image Mode (UI Mode):

This mode is applied to optimize for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less. NT35532 provides flexible configuration for UI-Mode via setting the register to choose prefer quality and brightness.

- Still Picture Mode (Still Mode):

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%. The NT35532 will automatically determine a better gamma setting and PWM duty based on different image contents, so the reduction ratio of the power consumption of backlight is not a constant ratio, this ratio will vary between 10% ~ 40% with different image contents.

- Moving Image Mode (Moving Mode):

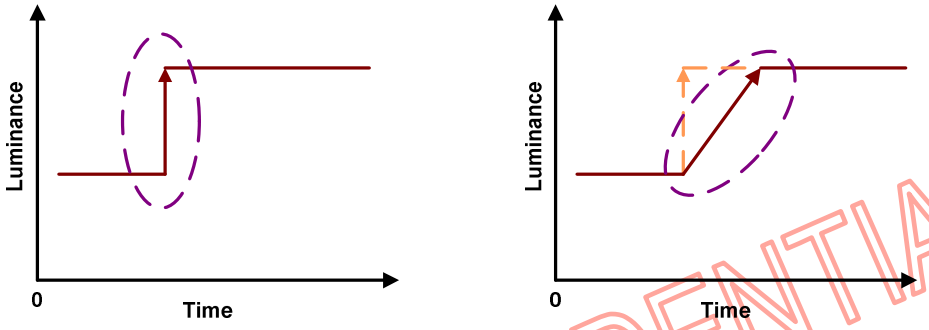
User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%. For this mode, user can flexibly configure a specified gamma algorithm to keep prefer image quality, and the brightness of backlight is dynamically varying with different image contents.

If the "force PWM duty" function is enabled (i.e. "FORCE_CABC_PWM" is set as '1') in any CABC mode, the output PWM duty of "LEDPWM" pin is followed the setting of "FORCE_CABC_DUTY[7:0]".

Note: The CABC can be operated only in the normal display mode.

5.3.2 Display Backlight Dimming Control

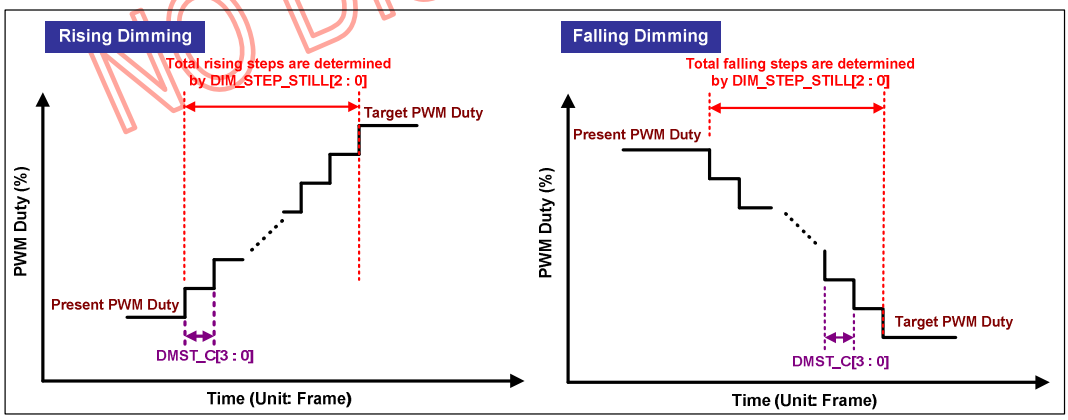
A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic concept is described below.



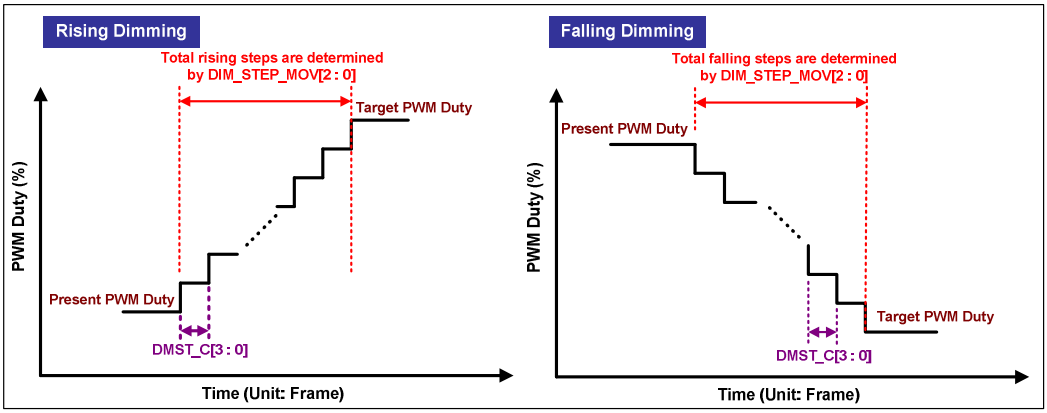
The luminance of the backlight is changed immediately without dimming function disabled

The luminance of the backlight is changed smoothly with dimming function enabled

Dimming function can be enabled and disabled by setting the register 5300h (the setting bit name is “DD”). If “DD” is set as ‘0’, the dimming function will be disabled, otherwise dimming function will be enabled while “DD” = ‘1’. From the original brightness value to the target brightness value, the transferring time steps between these two brightness values are equal making the linearly transition. The rising dimming (increase dimming) and the falling dimming (decrease dimming) use the same registers for setting (“DIM_STEP_STILL[2:0] and DMST_C[3:0]”, or “DIM_STEP_MOV[2:0] and DMST_C[3:0]”). Below figure illustrate the “Fixed-Time” dimming curves for CABC each mode.



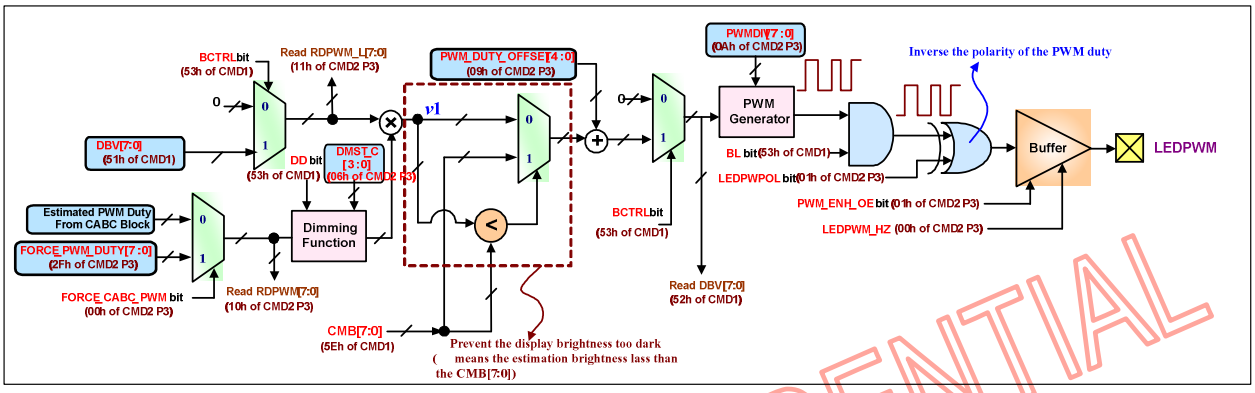
Dimming Mechanism in CABC Off-Mode / UI-Mode and Still-Mode



Dimming Mechanism in CABC Moving-Mode

5.3.3 Brightness Control Lines for Backlight

The NT35532 have a “LEDPWM” pin which can output a PWM signal to the external LED driver IC. There are several control registers which are applied to control the “LEDPWM” status as illustrated in below.



Internal Display Backlight Control Combined With CABC and Manual brightness adjustment

The control bit “BL” is used to keep the LEDPWM in a fixed logic state, here are listed some application in below table:

BL	LEDPWPOL	Status of LEDPWM
0	0	0 (Default)
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

The setting bit “PWM_ENH_OE” is applied to improvement the driving ability of LEDPWM signal, here are listed two driving ability for selection:

PWM_ENH_OE	Status of LEDPWM
0	1X driving ability of LEDPWM
1	2X driving ability of LEDPWM

The setting bit “LEDPWM_HZ” is applied to choose Hi-Z or output enables for “LEDPWM” pins, default 0 (output enable).

LEDPWM pin output	LEDPWPOL=0 & LEDPWM_HZ=0	LEDPWPOL=1 & LEDPWM_HZ=0	LEDPWM_HZ=1
(BL=1 and BCTRL=1) CABC off 0x5500=0	VDDI (LEDPWM_duty=100%)	GND (LEDPWM_duty=0%)	outputs Hi-Z
(BL=1 and BCTRL=1) CABC on 0x5500=1,UI mode 0x5500=2,still mode 0x5500=3,moving mode	PWM waveform (active high)	PWM waveform (active low)	outputs Hi-Z

CMB[7 : 0] (WRCABCMB[7 : 0]):

This register setting is used to limit the minimum PWM duty in order to prevent the backlight brightness too dark.

The registers PWMDIV[7:0] and PWM_DUTY_OFFSET[4:0] can change the frequency and duty compensation of the PWM signal. The PWM operation frequency "F_{OSC}" is "not" the real PWM frequency, the "F_{OSC}" is used to provide clock source for the internal PWM circuit. Two PWM operation frequencies can be chosen by setting register "PWMF", and the real PWM frequency can be quickly estimated by the bellow formula:

PWMF[1:0] (REG "07h" of CMD2 Page3)	PWM Operation Frequency (FOSC)	Real PWM Frequency of LEDPWM
00h	22MHZ	$PWMFrequency = \frac{FOSC}{(256 + Duty\_Count[7:0]) * PWMDIV[7:0]}$
01h (Default)	44MHZ	
02h/03h	Reserved	

For Example:

If the "PWMDIV[7:0]" = 0Ch, "Duty_Count[7:0]" = 00h and PWMF[1:0] = 01h, then:

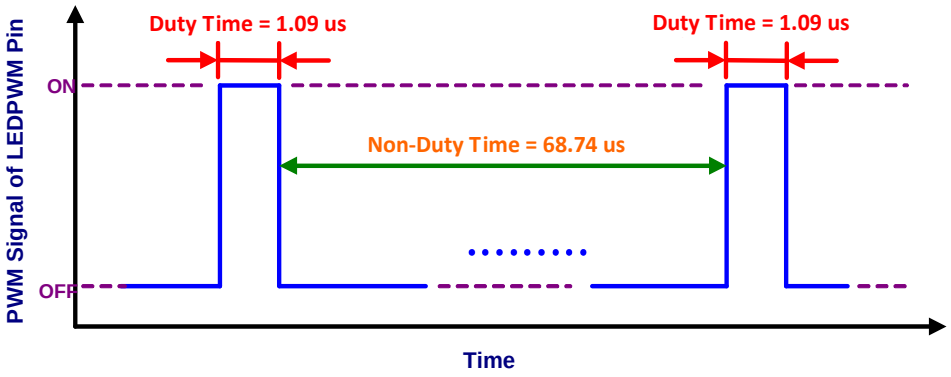
$$PWMFrequency = \frac{44(MHz)}{256*PWMDIV[7:0]} = \frac{44(MHz)}{256*12} \approx 14.32(KHz)$$

About the parameter of Duty_Count[7:0], please refer to the application notes. (CMD2 Page3, 46h)

In this condition, when PWM duty is estimated as "4" (Reading the register "RDDISBV[7:0]" = 03h), then the duty time of the PWM signal can be estimated as shown in below:

$$PWMDutyTime = \frac{4}{256} * \frac{1}{14.32(KHz)} = 1.09(u\,\sec)$$

$$PWMNon-DutyTime = \frac{(256-4)}{256} * \frac{1}{14.32(KHz)} = 68.74(u\,\sec)$$



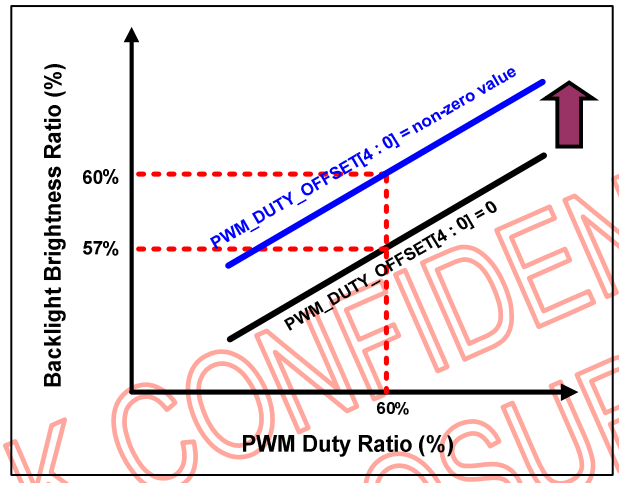
The same, when PWM frequency is 14.32 KHz, and PWM duty of LEDPWM is 256 (Reading the register "RDDISBV[7 : 0]" = FFh), then the duty time can be estimated as shown in below :

$$PWMDutyTime = \frac{256}{256} * \frac{1}{14.32(KHz)} = 69.83(u\,\sec)$$

PWM_DUTY_OFFSET[4:0]:

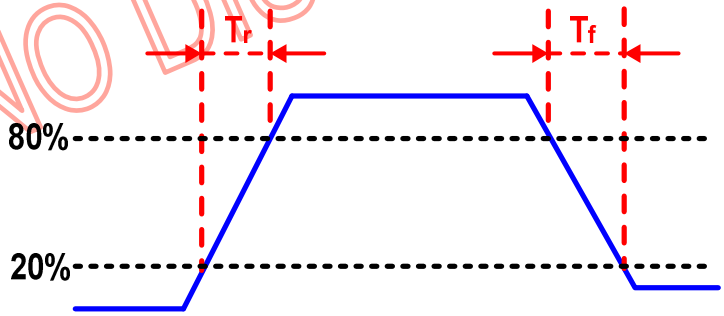
Because the external LED driver needs some stable time to drive the LED backlight, this necessary stable time will reduce the effective PWM duty period, so the PWM_DUTY_OFFSET[4:0] is used to compensate effective PWM duty.

An example is shown in below. When PWM duty of LEDPWM signal is 60%, the backlight brightness should be 60% of original. But user may find that the backlight brightness is 57% of original. So user can set PWM_DUTY_OFFSET[4:0] and let the backlight brightness becomes 60% of original.



Duty Compensation of LEDPWM Signal

Notes: The rising time (Tr) and falling time (Tf) of the "LEDPWM" signal is stipulated to equal to or less than 15ns when maximum load is 30pF.



5.4 MIPI Interface (Mobile Industry Processor Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified from of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

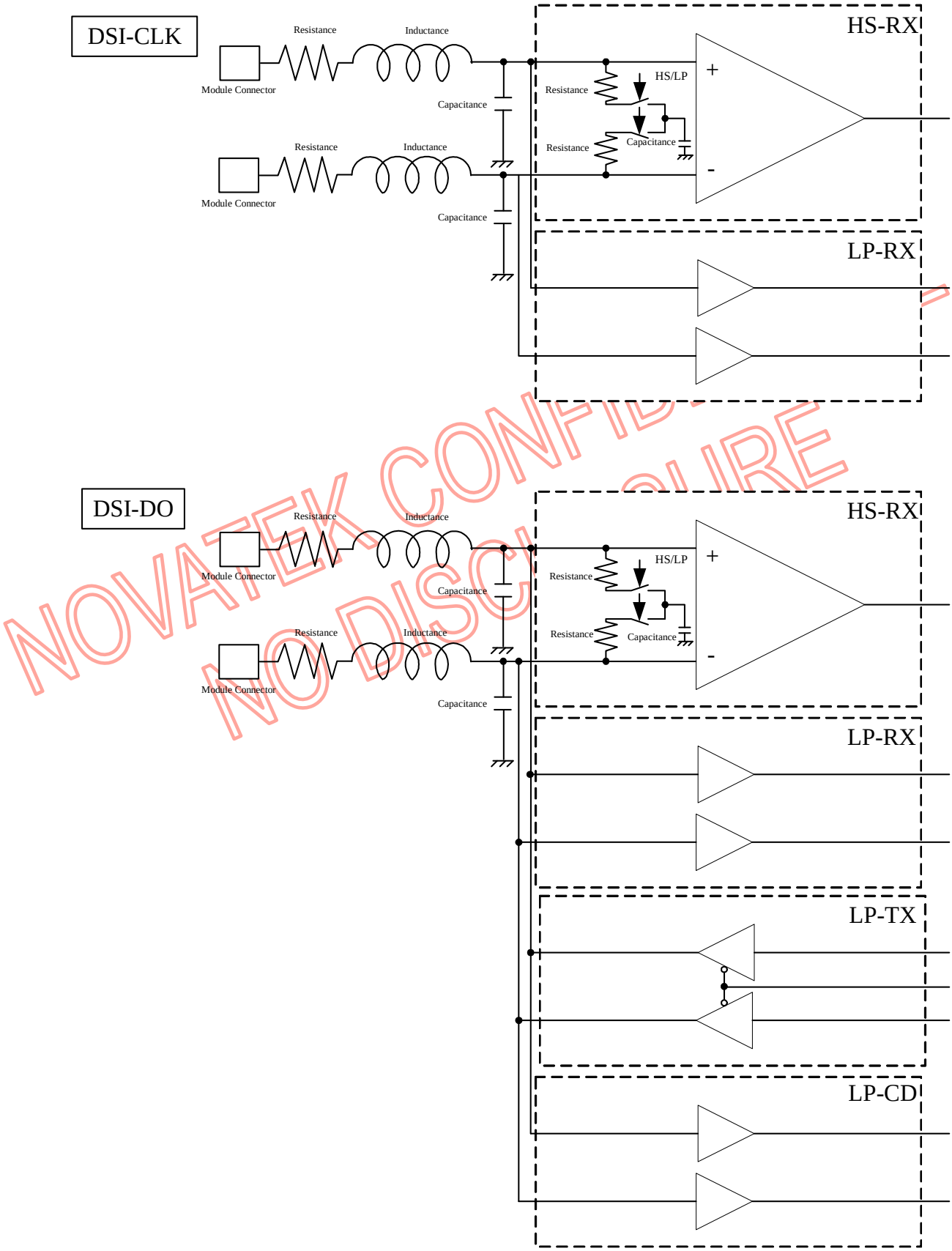
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

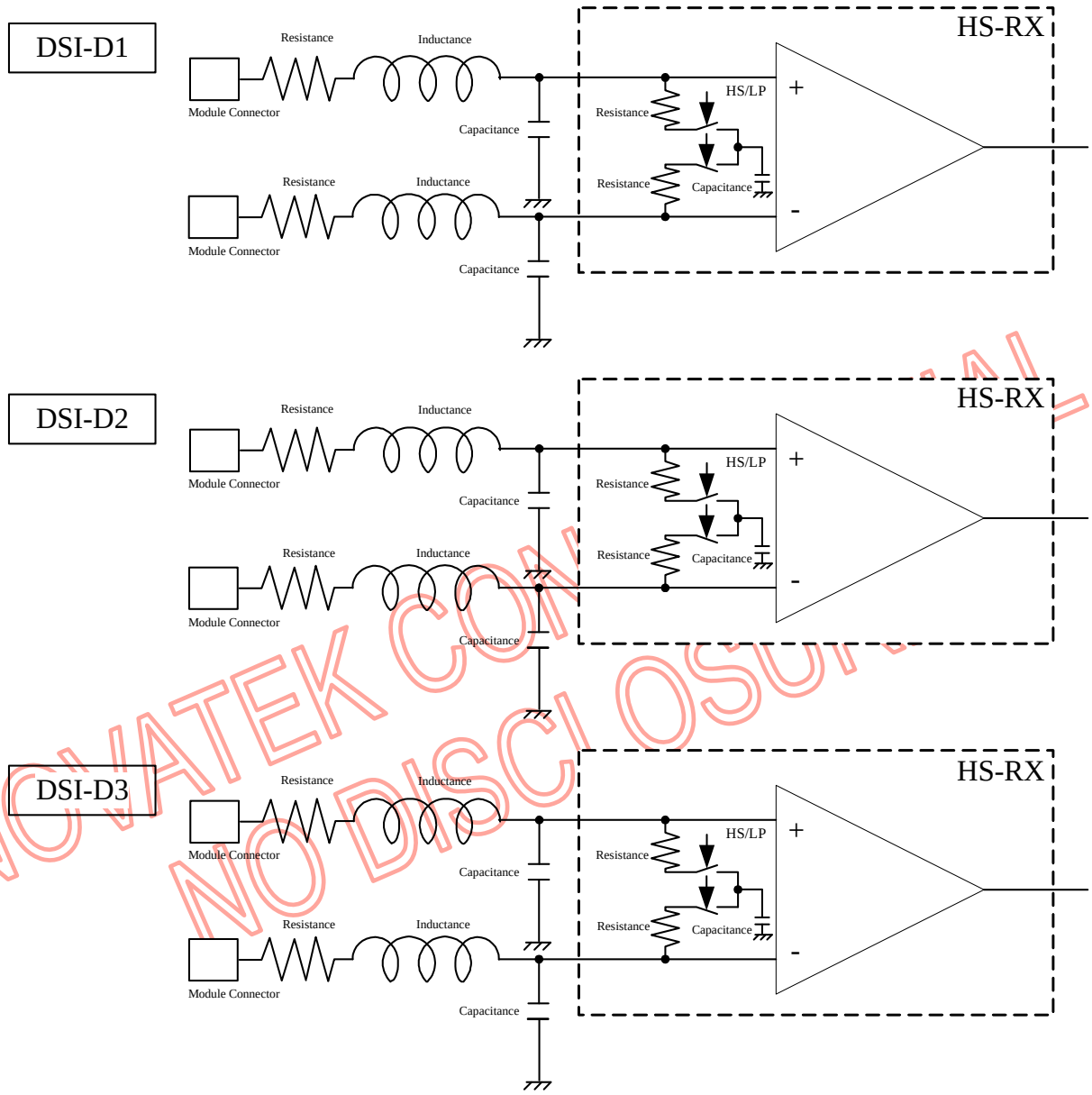
Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1~3	Unidirectional ■ Forward High-Speed

5.4.1 Display Module Pin Configuration for DSI





5.4.2 Display Serial Interface (DSI)

5.4.2.1 General Description

Communication sequences between the MCU and the display module are described on chapter “5.5.2.3.3 Communication Sequences”. The communication can be separated 2 different levels between the MCU and the display module:

- Low level communication what is done on the interface level
- High level communication what is done on the packet level

5.4.2.2 Interface Level Communication

5.4.2.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

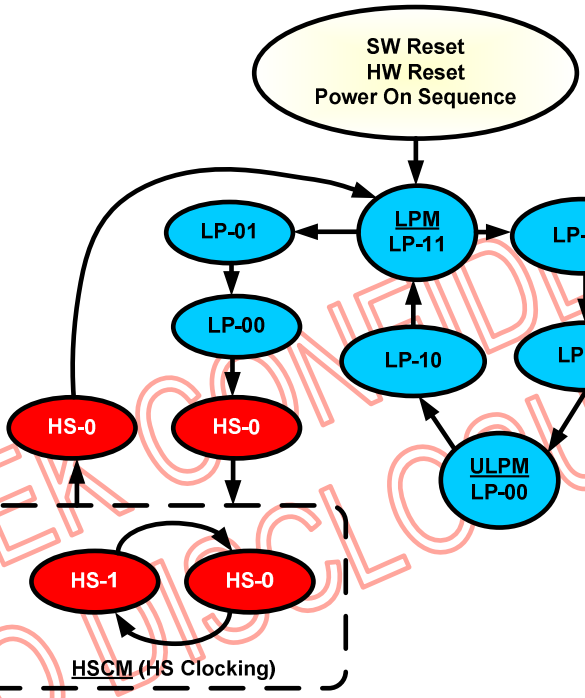
Lane Pair State Code	Line DC Voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dx+ - line	Dx- - line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes 1: Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

Notes 2: If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control mode.

5.4.2.2.2 DSI-CLOCK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences. The principle flow chart of the different clock lanes power modes is illustrated below



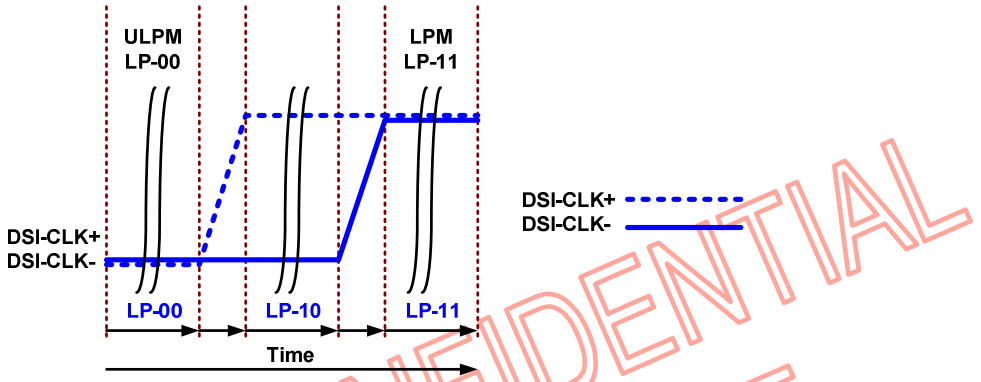
Clock Lanes Power Mode

5.4.2.2.2.1 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

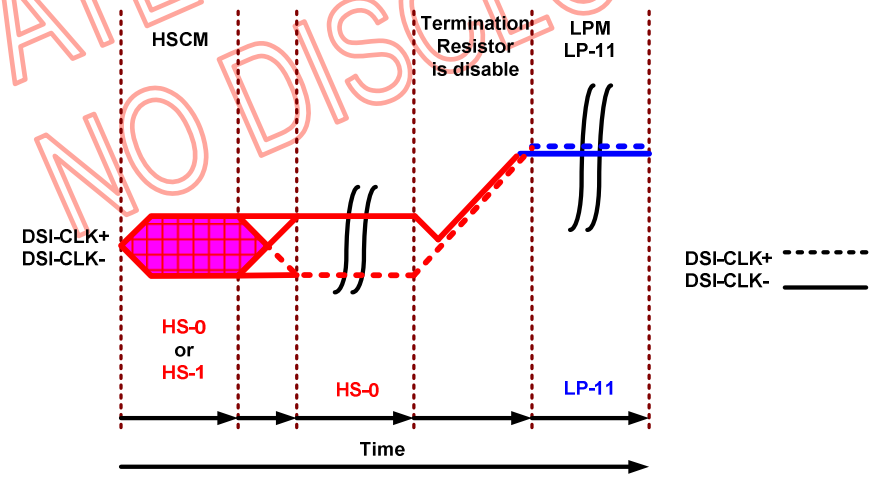
(1) After SW Reset, HW Reset or Power On Sequence =>LP-11

(2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

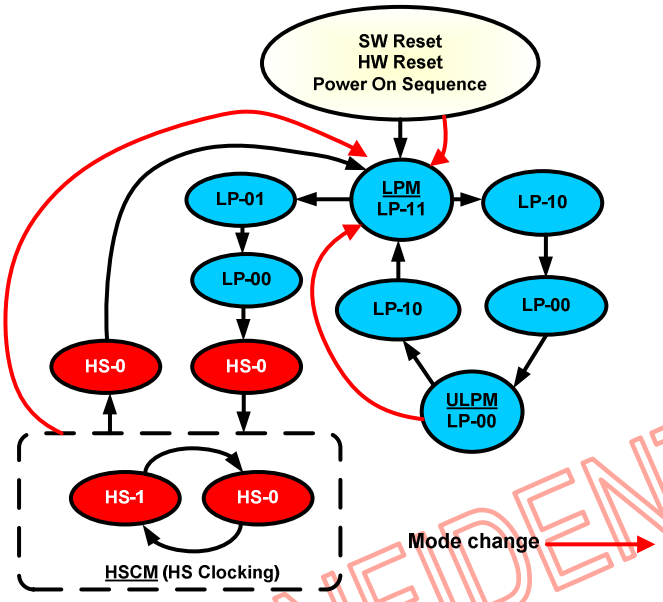


From ULPM to LPM

(3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.



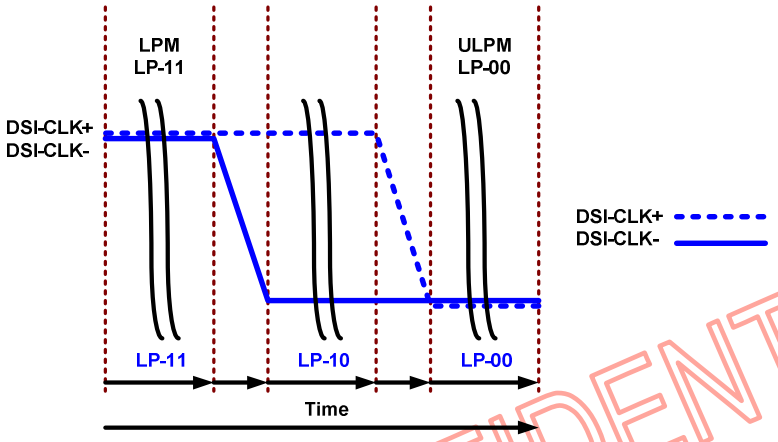
From High Speed Clock Mode (HSCM) to LPM



All Three Mode Changes to LPM on the Flow Chart

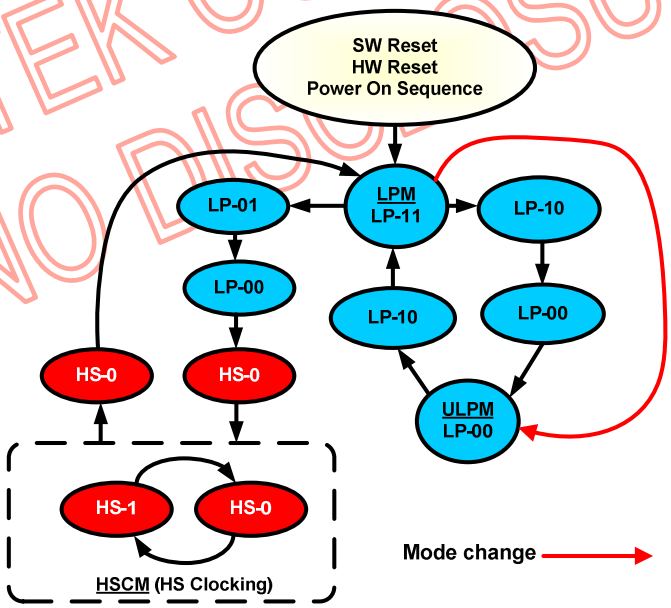
5.4.2.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.



From LPM to ULPM

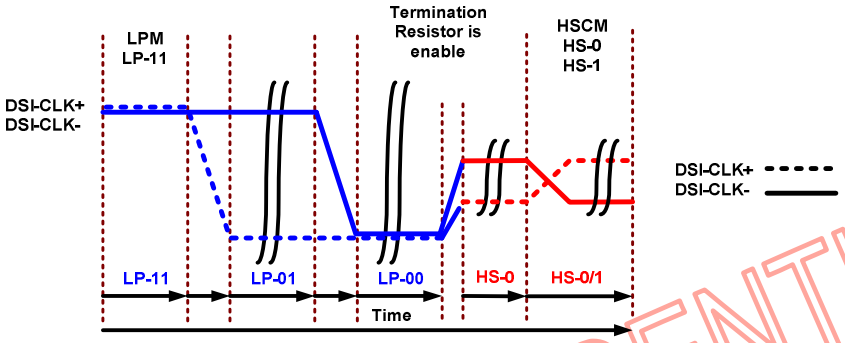
The mode change is also illustrated below.



Mode Change from LPM to ULPM on the Flow Chart

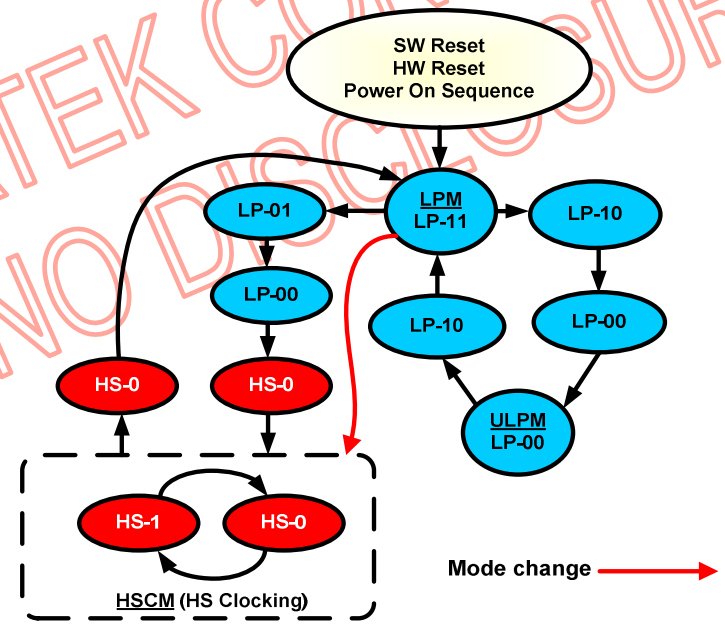
5.4.2.2.2.3 High Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



From LPM to HSCM

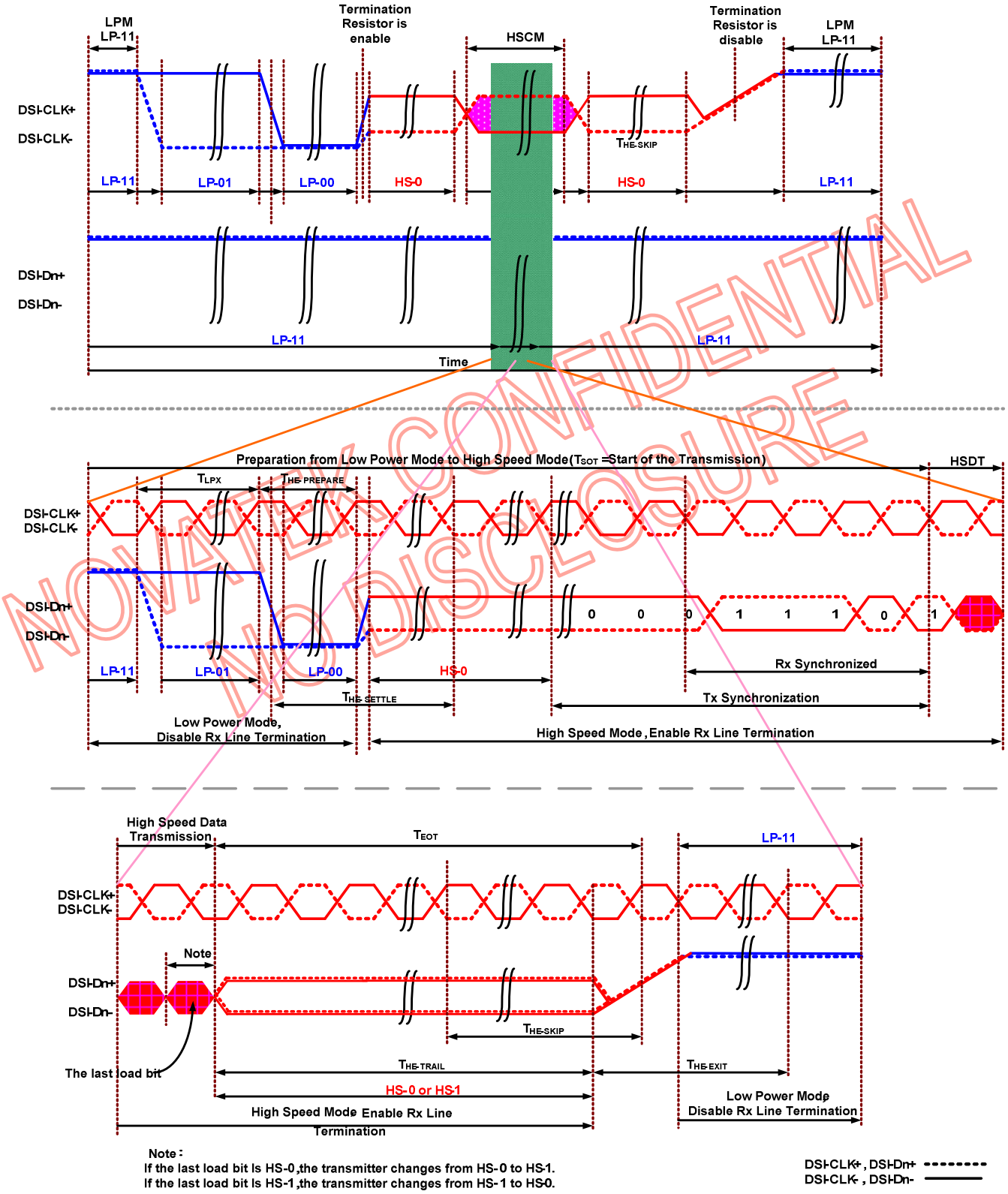
The mode change is also illustrated below.



Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:
- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note:
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-Dn+
DSI-CLK-, DSI-Dn-

High Speed Clock Burst

5.4.2.2.3 DSI-DATA Lanes

5.4.2.2.3.1 General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

• Escape Mode (Only DSI_D0+/- data lanes is used)

• High-Speed Data Transmission (all data lanes are used)

• Bus Turnaround Request (Only DSI_D0+/- data lanes is used)

These modes and their entering codes are defined on the following table.

Entering and Leaving Sequences:

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

5.4.2.2.3.2 Escape Mode

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

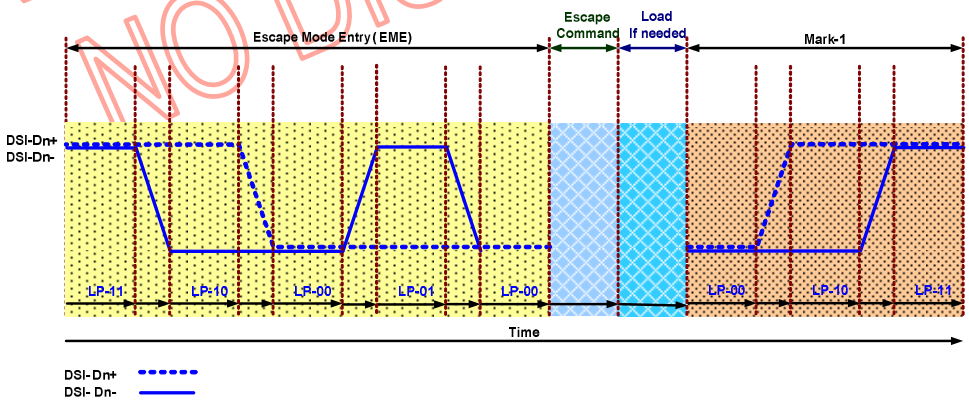
• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape Commands

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	★
Ultra-Low Power Mode	Mode	0001 1110 bin	★	★
Underfined-1, Note	Mode	1001 1111 bin	-	-
Underfined-2, Note	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	★
Tearing Effect	Trigger	0101 1101 bin	-	★
Acknowledge	Trigger	0010 0001 bin	-	★
Unknow-5, Note	Trigger	1010 0000 bin	-	-

Escape commands are defined

Notes: This Escape command support has not been implemented on the display module.

n=1: "★"= Supported; "-" = Not Supported

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Load (Data):

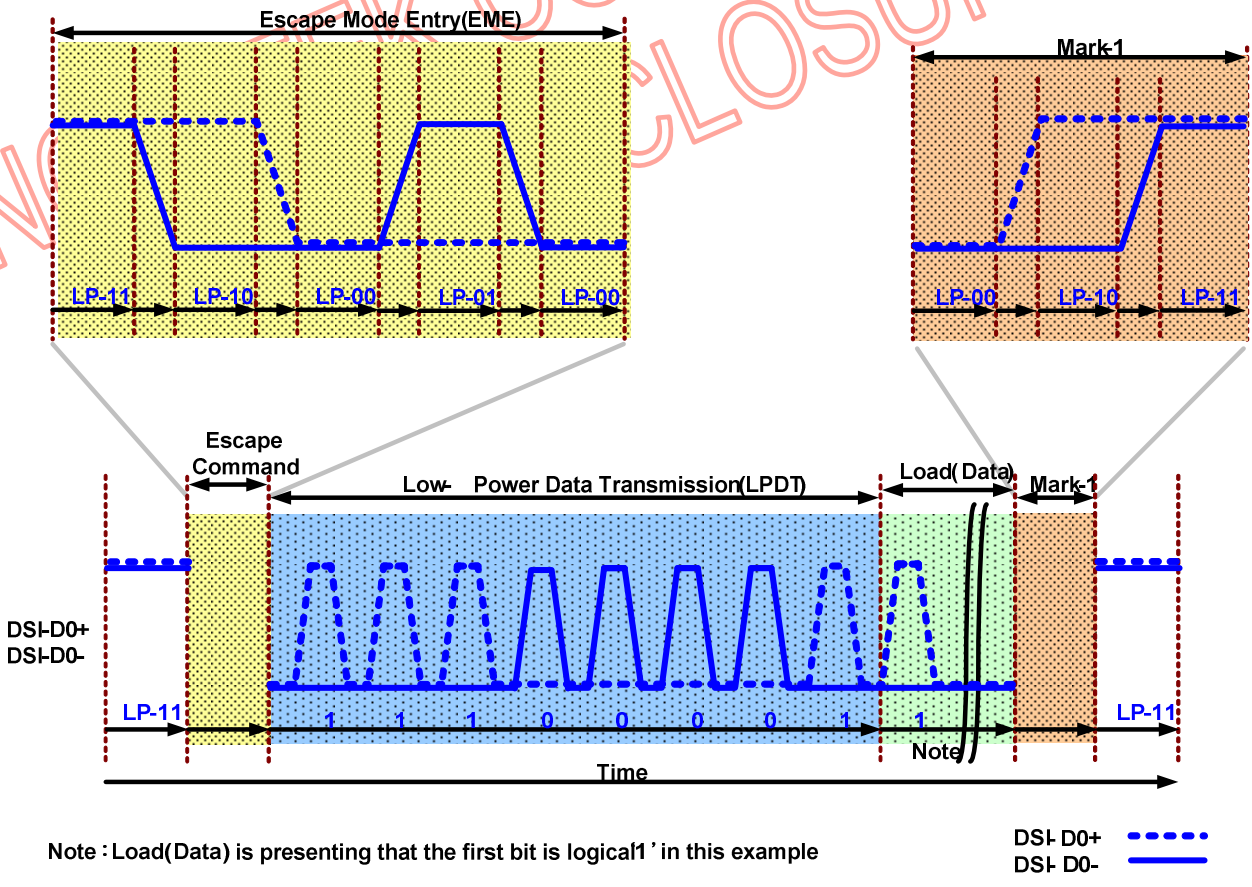
One or more bytes (8 bit)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

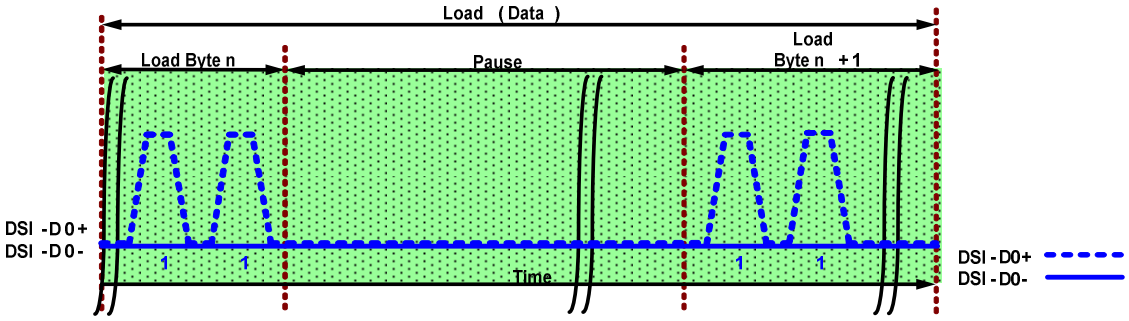
• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Low-Power Data Transmission (LPDT)



Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

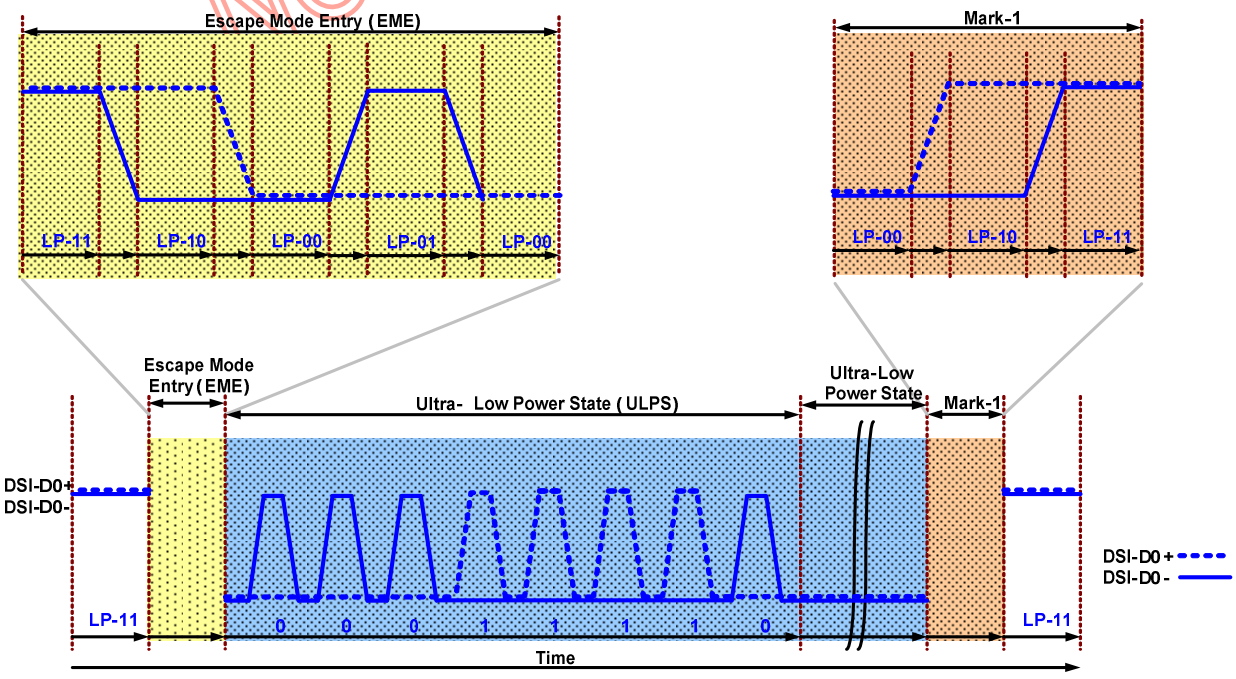
• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

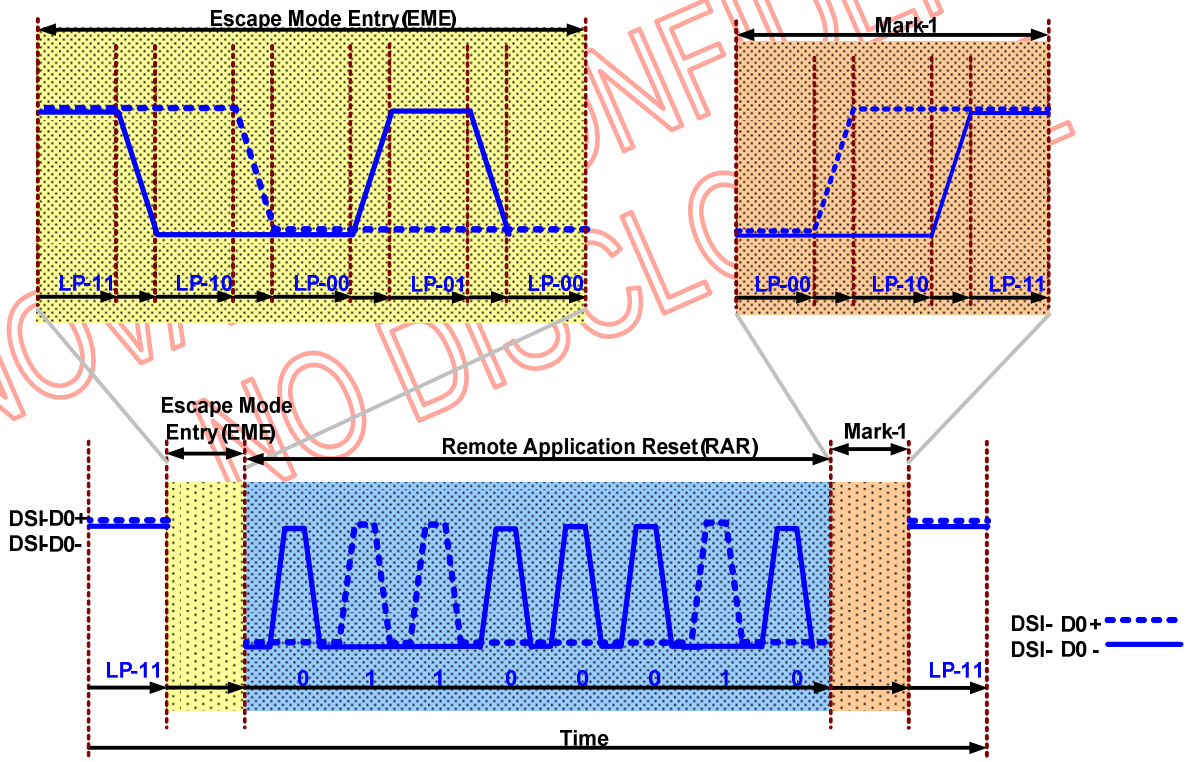
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

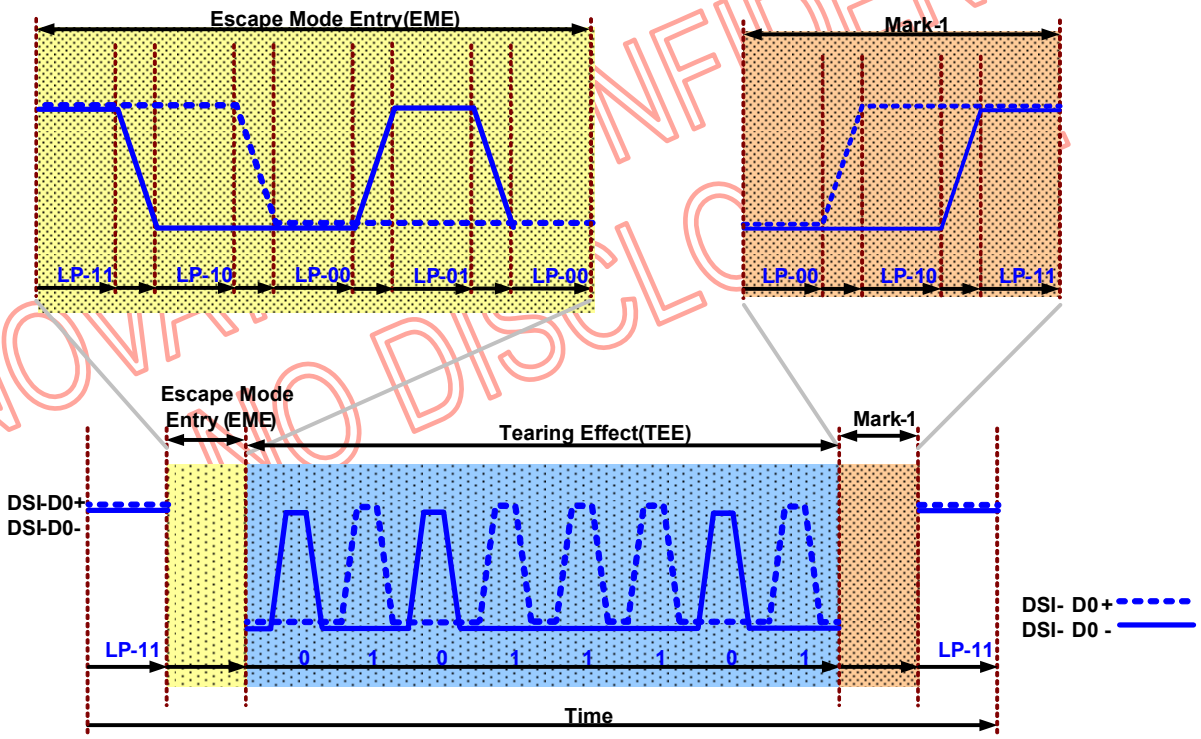
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

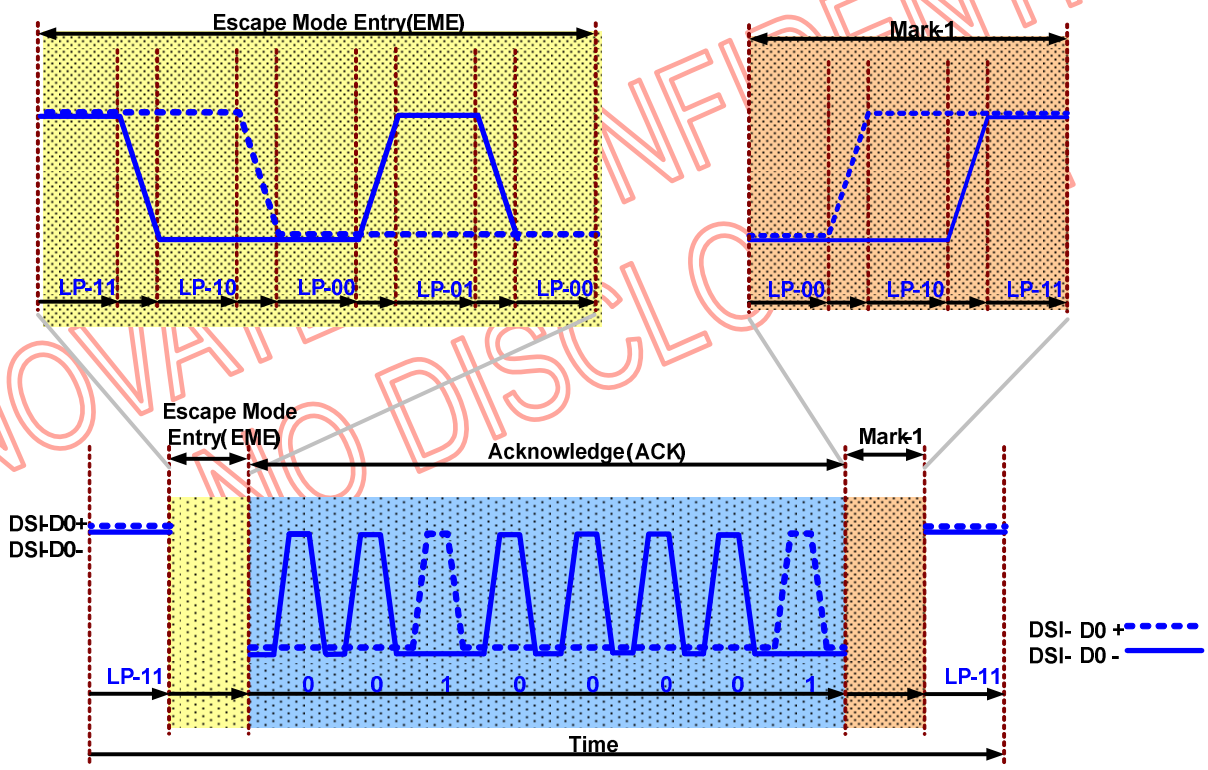
• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

5.4.2.2.3.3 High Speed Data Transmission

Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

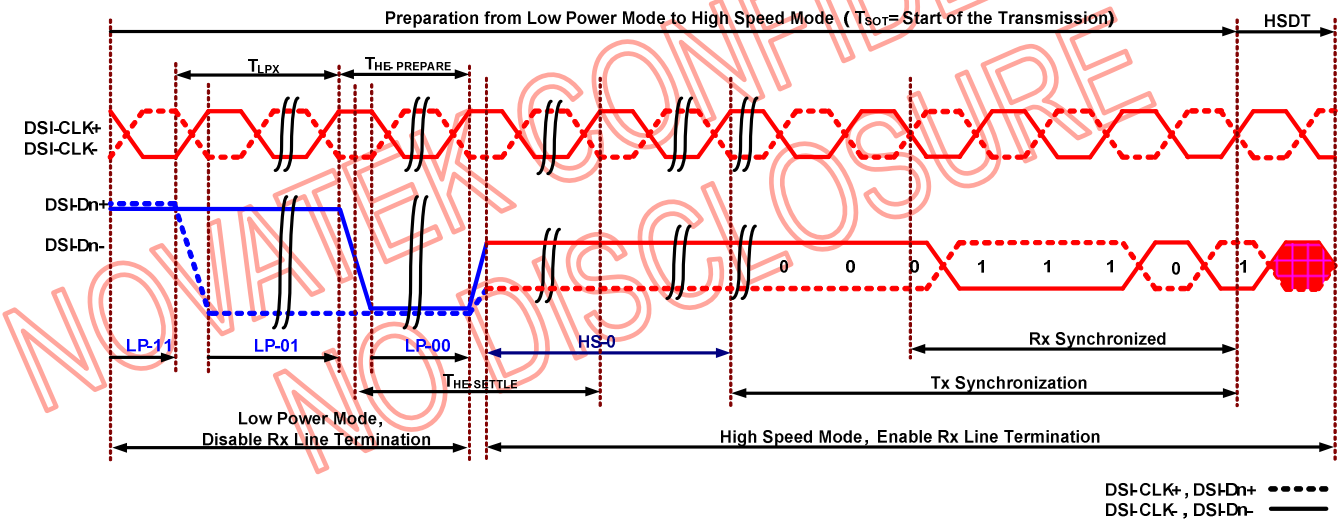
• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.



Entering High-Speed Data Transmission (TSOT of HSDT)

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

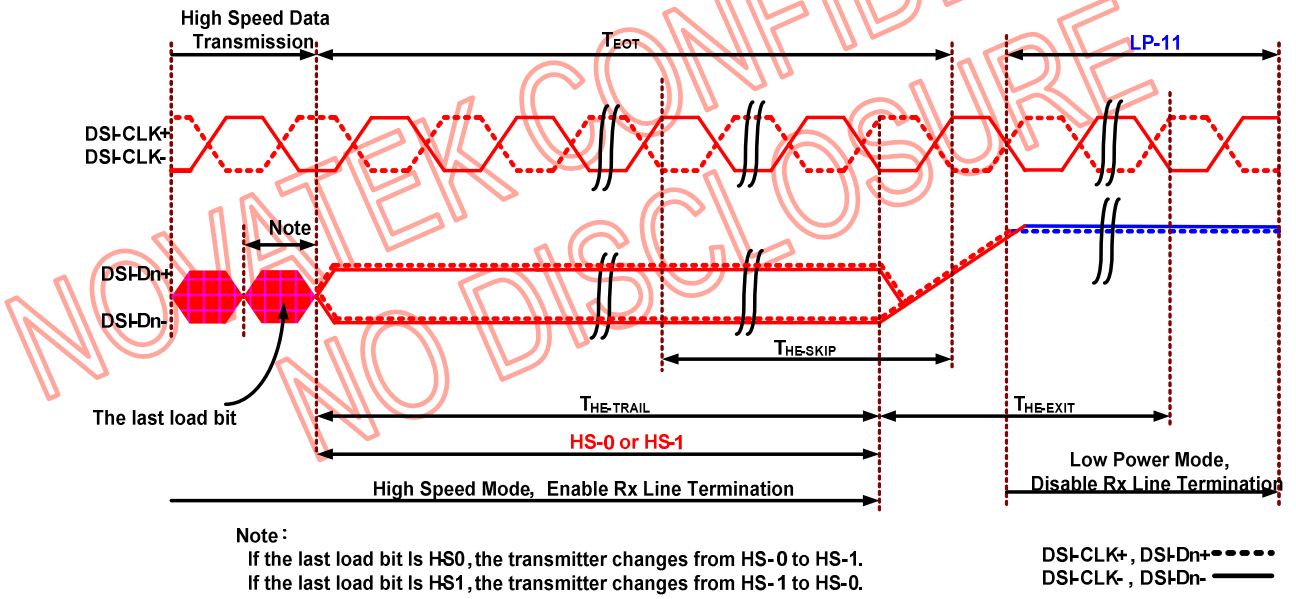
• Stops High-Speed Data Transmission

MCU changes to HS-1, if the last load bit is HS-0

MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below.

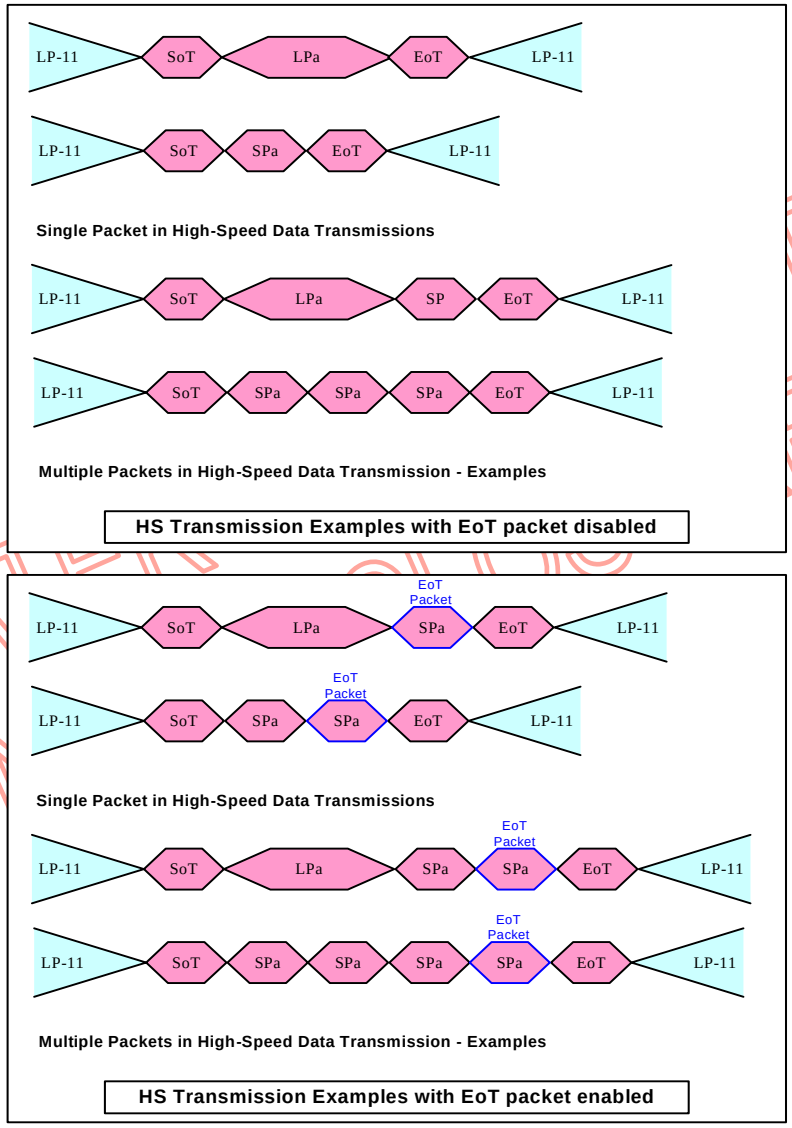


Leaving High-Speed Data Transmission (TEOT of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Abbreviations:

Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are’1’s (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

5.4.2.3 Packet Level Communication

5.4.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

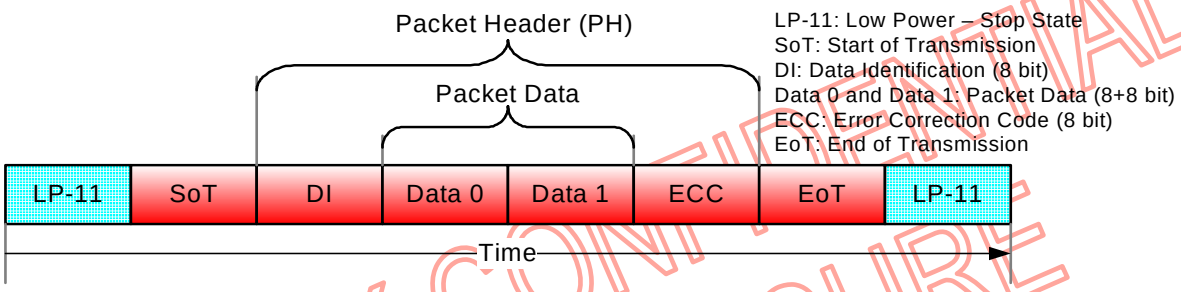
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

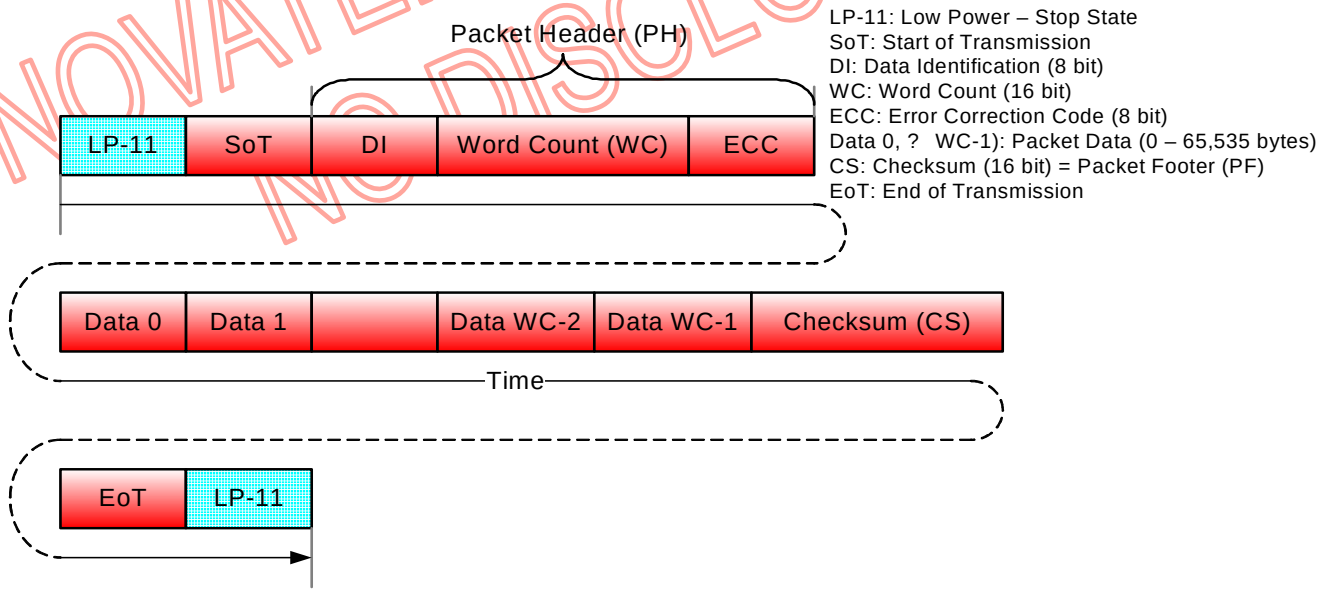
• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Short Packet (Spa) Structure

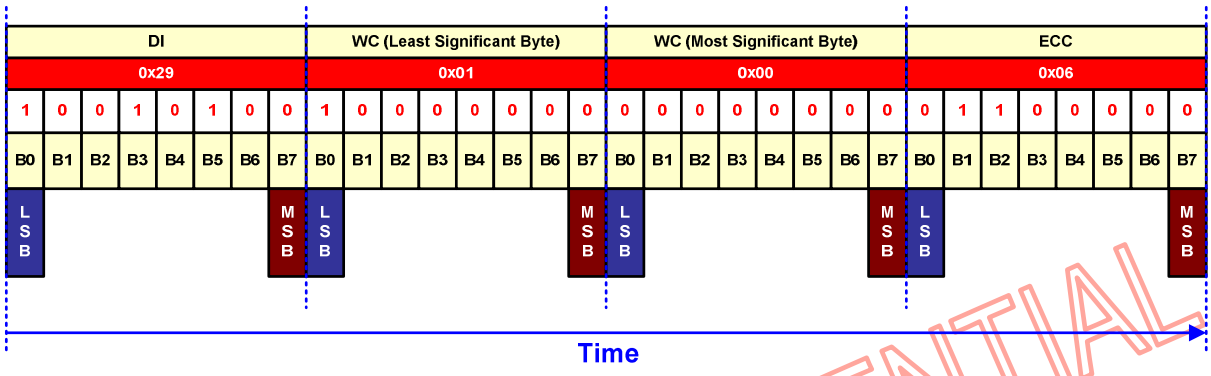


Long Packet (Lpa) Structure

Note:
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.
* LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
* LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
* LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.4.2.3.1.1 Bit Order of Byte on Packets

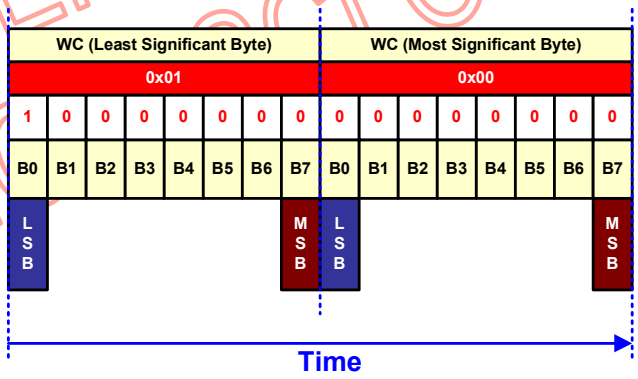
The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last. This same order is illustrated for reference purposes below.



Bit Order of the Byte on Packet

5.4.2.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last. This same order is illustrated for reference purposes below.



Byte Order of the Multiple Byte on Packet

5.4.2.3.1.3 Packet Header (PH)

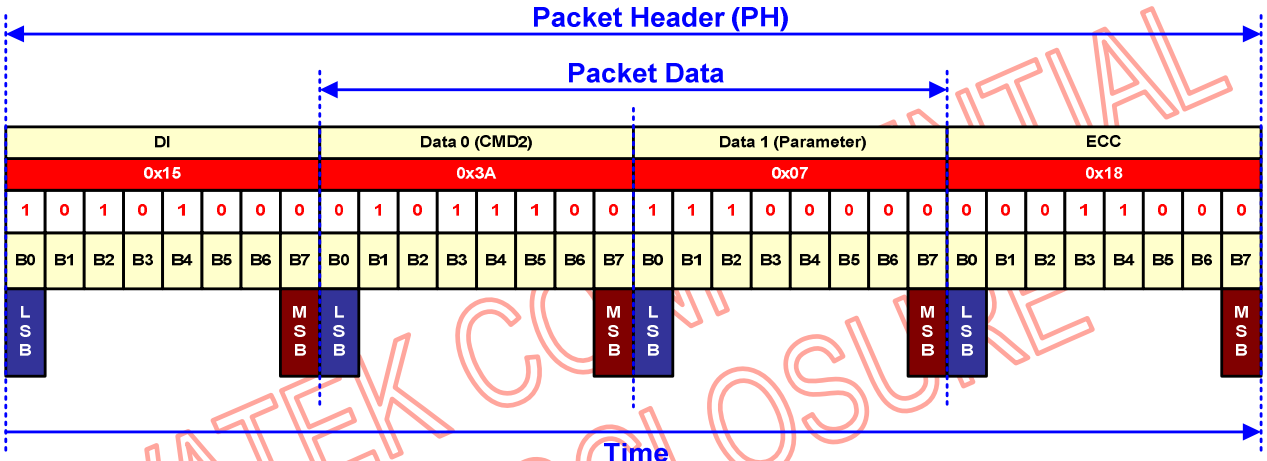
The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)



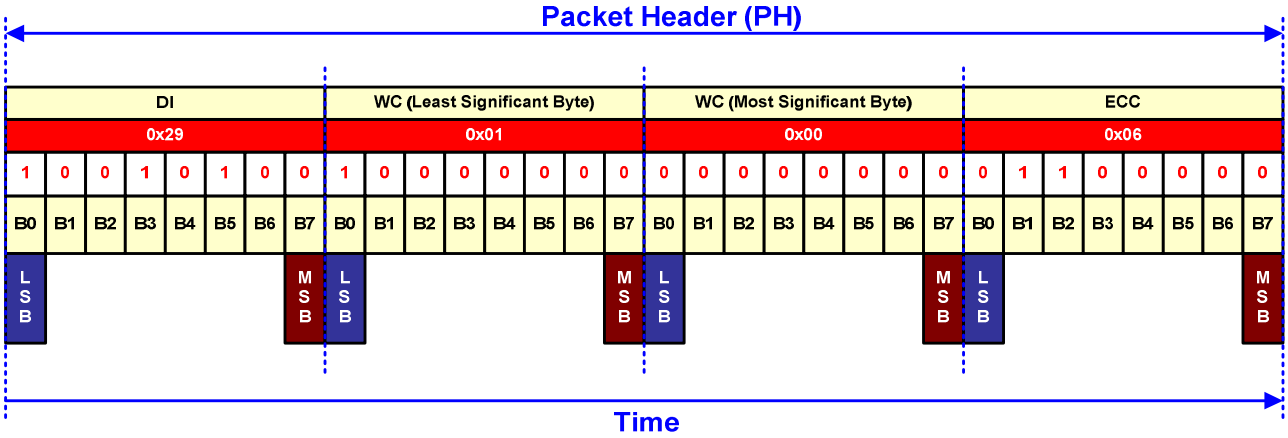
Packet Header (PH) on Short Packet (Spa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (Lpa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

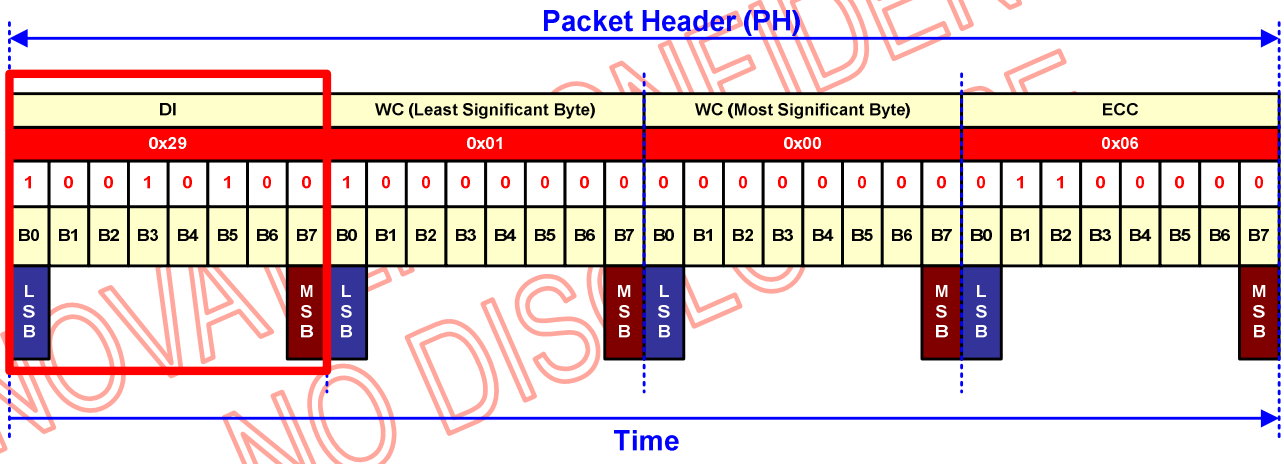
• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

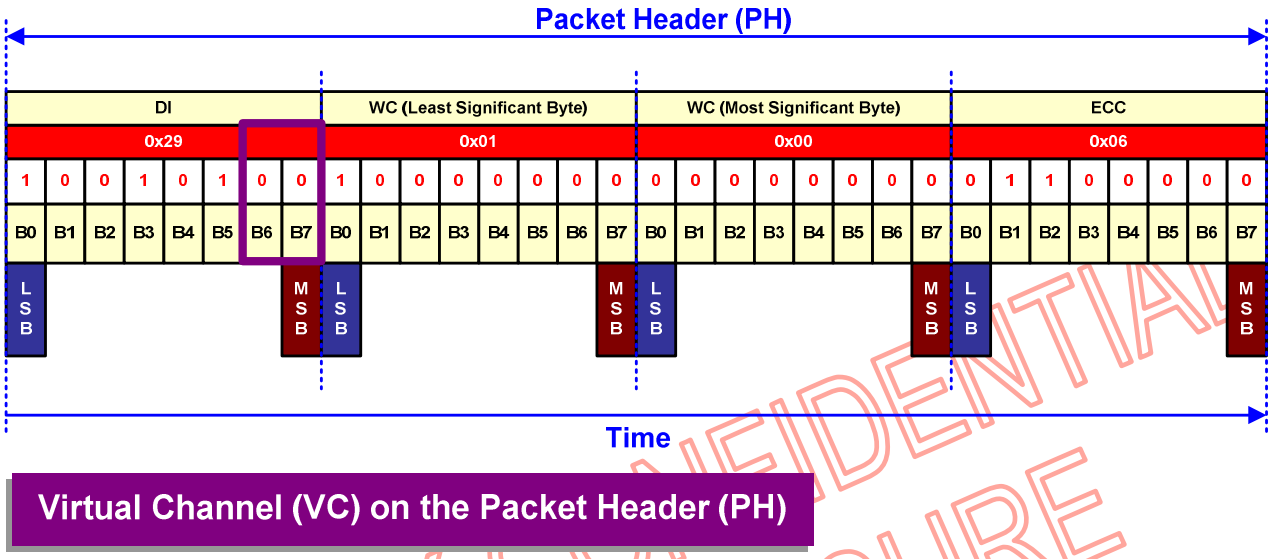


Data Identification (DI) on the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

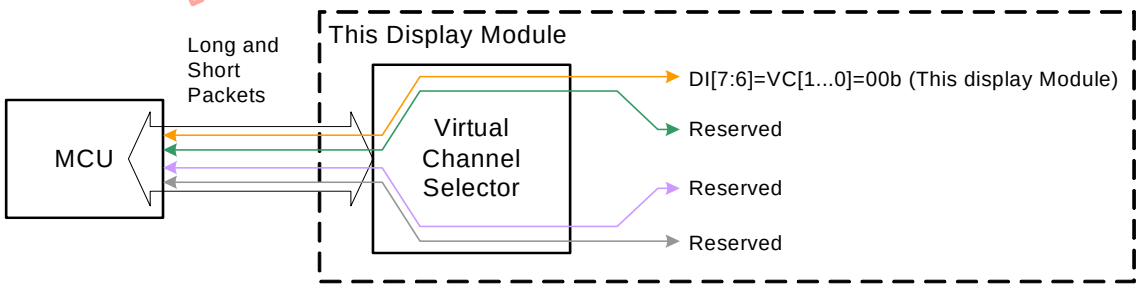


Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

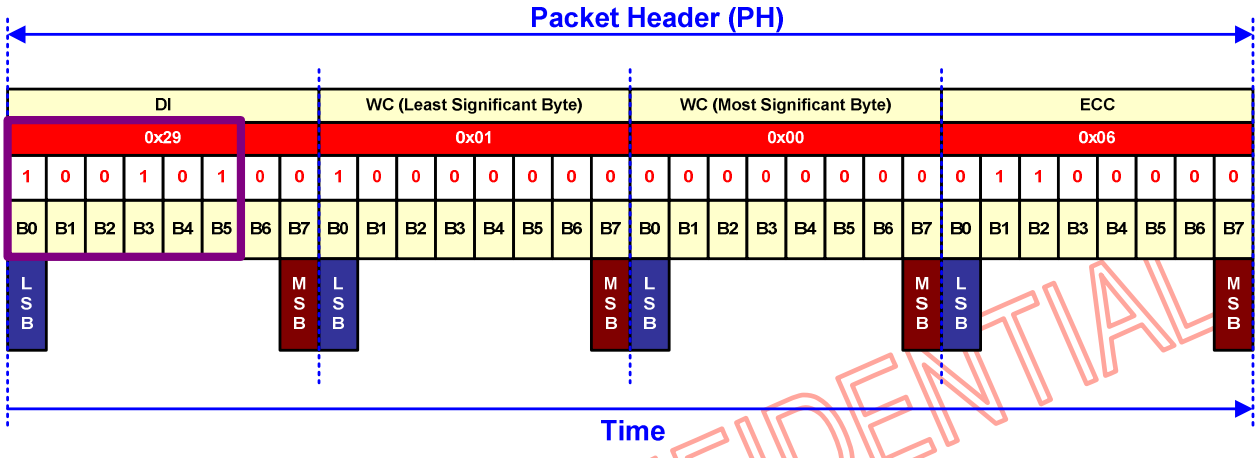


Virtual Channel (VC) Configuration

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. This Data Type (DT) are defined on tables below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type, hex	Data Type, binary	Description	Packet Size	Note
01h	00 0001	Sync Event, V Sync Start	Short	
11h	01 0001	Sync Event, V Sync End	Short	
21h	10 0001	Sync Event, H Sync Start	Short	
31h	11 0001	Sync Event, H Sync End	Short	
08h	00 1000	End of Transmission (EoT) packet	Short	
02h	00 0010	Color mode (CM) Off Command	Short	
12h	01 0010	Color mode (CM) On Command	Short	
03h	00 0011	Generic Short Write, no parameter	Short	
13h	01 0011	Generic Short Write, 1 parameter	Short	1,2
23h	10 0011	Generic Short Write, 2 parameter	Short	1,3
29h	10 1001	Generic Long Write	Long	1
04h	00 0100	Generic Read, no parameter	Short	
14h	01 0100	Generic Read, 1 parameter	Short	1,2
24h	10 0100	Generic Read, 2 parameter	Short	1,3
05h	00 0101	DCS WRITE, no parameters	Short	
15h	01 0101	DCS WRITE, 1 parameter	Short	
06h	00 0110	DCS READ, no parameters	Short	
37h	11 0111	Set Maximum Return Packet Size	Short	
09h	00 1001	Null Packet, no data	Long	
19h	01 1001	Blanking Packet, no data	Long	
39h	11 1001	DCS Long Write/Write LUT Command Packet	Long	
0Eh	00 1110	Packed Pixel Stream,16-bits RGB, 5-6-5 Format	Long	
1Eh	01 1110	Packed Pixel Stream,18-bits RGB, 6-6-6 Format	Long	
2Eh	10 1110	Loosely Packed Pixel Stream,18-bits RGB, 6-6-6 Format	Long	
3Eh	11 1110	Packed Pixel Stream,24-bits RGB, 8-8-8 Format	Long	
x0h and xFh unspecified	xx 0000 xx 1111	DON'T USE (All unspecified codes are reserved)		

Note: 1. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).

2. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.

3. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.

4. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU									
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Short / Long Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
08h	0	0	1	0	0	0	End of Transmission (EoT) packet	Short	EoT
1Ch	0	1	1	1	0	0	DCS Read Long Response	Long	DCSRR-L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1-S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2-S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response, 1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response, 2 byte returned	Short	GENRR2-S

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or " Data Type (DT) from the Display Module (or Other Devices) to the MCU".

Availability of MIPI Data Type for Instruction Code (User Command Set)

MIPI Data Type	03h (GENWN-S)	13h (GENW1-S)	23h (GENW2-S)	29h (GENW-L)	04h (GENRN-S)	14h (GENR1-S)	24h (GENR2-S)	05h (DCSWN-S)	15h (DCSW1-S)	39h (DCSW-L)	06h (DCSRN-S)
Instruction Code	Availability of MIPI Data Type										
00h (NOP)								Yes	Yes	Yes	
01h (SOFT_RESET)								Yes	Yes	Yes	
05h (RDNUMED)											Yes
0Ah (GET_POWER_MODE)											Yes
0Bh (GET_ADDRESS_MODE)											Yes
0Dh (GET_DISPLAY_MODE)											Yes
0Eh (GET_SIGNAL_MODE)											Yes
0Fh (RDDSDR)											Yes
10h (ENTER_SLEEP_MODE)								Yes	Yes	Yes	
11h (EXIT_SLEEP_MODE)								Yes	Yes	Yes	
20h (EXIT_INVERT_MODE)								Yes	Yes	Yes	
21h (ENTER_INVERT_MODE)								Yes	Yes	Yes	
26h (GMASET)									Yes	Yes	
28h (SET_DISPLAY_OFF)								Yes	Yes	Yes	
29h (SET_DISPLAY_ON)								Yes	Yes	Yes	
34h (SET_TEAR_OFF)								Yes	Yes	Yes	
35h (SET_TEAR_ON)									Yes	Yes	Yes
36h (SET_ADDRESS_MODE)									Yes	Yes	Yes
3Bh (MIPICTRL)										Yes	Yes
44h/45h (SET_TEAR_SCANLINE)										Yes	Yes
46h (RDSCL)											Yes
4Fh (ENTER_DSTB_MODE)									Yes	Yes	

MIPI Data Type	03h (GENWN-S)	13h (GENW1-S)	23h (GENW2-S)	29h (GENW-L)	04h (GENRN-S)	14h (GENR1-S)	24h (GENR2-S)	05h (DCSWN-S)	15h (DCSW1-S)	39h (DCSW-L)	06h (DCSRN-S)
Instruction Code	Availability of MIPI Data Type										
51h (WRIDSBV)									Yes	Yes	Yes
52h (RDDISBV)											Yes
53h (WRCTRLD)									Yes	Yes	
54h (RDCTRLD)											Yes
55h (WRCABC)									Yes	Yes	
56h (RDCABC)											Yes
5Eh (WRCABCMB)									Yes	Yes	
5Fh (RDCABCMB)											Yes
A1h (RDDDBS)											Yes
A8h (RDDDBC)											Yes
AAh (RDFCS)											Yes
AFh (RDCCS)											Yes
BAh(SET_MIPI_LANE)									Yes	Yes	Yes
D2h~D6h (RGB/MIPI Ctrl)									Yes	Yes	Yes
DAh (RDID1)											Yes
DBh (RDID2)											Yes
DCh (RDID3)											Yes
F3h(Multi-IF Function)									Yes	Yes	Yes
F4h (NOVATEK ID)											Yes
F5h (IF-TEST)									Yes	Yes	Yes
F6h~F7h (EXT CLK)									Yes	Yes	Yes
F8h (I2C SLAVE ADDR.)									Yes	Yes	Yes
F9h (PIXEL EXTEN.)									Yes	Yes	Yes
FEh (RDCMDSTATUS)											Yes

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

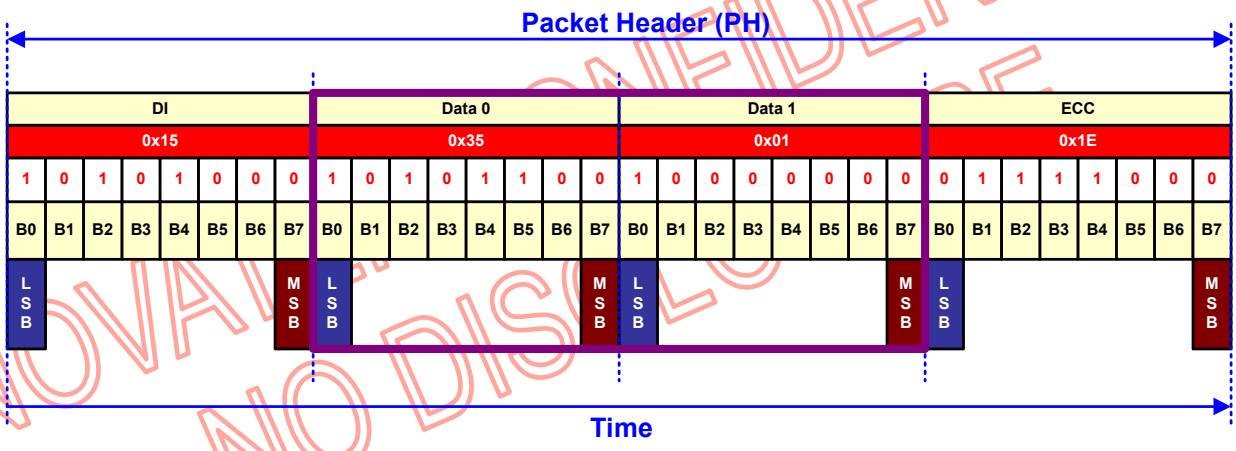
Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

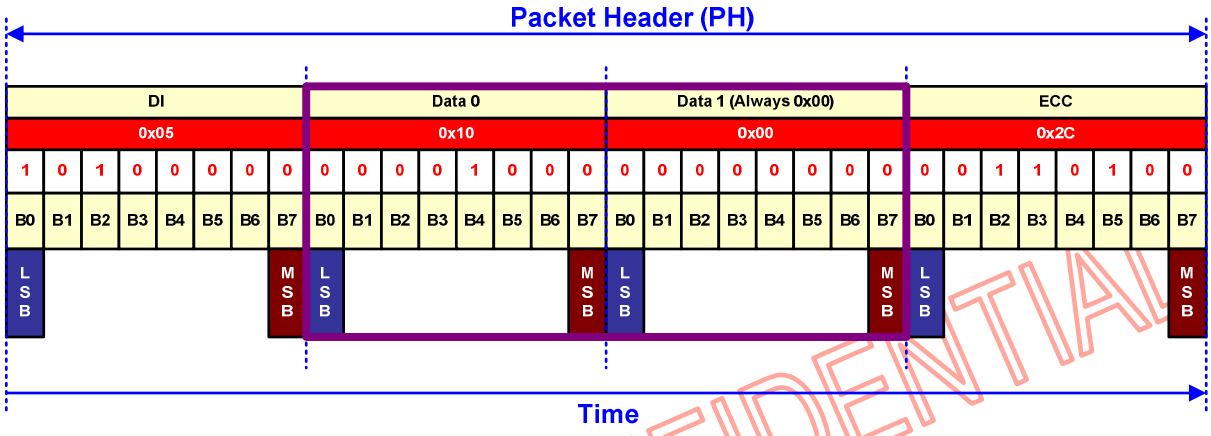


Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) Information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Byte Information

Word Count (WC) on the Long Packet (LPa)

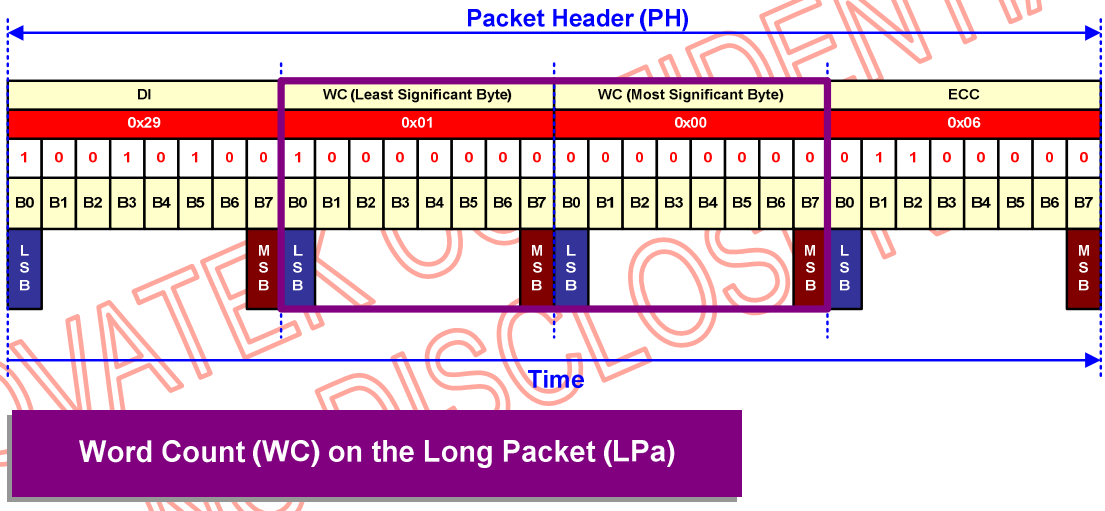
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

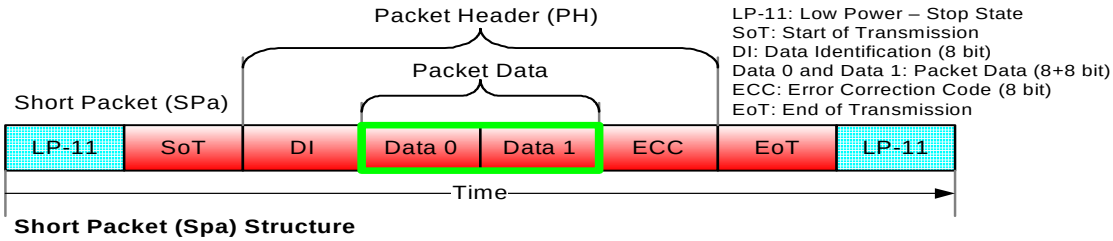
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

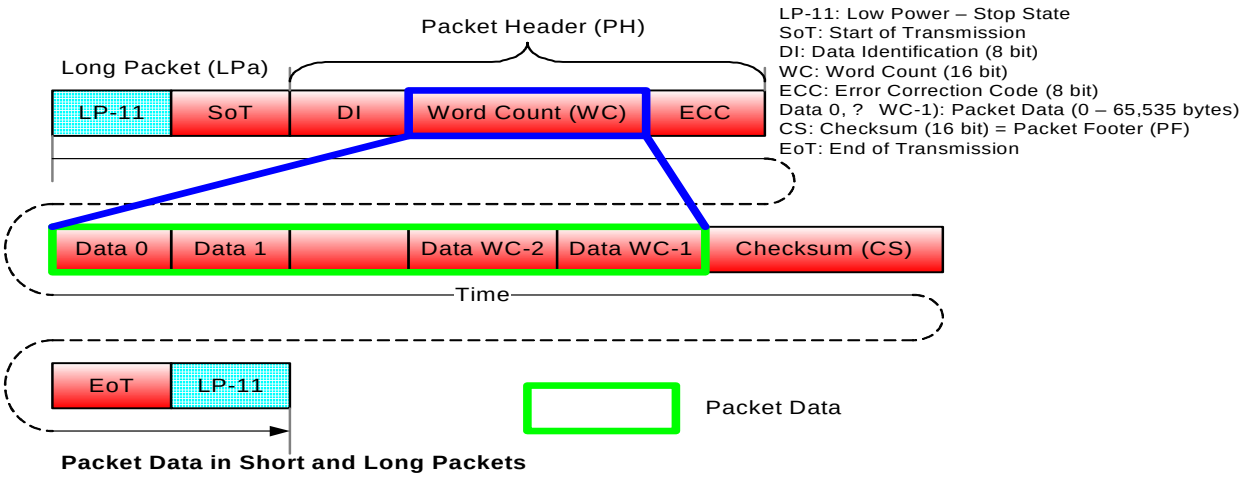
Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



Word Count (WC) on the Long Packet (LPa)



Short Packet (Spa) Structure



Packet Data in Short and Long Packets

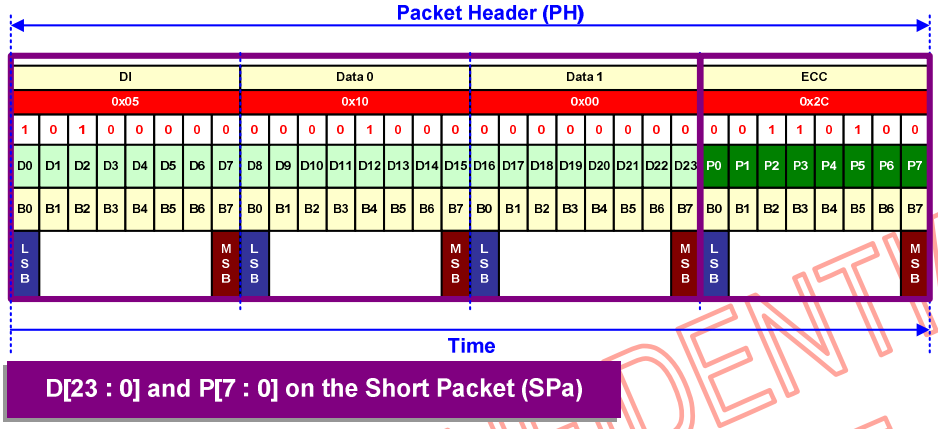
Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

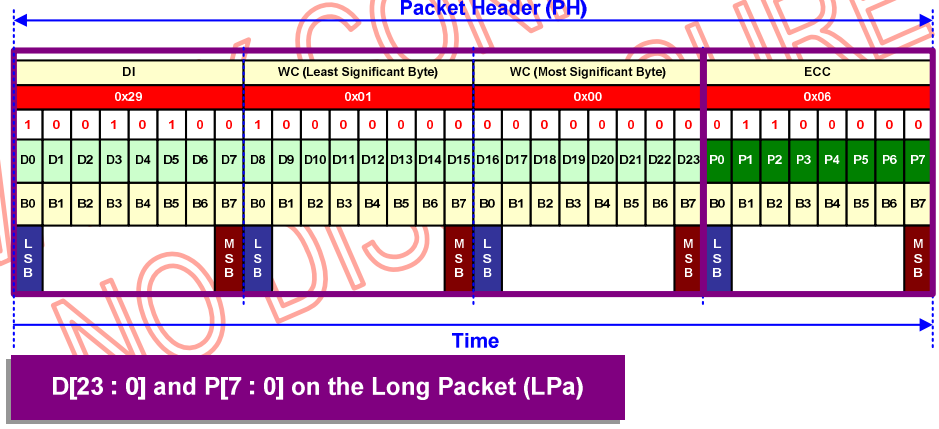
• Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])

• Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.



D[23 : 0] and P[7 : 0] on the Short Packet (SPa)



D[23 : 0] and P[7 : 0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

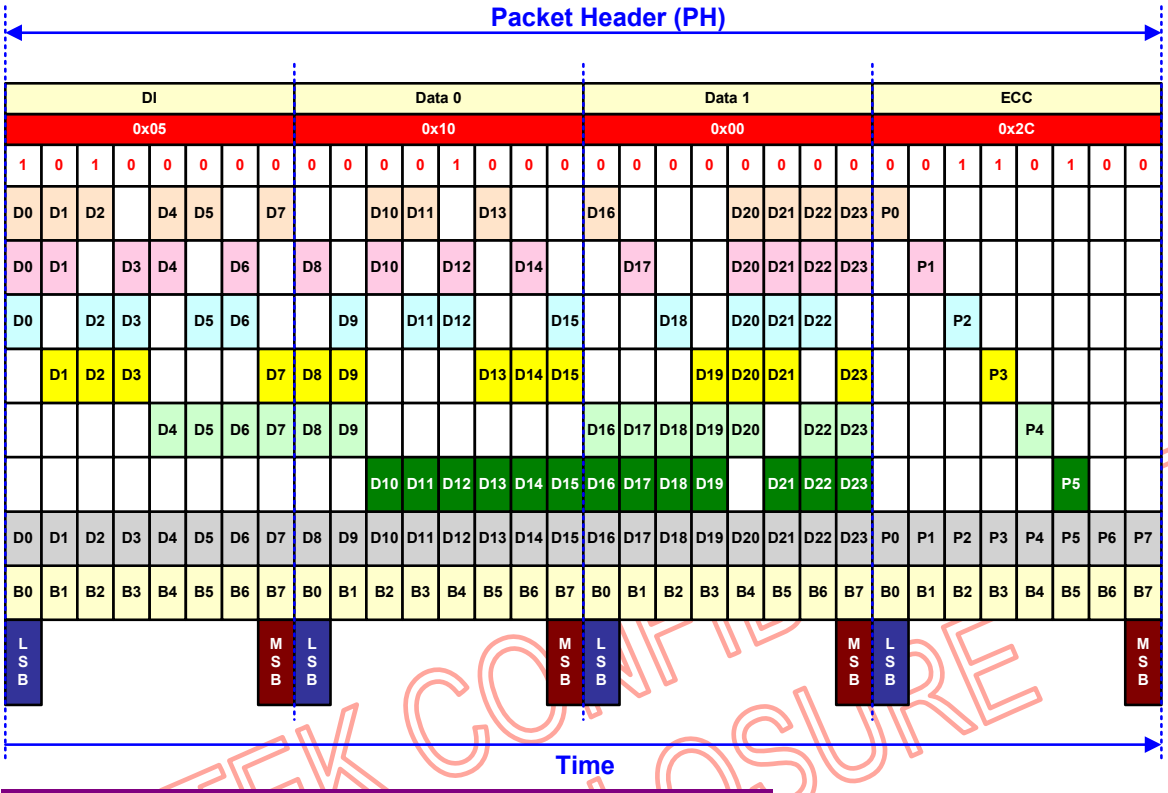
• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

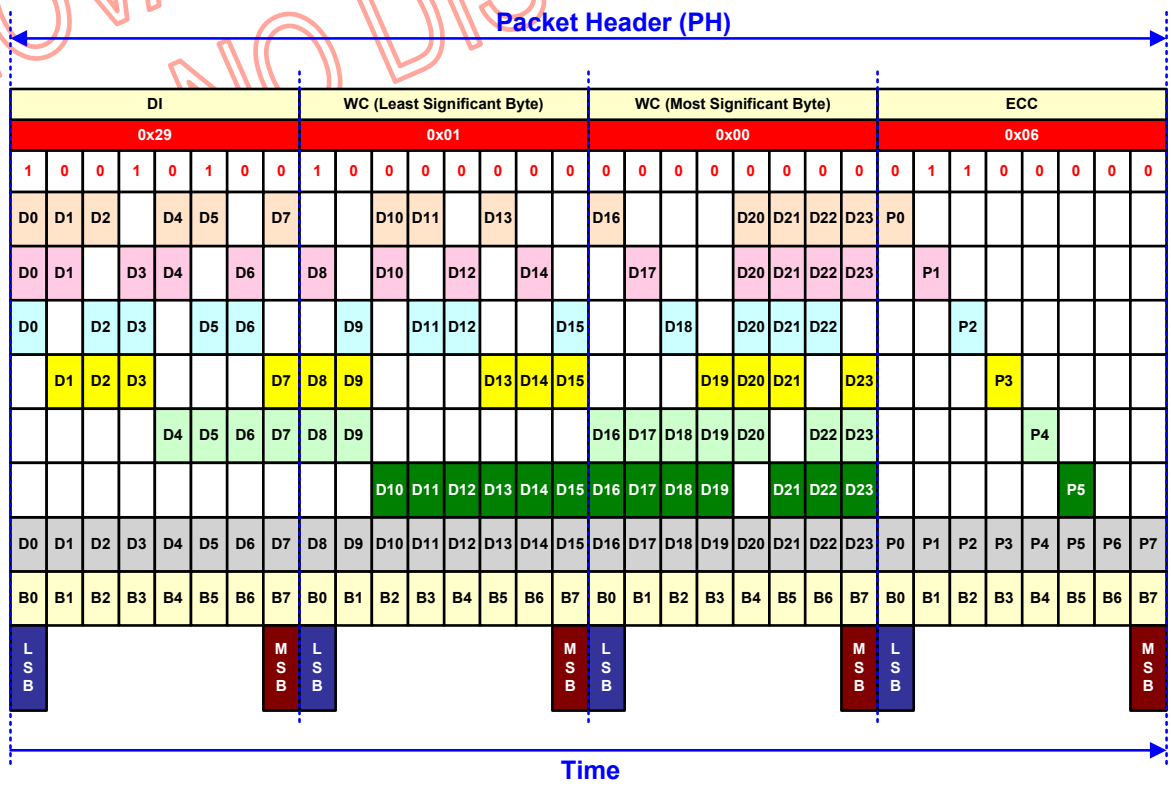
• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bits value ([D63…0]), but this implementation is based on 24 bits value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



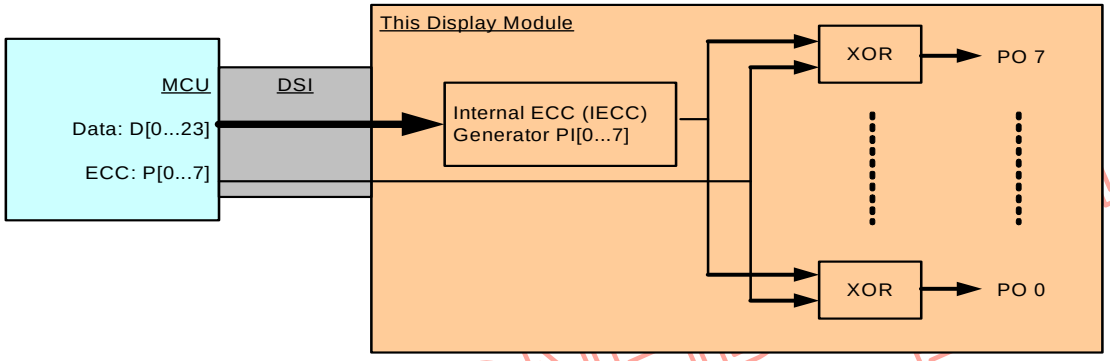
XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h => No Error
	LSB							MSB	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch => Error
	LSB							MSB	

Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

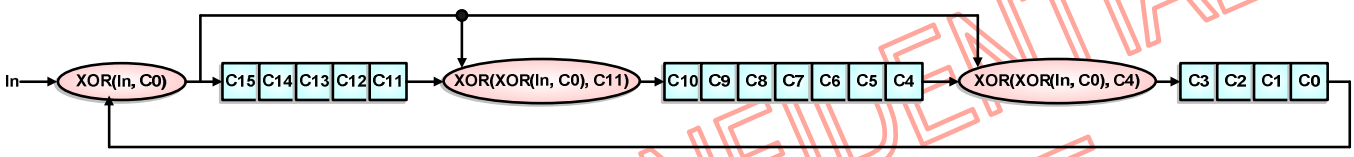
5.4.2.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.4.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

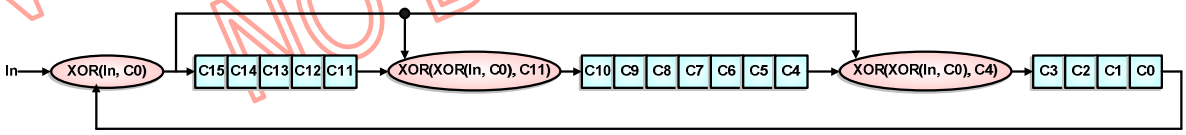
The checksum is using a 16-bits Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.



16-bits Cyclic Redundancy Check (CRC) Calculation

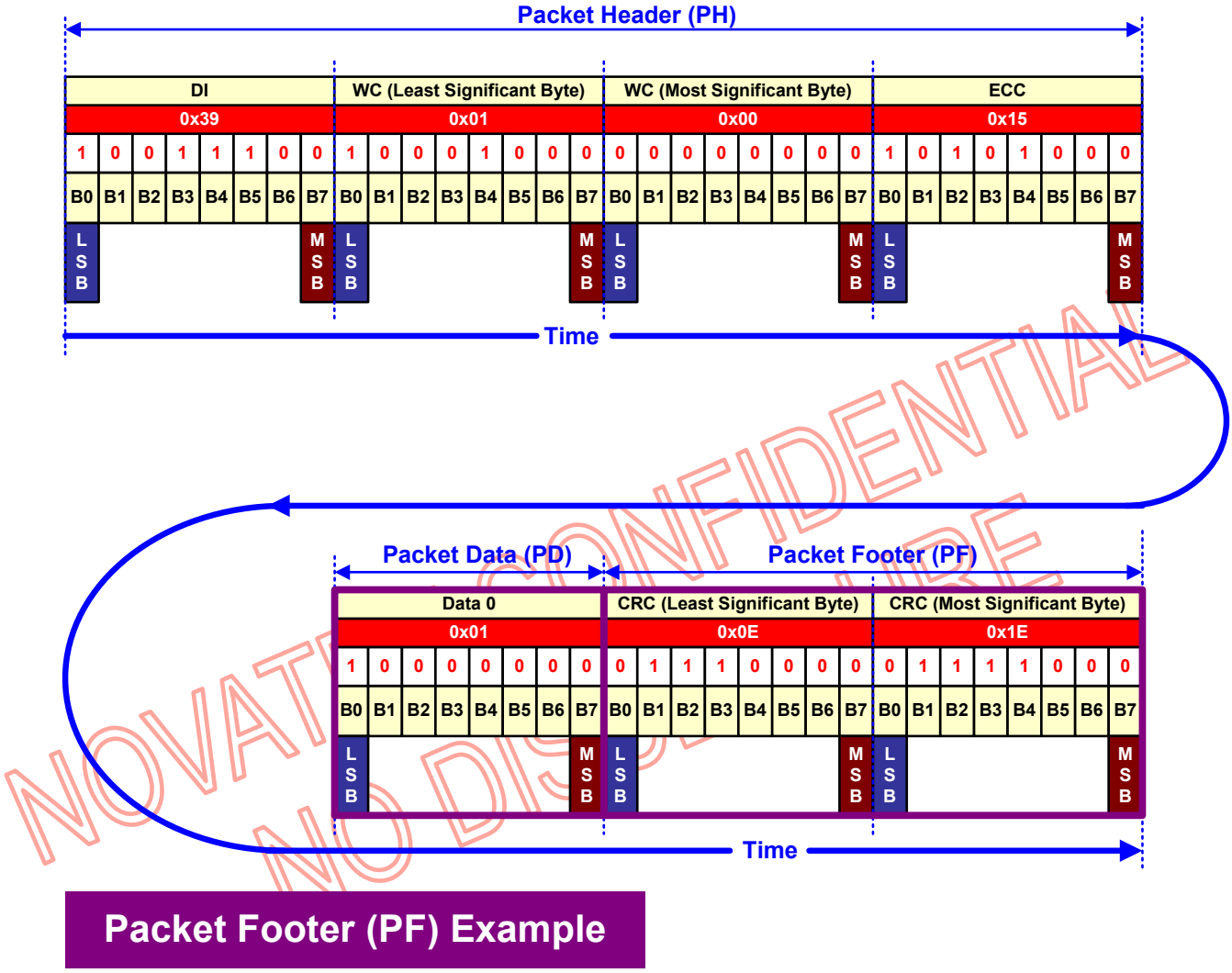
The 16-bits Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bits Cyclic Redundancy Check (CRC).

An example of the 16-bits Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In, C0)	C15	C14	C13	C12	C11	XOR(XOR(In, C0), C11(Step – 1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In, C0), C4(Step – 1))	C3	C2	C1	C0	C0
0	x	x	1	1	1	1	1	x	1	1	1	1	1	1	1	x	1	1	1	1	x
1	1 (LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0 (MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

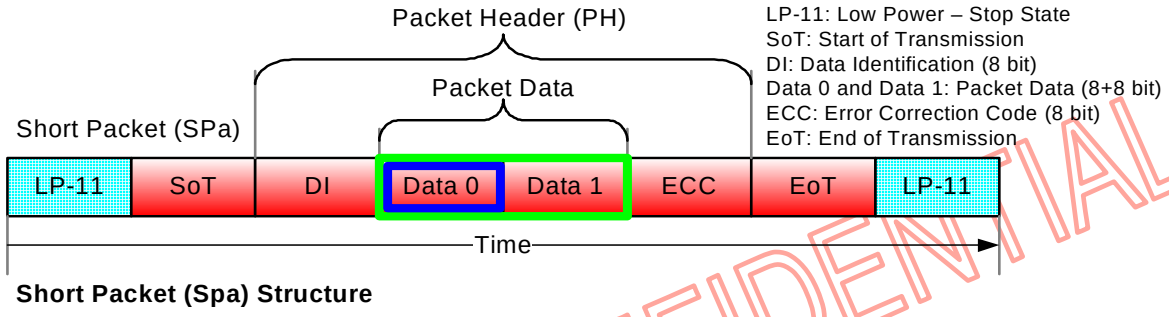
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.4.2.3.2 Packet Transmission

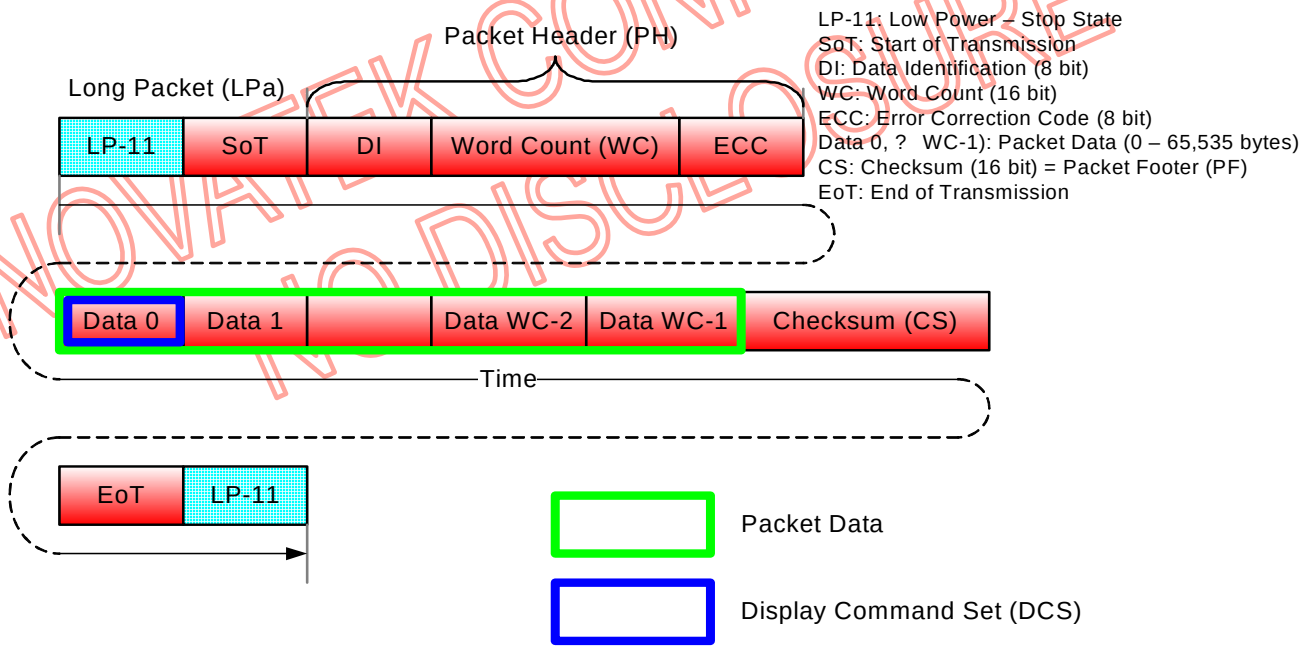
5.4.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



Short Packet (Spa) Structure



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, no Parameter (GENW0-S), Data Type = 00 0011 (03h)

This data type is useless in normal application.

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h. "Generic Write, 1 Parameter" (GENW1-S) is used for Manufacture Command Set (CMD2, means panel function registers) writing only. Since all CMD2 registers are 1 "address" byte with 1 "parameter" byte. Therefore, this data type is useless in normal application.

Short Packet (SPa) is defined e.g.

- **Data Identification (DI)**

  Virtual Channel (VC, DI[7…6]): 00b

  Data Type (DT, DI[5…0]): 01 0011b

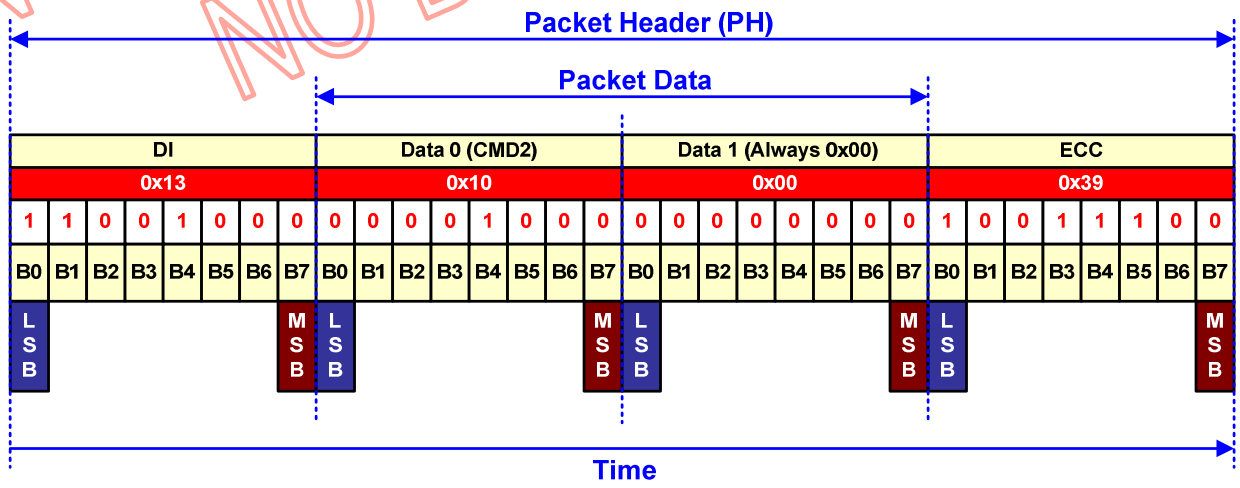
- **Packet Data (PD)**

  Data 0: "POWER_CTRL15 (10h)", the Power Control 15 in the page 0 of CMD2"

  Data 1: Always 00hex

- **Error Correction Code (ECC)**

This is defined on the Short Packet (SPa) as follows.



Generic Write, 1 Parameter (GENW1-S) - Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes are "command" and "parameter". "Generic Write, 2 Parameter" (GENW2-S) is used for Manufacture Command Set (CMD2, means panel function registers) writing only.

Notes: One Sub pixel has been written.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 10 0011b

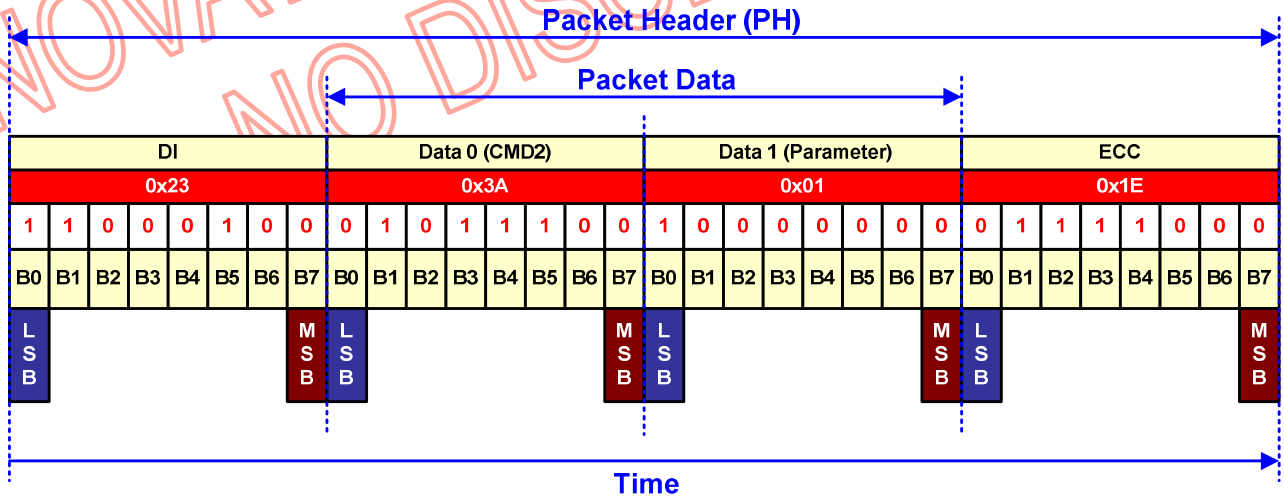
• Packet Data (PD)

Data 0: "3-GAMMA-R CTRL15 (3Ah)", the Red Gamma Control in page 0 of CMD2

Data 1: 01hex, the parameter of the CMD2

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) - Example

Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. The content of payload bytes are "command" with multiple "parameter". "Generic Write Long" (GENW-L) is used for Manufacture Command Set (CMD2, means panel function registers) writing only.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- **Data Identification (DI)**

  Virtual Channel (VC, DI[7…6]): 00b

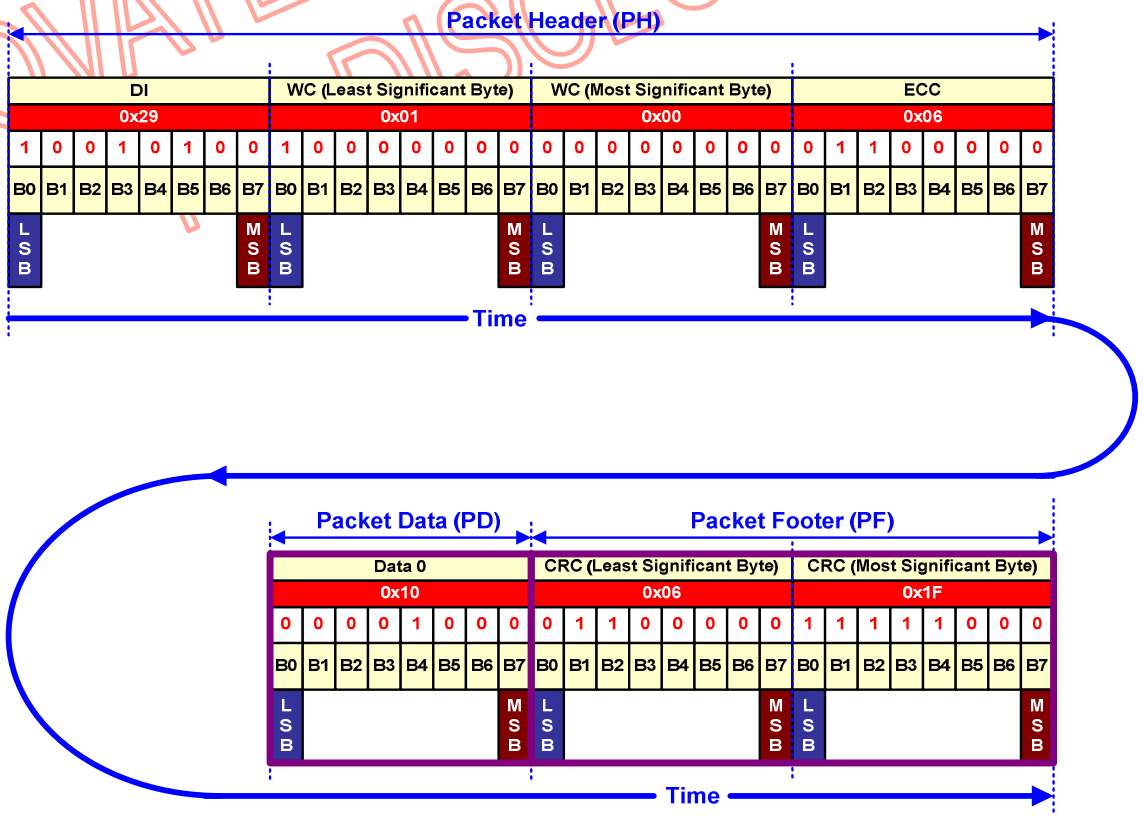
  Data Type (DT, DI[5…0]): 10 1001b

- **Word Count (WC)**

  Word Count (WC): 0001h

- **Error Correction Code (ECC)**
- **Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)**
- **Packet Footer (PF)**

This is defined on the Long Packet (LPa) as follows.



Generic Write Long (GENW-L) with CMD2 Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

Word Count (WC): 0002h

• Error Correction Code (ECC)

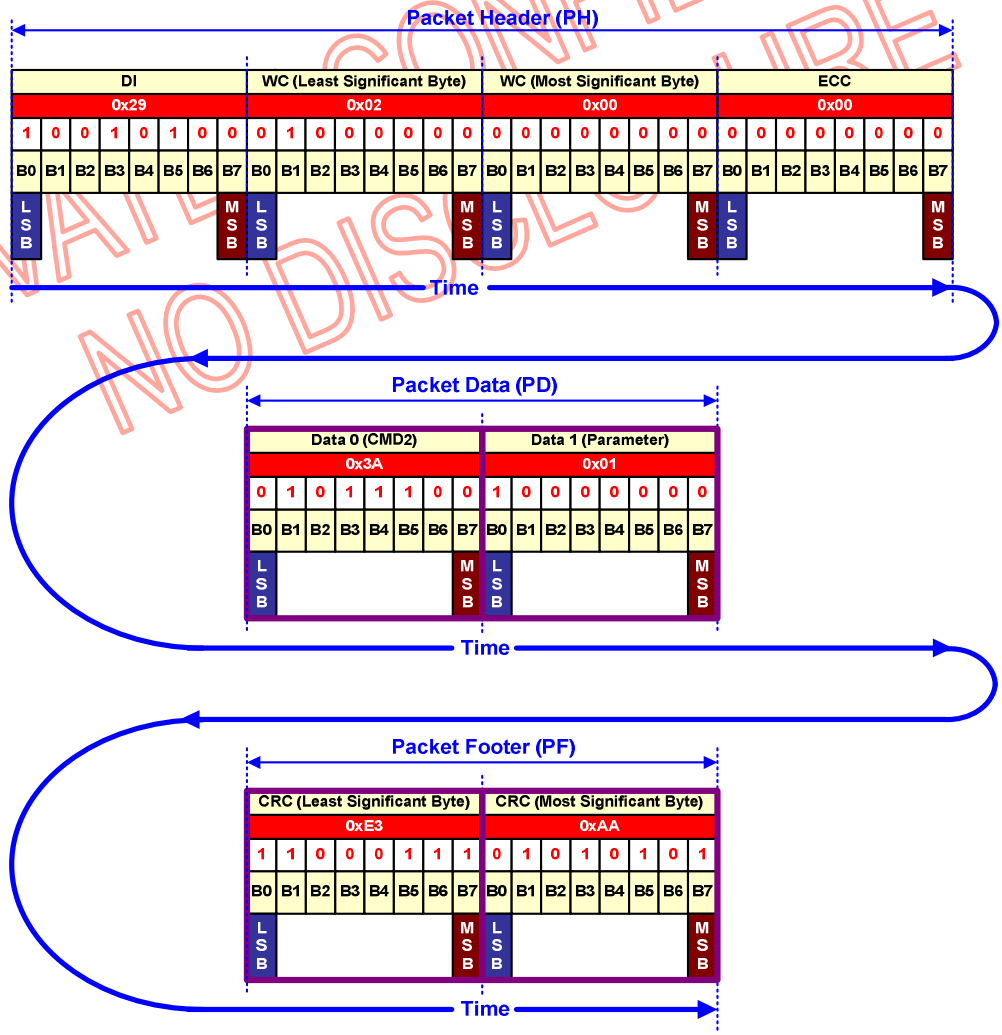
• Packet Data (PD):

Data 0: “3-GAMMA-R CTRL15 (3Ah)”, the Red Gamma Control in page 0 of CMD2

Data 1: 01hex, Parameter of the CMD2

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Generic Write Long with CMD2 and 1 Parameter - Example

Generic Read, No Parameter (GENR0-S) , Data Type = 00 0100 (04h);

This data type is useless in normal application.

Generic Read, 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h); Generic Read, 2 Parameter (GENR2-S) , Data Type = 10 0100 (24h)

"Generic Read, 1 Parameter / Generic Read, 2 Parameter" (GENR1-S / GENR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0100b) and Data Type (DT, 10 0100b), from the MCU to the display module. Generic read data type is used for Manufacture Command Set (CMD2, means panel function registers) reading only.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send ""Generic Read, 1 Parameter"" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

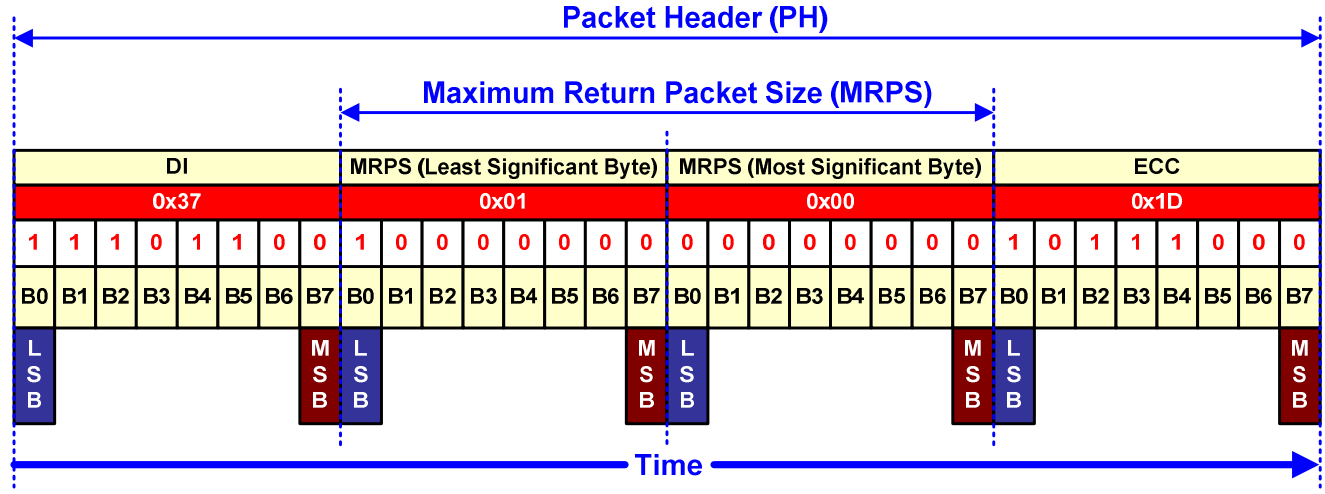
Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

Data 0: 01hex

Data 1: 00hex

• Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Generic Read, 1 Parameter" to the display module

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

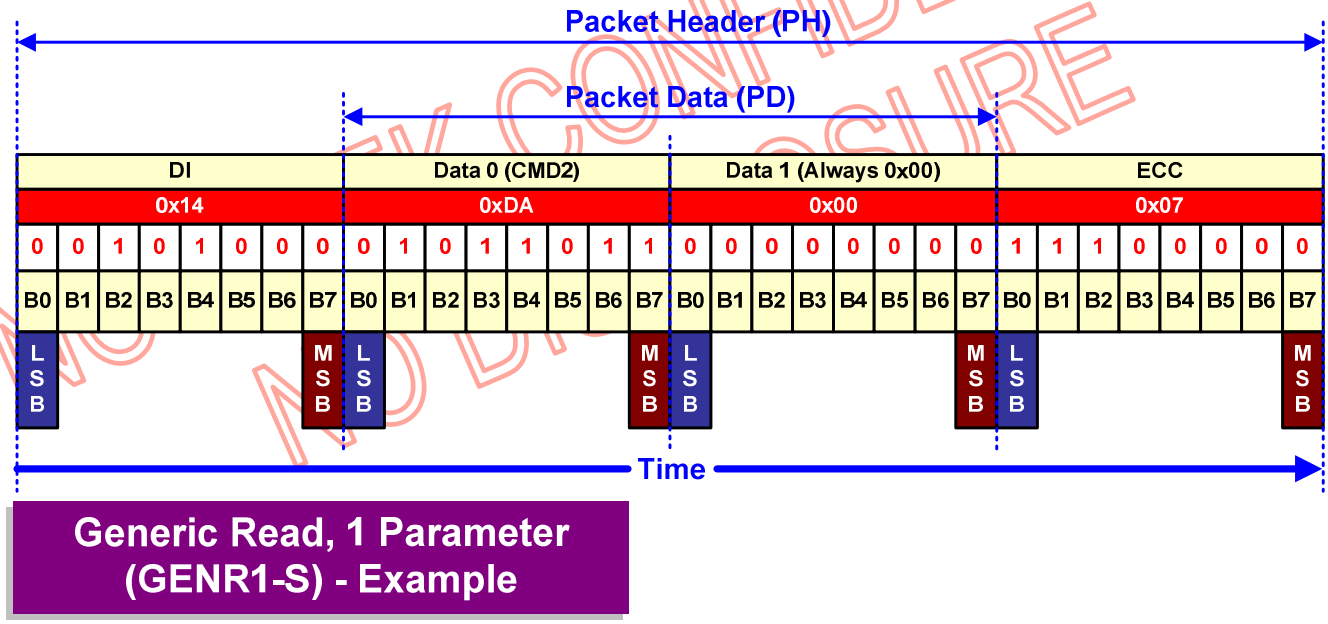
Data Type (DT, DI[5…0]): 01 0100b

• Packet Data (PD)

Data 0: "Read ID1 (DAh)", Display Command Set (DCS)

Data 1: Always 00hex

• Error Correction Code (ECC)



Generic Read, 1 Parameter (GENR1-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter "Acknowledge with Error Report (AwER)"

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. The content of payload bytes is "command" with "00h". "Display Command Set (DCS) Write, No Parameter" is used for User Command Set (CMD1) writing only.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 0101b

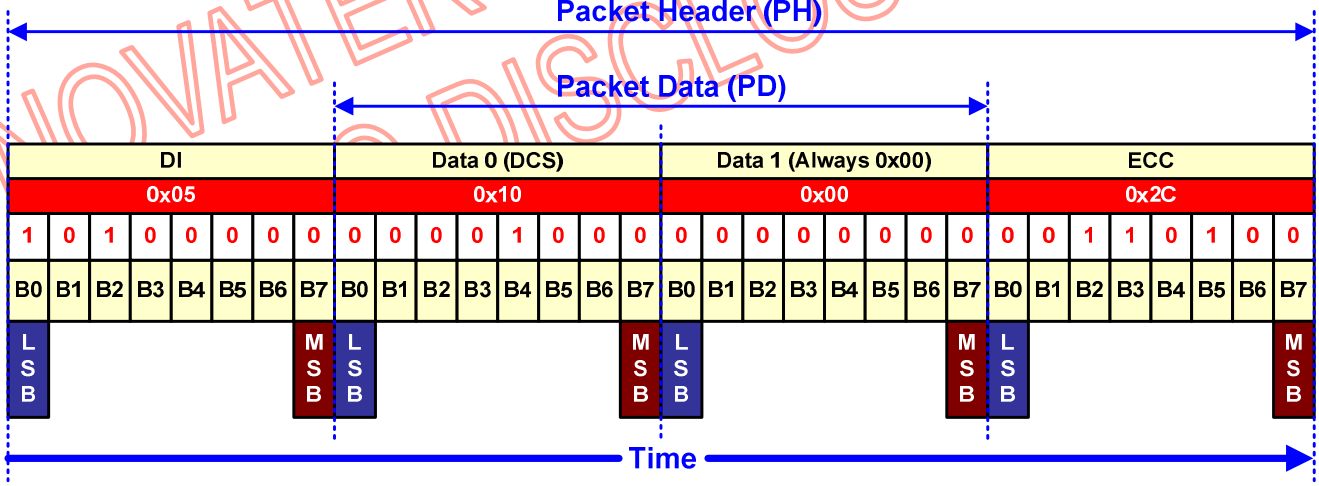
• Packet Data (PD)

Data 0: "ENTER_SLEEP_MODE (10h)", Display Command Set (DCS)

Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. The content of payload bytes are "command" with one "parameter". "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is used for User Command Set (CMD1) writing only.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 01 0101b

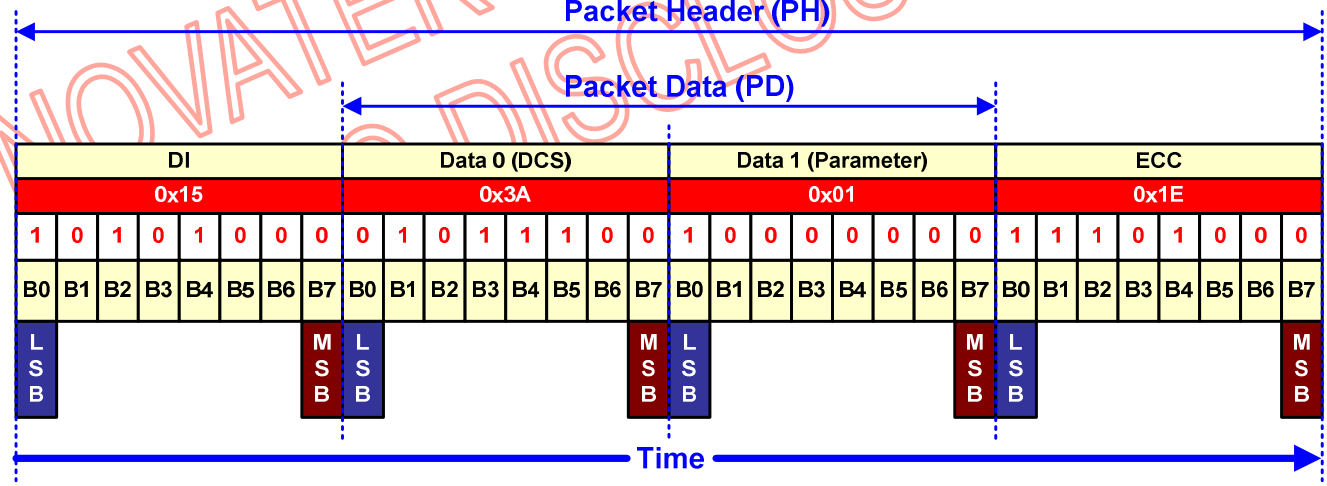
• Packet Data (PD)

Data 0: "SET_PIXEL_FORMAT (3Ah)", Display Command Set (DCS)

Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) - Example

Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. The content of payload bytes are "command" with multiple "parameter". "Display command Set (DCS) Write Long" (DCSW-L) is used for User Command Set (CMD1) writing only.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- **Data Identification (DI)**

  Virtual Channel (VC, DI[7…6]): 00b

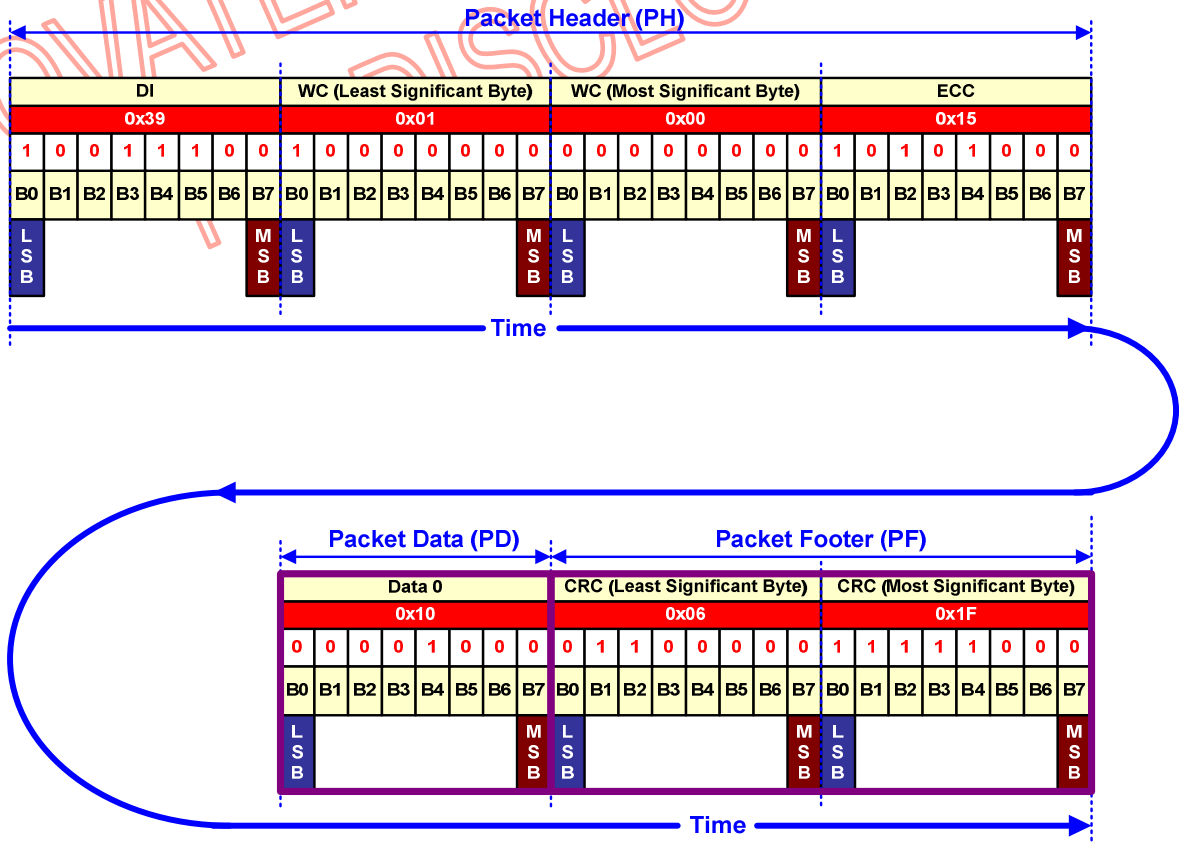
  Data Type (DT, DI[5…0]): 11 1001b

- **Word Count (WC)**

  Word Count (WC): 0001h

- **Error Correction Code (ECC)**
- **Packet Data (PD): Data 0: "EXTER_SLEEP_MODE (10h)", Display Command Set (DCS)**
- **Packet Footer (PF)**

This is defined on the Long Packet (LPa) as follows.



Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

Word Count (WC): 0002h

• Error Correction Code (ECC)

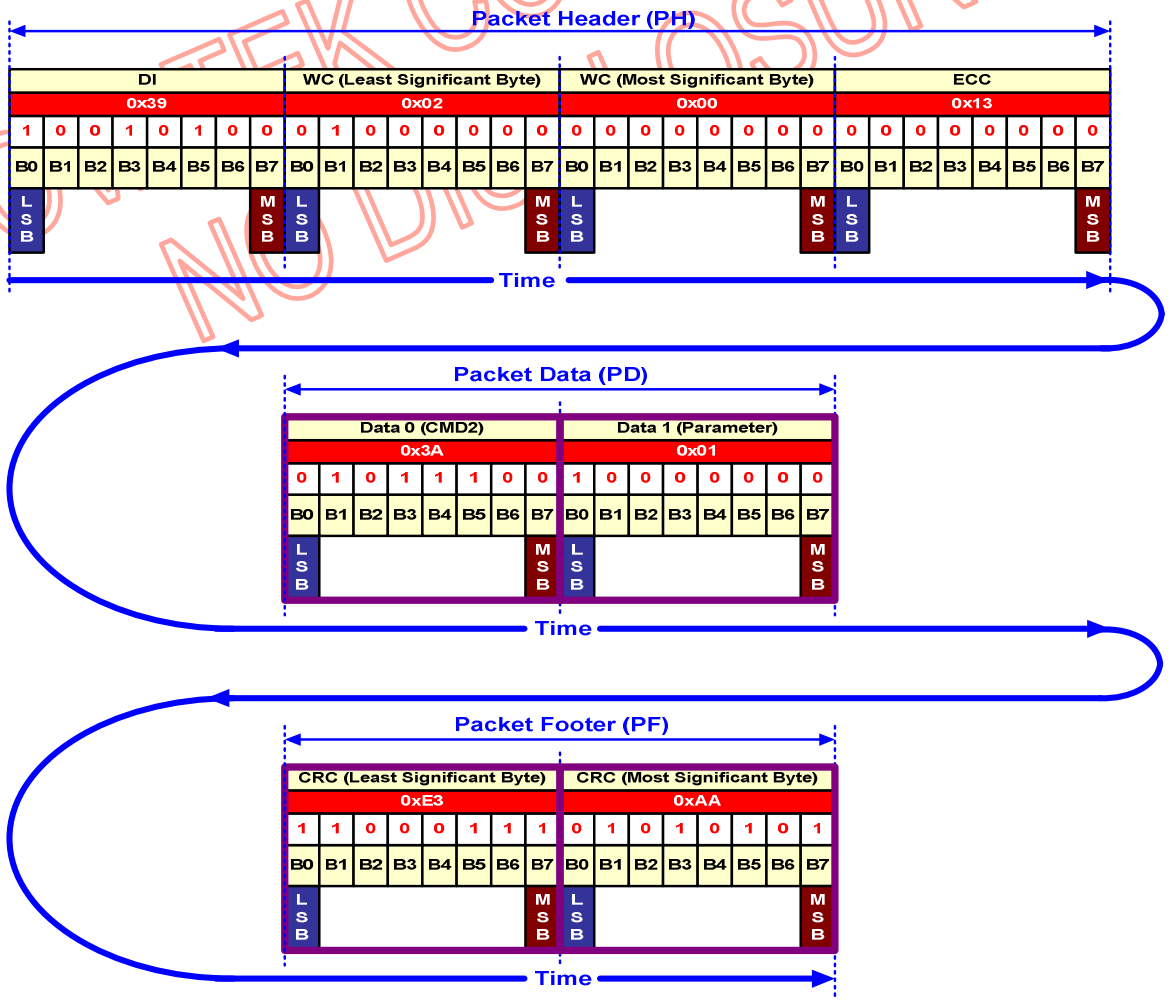
• Packet Data (PD):

Data 0: “SET_PIXEL_FORMAT (3Ah)”, Display Command Set (DCS)

Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

Data 0: “PARLINES (30h)”, Display Command Set (DCS)

Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

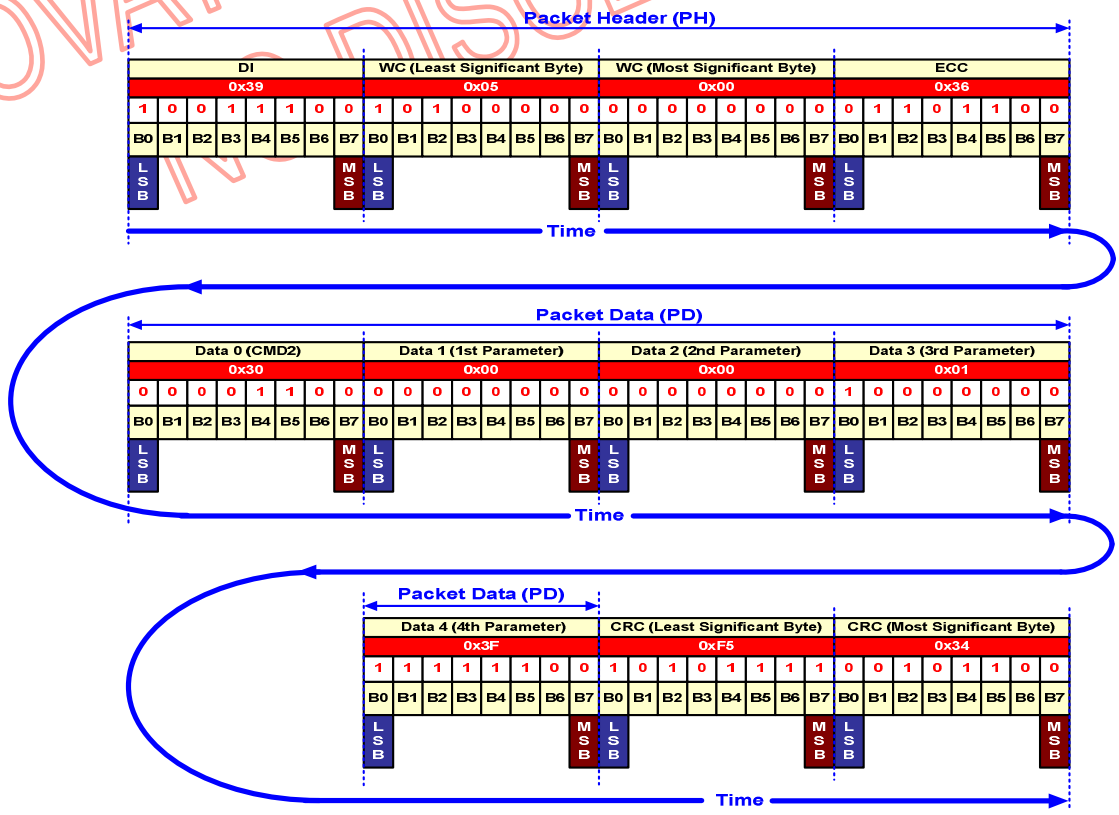
Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]

Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S) , Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. The content of payload bytes are "command" with "00h". Display Command Set (DCS) Read, No Parameter (DCSRN-S) is used for User Command Set (CMD1) reading only.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

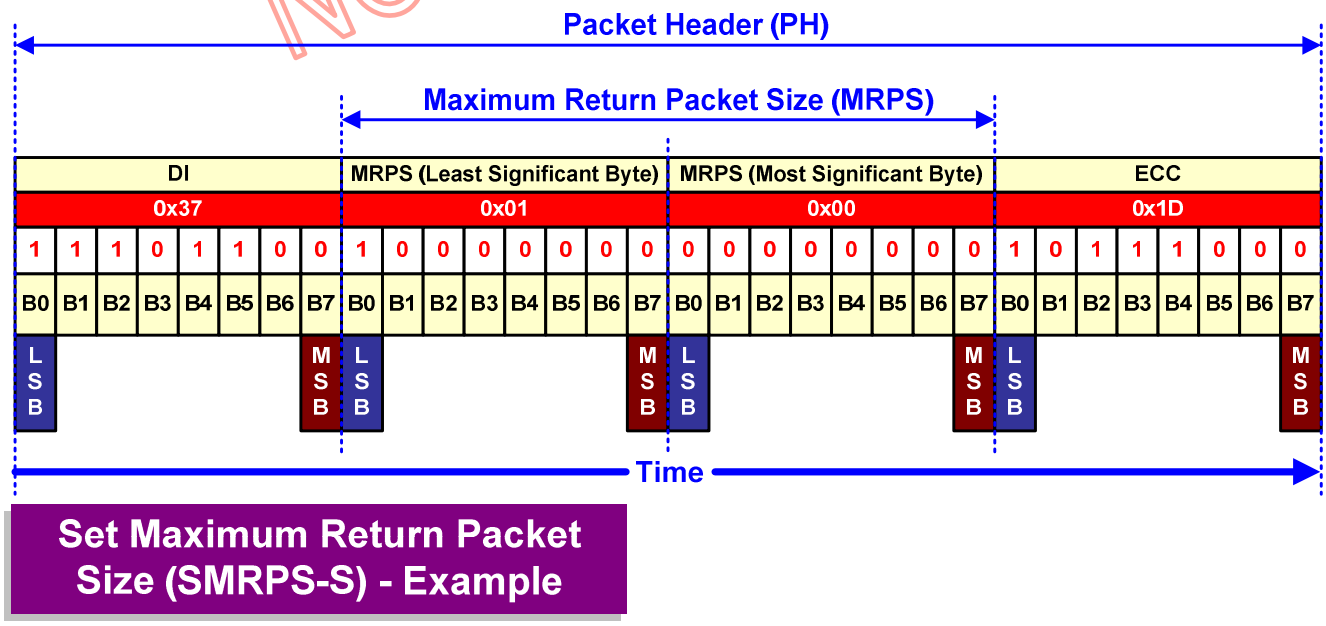
Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

Data 0: 01hex

Data 1: 00hex

• Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

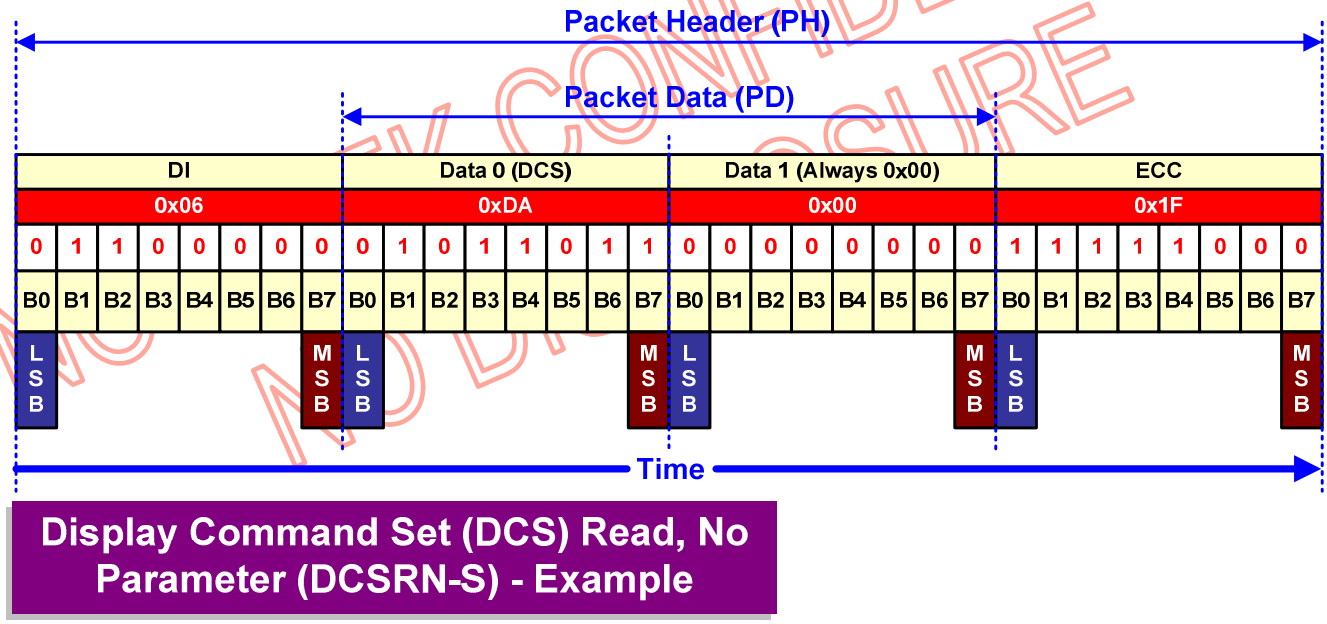
Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

Data 0: "Read ID1 (DAh)", Display Command Set (DCS)

Data 1: Always 00hex

• Error Correction Code (ECC)



Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter "Acknowledge with Error Report (AwER)"
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending. Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

• **Data Identification (DI)**

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 1001b

• **Word Count (WC)**

Word Count (WC): 0005hex

• **Error Correction Code (ECC)**

• **Packet Data (PD):**

Data 0: 89hex (Random data)

Data 1: 23hex (Random data)

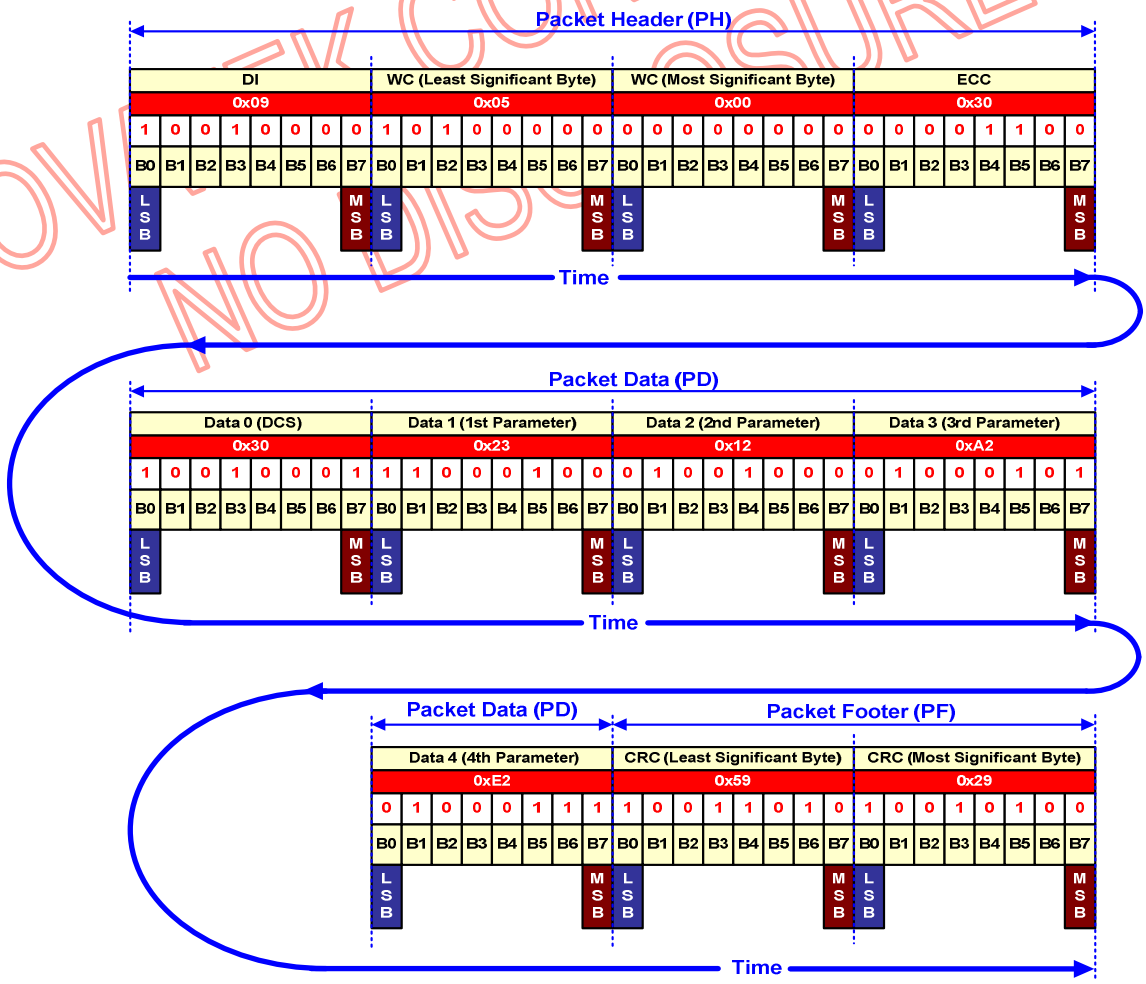
Data 2: 12hex (Random data)

Data 3: A2hex (Random data)

Data 4: E2hex (Random data)

• **Packet Footer (PF)**

This is defined on the Long Packet (LPa) as follows.



Null Packet, No Data (NP-L) - Example

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

EoT Packet, Data Type = 00 1000 (08h)

This new short packet is used for indicating the end of a HS transmission to the data link layer. As a result, detection of the end of HS transmission may be decoupled from physical layer characteristics. D-PHY defines an EoT sequence composed of a series of all 1's or 0's depending on the last bit of the last packet within a HS transmission. Due to potential errors, the EoT sequence could wrongly be interpreted as valid data types. Although EoT errors are not expected to happen frequently, the addition of this new packet will enhance overall system reliability.

Older devices compliant to earlier revisions of DSI specification do not support EoT packet generation or detection. All Hosts and Peripheral devices compliant to this revision of DSI specification, and going forward, shall incorporate capability of supporting EoT packet. They shall also provide means for enabling and disabling this capability – implementation specific – to ensure interoperability with older DSI devices not supporting EoT packet.

As mentioned earlier, the main objective of an EoT packet is to enhance overall robustness of the system during HS transmission mode. Therefore, DSI transmitters should not generate an EoT packet when transmitting in LP mode. The data link layer of DSI receivers shall detect and interpret arriving EoT packets regardless of transmission mode (HS or LP modes) in order to decouple itself from the PHY layer. Table below describes how DSI mandates EoT packet support for different transmission and reception modes.

EoT Support for Host and Peripheral

DSI Host (EoT capability enable)				DSI Peripheral (EoT capability enable)			
HS Mode		LP Mode		HS Mode		LP Mode	
Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit
Not Applicable	"Shall"	"Shall"	"Should not"	"Shall"	Not Applicable	"Shall"	"Should not"

Unlike other DSI packets, an EoT packet has a fixed format as follows:

- **Data Type = DI [5:0] = 0b001000**
- **Virtual Channel = DI [7:6] = 0b00**
- **Payload Data [15:0] = 0x0F0F**
- **ECC [7:0] = 0x01**

The virtual channel identifier associated with an EoT packet is fixed to 0, regardless of the number of different virtual channels present within the same transmission. For multi-Lane systems, the EoT packet bytes are distributed across multiple Lanes.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

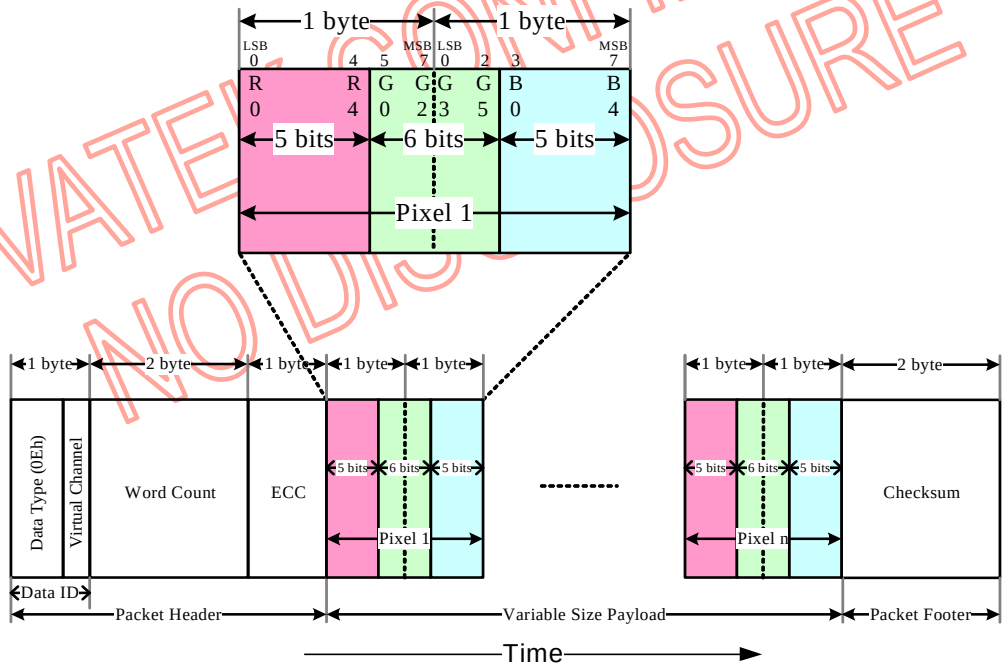
Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bits Format, Long packet, Data Type 1228 pe 00 1110 (0Eh)



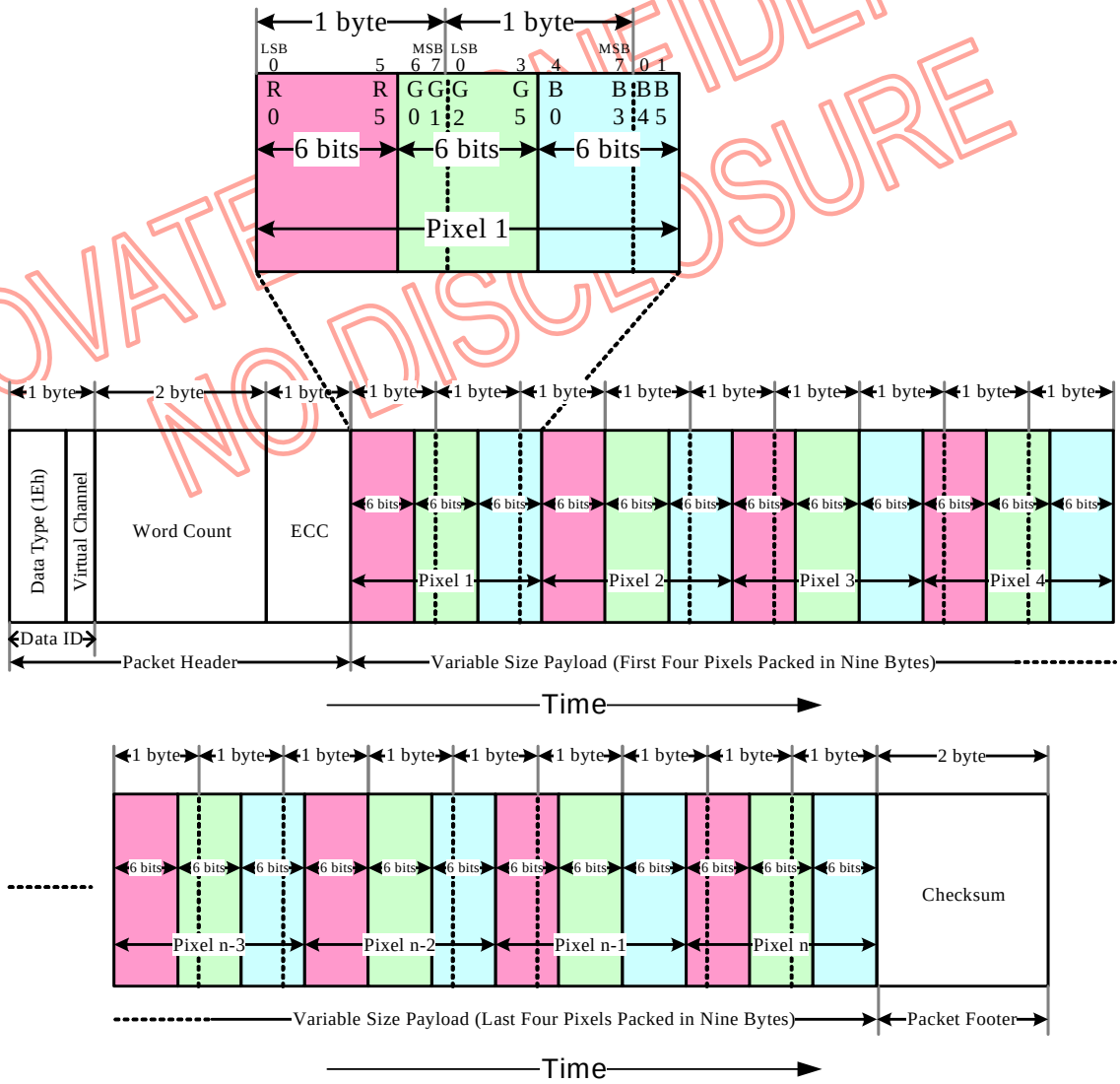
16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 16-bits Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bits Format, Long packet, Data type = 01 1110 (1Eh)



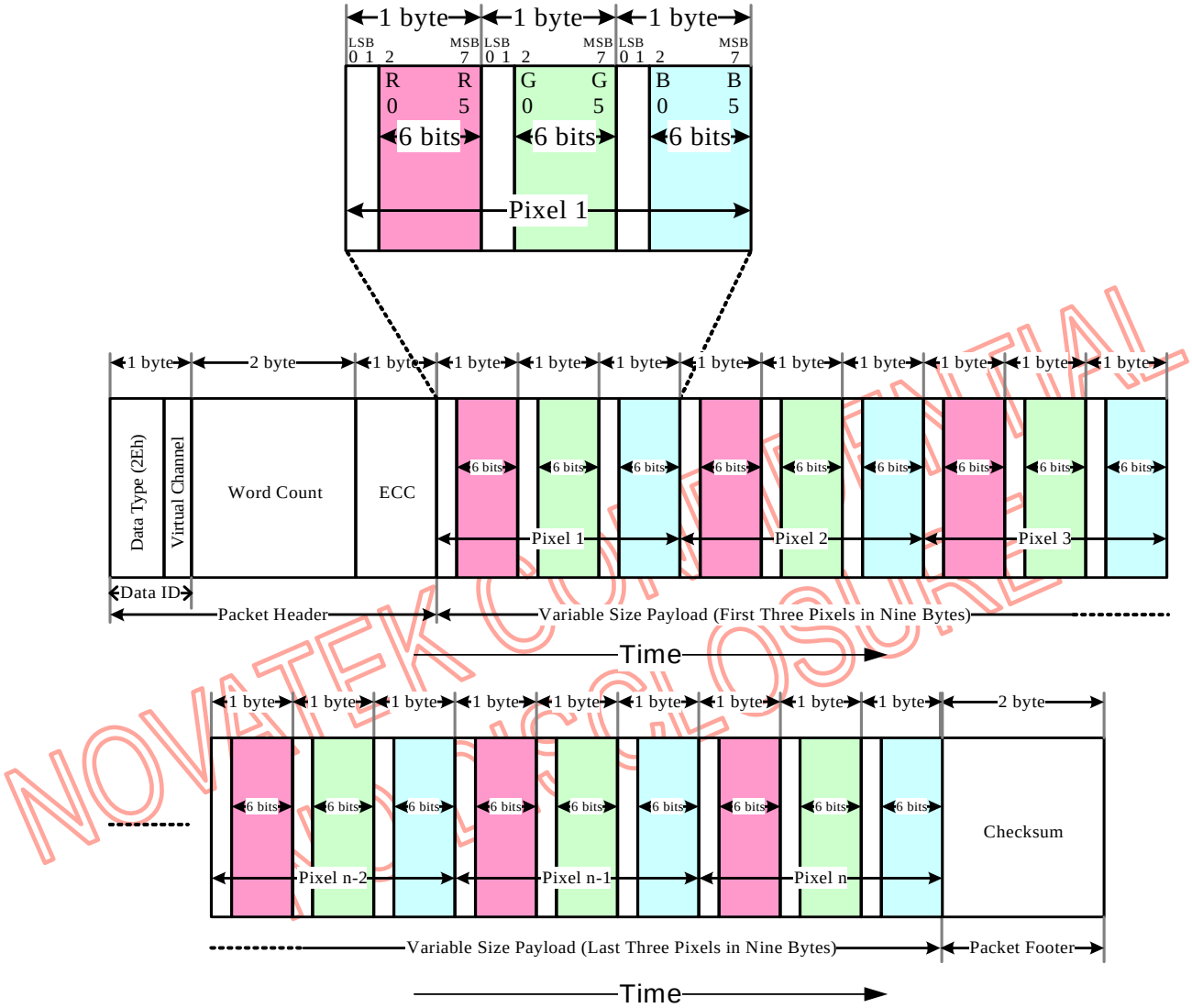
18-bit per Pixel (Packed)– RGB Color Format, Long packet

Packed Pixel Stream 18-bits Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bits pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bits Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



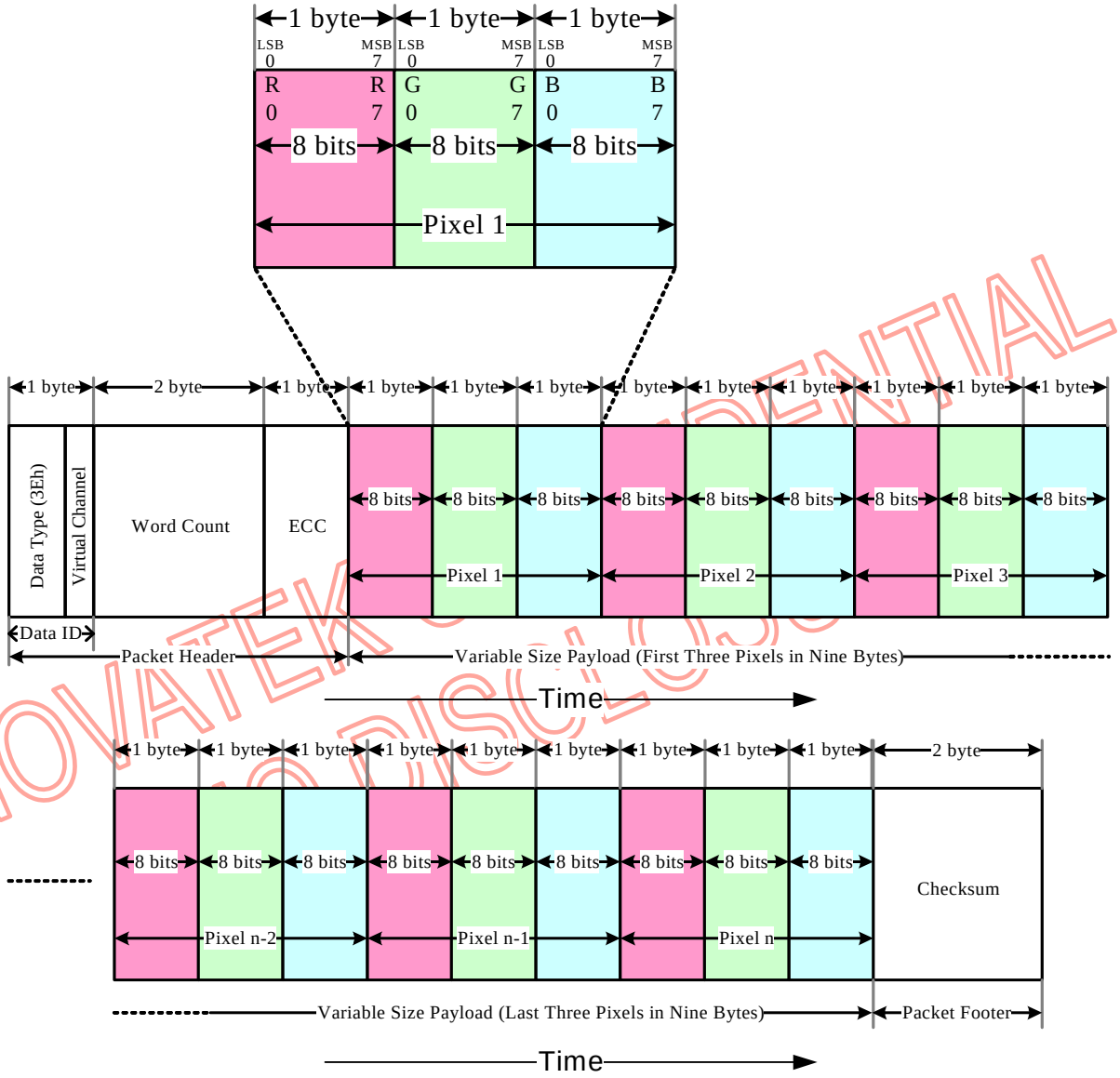
18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

In the 18-bits Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bits pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Packed Pixel Stream, 24-bits Format, Long packet, Data Type = 11 1110 (3Eh)



24-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 24-bits Format is a Long packet. It is used to transmit image data formatted as 24-bits pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.4.2.3.2.2 Packet from the Display Module to the MCU

Used Packet Types

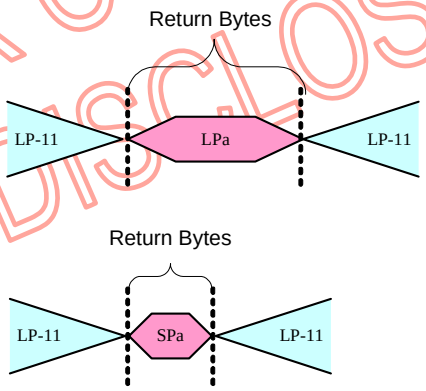
The display module is always using Short Packet (Spa) or Long Packet (Lpa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”.

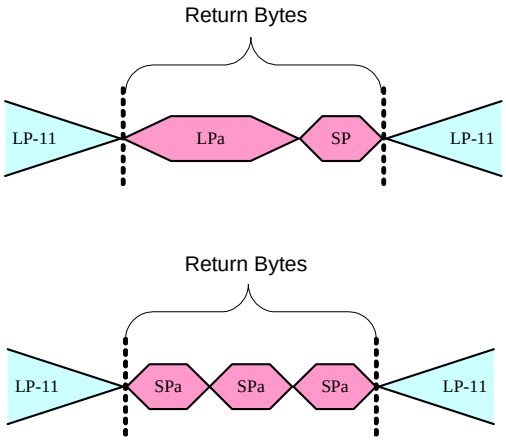
A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (Lpa) or Short Packet (Spa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is also possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.



Return Bytes on Single Packet



Return Bytes on Several Packets – Only for Reference Purposes

Data Types for Display Module-Sourced Packets

Data Type, (HEX)	Data Type, (BINARY)	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
08h	00 1000	EoT	End of Transmission (EoT) Packet	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	DCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	10 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Short Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Short Read Response, 2 Byte returned	Short

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Reserved
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 0010b

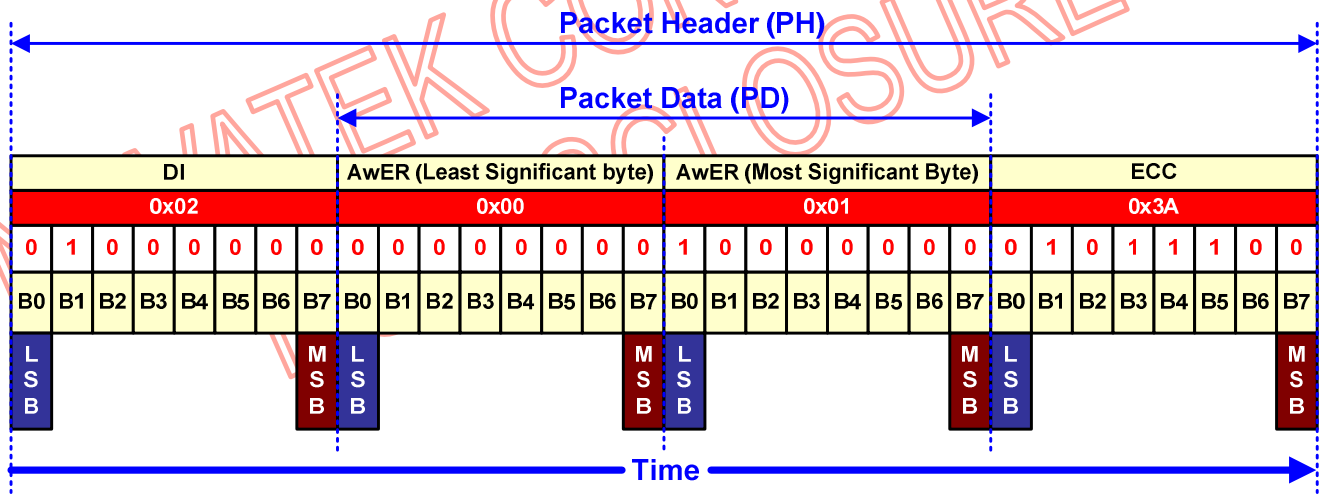
• Packet Data (PD)

Bit 8: ECC Error, single-bit (detected and corrected)

AwER: 0100h

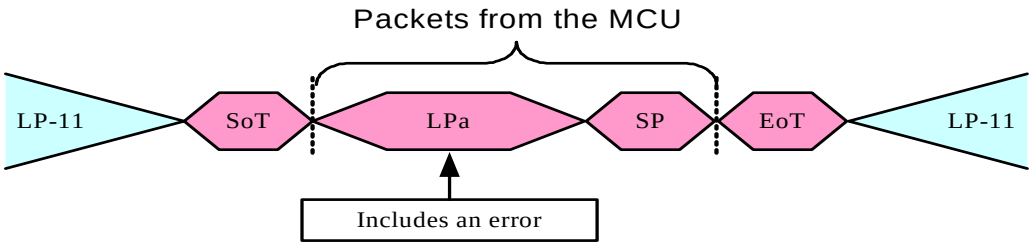
• Error Correction Code (ECC)

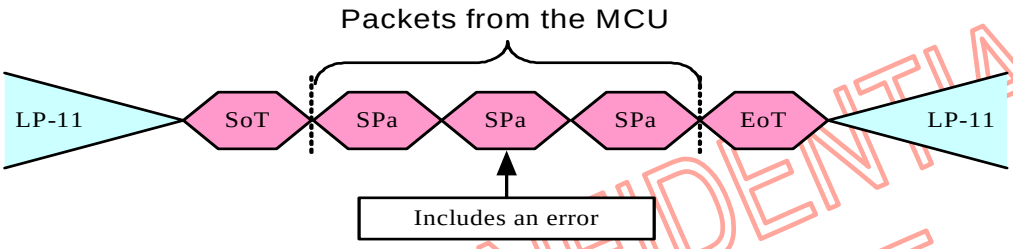
This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER) - Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.





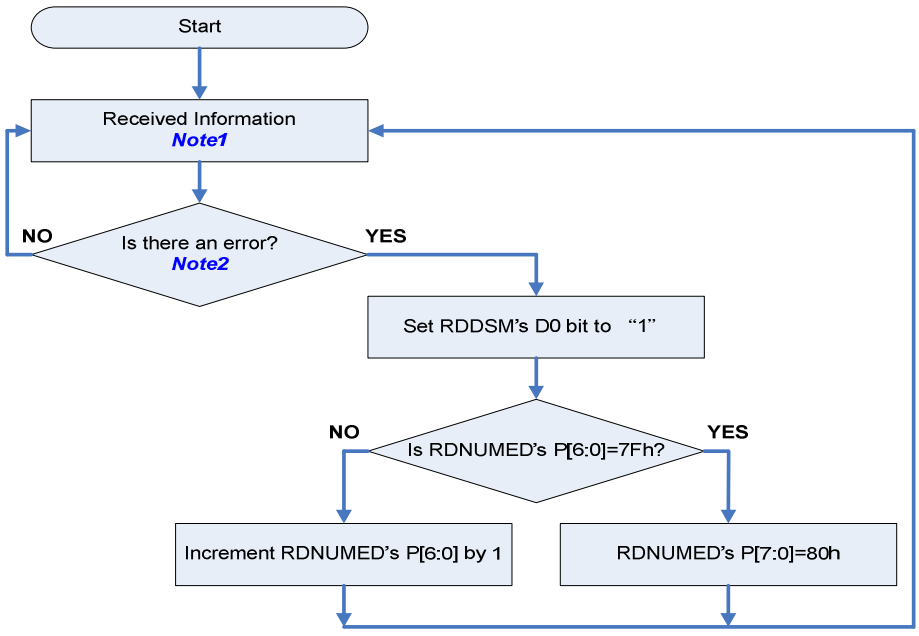
Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands.

The bit D0 of the "Read Display Signal Mode (0Eh)" command has been set to '1' if a received packet includes an error.

The numbers of the packets, which are including an ECC (multi and single) or CRC error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the "Read Display Signal Mode (0Eh)" command to '0' after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note1: This information can be interface or packet level communication but it is always from the MCU to the display module in this case.

Note2: CRC or ECC (multi and single) error

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 01 1100b

• Word Count (WC)

Word Count (WC): 0005hex

• Error Correction Code (ECC)

• Packet Data (PD):

Data 0: 89hex

Data 1: 23hex

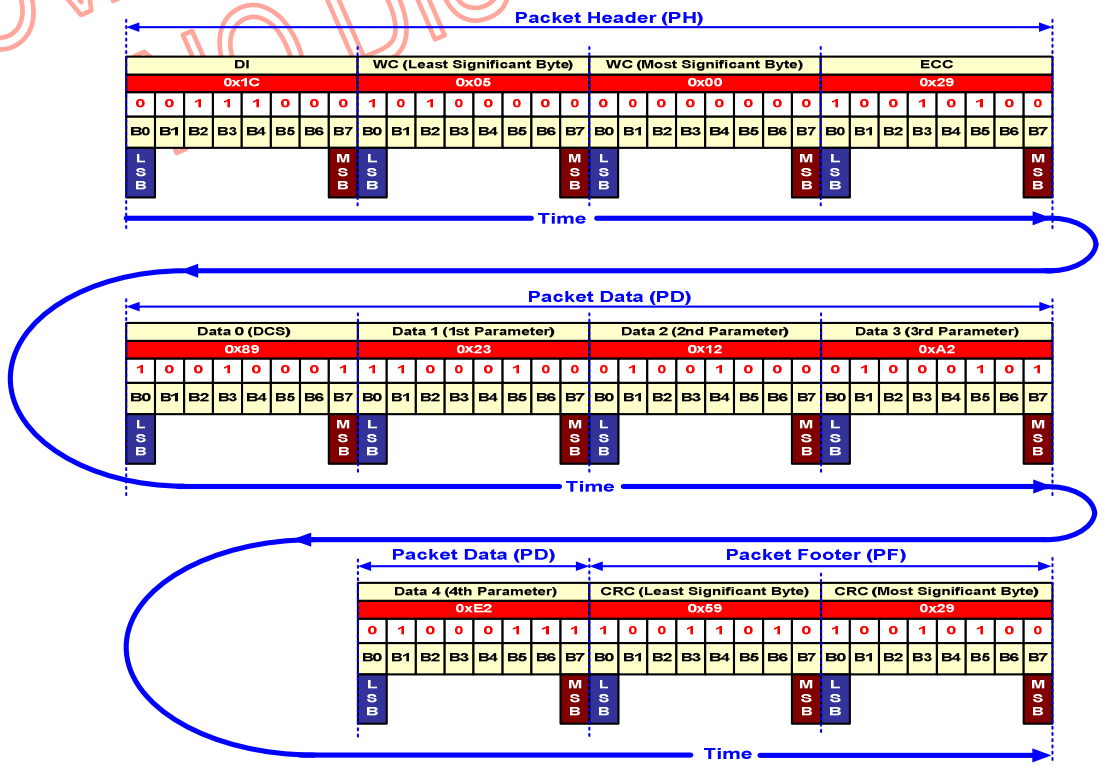
Data 2: 12hex

Data 3: A2hex

Data 4: E2hex

• Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response (DCSRR-L) - Example

DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 10 0001b

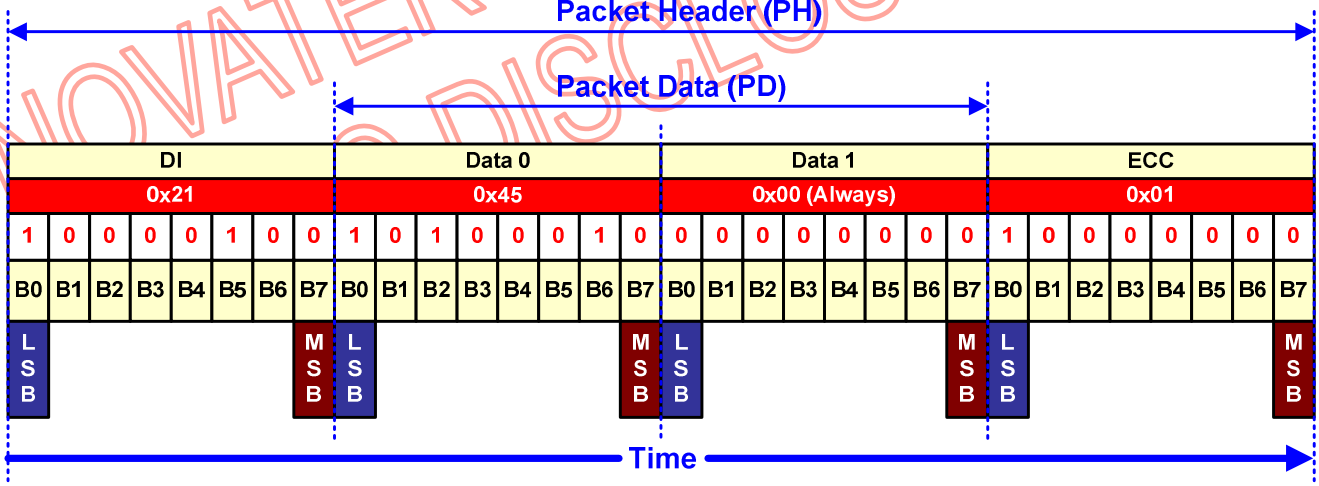
• Packet Data (PD)

Data 0: 45hex

Data 1: 00hex (Always)

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 10 0010b

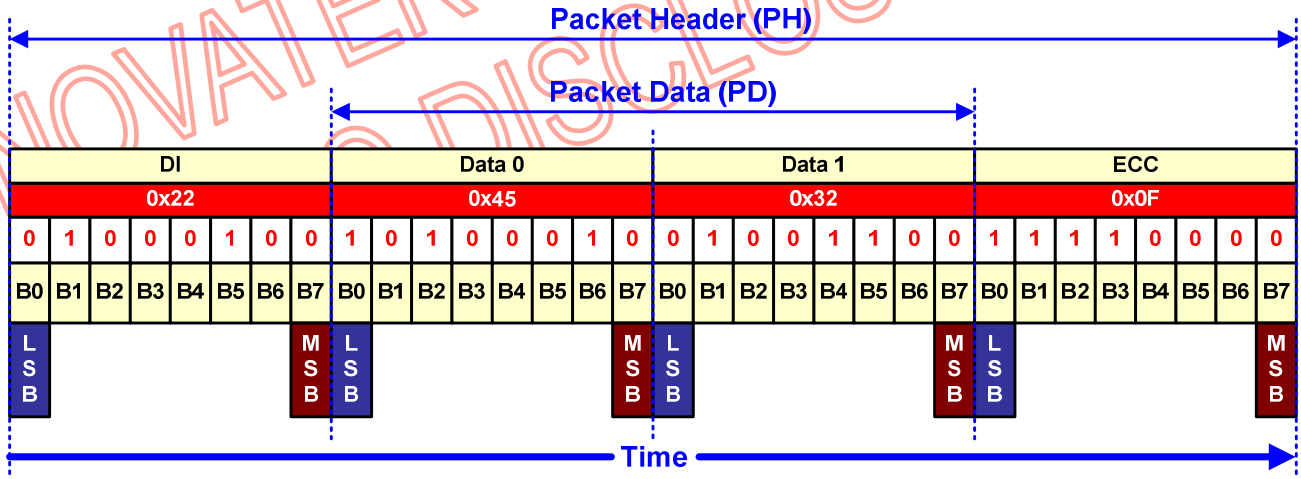
• Packet Data (PD)

Data 0: 45hex

Data 1: 32hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 01 1010b

• Word Count (WC)

Word Count (WC): 0005hex

• Error Correction Code (ECC)

• Packet Data (PD):

Data 0: 89hex

Data 1: 23hex

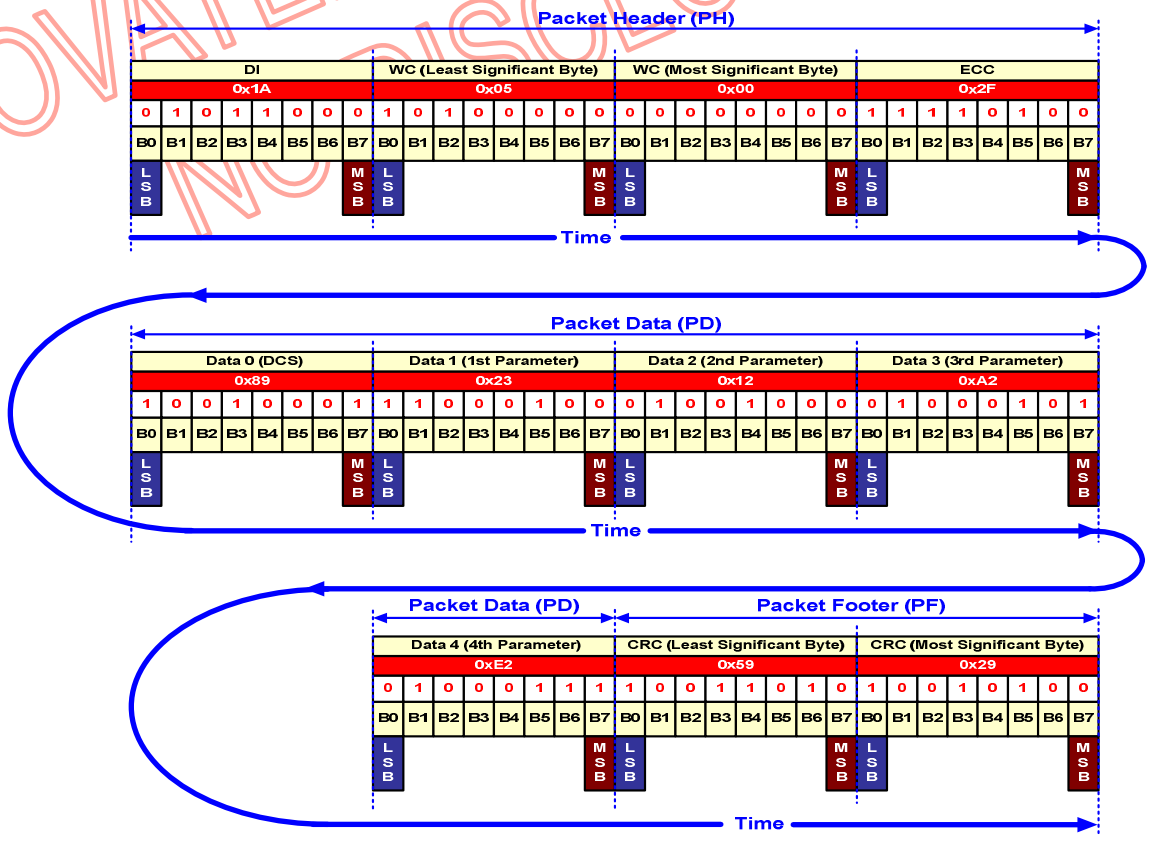
Data 2: 12hex

Data 3: A2hex

Data 4: E2hex

• Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Generic Read Long Response (GENRR-L) - Example

Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

"Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. "Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- **Data Identification (DI)**

  Virtual Channel (VC, DI[7…6]): 00b

  Data Type (DT, DI[5…0]): 01 0001b

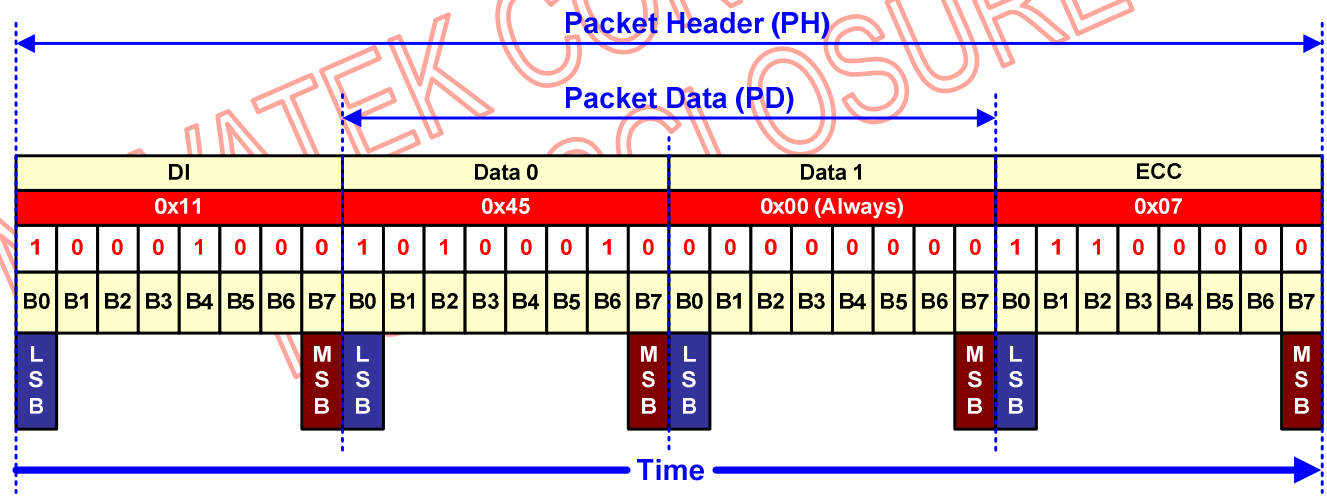
- **Packet Data (PD)**

  Data 0: 45hex

  Data 1: 00hex (Always)

- **Error Correction Code (ECC)**

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S) - Example

Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 01 0010b

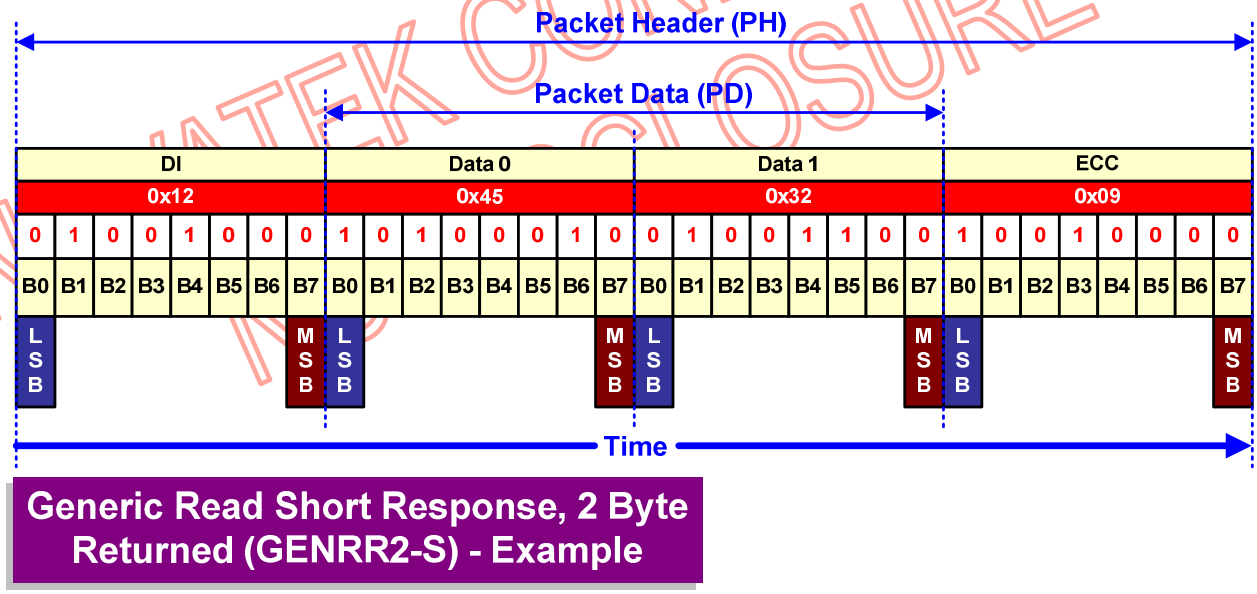
• Packet Data (PD)

Data 0: 45hex

Data 1: 32hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Read Short Response, 2 Byte Returned (GENRR2-S) - Example

5.4.2.3.3 Communication Sequence

5.4.2.3.3.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”. This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.4.2.3.3.2 Sequences

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Memory Write (2Ch)
3	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
4	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
5	DCSW1-S	HSDT	=>	-	-	Memory Write Continue(3Ch) with 1 parameter
6	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	LPDT	DCSRR1-S	Response 1 byte return
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	LPDT	DCSRR-L	Response 200 bytes return
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7						
8	-	-	<=	LPDT	DCSRR-L	Responsed 100 bytes return
9	-	-	<=	LPDT	DCSRR-L	Responsed 100 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7						
8	-	-	<=	LPDT	DCSRR-L	Response 199 bytes return
9	-	-	<=	LPDT	DCSRR1-L	Response 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 5

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7						
8	-	-	<=	LPDT	DCSRR-L	Response 198 bytes return
9	-	-	<=	LPDT	DCSRR2-L	Response 2 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	-	LP-11	=>	-	-	End

5.4.2.3.3.3 Tearing Effect Bus Trigger Sequences

Tearing Effect Bus Trigger Enable Sequence – DCSW-L and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWL	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 If Error => Goto Line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11	-	LP-11	=>	-	--	
12		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
13		--	<=	LP-11	-	
14		--	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
15		--	<=	LP-11	-	
16	-	BTA	<=>	BTA	--	Interface Control Change from the display module to the MCU
17		LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
22	-	LP-11	=>	-	-	
23		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module

24	-	--	<=	LP-11	-	
25	-	--	<=	TEE	-	
26	-	--	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	
28	-	LP-11	=>		-	End
29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 If the MCU is forcing BTA => Goto Line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	=>		-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
44	-	LP-11	=>		-	End

Notes: 1. Lines 1 – 17 are needed for every frame.

2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW-L and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWL	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet

4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 If Error => Goto Line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11	-	LP-11	=>	-	--	
12		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
13		--	<=	LP-11	-	
14		--	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
15		--	<=	LP-11	-	
16	-	BTA	<=>	BTA	--	Interface Control Change from the display module to the MCU
17		LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
22	-	LP-11	=>	-	-	
23		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
24	-	--	<=	LP-11	-	
25	-	--	<=	TEE	-	
26	-	--	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	
28	-	LP-11	=>		-	End
29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	

32	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 If the MCU is forcing BTA => Goto Line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
37	-		<=	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	=>		-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
44	-	LP-11	=>		-	End

Notes: 1. Lines 1 – 17 are needed for every frame.

2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence –DCSW1-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 If Error => Goto Line 30
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	

9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
10	-	LP-11	=>	-	--	
11		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
12		--	<=	LP-11	-	
13		--	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
14		--	<=	LP-11	-	
15	-	BTA	<=>	BTA	--	Interface Control Change from the display module to the MCU
16		LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
21	-	LP-11	=>	-	-	
22		BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
23	-	--	<=	LP-11	-	
24	-	--	<=	TEE	-	
25	-	--	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	
27	-	LP-11	=>		-	End
28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 If the MCU is forcing BTA => Goto Line 36
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
36	-		<=	LP-11	-	Dead-Lock (No TE information) See Note 2

37	-	LP-11	=>		-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
43	-	LP-11	=>		-	End

Notes: 1. Lines 1 – 17 are needed for every frame.

2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	=>	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Disable
	EoTp	HSDT				End of Transmission Packet
3	-	LP-11	=>	-	-	End

5.4.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.4.2.4.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

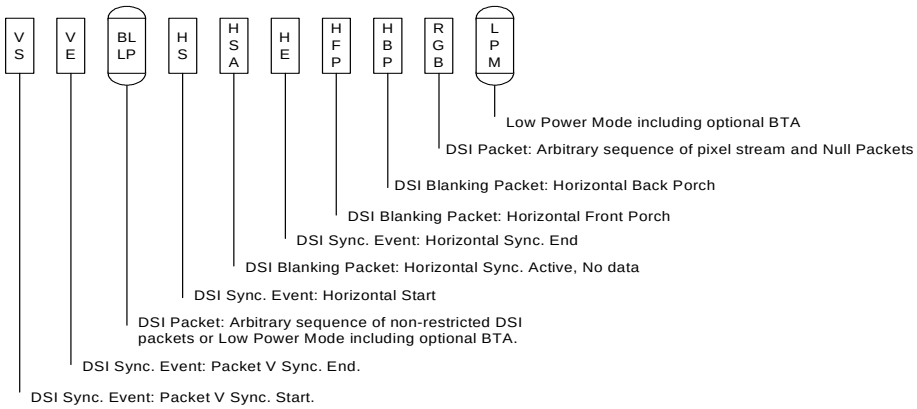
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

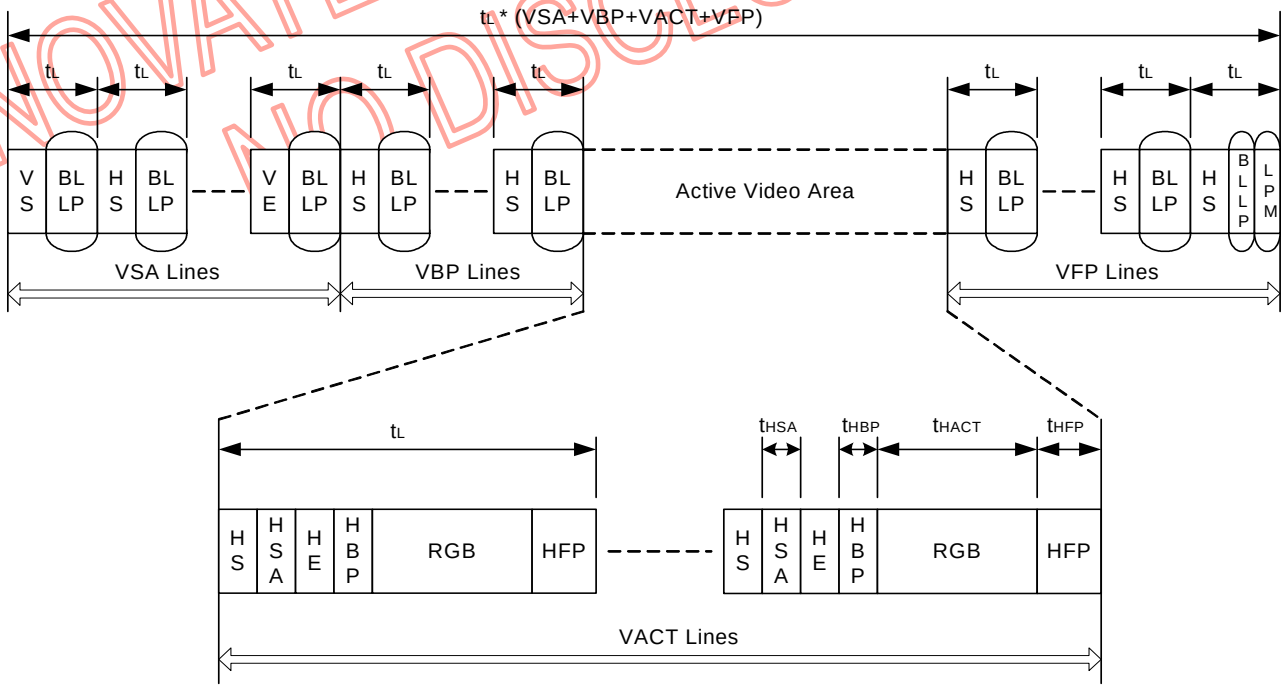


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.4.2.4.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

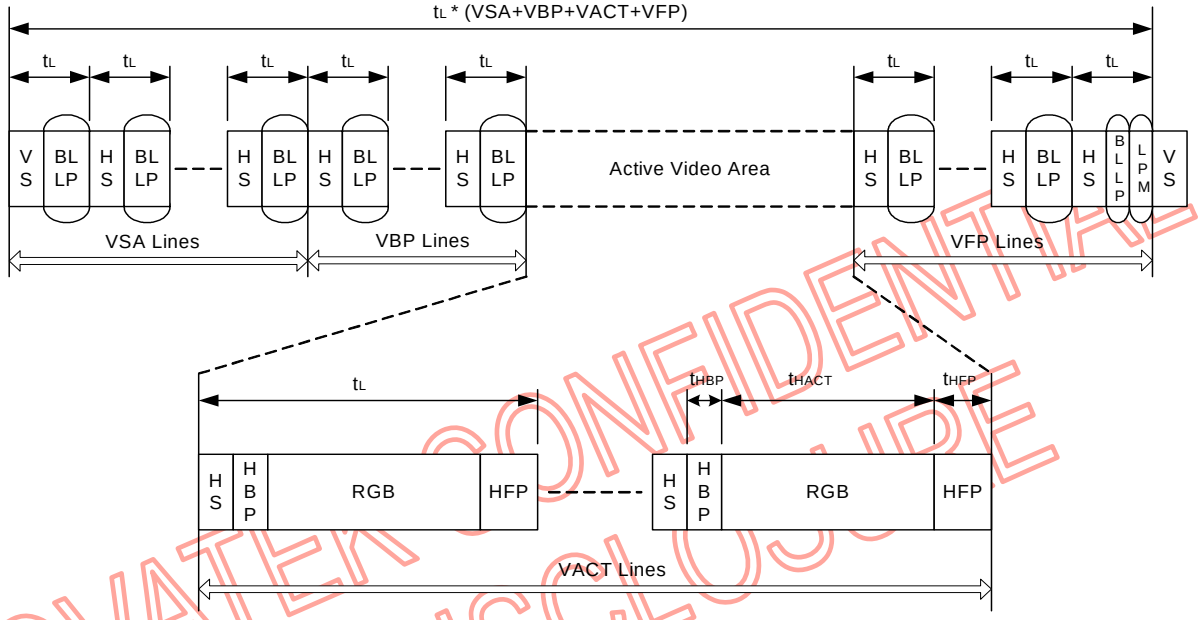


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.4.2.4.3 Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section 5.8.2.4.2 “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

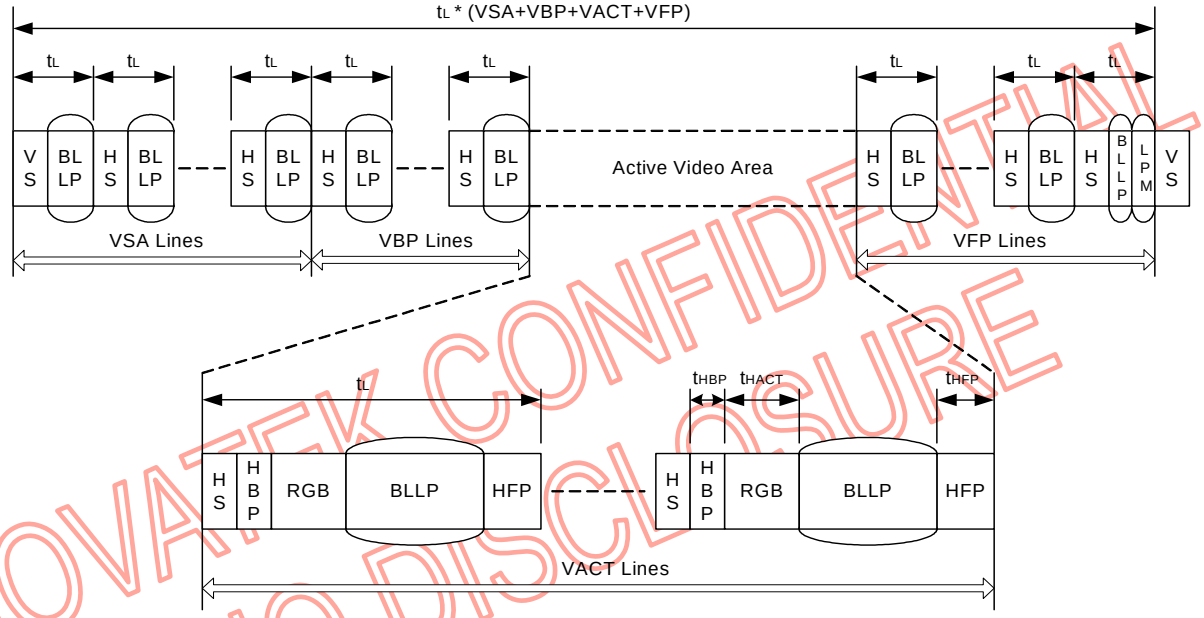


DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.4.2.4.4 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.4.2.4.5 Parameters

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

Required Peripheral Timing Parameters (Base on 1080RGBx1920)

Symbol	Parameter	Condition	Min	Typ	Max	Units
BR_{PHY}	Bit rate per Lane (Note3)	Full-HD(1080RGB x 1920)	80	-	1000	Mbps
t_L	Line time	Full-HD(1080RGB x 1920)	-	8.6 (Note 1)	-	us
t_{HBP}	Horizontal back porch	Full-HD (1080RGB x 1920)	16	-	-	pixel clock
t_{HACT}	Time for image data	4 data lane	1080	-	(Note 2)	pixel clock
HACT	Active pixels per line	Full-HD (1080RGB x 1920)		1080	-	pixels
t_{HFP}	Horizontal front porch		0.65		-	us
VSA	Vertical sync active		1	-	-	H
VBP	Vertical back porch		2	-	-	H
VACT	Active lines per frame	Full-HD (1080RGB x 1920)		1920		H
VFP	Vertical front porch		4	-	-	H

Note 1: Frame rate (Typ) = 60Hz, and VBP is set to 2 / VFP is set to 4.

Note 2: t_{HACT} (max)= $t_L - t_{HFP} - t_{HBP}$ (us)

Note 3: For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for5-6-5.

5.5 Display Reference Clock Function

The NT35532 provides a function to decide internal oscillator or external clock for display clock reference of driver IC. User can set this register of CMD1 address F8h. When user sets EN_EXCK of F6h to “1”, the display clock will refer to external clock, and user must set the frequency of external clock in register F6h/F7h, and then sets the RTN value for 1H line period (About RTN setting value, please always refers to 14.66MHz frequency basis). If user sets EN_EXCK to “0”, the display clock will refer to NT35532 internal oscillator, and user only need to set RTN value to decide 1H period.

External Clock Frequency must be filled in CMD1 register F6h/F7h if EN_EXCK bit is “1”:

$$EXCK\_FREQ[11:0] = 100 * f(MHz)$$

“***f***“ is external oscillator frequency in unit “MHz”

EXCK_FREQ: External Clock Frequency include 2-digit decimal point accuracy

RTN setting for 1H period (for detailed, please refer to NT35532 application note):

$$RTN = \frac{14.66MHz}{(Line + BP + FP) * FrameRate(Hz)}$$

RTN: Number of clocks per line.

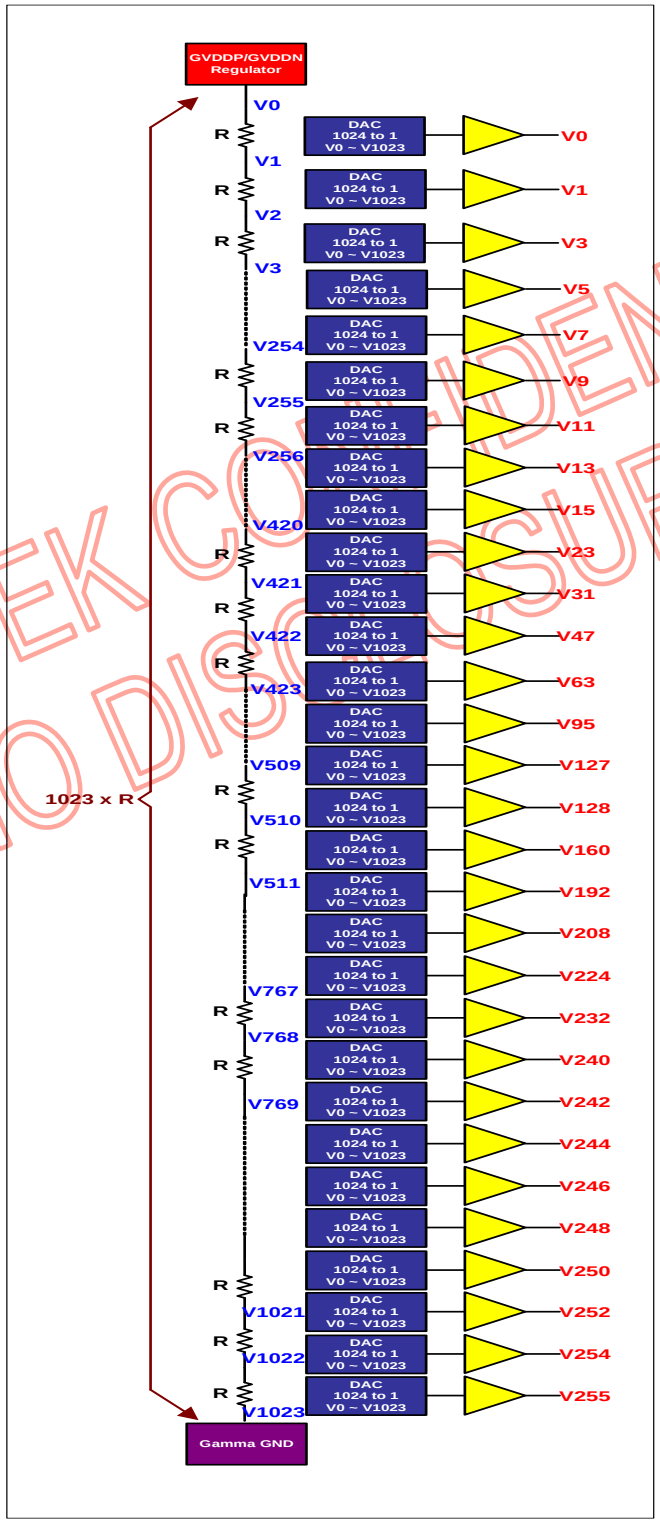
Line: Display Line Number

FP: Number of lines for front porch.

BP: Number of lines for back porch.

5.6 GAMMA Function

The structure of grayscale amplifier is shown as below. The 30 voltage levels between GVDDP/GVDDN and GND determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



Gamma Architecture for NT35532

5.7 Reset Function

The RESET function of NT35532 is triggered by a RESX input. After reset function triggered, the NT35532 enter a reset period, and the duration of this period must be at least 1ms. During this period, the NT35532 and its power circuit is initialized. In the meanwhile, because the NT35532 will be in a busy state, neither instruction from MPU nor GRAM data access request are not acceptable. In addition, for power-on reset case, there will be a 20ms period for oscillator to be stable. Therefore, any instructions or GRAM access request must be made after this 20ms period is over.

Initial States of Output Pins

The following table represents the output pins and its initial state

Output Pins	Initial State
Liquid crystal driver (Source driver output)	All output VSS
VCOMDC3	Disabled (VSS level output)
GVDD P/N	Disabled (VSS level output)
CGOUTR1~R20, CGOUTL1~L20	Disabled (VSS level output)
FTE / FTE1/LEDPWM	Disabled (VSS level output)
VGH	AVDD
VGL	AVEE
VGHO	VSS
VGLO	VSS
VCL	CVSS
VCI1	VSS
AVDDR	VSS
AVEER	VSS

Initial States of Input / Output Pins

The following table represents the input/output pins and its initial state

Input/Output Pins	Initial State
C21P/M	Hi-z
C22P/M	Hi-z
C31P/M	Hi-z
C41P/M	Hi-z

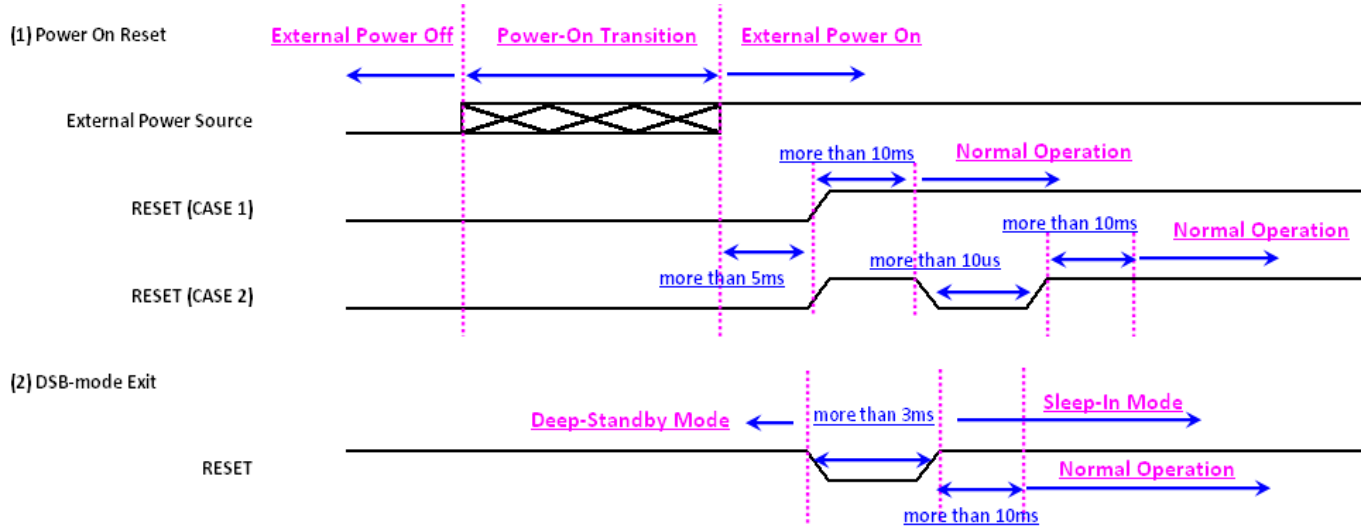
Notes: The initial states of input/output pins listed above are proper under the condition that LCD module is connected as shown in the connection example.

Initial State of Instruction Set

The initial state of instruction set is listed in next chapter, and the default values are shown in the parenthesis of each instruction bit cell.

5.7.1 Timing of Reset Pin

NT35532 provides H/W pin to do driver IC initialization and exit of "Deep Standby Mode ". For power-on reset, one-finger reset or two-finger reset method to do driver IC initialization. For “Deep Standby Mode” exit method, H/W reset pin must be keep low state more than 3ms. The detailed H/W reset pin timing is shown as below figure.

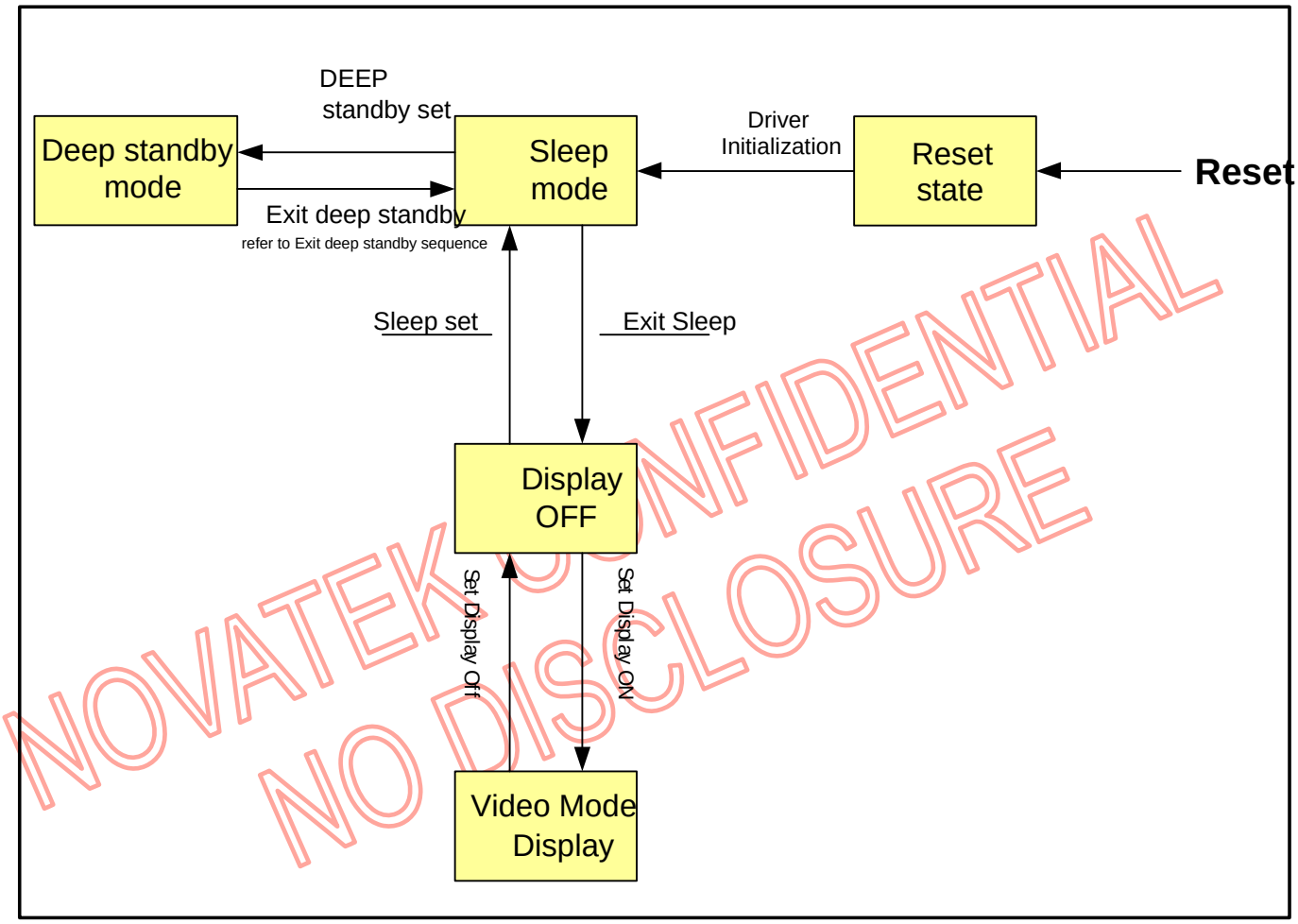


H/W reset pin timing for power-on reset and exit of "Deep Standby Mode"

Note: For detailed architecture of each power on/off sequence with reset pin, please refer to NT35532 application note.

5.8 Basic Operation Mode

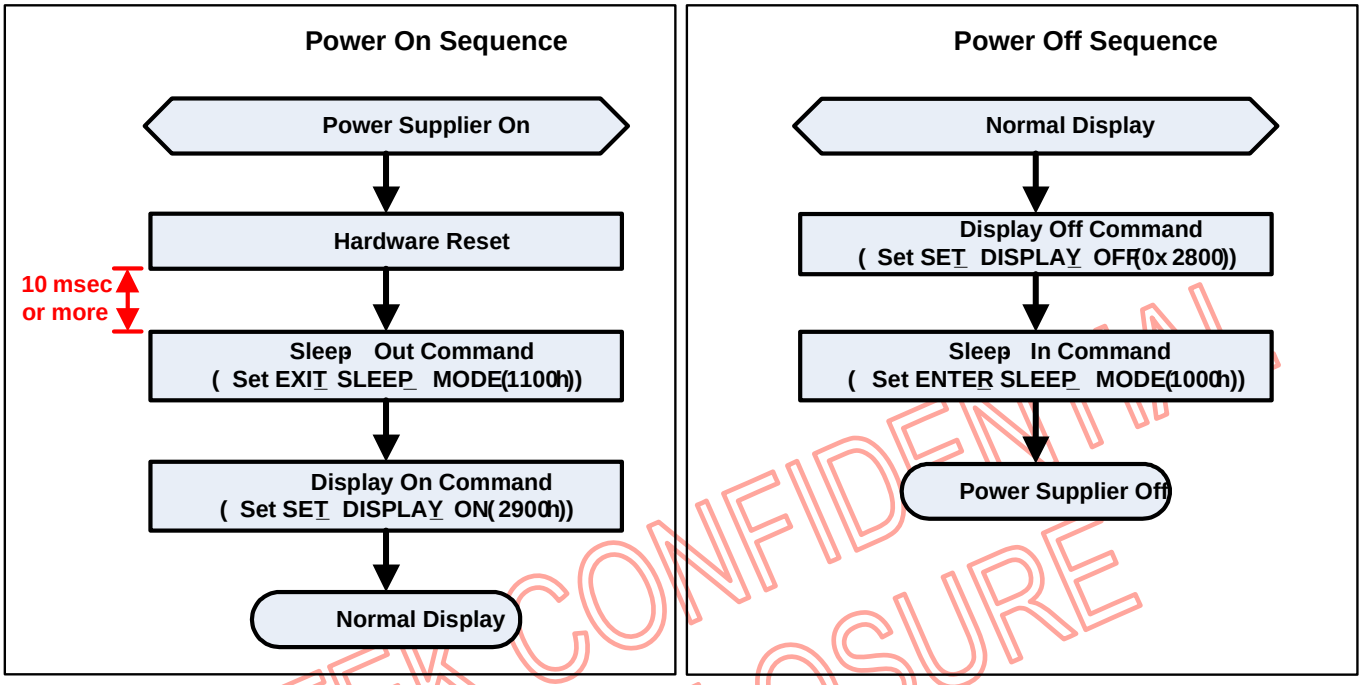
The basic operation mode of NT35532 is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in the figure.



Operation Mode Change

5.9 Power On/Off Sequence

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.

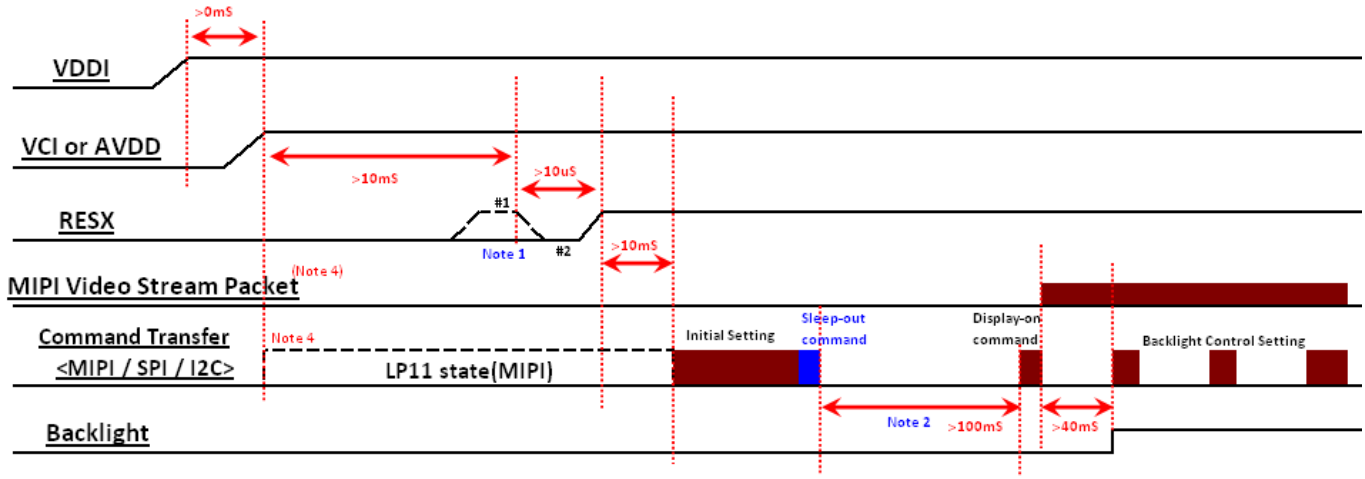


Power Supply Setting Sequence

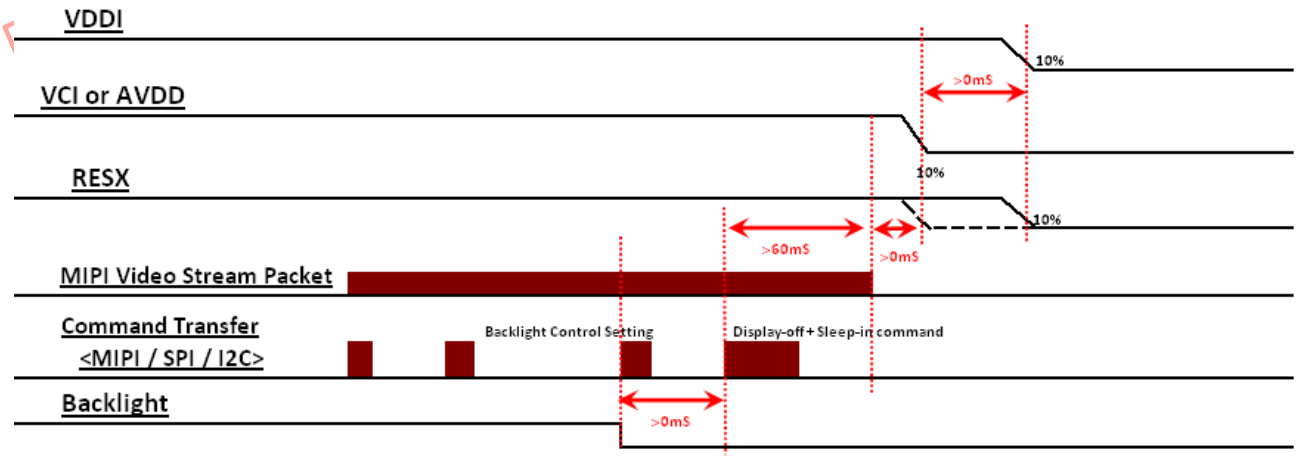
Note: If user wants to change the a-Si timing, frame rate, porch settings, it would be necessary to delay 6 frames or more after sleep out command.

5.9.1 Power Supply On/Off setting sequence

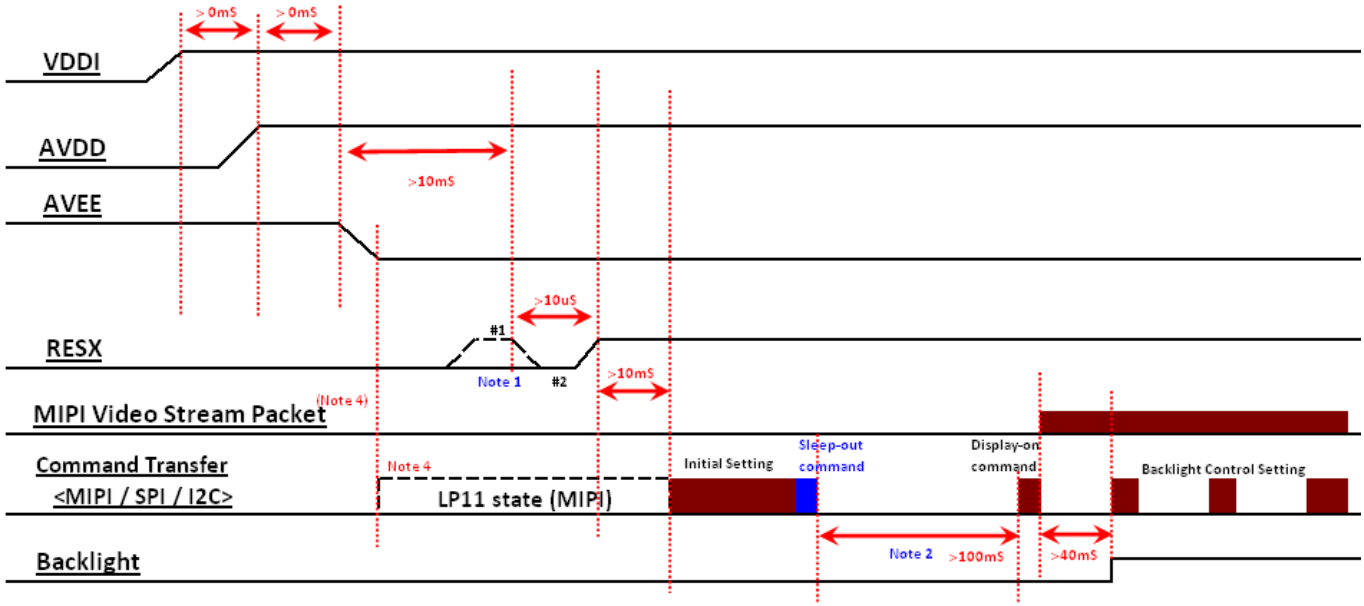
5.9.1.1 {ENPWRP, ENPWRN} = 00b or 10b (two power (VDDI/VCI or VDDI/AVDD) input)



Note 1: The RESX waveform #1 is better than #2
Note 2: After Sleep-Out Command, Driver IC will reload MTP registers and do internal power on action.
Therefore, any initial settings by MIPI, SPI or I2C should be set after Sleep-Out command
with minimum delay time 100mS.
Note 3: For detailed panel-related power sequence, please refer to NT35532 Application Notes.
Note 4: When use MIPI I/F, MIPI Lanes must go to LP11 after Power VCI or AVDD is ready



5.9.1.2 {ENPWRP, ENPWRN} = 11b and EN4PWR=0 (three power (VDDI/AVDD/AVEE) input)

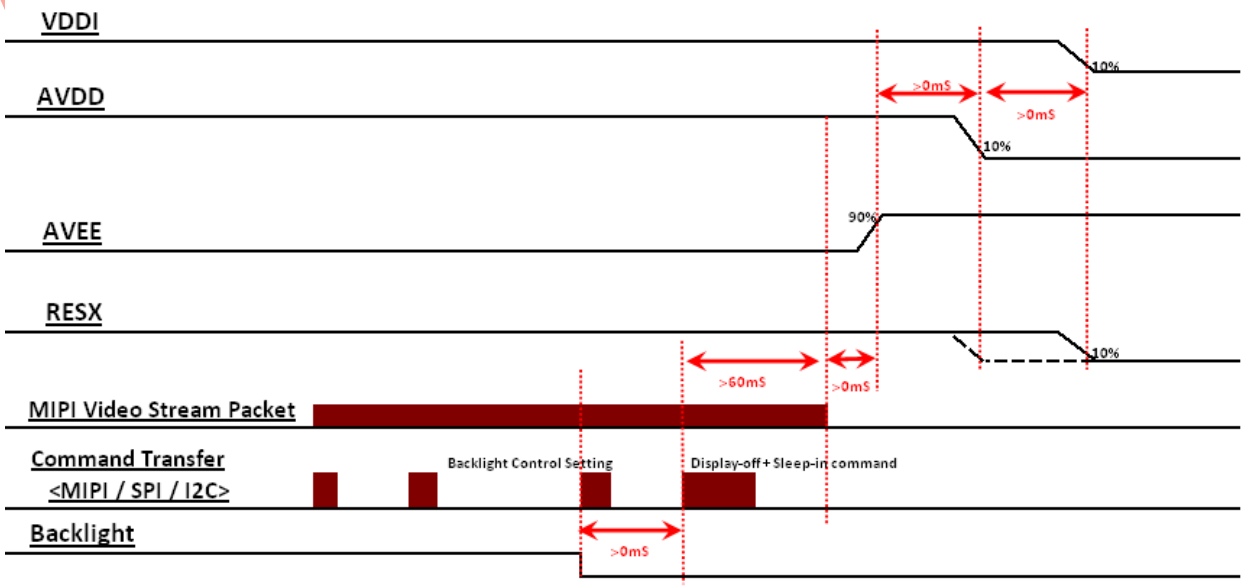


Note 1: The RESX waveform #1 is better than #2

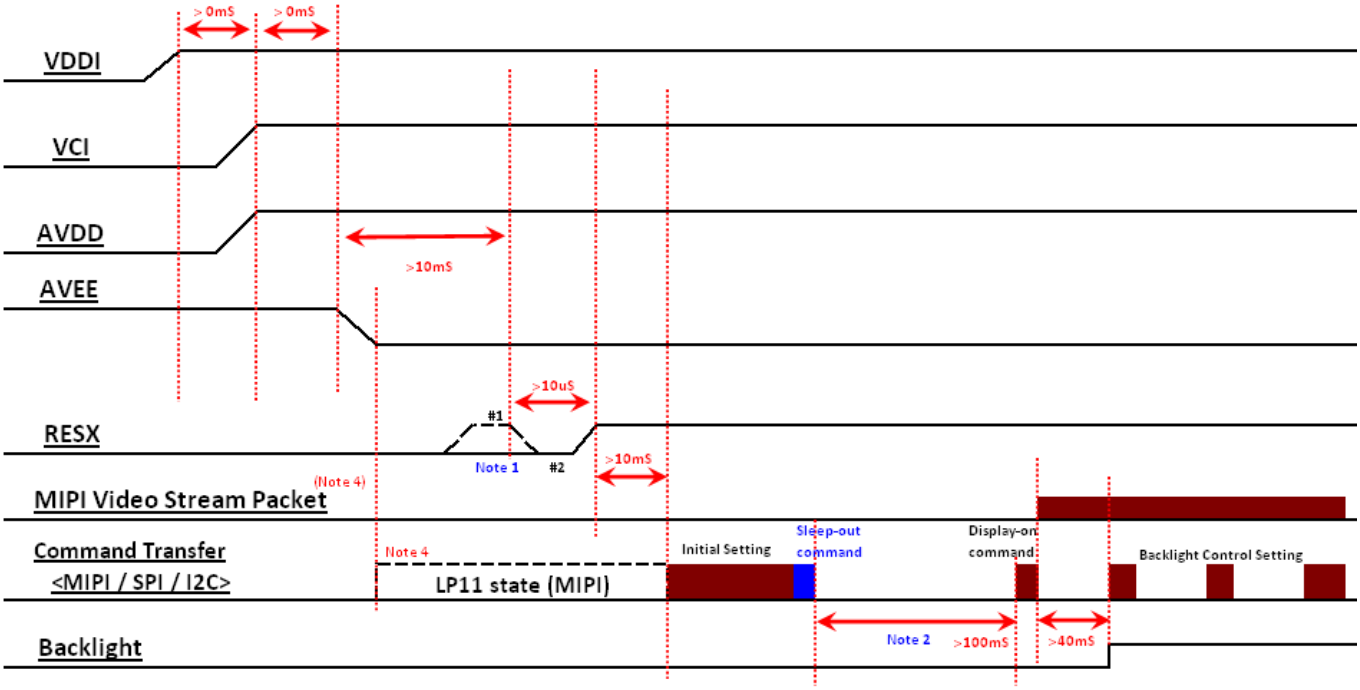
Note 2: After Sleep-Out Command, Driver IC will reload MTP registers and do internal power on action.
Therefore, any initial settings by MIPI, SPI or I2C should be set after Sleep-Out command
with minimum delay time 100mS.

Note 3: For detailed panel-related power sequence, please refer to NT35532 Application Notes.

Note 4: When use MIPI I/F, MIPI Lanes must go to LP11 after Power AVEE is ready



5.9.1.3 {ENPWRP, ENPWRN} = 11b and EN4PWR=1 (four power (VDDI/VCI/AVDD/AVEE) input)

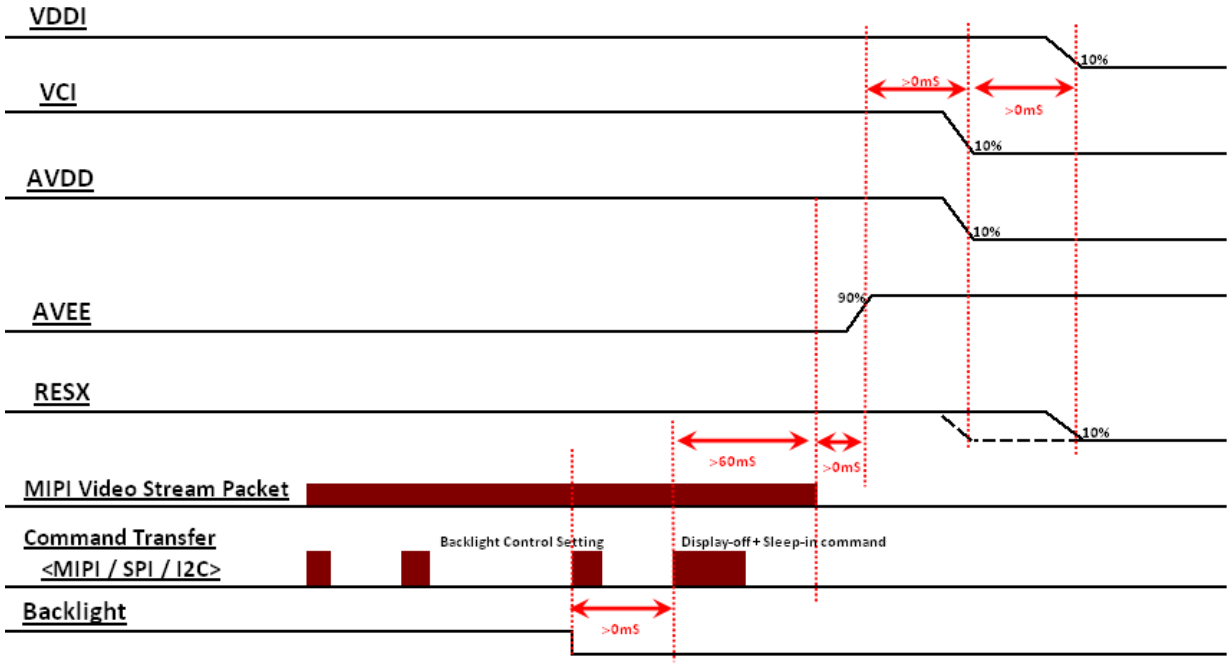


Note 1: The RESX waveform #1 is better than #2

Note 2: After Sleep-Out Command, Driver IC will reload MTP registers and do internal power on action.
Therefore, any initial settings by MIPI, SPI or I2C should be set after Sleep-Out command
with minimum delay time 100mS.

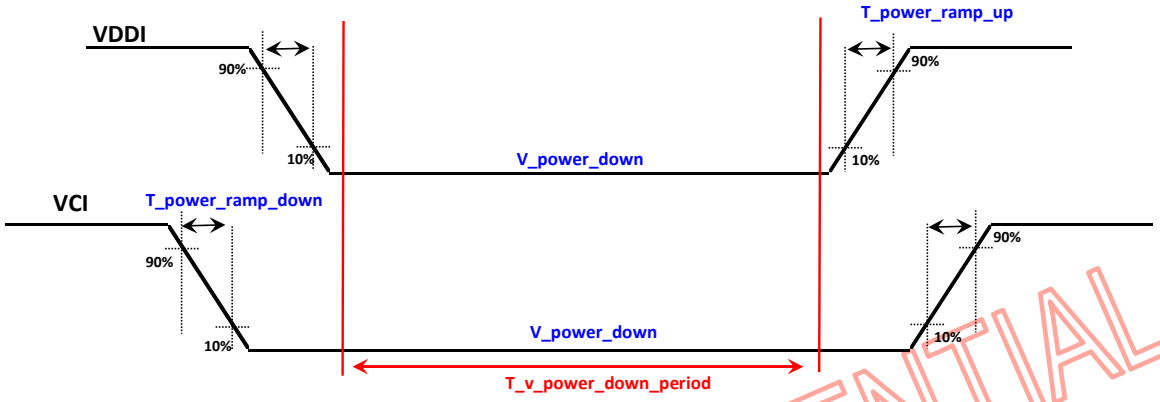
Note 3: For detailed panel-related power sequence, please refer to NT35532 Application Notes.

Note 4: When use MIPI I/F, MIPI Lanes must go to LP11 after Power AVEE is ready



5.9.2 Power Ramp-up/down SPEC

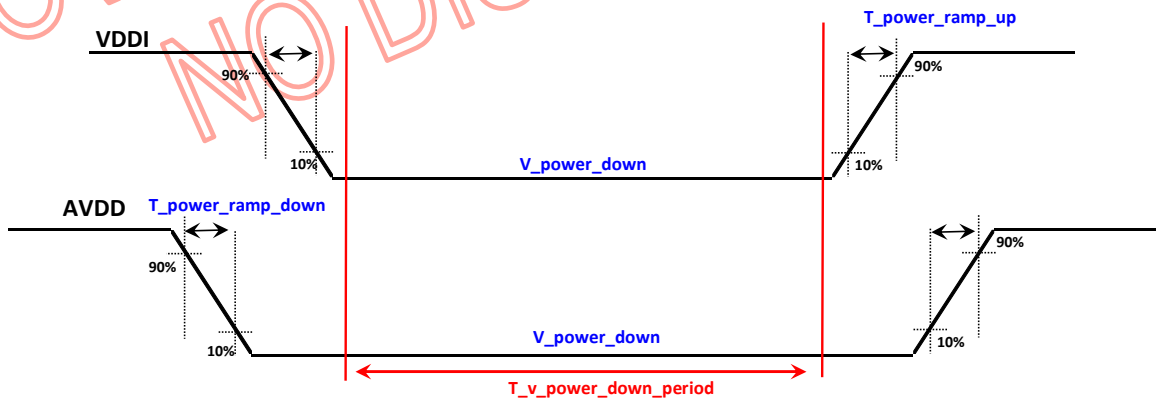
5.9.2.1 Two Input Power (VCI / VDDI)



	Min.	Typ.	Max.
Tpower_ramp_up (10% - 90%) for VDDI			2ms
Tpower_ramp_up (10% - 90%) for VCI	1ms		5ms
Tpower_ramp_down (90% - 10%) for VDDI			2ms
Tpower_ramp_down (90% - 10%) for VCI	1ms		5ms
T_v_power_down_period	10ms		
V_power_down			100mV

Note: For detailed application circuit, please refer to NT35532 Application Note.

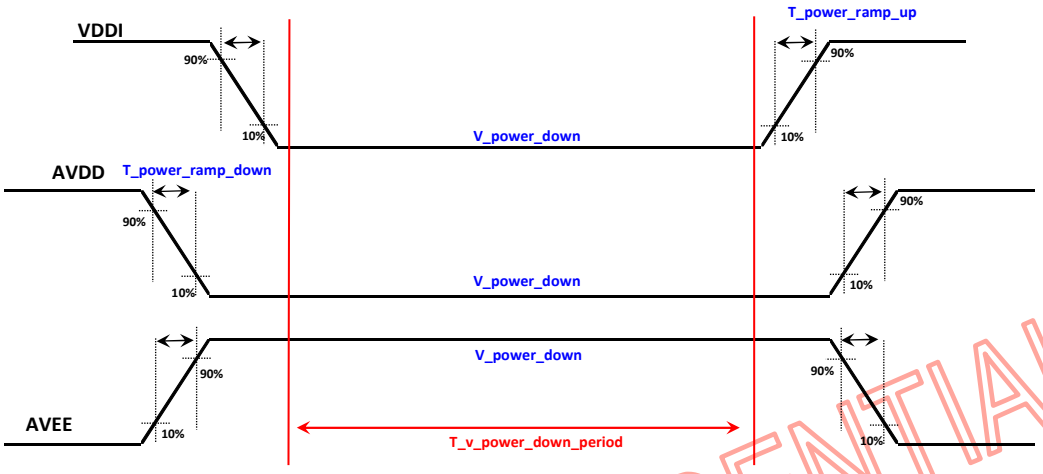
5.9.2.2 Two Input Power (VDDI / AVDD)



	Min.	Typ.	Max.
Tpower_ramp_up (10% - 90%) for VDDI			2ms
Tpower_ramp_up (10% - 90%) for AVDD	1ms		5ms
Tpower_ramp_down (90% - 10%) for VDDI			2ms
Tpower_ramp_down (90% - 10%) for AVDD	1ms		5ms
T_v_power_down_period	10ms		
V_power_down			100mV

Note: For detailed application circuit, please refer to NT35532 Application Note.

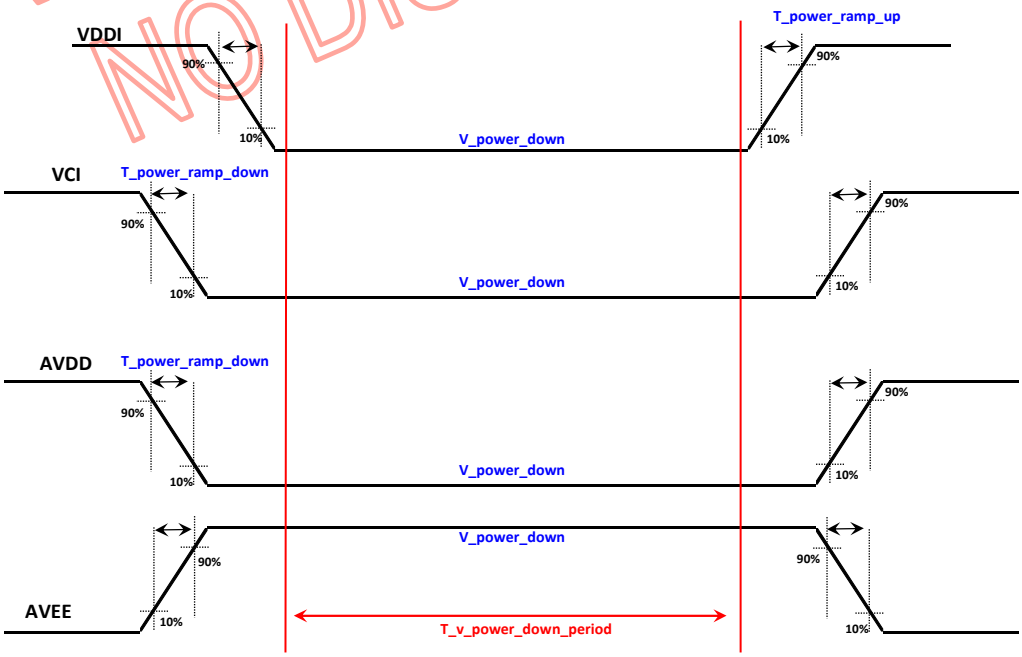
5.9.2.3 Three Input Power (VDDI / AVDD / AVEE)



	Min.	Typ.	Max.
Tpower_ramp_up (10% - 90%) for VDDI			2ms
Tpower_ramp_up (10% - 90%) for AVDD / AVEE	1ms		5ms
Tpower_ramp_down (90% - 10%) for VDDI			2ms
Tpower_ramp_down (90% - 10%) for AVDD / AVEE	1ms		5ms
T_v_power_down_period	10ms		
V_power_down			100mV

Note: For detailed application circuit, please refer to NT35532 Application Note.

5.9.2.4 Four Input Power (VDDI / VCI / AVDD / AVEE)



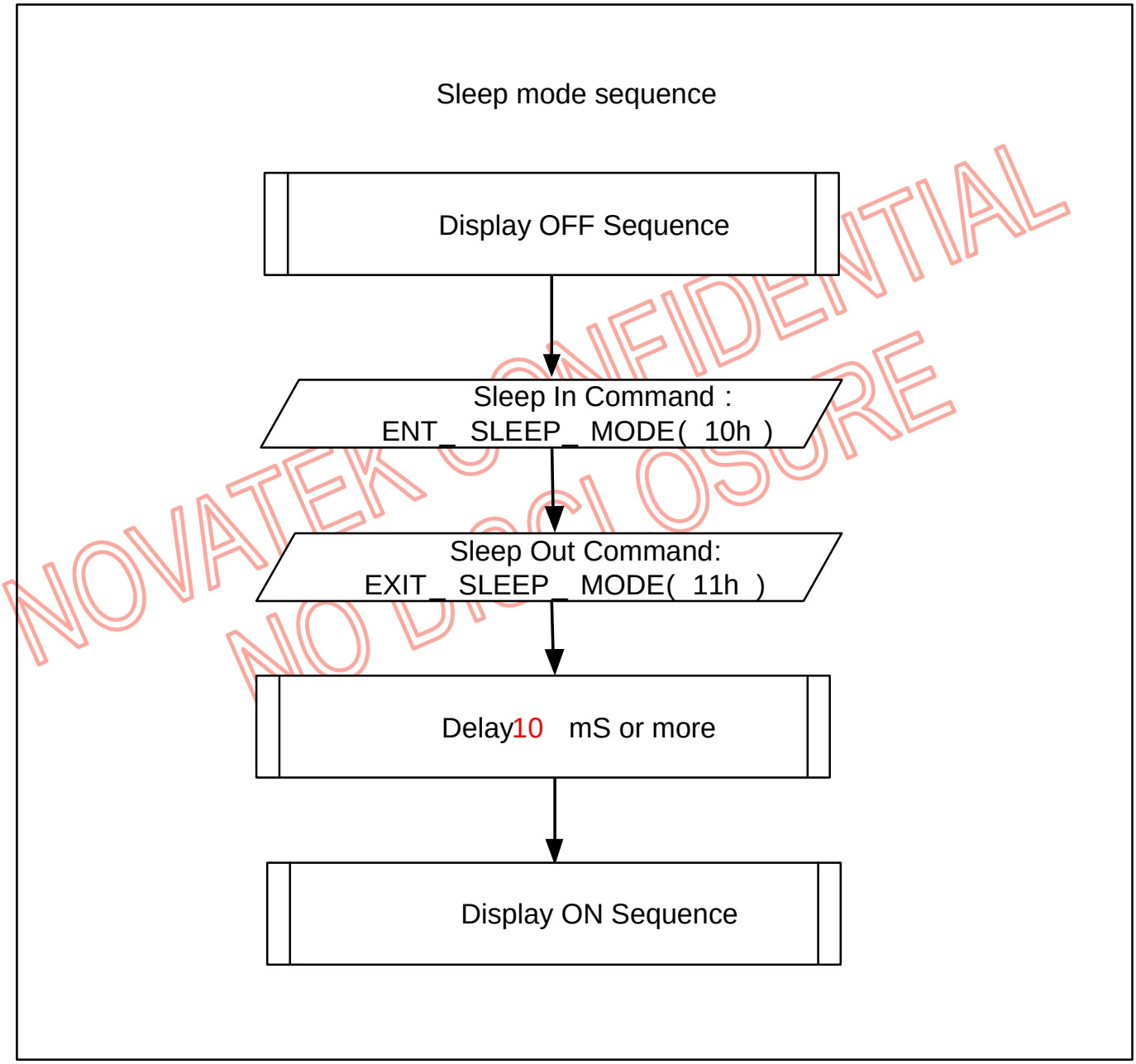
	Min.	Typ.	Max.
Tpower_ramp_up (10% - 90%) for VDDI			2ms
Tpower_ramp_up (10% - 90%) for AVDD / VCI / AVEE	1ms		5ms
Tpower_ramp_down (90% - 10%) for VDDI			2ms
Tpower_ramp_down (90% - 10%) for AVDD / VCI / AVEE	1ms		5ms
T_v_power_down_period	10ms		
V_power_down			100mV

Note: For detailed application circuit, please refer to NT35532 Application Note.

5.10 Instruction Setting Sequence

When setting instruction to the NT35532, the sequences shown in below figures must be followed to complete the instruction setting.

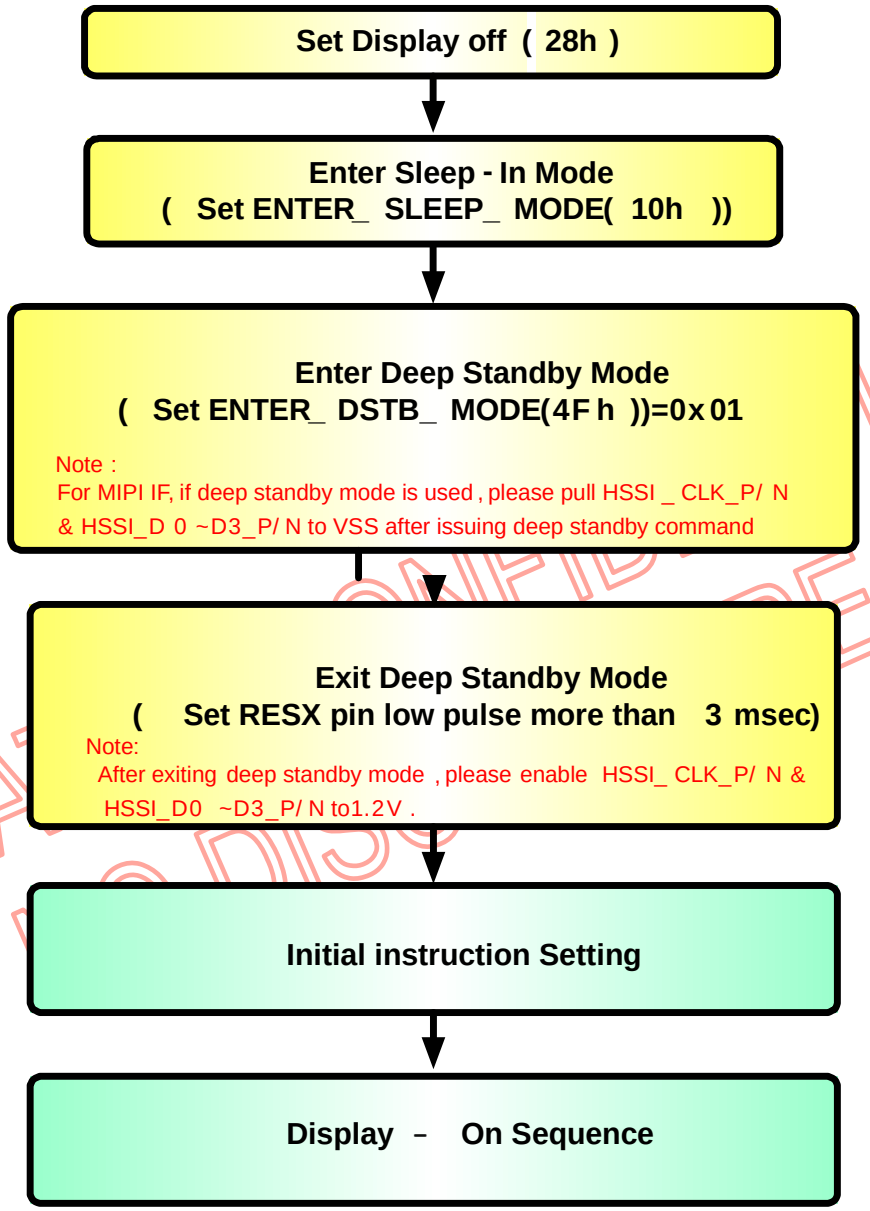
5.10.1 Sleep SET/EXIT Sequences



Sleep SET/EXIT Sequences

Note: If user wants to change the a-Si timing, frame rate, porch settings, it would be necessary to delay 6 frames or more after sleep out command.

5.10.2 Deep Standby Mode ENTER/EXIT Sequences



Deep Standby Mode ENTER/EXIT Sequences

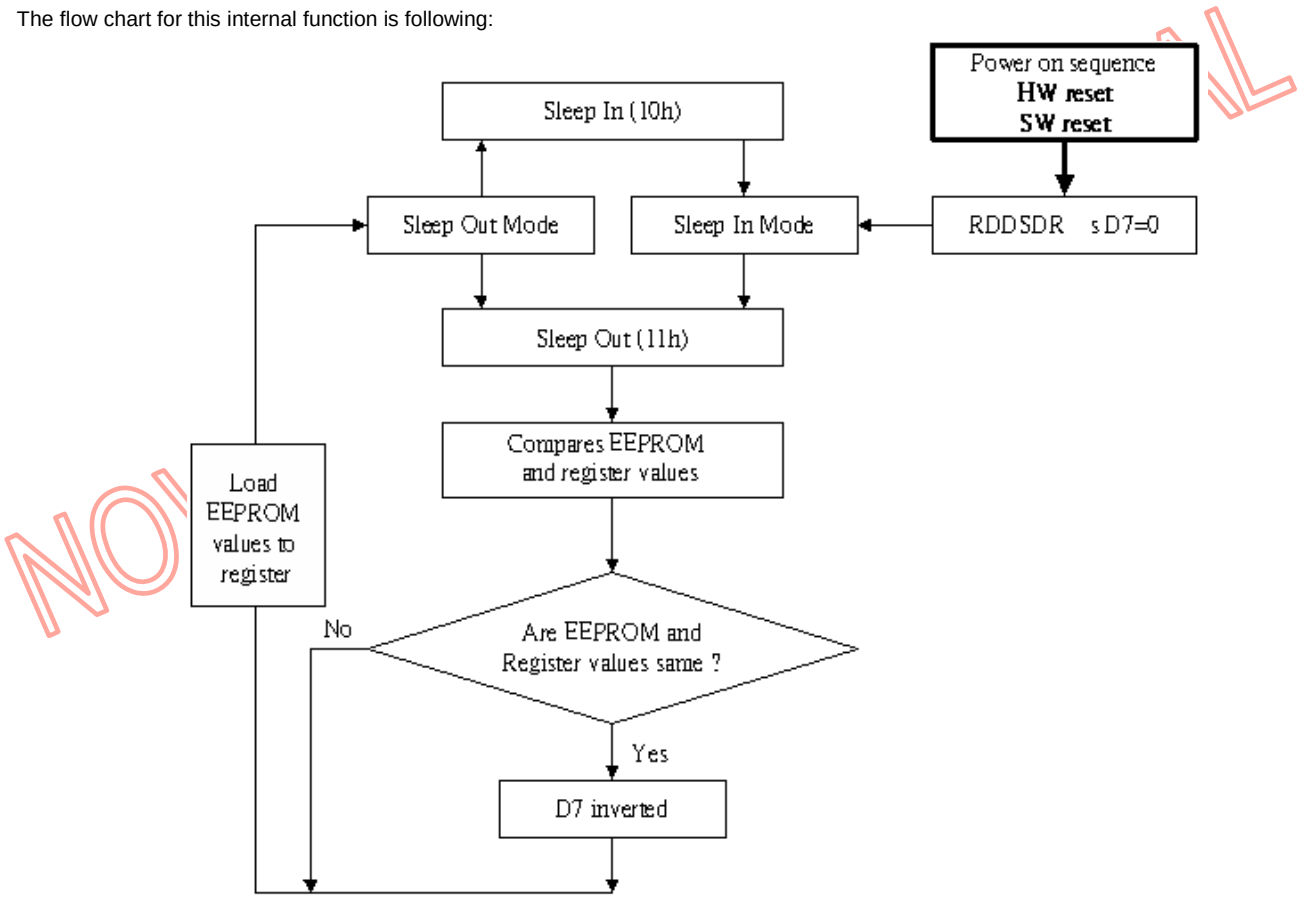
5.11 SLEEP OUT-COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE

5.11.1 Register Loading Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



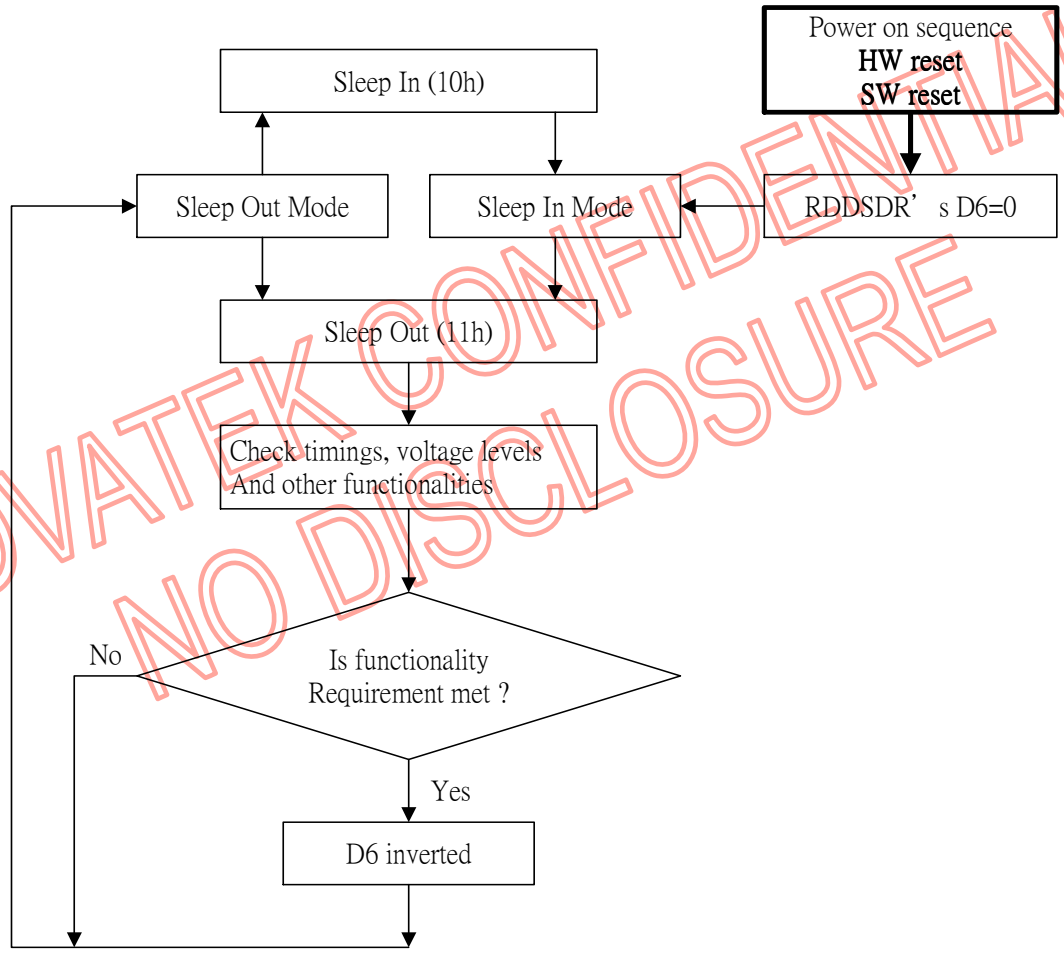
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

5.11.2 Functionality Detection

Sleep Out-command (See "Sleep Out (11h)" is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

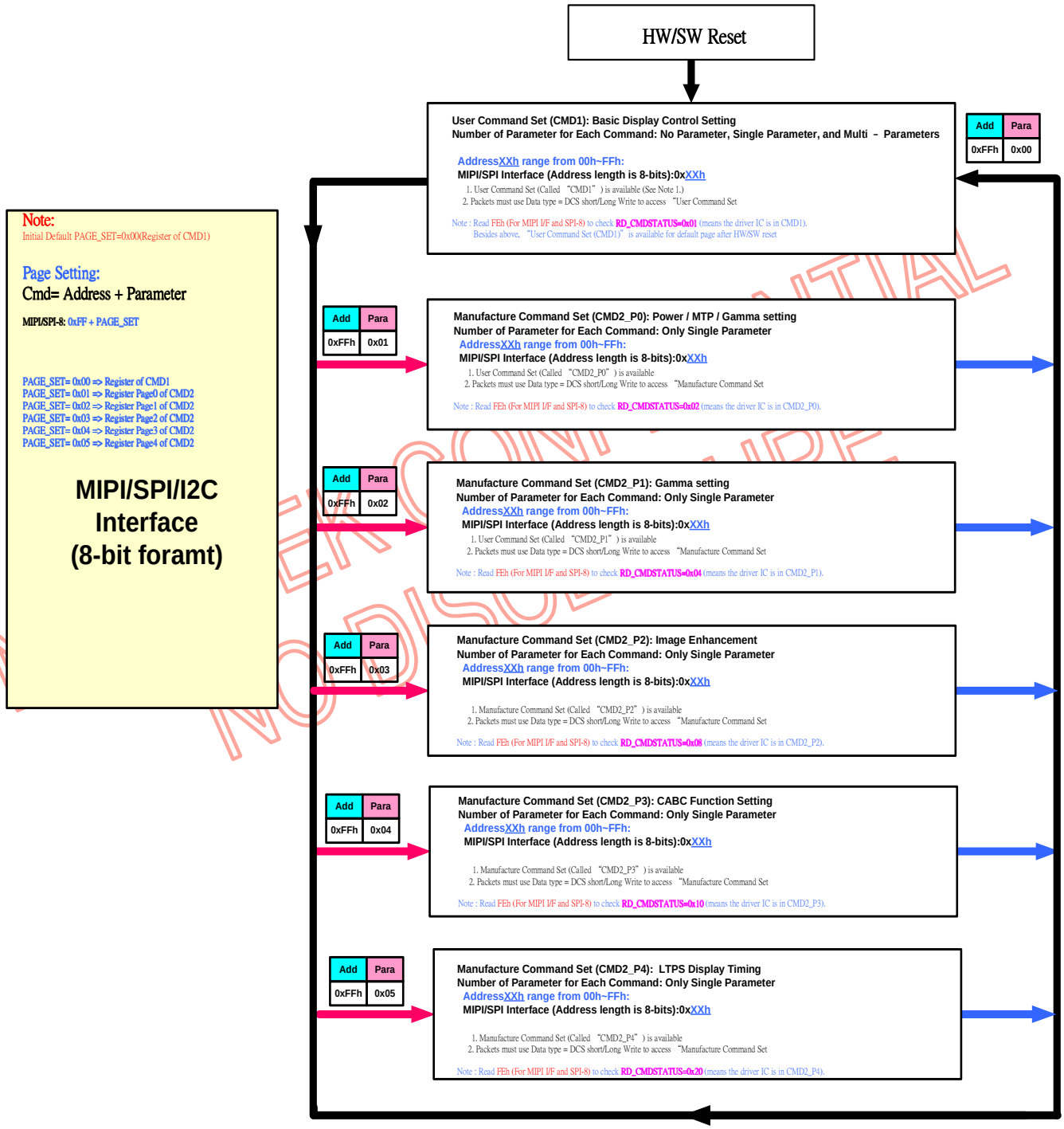
The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

6. Command Descriptions

MIPI/SPI/I2C Interface Application



Working Flow for Accessing Registers in CMD1 / CMD2 for MIPI/SPI/I2C interface.

Note: At MIPI interface, the page setting command must be sent by single packet transmission, or insert 1us delay after page setting command.

The address mapping of registers for these 2 command sets is summarized as table below:

User Command Set (CMD1)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS Short Write, No Parameter	Address	XXh	Address	XX00h
XXh + 1 Parameter	DCS Short Write, 1 Parameter	Address	XXh	Address	XX00h
		Parameter	PA1h	Parameter	PA1h
XXh + 2 Parameters	DCS LongWrite with 2 Parameters	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
				Parameter 2	PA2h
XXh + n Parameters (n > 2)	DCS Long Write with n Parameters	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
		Parameter 3	PA3h	Parameter2	PA2h
		:	:	Address	XX02h
		:	:	Parameter3	PA3h
		Parameter n-th	PAnh	Address	XX03h
				Parameter4	PA4h
				:	:
				:	:
				Address	XXXnh
				Parameter n	PAnh

Note: CMD1 is for Basic Display Control Setting use only

Manufacture Command Set (Register Page 0 of CMD2)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	**DCS Short Write, No Parameter**	Address	XXh	Address	XX40h
XXh + 1 Parameter	**DCS Short Write, 1 Parameter**	Address	XXh	Address	XX40h
		Parameter	PA1h	Parameter	PA1h

Note: Page0 of CMD2 is for Power / MTP / Gamma setting use only

Manufacture Command Set (Register Page 1 of CMD2)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS Short Write, No Parameter	Address	XXh	Address	XX50h
XXh + 1 Parameter	DCS Short Write, 1 Parameter	Address	XXh	Address	XX50h
		Parameter	PA1h	Parameter	PA1h

Note: Page1 of CMD2 is for Gamma setting use only

Manufacture Command Set (Register Page 3 of CMD2)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS Short Write, No Parameter	Address	XXh	Address	XX60h
XXh + 1 Parameter	DCS Short Write, 1 Parameter	Address	XXh	Address	XX60h
		Parameter	PA1h	Parameter	PA1h

Note: Page2 of CMD2 is for Image Enhancement use only

Manufacture Command Set (Register Page 3 of CMD2)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS Short Write, No Parameter	Address	XXh	Address	XX70h
XXh + 1 Parameter	DCS Short Write, 1 Parameter	Address	XXh	Address	XX70h
		Parameter	PA1h	Parameter	PA1h

Note: Page3 of CMD2 is for CABC Function Setting use only

Manufacture Command Set (Register Page 4 of CMD2)					
Command Table	MIPI / SPI / I2C			CPU (For Test Mode)	
	Data Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS Short Write, No Parameter	Address	XXh	Address	XX80h
XXh + 1 Parameter	DCS Short Write, 1 Parameter	Address	XXh	Address	XX80h
		Parameter	PA1h	Parameter	PA1h

Note: Page4 of CMD2 is for Display a-Si timing setting use only

6.1 User Command Set (Command 1)

MIPI/SPI/I2C Interface		Other I/F Address	Instruction	D7	D6	D5	D4	D3	D2	D1	D0
CMD	Parameter										
00h	-	0000h	NOP	No Argument							
01h	-	0100h	SOFT_RESET	No Argument							
04h	1st Parameter	0400h	RDID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
	2nd Parameter	0401h	RDID2	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20
	3rd Parameter	0402h	RDID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
05h	1st Parameter	0500h	RDNUMED	D[7:0]							
0Ah	1st Parameter	0A00h	GET_POWER_MODE	D7	0	0	D4	0	D2	0	0
0Bh	1st Parameter	0B00h	GET_ADDRESS_MODE	D7	D6	0	0	D3	0	0	0
0Dh	1st Parameter	0D00h	GET_DISPLAY_MODE	0	0	D5	0	0	D2	D1	D0
0Eh	1st Parameter	0E00h	GET_SIGNAL_MODE	D7	D6	0	0	0	0	0	D0
0Fh	1st Parameter	0F00h	RDDSDR	D7	D6	0	0	0	0	0	D0
10h	-	1000h	ENTER_SLEEP_MODE	No Argument							
11h	-	1100h	EXIT_SLEEP_MODE	No Argument							
20h	-	2000h	EXIT_INVERT_MODE	No Argument							
21h	-	2100h	ENTER_INVERT_MODE	No Argument							
26h	1st Parameter	2600h	GAMSET	GC[7:0]							
28h	-	2800h	SET_DISPLAY_OFF	No Argument							
29h	-	2900h	SET_DISPLAY_ON	No Argument							
34h	-	3400h	SET_TEAR_OFF	No Argument							
35h	1st Parameter	3500h	SET_TEAR_ON	TEW3	TEW2	TEW1	TEW0	0	0	TEP	M
36h	1st Parameter	3600h	SET_ADDRESS_MODE	SD_MY	SD_MX	0	0	RGB	0	0	0
3Ah	1st Paramete	3A00h	SET_PIXEL_FORMAT	0	0	0	0	0	IFPF2	IFPF1	IFPF0
44h	1st Parameter	4400h	SET_TEAR_SCANLINE	0	0	0	0	0	N10	N9	N8
45h	1st Parameter	4500h		N7	N6	N5	N4	N3	N2	N1	N0
46h	1st Parameter	4500h	RDSCL	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8
	2nd Parameter	4501h		SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
4Fh	1st Parameter	4F00h	ENTER_DSTB_MODE	0	0	0	0	0	0	0	DSTB
51h	1st Parameter	5100h	WRDISBV	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
52h	1st Parameter	5200h	RDDISBV	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
53h	1st Parameter	5300h	WRCTRLD	HBM[1:0]		BCTRL	0	DD	BL	0	0
54h	1st Parameter	5400h	RDCTRLD	HBM[1:0]		BCTRL	0	DD	BL	DB	G
55h	1st parameter	5500h	WR PWR SAVE	IMAGE_ENHANCEMENT [3:0]				0	0	CABC_COND[1:0]	
56h	1st parameter	5600h	RDPWR SAVE	IMAGE_ENHANCEMENT [3:0]				0	0	CABC_COND[1:0]	

5Eh	1st Parameter	5E00h	WRCABCMB	CMB[7 : 0]							
5Fh	1st Parameter	5F00h	RDCABCMB	CMB[7 : 0]							
A1h	1st Parameter	A100h	RDDDBS	SID[7 : 0]: LSB of Supplier ID							
	2nd Parameter	A101h		SID[15: 8]: MSB of Supplier ID							
	3rd Parameter	A102h		MID[7 : 0]: LSB of Model Number ID							
	4th Parameter	A103h		MID[15 : 8]: MSB of Model Number ID							
	5th Parameter	A104h		RID[7 : 0]: LSB of Revision ID							
	6th Parameter	A105h		RID[15 : 8]: MSB of Revision ID							
	7th Parameter	A106h		1	1	1	1	1	1	1	1
A8h	1st Parameter	A800h	RDDDBC	SID[7 : 0]: LSB of Supplier ID							
	2nd Parameter	A801h		SID[15: 8]: MSB of Supplier ID							
	3rd Parameter	A802h		MID[7 : 0]: LSB of Model Number ID							
	4th Parameter	A803h		MID[15 : 8]: MSB of Model Number ID							
	5th Parameter	A804h		RID[7 : 0]: LSB of Revision ID							
	6th Parameter	A805h		RID[15 : 8]: MSB of Revision ID							
	7th Parameter	A806h		1	1	1	1	1	1	1	1
AAh	1st Parameter	AA00h	RDFCS	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0
ABh	1st Parameter	AB00h	MIPI Error Report	AWER15	AWER14	AWER13	AWER12	AWER11	AWER10	AWER9	AWER8
	2nd Parameter	AB01h		AWER7	AWER6	AWER5	AWER4	AWER3	AWER2	AWER1	AWER0
ACh	1st Parameter	AC00h	DCS Long Write Payload Counter	LPa15	LPa14	LPa13	LPa12	LPa11	LPa10	LPa9	LPa8
	2nd Parameter	AC01h		LPa7	LPa6	LPa5	LPa4	LPa3	LPa2	LPa1	LPa0
AEh	1st Parameter	AE00h	STB EDGE POSITION	STB_EDGE_SEL[7:0]							
AFh	1st Parameter	AF00h	RDCCS	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0
BAh	1st Parameter	BA00h	SET_MIPI_LANE	mipi_ecc_disable	mipi_crc_disable	DSI_MODE[1:0]		0	0	DSI_LANE[1:0]	
D2h	1st Parameter	D200h	RGBCTRL	0	CRCM	0	0	DP	EP	HSP	VSP
D3h	1st Parameter	D300h	RGBMIPICTRL	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
D4h	1st Parameter	D400h		VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0
D5h	1st Parameter	D500h		HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
D6h	1st Parameter	D600h		HFP6	HFP6	HFP5	HFP4	HFP3	HFP2	HFP1	HFP0
D7h	1st Parameter	D700h		0	0	0	0	0	0	HBP8	HFP8
D9h	1st Parameter	D900h	EXCK_CTRL	0	0	EXTOSCDIV[2:0]		0	0	EXTOSC_SEL[1:0]	
DAh	1st Parameter	DA00h	RDID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
DBh	1st Parameter	DB00h	RDID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
DCh	1st Parameter	DC00h	RDID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
E1h	1st Parameter	E100h	Write	0	0	0	0	0	0	IDLE_ON_S	IDLE_MODE

			IDLEMODE_BL_Control							IGNAL_EN	_BL_EN
E2h	1st Parameter	E200h	Read IDLEMODE_BL_Control	0	0	0	0	0	0	IDLE_ON_S IGNAL_EN	IDLE_MODE _BL_EN
F3h	1st Parameter	F300h	MULTIIF	IM_IF_SEL	0	0	0	SECOND_IF_SEL[1:0]		0	MULTIIF_EN
F4h	1st Parameter	F400h	Novatek ID	0	0	1	1	0	0	1	0
F5h	1st Parameter	F500h	IF_TEST	IF_TEST[7:0]							
F6h	1st Parameter	F600h	EXCK_CTRL	EXCK_FREQ[11:8]				0	0	0	EN_EXCK
F7h	1st Parameter	F700h		EXCK_FREQ[7:0]							
F8h	1st Paramete	F900h	I2C_SLAVE_ADDR	0	I2C_SLAVE_ADDR[1:0]						
F9h	1st Paramete	FA00h	PIXEL_EXTEN	0	0	0	0	0	0	PIXEL_EXTEN[1:0]	
FBh	1st Parameter	FB00h	Reload CMD1	0	0	0	0	0	0	0	Reload_ CMD1
FEh	-	FE00h	RD_CMDSTATUS	0	0	CMD2_P4	CMD2_P3	CMD2_P2	CMD2_P1	CMD2_P0	CMD1
FFh	-	FF00h	CMD Page Select	PAGE_SEL[7:0]							

(00h) NOP: No Operation

Address	00h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								N/A

Description	- This command performs no operation and is ignored by the device.
Restriction	-
Register Availability	
Default Value	N/A

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

(01h) SOFT_RESET: Software Reset

Address	01h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								N/A

Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset register values and all source & gate outputs are set to GND (display off).
Restriction	(1) It will be necessary to wait 20msec before sending new command following software reset. (2) The display module loads all display suppliers' factory default values to the registers during 8 msec. (3) If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120 msec before sending Sleep- Out command. (4) Software reset command cannot be sent during Sleep Out sequence.
Register Availability	
Default Value	N/A

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

(04h) RDID: Read Display ID

Address	04h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	N/A
Parameter 2	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	N/A
Parameter 3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	N/A

Description

- This read byte returns display identification information.

The 1st parameter (ID17 to ID10)：LCD module's manufacturer ID.
The 2nd parameter (ID26 to ID20)：LCD module/driver version ID.

It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value	Version	Change
8'h80	Version1	:
8'h81	Version2	:
8'h82	Version3	:

The 3rd parameter (ID37 to ID30)：LCD module/driver ID.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value		
	04h-1st	04h-2nd	04h-3rd
Power On Sequence	N/A	N/A	N/A
S/W Reset	N/A	N/A	N/A
H/W Reset	N/A	N/A	N/A

(05h) RDNUMED: Read Number of the Error on DSI

Address	05h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description

- The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is explained in below.

D[6 : 0] bits are telling a number of the errors.

D[7] is set to '1' if there is overflow with P[6 : 0] bits.

D[7 : 0] bits are set to '0's (as well as GET_SIGNAL_MODE (0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed).

Please also refer to the sections: "Acknowledge with Error Report (AwER)" and "Read Display Signal Mode (0Eh)".

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(0Ah) GET_POWER_MODE: Read Display Power Mode

Address	0Ah				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	D7	0	0	D4	1	D2	0	0	08h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	“1”=Booster on, “0”=Booster off
D6	Reserved	“0” (Not used)
D5	Reserved	“0” (Not used)
D4	Sleep In/Out	“1” = Sleep Out, “0” = Sleep In
D3	Reserved	“1” (Not used)
D2	Display On/Off	“1” = Display On, “0” = Display Off
D1	Reserved	“0” (Not used)
D0	Reserved	“0” (Not used)

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

(0Bh) GET_ADDRESS_MODE: Get the Display Panel Read Order

Address	0Bh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	D7	D6	0	0	D3	0	0	0	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scan Direction (SD_MY)	“1”=Decrement (MY = 1), “0”=Increment (SD_MY = 0)
D6	Horizontal Scan Direction (SD_MX)	“1”=Decrement (MX = 1), “0”=Increment (SD_MX = 0)
D5	Reserved	“0” (Not used)
D4	Reserved	“0” (Not used)
D3	RGB/BGR Order	“1”=BGR (register bit RGB of register 0x36 is “1”) “0”=RGB (register bit RGB of register 0x36 is “0”)
D2	Reserved	“0” (Not used)
D1	Reserved	“0” (Not used)
D0	Reserved	“0” (Not used)

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(0Dh) GET_DISPLAY_MODE: Read the Current Display Mode

Address	0Dh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	D5	0	0	D2	D1	D0	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Reserved	“0” (Not used)
D6	Reserved	“0” (Not used)
D5	Inversion On/Off	“0” = Inversion is Off, “1” = Inversion is On
D4	Reserved	“0” (Not used)
D3	Reserved	“0” (Not used)
D[2 : 0]	Gamma Curve Selection	See table below

D2	D1	D0	Gamma Curves Selection (Based on Register 26h Setting)
0	0	0	Gamma 2.2
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
Others			Reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(0Eh) GET_SIGNAL_MODE: Get Display Module Signaling Mode

Address	0Eh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	D7	D6	0	0	0	0	0	D0	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Frame Tearing Effect Line On/Off	“1” = On, “0” = Off
D6	Tearing Effect Line Output Mode	“1” = Mode B, “0” = Mode A
D5	Reserved	“0” (Not used)
D4	Reserved	“0” (Not used)
D3	Reserved	“0” (Not used)
D2	Reserved	“0” (Not used)
D1	Reserved	“0” (Not used)
D0	Error on DSI	“1” = Error, “0” = No Error

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(0Fh) RDDSDR: Read Display Self-Diagnostic Result

Address	0Fh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	D7	D6	0	0	0	0	0	D0	00h

Description

- This command indicates the status of the display self-diagnostic results after Sleep Out. This command is described in the table below.

Bit	Description	Value	
D7	Register Loading Detection	See section "Register Loading Detection"	
D6	Functionality Detection	See section "Functionality Detection"	
D5	Not Used	“0” (Not used)	
D4	Not Used	“0” (Not used)	
D3	Not Used	“0” (Not used)	
D2	Not Used	“0” (Not used)	
D1	Not Used	“0” (Not used)	
D0	Checksums Compare	“1”=Checksums are not same	“0”=Checksums are same (Default)

Restriction

- It will be necessary to wait 300ms after there is the last write access on DCS area registers before there can read Bit D0 value.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(10h) ENTER_SLEEP_MODE: Enter the Sleep-In Mode

Address	10h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Sleep-In Mode

Description	- This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received.
Restriction	- This command has no effect when the display module is already in Sleep Mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	Sleep-In
S/W Reset	Sleep-In
H/W Reset	Sleep-In

(11h) EXIT_SLEEP_MODE: Exit the Sleep-In Mode

Address	11h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Sleep-In Mode

Description	- This command initiates the power-up sequence. The Sleep Out profile will be executed when this command is received. The Sleep Out will re-load register value. It will be necessary to delay 10 ms or more before sending next command.
Restriction	- This command will not cause any visible effect on the display when the display is not in Sleep Mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	Sleep-In
S/W Reset	Sleep-In
H/W Reset	Sleep-In

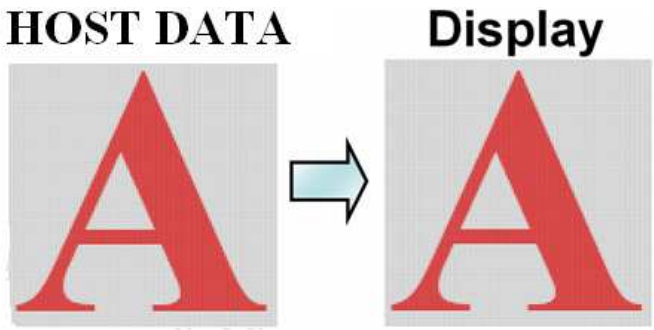
(20h) EXIT_INVERT_MODE: Display Inversion Off

Address	20h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Inversion Off

Description

- This command is used to keep image from host to display and does not change any other status.

Example:



Restriction

- This command has no effect when the module is already in inversion off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

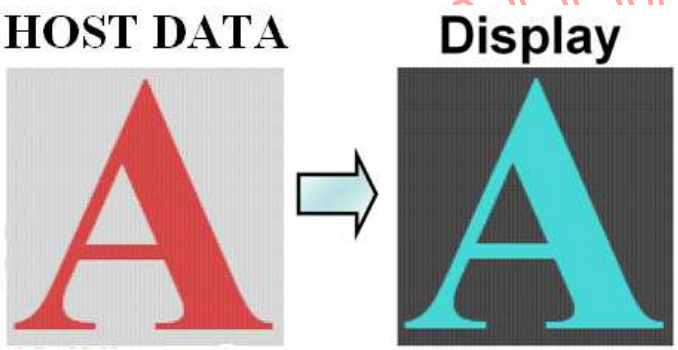
(21h) ENTER_INVERT_MODE: Display Inversion On

Address	21h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Inversion Off

Description

- This command is used to enter display Inversion mode, makes no change of contents of frame memory, and does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

Example:



Restriction

- This command has no effect when the module is already in inversion off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

(26h) GMASET: Gamma Curves Selection

Address	26h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

Description

- This command is used to select the desired Gamma curve for the current display. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7 : 0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (Gamma 2.2)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Restriction

- Values of GC[7 : 0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.
- When register GMASET (26h) is changed, user should not access gamma registers within 20msec because internal circuit needs some time for gamma curve switch.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

(28h) SET_DISPLAY_OFF: Display Off

Address	28h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Display Off

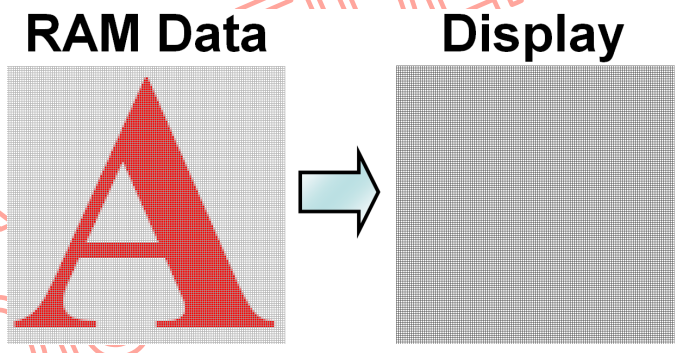
Description

- This command is used to enter to the DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page is inserted.

This command makes no change of contents of frame memory, and does not change any other status.

There will be no abnormal visible effects on the display. Exit from this command by the Display On command (29h)

Example:



Restriction

- This command has no effect when the module is already in Display Off mode.

Register Availability

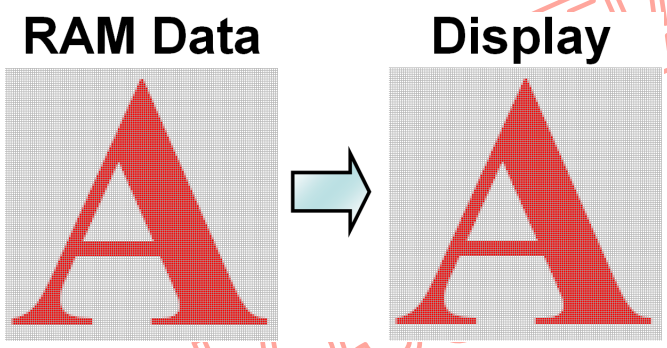
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

(29h) SET_DISPLAY_ON: Display On

Address	29h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								Display Off

Description	- This command is used to recover from the DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory, and does not change any other status. **Example:** 
Restriction	- This command has no effect when the module is already in Display On mode
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: N.A. Partial Mode On, Idle Mode Off, Sleep Out: N.A. Partial Mode On, Idle Mode On, Sleep Out: N.A. Sleep In: Yes
Default Value	Status / Default Status: Power On Sequence: Display Off S/W Reset: Display Off H/W Reset: Display Off

(34h) SET_TEAR_OFF: Tearing Effect Line OFF

Address	34h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	No Argument								TE Line Off

Description	- This command is used to turn OFF (Active Low) the output TE trigger message from the display module.
Restriction	- This command has no effect when TE is already OFF.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Status
Power On Sequence	TE Line Off
S/W Reset	TE Line Off
H/W Reset	TE Line Off

(35h) SET_TEAR_ON: Tearing Effect Line ON

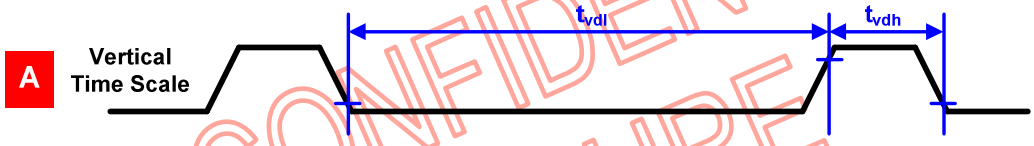
Address	35h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	TEW3	TEW2	TEW1	TEW0	0	0	TEP	M	00h

Description

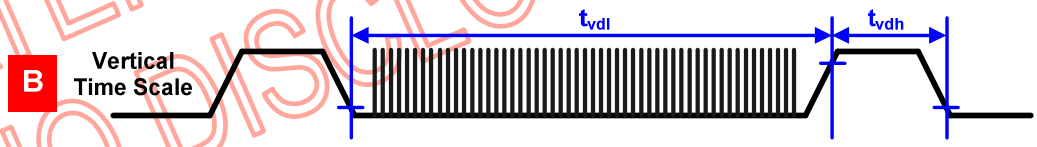
- This command is used to turn ON the Tearing Effect output from the TE signal. This output is not affected by changing MADCTR bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

When **M = 0**：The Tearing Effect Output line consists of V-Blanking information only.



When **M = 1**：The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.



Notes: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Register 35h & 44h both define TE Output：

R3500h	R4400h/R4500h	TE Output
M	N	
0	0	TE high in V-porch region (A)
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

This command is used to turn ON the output TE trigger message from display module.

This output is not affected by changing SET_ADDRESS_MODE bit ML.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

Description

TEP: Set the polarity of FTE signal.

0: Active High.

1: Active Low.

TEW[3 : 0]: FTE active duration selection.

TEW[3 : 0]	FTE Active Duration (Unit: Line)
0	1
1	2
2	3
:	:
:	:
15	16

Restriction

- This command has no effect when Tearing Effect output is already ON.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value	Notes
Power On Sequence	00h	TEW[3 : 0]= 0 (1 Line) TEP = 0 (Active High) M = 0(TE high in V-porch region (A))
S/W Reset	00h	
H/W Reset	00h	

(36h) SET_DIRECTION_MODE: Data Direction Access Control

Address	36h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	SD_MY	SD_MX	0	0	RGB	0	0	0	00h

Description

- This command defines write scanning direction.

This command makes no change on the other driver status.

SD_MY: To set vertical scan direction.

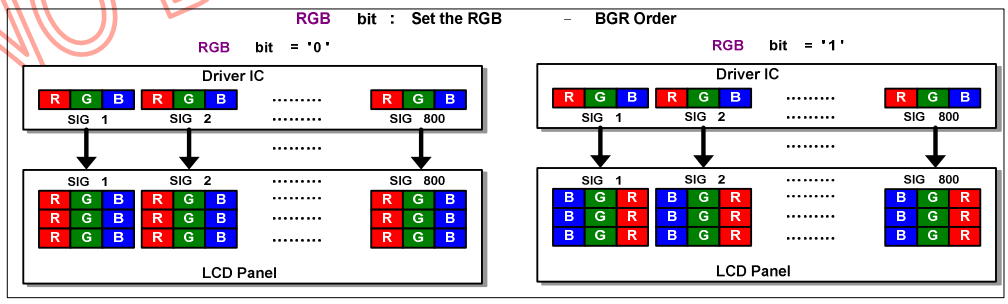
SD_MY	Function
0	**Increase in vertical**
1	Decrease in vertical

SD_MX: To set horizontal scan direction.

SD_MX	Function
0	**Increase in horizontal**
1	Decrease in horizontal

RGB: To set sub-pixel output sequence in RGB order or BGR order.

RGB	Function
0	**Write data in RGB sequence**
1	Reverse sequence from RGB to BGR



<table>
<tr><td>Restriction</td><td>- This command has no effect when Tearing Effect output is already ON.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default Value</td><td>
<table>
<tr><th>Status</th><th>Default Value</th><th>Notes</th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td rowspan="3">MY = 0 (Increase in vertical)
MX = 0 (Increase in horizon)
RGB = 0 (RGB sequence)</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

(3Ah) SET_PIXEL_FORMAT: Set the Interface Pixel Format

Address (MIPI I/F)		3Ah					Access Attribute			R/W
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	0	0	0	0	0	IFPF [2:0]			07h

Description

- This command is used to define the format of RGB picture data, which is to be transferred via the MPU Interface.

The formats are shown in the table:

IFPF[2 : 0]: Set the pixel format on MCU I/F

IFPF[2 : 0]		MCU Interface Color Format
Binary	DEC	
101	5	16-bits / pixel
110	6	18-bits / pixel
111	**7**	**24-bits / pixel**
Others are not defined.		

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default Value

Status	Default Value	Note
Power On Sequence	07h	VIPF[2 : 0] = 07h (24 bits / pixel (1-time transfer)) IFPF[2 : 0] = 07h (24-bits / pixel)
H/W Reset	07h	
S/W Reset	07h	

(44h~45h) SET_TEAR_SCANLINE: Set Tear Line

Address	44h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
44h	0	0	0	0	0	N[10:8]			00h
45h	N [7:0]								00h

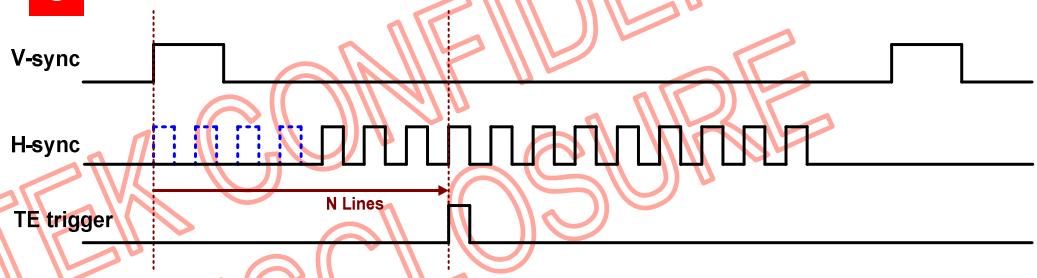
Description

- The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.

Notes 1: That TEARLINE with N = '0' is equivalent to TEON with M = '0'.

Notes 2: The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

C



Register 35h and 44h both define TE Output：

R35h	R44h/45h	TE Output
M	N	
0	**0**	**TE high in V-porch region (A)**
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

This command is used to set the FTE output position.

Use "SET_TEAR_ON (35h)" to set the FTE polarity and pulse width.

Description

N[10 : 0]	Function Description
000h	VBP Region
001h	2nd Line
002h	3rd Line
003h	4th Line
:	:
77Dh	1918th Line
77Eh	1919th Line
77Fh	1920th Line

Restriction

- This command takes affect on the frame following the current frame. Therefore, if the Tear Effect (FTE) output is already ON, the FTE output shall continue to operate as programmed by the previous SET_TEAR_ON, or SET_TEAR_SCANLINE, command until the end of the frame.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value	Note
Power On Sequence	00h	(1) N[10 : 0] = 000h: FTE outputs at 1st line. (2) Tearing effect off and M = '0'.
S/W Reset	00h	
H/W Reset	00h	

(46h) RDSCL：Read Scan Line

Address	45h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8	N/A
Parameter 2	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	N/A

Description	- This command is used to read scan line data.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value

(4Fh) ENTER_DSTB_MODE: Enter the Deep Standby Mode

Address	4Fh				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	0	0	0	0	0	DSTB	00h

Description

- This command is used to enter deep standby mode.

DSTB = '1': Enter the deep standby mode.

Note 1: It can't exit deep standby mode when set DSTB from '1' to '0'.

Note 2: User can not write this register in Sleep-Out and Display-On mode.

Note 3: To exit deep standby mode, please set RESX pin low pulse more than 3msec

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(51h) WRDISBV: Write Display Brightness

Address	51h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description

- This command is used to adjust or returns the brightness value of the display.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7：0]	PWM Duty (Ratio)	PWM Duty (%)
00h	**Off**	**0%**
01h	2 / 256	0.78125 %
02h	3 / 256	1.171875 %
03h	4 / 256	1.5625 %
:	:	:
FDh	254 / 256	99.21875 %
FEh	255 / 256	99.609375 %
FFh	1 (Default)	100 %

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(52h) RDDISBV: Read Display Brightness

Address	52h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description

- This command is used to returns the brightness value of the display.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. Please refer the register "WRDISBV (5100h)" for detailed.

DBV[7 : 0] is “0” (RDDISBV, 52h) when display is in sleep-in mode.

DBV[7 : 0] is "0" (RDDISBV, 52h) when bit BCTRL of "Write CTRL Display (5300h)" command is "0".

DBV[7 : 0] is manual set brightness specified with "Write CTRL Display (5300h)" command when bit BCTRL is "1".

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(53h) WRCTRLD: Write CTRL Display

Address	53h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	HBM [1:0]		BCTRL	0	DD	BL	0	0	00h

Description

- This command is used to control the "LEDPWM" pin, dimming function for CABC.

BCTRL: Turn On / Off the brightness control block with the dimming effect.

About the register "LEDPWPOL", please refer to the register "ABC_CTRL2"

BCTRL	LEDPWPOL	LEDPWM Pin Final State	Backlight Final State
0	**0**	**Keep "LOW" (0% PWM Duty) (Default)**	**OFF**
1	0	PWM Output (High level is duty)	ON
0	1	Keep "HIGH" (0% PWM Duty)	OFF
1	1	Inversed PWM Output (Low level is duty)	ON

DD: Enable / Disable dimming function only for CABC.

DD	CABC Dimming Function
0	**Disabled**
1	Enabled (Default)

BL: Turn On/Off the backlight control without dimming effect.

BL	Backlight Control
0	**OFF (Default)**
1	ON

When BL bit change from '1' to '0', backlight is turned off without gradual dimming, even if dimming-on (DD = '1') are selected.

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0

HBM: High Brightness Control Block On/Off.

HBM[1:0]		LED_BOOST Pin
0	**0**	**HBM mode OFF (Default)**
1	0	HBM mode ON
0	1	HBM mode ON
1	1	HBM mode ON

When HBM[1:0] bit change from '11' to '00', LED_BOOST pin will be output to external LED driver IC in the high brightness mode for display

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(54h) RDCTRLD: Read CTRL Display

Address	54h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	HBM [1:0]		BCTRL	0	DD	BL	0	0	00h

Description

- This command is used to "read" the setting status of "LEDPWM" pin, dimming function for CABC.

BCTRL: Turn On / Off the brightness control block with the dimming effect.

About the register "LEDPWPOL", please refer to the register "ABC_CTRL02"

BCTRL	LEDPWPOL	LEDPWM Pin Final State	Backlight Final State
0	**0**	**Keep “LOW” (0% PWM Duty) (Default)**	**OFF**
1	0	PWM Output (High level is duty)	ON
0	1	Keep “HIGH” (0% PWM Duty)	OFF
1	1	Inversed PWM Output (Low level is duty)	ON

DD: Enable / Disable dimming function only for CABC.

DD	CABC Dimming Function
0	**Disabled**
1	Enabled (Default)

BL: Turn On/Off the backlight control without dimming effect.

BL	Backlight Control
0	**OFF (Default)**
1	ON

When BL bit change from '1' to '0', backlight is turned off without gradual dimming, even if dimming-on (DD = '1') are selected.

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0

HBM: High Brightness Control Block On/Off.

HBM[1:0]		LED_BOOST Pin
0	**0**	**HBM mode OFF (Default)**
1	0	HBM mode ON
0	1	HBM mode ON
1	1	HBM mode ON

When HBM[1:0] bit change from '11' to '00', LED_BOOST pin will be output to external LED driver IC in the high brightness mode for display

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(55h) WRPWRSAVE: Write Power Save

Address	55h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	IMAGE_ENHANCEMENT[3:0]				0	0	CABC_COND[1:0]		00h

Description

- This command is used to set parameters for image content based adaptive brightness control and image enhancement level control functionality.
- There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_COND[1 : 0]		Function
0	**0**	**Off (Default)**
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Image (Moving-Mode)

- The NT35532 provides 4 different Image Enhancement (IE) technologies that include Smart Contrast, Vivid Color, Smart Color and Edge Enhancement. The three sets for IE Low/Medium/High level can be selected by **IMAGE_ENHANCE[3:0]** as below table. User can define each IE level value of these four IE technologies independently in “CMD2 Page2” and these registers in below table can also be programmed in MTP.

- The NT35532 also provides three Sunlight Readability Enhancement (SRE) levels to enhance IE function in outdoor.

  Each SRE level also can be set independently in “CMD2 Page 2” Registers and these registers in below table can also be programmed in MTP.

IMAGE_ENHANCEMENT[3:0]				IE Level	Smart Contrast	Vivid Color	Smart Color	Edge Enhancement
0	**0**	**0**	**0**	**IE OFF**				
1	0	0	0	IE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	COEFF_01
1	0	0	1	IE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	COEFF_02
1	0	1	1	IE_High	LEVEL_03	LEVEL03	RATIO_SEL03	COEFF_03
0	1	0	0	SRE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	COEFF_01
0	1	0	1	SRE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	COEFF_02
0	1	1	0	SRE_High	LEVEL_03	LEVEL03	RATIO_SEL03	COEFF_03
Others				N.A. (Reserved)				

Restriction

- This register is synchronized with V-sync by internal circuit.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(56h) RDPWRSAVE: Read Power Save

Address	56h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	IMAGE_ENHANCEMENT[3:0]				0	0	CABC_COND[1:0]		00h

Description

- This command is used to "read" the CABC operation mode and image enhanced level.
- There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_COND[1 : 0]		Function
0	**0**	**Off (Default)**
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Image (Moving-Mode)

- Image Enhancement (IE) and Sunlight Readability Enhancement (SRE) levels are read by IMAGE_ENHANCEMENT [3:0] as below table.

IMAGE_ENHANCEMENT[3:0]				IE Level	Smart Contrast	Vivid Color	Smart Color	Edge Enhancement
0	**0**	**0**	**0**	**IE OFF**				
1	0	0	0	IE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	COEFF_01
1	0	0	1	IE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	COEFF_02
1	0	1	1	IE_High	LEVEL_03	LEVEL03	RATIO_SEL03	COEFF_03
0	1	0	0	SRE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	COEFF_01
0	1	0	1	SRE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	COEFF_02
0	1	1	0	SRE_High	LEVEL_03	LEVEL03	RATIO_SEL03	COEFF_03
Others				N.A. (Reserved)				

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(5Eh) WRCABCMB: Write CABC Minimum Brightness

Address	5Eh				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	CMB[7 : 0]								00h

Description	- This command is used to set the minimum brightness value of the display for CABC function. 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(5Fh) RDCABCMB: Read CABC Minimum Brightness

Address	5Fh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	CMB[7 : 0]								00h

Description	- This command is used to “read” the minimum brightness value of the display for CABC function. 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(A1h) RDDDBS: Read DDB Start

Address	A1h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	SID[7 : 0]								N/A
Parameter 2	SID[15 : 8]								N/A
Parameter 3	MID[7 : 0]								N/A
Parameter 4	MID[15 : 8]								N/A
Parameter 5	RID[7 : 0]								N/A
Parameter 6	RID[15 : 8]								N/A
Parameter 7	FFh								FFh

Description

- This command returns supplier identification and display module model / revision information.

Note: This information is "not" the same what "Read ID1 (DA00h)", "Read ID2 (DB00h)" and "Read ID3 (DC00h)" commands are returning.

Note: Parameter 7 is an "Exit Code", this means that there is no more data in the DDB block.

This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A800h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd Parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.

Note:

SID[15 : 0]: MIPI member ID number

MID[15 : 0]: Module ID

RID[15 : 0]: Revision ID

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Parameter 1~6:

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Parameter 7:

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

(A8h) RDDDBC: Read DDB Continue

Address	A8h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	SID[7 : 0]								N/A
Parameter 2	SID[15 : 8]								N/A
Parameter 3	MID[7 : 0]								N/A
Parameter 4	MID[15 : 8]								N/A
Parameter 5	RID[7 : 0]								N/A
Parameter 6	RID[15 : 8]								N/A
Parameter 7	FFh								FFh

Description

- A read_DDB_start (RDDDBS) command should be executed at least once before a read_DDB_continue (RDDDBC) command to define the read location.

Otherwise, data read with a read_DDB_continue command is undefined.

Note: (1) Parameter 7 is an "Exit Code", this means that there is no more data in the DDB block.

(2) for use example:

Step 1. HW Reset.

Step 2: write 0x11, set sleep out mode.

Step 3: set max. return packet size =5.

Step 4. Read 0xA1, Return 5 bytes. Return SID[7:0], SID[15:8], MID[7:0], MID[15:8], RID[7:0]

Step 5. Read 0xA8, DDI return 2 bytes (RID[15:8], 0xFF)

Restriction

- SPI don't support continue read, only supports completely read.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Parameter 1~6:

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Parameter 7:

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

(AAh) RDFCS: Read First Checksum

Address	AAh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00h

Description	- This command returns the first checksum what has been calculated from System function registers and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	(1) It will be necessary to wait 150 ms after there is the last write access on System function registers before there can read this checksum value.
Register Availability	
Default Value	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(ABh) MIPI Error Report

Address	ABh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	AWER15	AWER14	AWER13	AWER12	AWER11	AWER10	AWER9	AWER8	NA
Parameter 2	AWER7	AWER6	AWER5	AWER4	AWER3	AWER2	AWER1	AWER0	NA

Description

- Peripheral sourced MIPI error report for software debug in development stage.
- It is an alternative way to use DCS short read packet (with 2 parameters) for error report readout besides of DSI packet type 02h

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

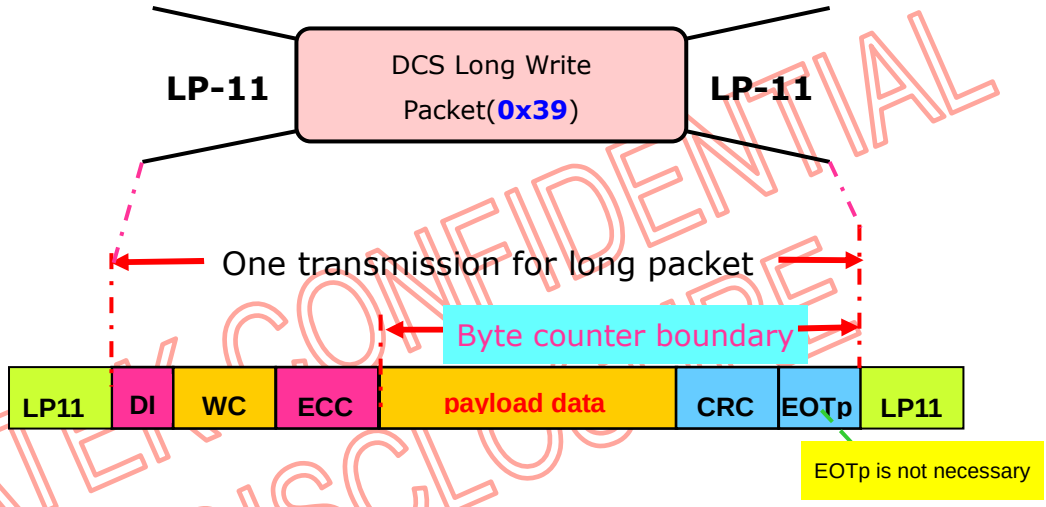
Status	Default Value
Power On Sequence	NA
S/W Reset	NA
H/W Reset	NA

(ACh) DCS long write payload counter

Address	ACh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	LPa15	LPa14	LPa13	LPa12	LPa11	LPa10	LPa9	LPa8	NA
Parameter 2	LPa7	LPa6	LPa5	LPa4	LPa3	LPa2	LPa1	LPa0	NA

Description

- DCS long write payload counter, used for software debug in development stage.



Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

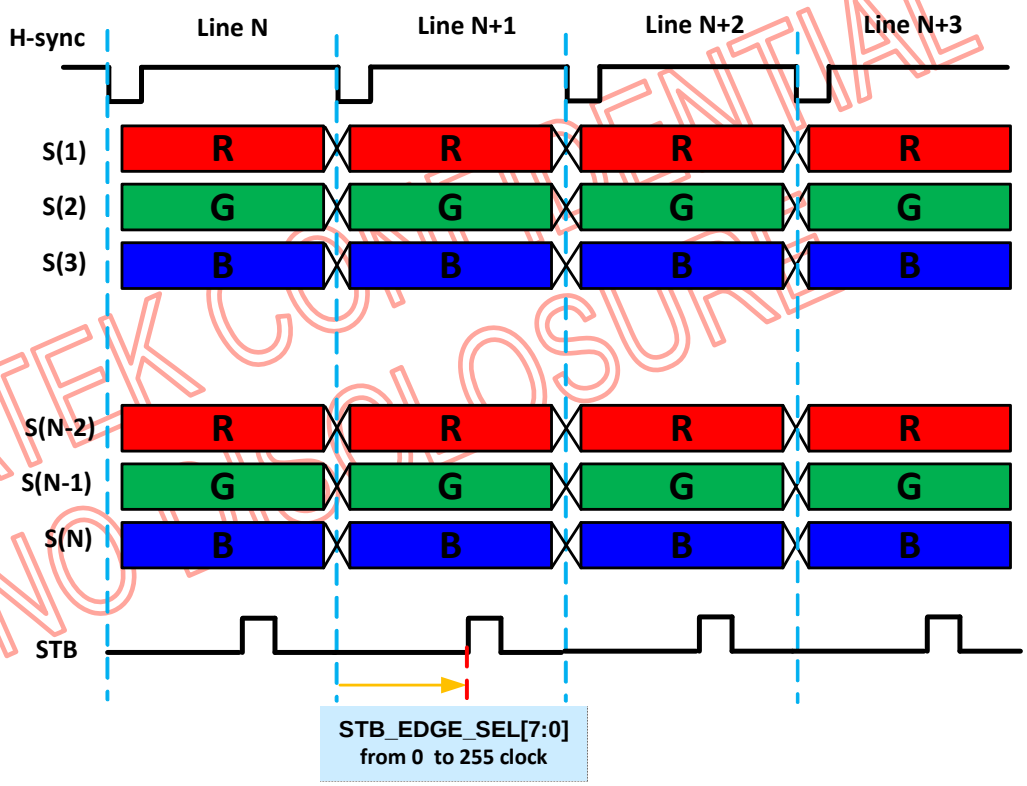
Status	Default Value
Power On Sequence	NA
S/W Reset	NA
H/W Reset	NA

(AEh) STB EDGE POSITION

Address	AEh				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	STB_EDGE_SEL[7:0]								00h

Description

- It is used to set a rising edge position of STB signal that refers to the falling edge of Display HSYNC. STB signal is repeated at per line except VBP/VFP region and outputs from FTE/FTE1/LEDPWM/VSOUT /REQOUT/HSOUT pad.



STB_EDGE_SEL[7:0]	Adjusted STB rising edge position
00h	Aligned to the falling edge of HSYNC
01h	+1
02h	+2
:	:
:	:
80h	+128
:	:
:	:
FFh	+255

Note:
1. In above table, “+” index that STB rising edge is set to lag the falling edge of Display HSYNC.
2. The unit of “Adjusted STB rising edge position” is number of Display Clock.

Restriction -

Register Availability

Status	Availability

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(AFh) RDCCS: Read Continue Checksum

Address	AFh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00h

Description

- This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from System function registers and the frame memory after the write access to those registers and/or frame memory has been done.

Restriction

(1) It will be necessary to wait 300 ms after there is the last write access on System function registers before there can read this checksum value in the first time.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(BAh) SET_MIPI_LANE and DSI MODE SELECTION

Address	BAh				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	MIPI_ECC_DISABLE	MIPI_CRC_DISABLE	DSI_MODE[1:0]		0	0	DSI_LANE[1:0]		03h

Description

- MIPI data lane number selection.

DSI_LANE[1 :0]	Function Description
00	Reserved
01	MIPI DSI with 2 lanes
10	MIPI DSI with 3 lanes
11	**MIPI DSI with 4 lanes**

- MIPI DSI mode selection

DSI_MODE[1:0]	Function Description
00	**MIPI Video mode**
01	Reserved
10	Reserved
11	Reserved

- MIPI DSI ECC error report detection Enable/Disable function.

MIPI_ECC_DISABLE	Function Description
0	Enable
1	**Disable**

- MIPI DSI CRC error report detection Enable/Disable function.

MIPI_CRC_DISABLE	Function Description
0	Enable
1	**Disable**

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	03h
S/W Reset	N.A.
H/W Reset	03h

(D2h~D7h) RGBMIPICTRL: RGB-MIPI-Video-Mode Signal Control

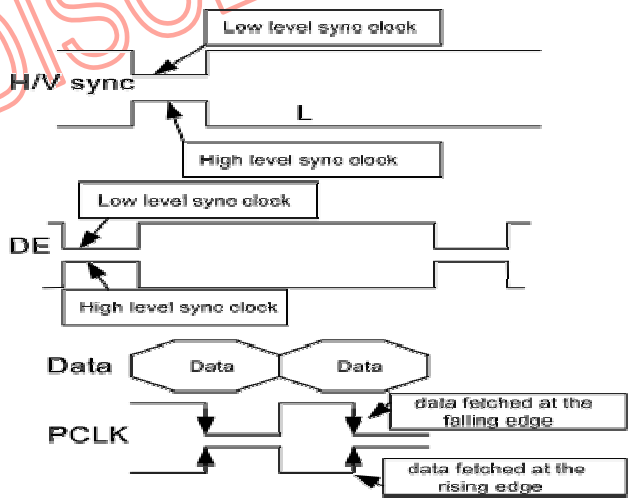
Address	3Bh				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D2h	0	CRCM	0	0	DP	EP	HSP	VSP	03h
D3h	VBP [7:0]								10h
D4h	VFP [7:0]								10h
D5h	HBP [7:0]								04h
D6h	HFP [7:0]								04h
D7h	0	0	0	0	0	0	HBP[8]	HFP[8]	00h

Description

- Set the operation status on the RGB interface. The setting becomes effective as long as the command is received.
- RGB Interface is used in NOVATEK engineering mode.

CRCM: Determines the RGB Mode 1 & RGB Mode 2

CRCM	RGB Mode Selection
0	RGB Mode 1
1	RGB Mode 2



RGB I/F Mode	PCLK	DE	D[23 : 0]	VS	HS	VBP[5 : 0], HBP[5 : 0], VFP[5 : 0], HFP[5 : 0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Description

DP / EP / HSP / VSP: Clock polarity set for RGB Interface

Symbol	Name	Clock Polarity Set For RGB Interface
DP	PCLK Polarity Set	'0' = Data fetched at the rising edge '1' = Data fetched at the falling edge
EP	DE Polarity Set	'0' = High enable for RGB interface '1' = Low enable for RGB interface
HSP	Hsync Polarity Set	'0' = High level sync clock '1' = Low level sync clock
VSP	Vsync Polarity Set	'0' = High level sync clock '1' = Low level sync clock

VBP[7 : 0], VFP[7 : 0], HBP[8 : 0] and HFP[8 : 0]:

Vertical back and front porch setting are used for MIPI video mode and RGB I/F mode 2.

Horizontal back and front porch setting are used for RGB I/F mode 2.

VBP[7 : 0]: Number of lines for the back porch of VSYNC.

VFP[7 : 0]: Number of lines for the front porch of VSYNC.

HBP[8 : 0]: Number of pixels for the back porch of HSYNC.

HFP[8 : 0]: Number of pixels for the front porch of HSYNC.

Description

VBP[7 : 0]	Back Porch Line Number	VFP[7 : 0]	Front Porch Line Number	HBP[8 : 0]	Back Porch Pixel clocks	HFP[8 : 0]	Front Porch Pixel Clocks
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
:	:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
:	:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
02d	2	04d	4	04d	4	04d	4
03d	3	05d	5	05d	5	05d	5
: : :	: (STEP 1) :	: : :	: (STEP 1) :	: : :	: (STEP 1) :	: : :	: (STEP 1) :
125d	125	125d	125	509d	509	509d	509
126d	126	126d	126	510d	510	510d	510
127d	127	127d	127	511d	511	511d	511

Note: VBP >=4 and VFP>=4.

Restriction

- Register VBP and VFP setting should same as CMD2_P4, BP and FP.

CMD1, D3h (VBP) = CMD2_P4, 92h (BP)

CMD1, D4h (VFP) =CMD2_P4, 91h (FP)

- In MIPI Video mode I/F, the minimum HBP (unit: pixel clock)/HFP (unit: us) constraint as below.

Lane numbers	HBP (pixel clock)	HFP
1 Lane	> 4	> 0.65us
2 Lanes	> 8	> 0.65us
3 Lanes	> 12	> 0.65us
4 Lanes	> 16	> 0.65us

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

D2h:

Status	Default Value	Note
Power On Sequence	03h	CRCM = '0' (RGB Mode 1) DP = '0', EP = '0', HSP = '1' (Low Level), VSP = '1' (Low Level)
H/W Reset	03h	
S/W Reset	03h	

D3h ~ D7h:

Status	Default Value			
	VBP	VFP	HBP	HFP
Power On Sequence	10h	10h	04h	04h
H/W Reset	10h	10h	04h	04h
S/W Reset	10h	10h	04h	04h

(D9h) EXCK_CTRL: Display Clock Source Control

Address	F8h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D9h	0	EXTOSCDIV [2:0]			0	0	EXTOSC_SEL [1:0]		00h

Description

EXTOSC_SEL [1 : 0] : External Clock Source selection for Display Clock Source.

EXTOSC_SEL [1:0]	Display Clock Source
00b	**Internal OSC**
01b	MIPI CLK input
10b	External CLK input
11b	Reserved

EXTOSCDIV [2 : 0] : External Clock Source frequency division (N).

EXTOSCDIV [2:0]	EXTOSCDIV [2:0]
000b	**1**
001b	2
010b	3
011b	4
100b	5
101b	6
110b	7
111b	8

When using external clock source for display clock reference, user must set external clock source in "**EXTOSC_SEL [1 : 0]**".

NT35532 can accept the external oscillator frequency and MIPI clock bit rate for display clock reference.

1. For external oscillator frequency, the range is from 9MHz to 40MHz, from N=1 to N=4.

Note:

*If Display clock source refer to External Clock (**9MHz~40MHz**), user only can choice division (N) from **N=1** to **N=4,** but please keep Display reference clock around 14MHz~15MHz.*

2. For MIPI clock bit rate, the range is from 500Mbps to 1Gbps in the below table.

MIPI clock bit rate	EXTOSCDIV [2:0]
500 ~ 599 Mbps	4
600 ~ 699 Mbps	5
700 ~ 799 Mbps	6
800 ~ 899 Mbps	7
900 ~ 999Mbps	8
1Gbps	**8**

Note:

1. *Display reference clock is fixed around **14MHz~15MHz** from **External clock source**.*
2. *If Display clock source refers to **MIPI Clock**, user can choice division (N) from **N=1** to **N=8** , but please keep Display reference clock around 14MHz~15MHz.*
3. *While using MIPI Clock mode, MIPI Clock lane must keep continuous clock mode not to return LP-11.*

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	N.A.
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value	
	EXTOSCDIV [2:0]	EXTOSC_SEL [1:0]
Power On Sequence	00h	00h
S/W Reset	00h	00h
H/W Reset	00h	00h

(DAh) RDID1: Read ID1

Address	DAh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	N/A

Description	- This read byte identifies the display module's manufacturer.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

(DBh) RDID2: Read ID2

Address	DBh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	N/A

Description

- This read byte is used to track the display module/driver version.

It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value	Version	Changes
80h	:	:
81h	:	:
82h	:	:

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

(DCh) RDID3: Read ID3

Address	DCh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	N/A

Description	- This read byte identifies the display module / driver.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

(E1h) IDLEMODE_BL_Control: Write IDLEMODE_BL_Control

Address	E1h				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	0	0	0	0	IDLE_ON_SIGNAL_EN	IDLE_MODE_BL_EN	00h

Description

- The content of the register IDLEMODE_BL_control will define the functionality of the transmissive LCD display backlight behavior in idle mode which is enabled by command IDMON (39h). In this mode, the backlight power consumption will be reduced with several methods.

IDLE_ON_SIGNAL_EN: This bits controls the HW signal called IDLE_ON, which is wired from display to handset backlight drive. This bits can be used to dim handset backlight DC drive current in the idle mode. Note that display BC output will be still controllable by the register Write Display Brightness.

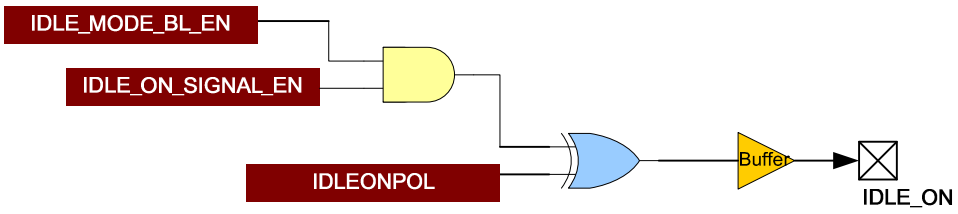
IDLE_ON_SIGNAL_EN	Function
0	output signal IDLE_ON is disabled and set to GND
1	Output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).

※The idle on signal should toggle state upon falling edge of the BC signal.

IDLE_MODE_BL_EN:

0 = Entering idle mode using command IDMON has no effect to display backlight behavior. Backlight control is controlled by Write Display Brightness (51h) and Write CTRL Display (53h) registers.

1 = Entering the idle mode will cause display to enter into idle mode specific backlight state defined by IDLE_ON_SIGNAL_EN bit.



<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default Value</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>N.A.</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

(E2h) IDLEMODE_BL_Control: Read IDLEMODE_BL_Control

Address	E1h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	0	0	0	0	IDLE_ON_SIGNAL_EN	IDLE_MODE_BL_EN	00h

Description

- The content of the register IDLEMODE_BL_control will define the functionality of the transmissive LCD display backlight behavior in idle mode which is enabled by command IDMON (39h). In this mode, the backlight power consumption will be reduced with several methods.

IDLE_ON_SIGNAL_EN: This bits controls the HW signal called IDLE_ON, which is wired from display to handset backlight drive. This bits can be used to dim handset backlight DC drive current in the idle mode. Note that display BC output will be still controllable by the register Write Display Brightness.

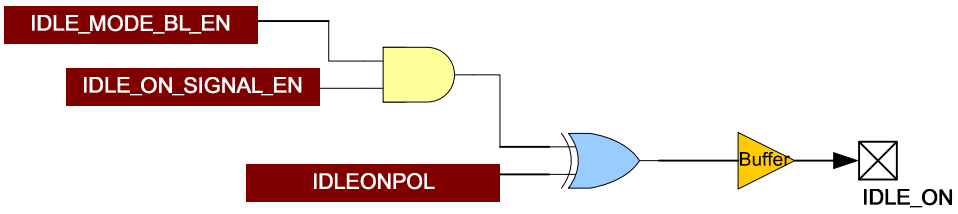
IDLE_ON_SIGNAL_EN	Function
0	output signal IDLE_ON is disabled and set to GND
1	Output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).

※The idle on signal should toggle state upon falling edge of the BC signal.

IDLE_MODE_BL_EN:

0 = Entering idle mode using command IDMON has no effect to display backlight behavior. Backlight control is controlled by Write Display Brightness (51h) and Write CTRL Display (53h) registers.

1 = Entering the idle mode will cause display to enter into idle mode specific backlight state defined by IDLE_ON_SIGNAL_EN bit.



<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N.A.</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default Value</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>N.A.</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

(F3h) MULTIIF: Multi-Interface Function

Address	F3h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	IM_IF_SEL	0	0	0	SECOND_IF_SEL[1:0]		0	MULTIIF_EN	80h

Description

IM_IF_SEL : To decide the main IF to access register. This bit is available when IM[2:0] = 000b / 010b / 011b.

IM_IF_SEL	Function
0	MIPI VIDEO MODE + MIPI ACCESS REGISTER
1	MIPI VIDEO MODE + SECONDARY IF (I2C or SPI) ACCESS REGISTER

MULTIIF_EN : Enable or Disable multi-interface function by register. It's only available when HW pin IM[2:0]=110b.

MULTIIF_EN	Function
0	Only MIPI I/F
1	Multi-IF Enable

SECOND_IF_SEL[1:0]: To select the main Interface to access register when MULTIIF_EN=1. It is only available when HW pin IM[2:0]=110b. MIPI VIDEO mode is always available.

Primary I/F	Secondary I/F			
IM[2:0] = 110b	SECOND_IF_SEL[1:0]			
MIPI	00b	01b	10b	11b
	I2C	9-bit SPI	8-bit SPI	N.A.

Restriction

- Do Not support two I/F access register simultaneously when Multi-IF function enable.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value	

Status	Default Value
Power On Sequence	80h
S/W Reset	N.A.
H/W Reset	80h

(F4h) Novatek ID: Read Novatek ID

Address	F4h				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	1	1	0	0	1	0	32h

Description	- This read byte identifies the Novatek ID code.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	32h
S/W Reset	32h
H/W Reset	32h

(F5h) IF_TEST: INTERFACE TEST

Address	F5h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	IF_TEST[7:0]								00h

Description	- This byte is used for interface test.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value	
	IF_TEST[7]	IF_TEST[6:0]
Power On Sequence	00h	00h
S/W Reset	00h	No effect
H/W Reset	00h	

(F6h~F7h) EXCK_CTRL: Display Clock Source Control

Address	F8h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
F6h	EXCK_FREQ[11:8]				0	0	0	EN_EXCK	50h
F7h	EXCK_FREQ[7:0]								78h

Description

- **EN_EXCK**: Display Clock Source selection.

EN_EXCK	Display Clock Source
0	**Display refer to Internal Oscillator**
1	Display refer to External Clock

- **EXCK_FREQ[11:0]** : When using external clock source for display reference, user must set external oscillator frequency in "**EXCK_FREQ[11:0]**". NT35532 can accept the external oscillator frequency range from 9MHz to 40MHz and frequency accuracy can be accepted to 2-digit decimal point. The formula is as below:

$EXCK\_FREQ[11:0] = 100 * f(MHz)$, "***f*** " is external oscillator frequency in unit "MHz"

Example 1: If external oscillator frequency is 20MHz :

*EXCK_FREQ[11:0] = 100 * 20 = 2000(Decimal) = 7D0(Hex)*

Example 2: If external oscillator frequency is 14.14MHz :

*EXCK_FREQ[11:0] = 100 * 14.14 = 1414(Decimal) = 586(Hex)*

Note: If external oscillator frequency is 14.145, user must use 14.14MHz or 14.15MHz to fill this register.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	N.A.
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value	
	EXCK_EXCK	EXCK_FREQ[11:0]
Power On Sequence	00h	578h
S/W Reset	00h	578h
H/W Reset	00h	578h

(F8h) I2C_SLAVE_ADDR: I2C Slave Address

Address	F9h				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	I2C_SLAVE_ADDR[6:0]							00h

Description

-Set the slave address of I2C interface.

- Default slave address is 00h, and this slave address always can access register whether this register have been filled another slave address or not. It means that user can use the slave address that you fill into this register to access registers or uses global slave address 00h to access registers.

Restriction

- NT35532 does not support “general call address” function.

- In end-customer terminal (system platform), it can Not send “hardware general call” function of standard I2C SPEC. This function will lead NT35532 work abnormally.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
	I2C_SLAVE_ADDR[1:0]
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(F9h) PIXEL_EXTEN: PIXEL EXTENSION FORMAT

Address	FAh				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	0	0	0	0	PIXEL_EXTEN[1:0]		00h

Description

- This byte is used for pixel extension format.

PIXEL_EXTEN[1:0]	5-6-5 format	6-6-6 format	8-8-8 format
00b	R[7:0] = {R[4:0], R[4:2]} G[7:0] = {G[5:0], G[5:4]} B[7:0] = {B[4:0], B[4:2]}	R[7:0] = {R[5:0], R[5:4]} G[7:0] = {G[5:0], G[5:4]} B[7:0] = {B[5:0], B[5:4]}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
01b	R[7:0] = {R[4:0], 3'b0} G[7:0] = {G[5:0], 2'b0}} B[7:0] = {B[4:0], 3'b0}	R[7:0] = {R[5:0], 2'b0} G[7:0] = {G[5:0], 2'b0}} B[7:0] = {B[5:0], 2'b0}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
10b	R[7:0] = {R[4:0], 3'b111} G[7:0] = {G[5:0], 2'b11} B[7:0] = {B[4:0], 3'b111}	R[7:0] = {R[5:0], 2'b11} G[7:0] = {G[5:0], 2'b11} B[7:0] = {B[5:0], 2b11}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
11b	N.A.		

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
	PIXEL_EXTEN[1:0]
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(FBh) RELOAD CMD1

Address	FBh				Access Attribute				R/W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	0	0	0	0	0	RELOAD_CMD1	00h

Description

RELOAD_CMD1: The RELOAD_CMD1 is used to select the control value of CMD1.

RELOAD_REG	MIPI LANE, STB Function
0	**Reload setting value from MTP or register default value to register**
1	Don't reload MTP or register default value to register

Notes:

1. *If the user doesn't program any MTP, these above descript MTP registers default value equal to NT35532 Driver IC default value as Specification definition.*
2. *If the user programmed MTP, these above descript registers default value equal to MTP Value after hardware reset or software reset again.*
3. *When the NT35532 exit sleep mode, the driver IC will reload MTP or register default value to the above descript MTP register to change these registers contents.*
4. *The user can set the RELOAD_CMD1 bit to one to keep current register value by user's software setting, before the driver IC Exit sleep mode.*

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(FEh) RD_CMDSTATUS: Read the Current Register Set

Address	FEh				Access Attribute				R
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	0	0	CMD2_P4	CMD2_P3	CMD2_P2	CMD2_P1	CMD2_P0	CMD1	01h

Description

- This command is used for checking the current CMD accessing status, especially when MIPI interface is selected.

CMD1 = 1, host is accessing registers of CMD1 Set.

CMD2_P0 = 1, host is accessing registers of CMD2 Page 0.

CMD2_P1 = 1, host is accessing registers of CMD2 Page1.

CMD2_P2 = 1, host is accessing registers of CMD2 Page2.

CMD2_P3 = 1, host is accessing registers of CMD2 Page3.

CMD2_P4 = 1, host is accessing registers of CMD2 Page4.

0	0	CMD2_P4	CMD2_P3	CMD2_P2	CMD2_P1	CMD2_P0	CMD1	Current Register Set Status
0	0	0	0	0	0	0	1	In Command 1
0	0	0	0	0	0	1	0	In the Page 0 of Command 2
0	0	0	0	0	1	0	0	In the Page 1 of Command 2
0	0	0	0	1	0	0	0	In the Page 2of Command 2
0	0	0	1	0	0	0	0	In the Page 3 of Command 2
0	0	1	0	0	0	0	0	In the Page 4 of Command 2
Others								Reserved

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value	

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

(FFh) CMD Page Select

Address	FFh				Access Attribute				W
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	PAGE_SEL[7:0]								00h

Description	- This command is used to select page. - PAGE_SEL[7:0] : it defines how to select a register page that you want to access. 00h → CMD1 is selected 01h → CMD2 Page0 is selected 02h → CMD2 Page1 is selected 03h → CMD2 Page2 is selected 04h → CMD2 Page3 is selected 05h → CMD2 Page4 is selected *Note: When the driver IC received this command, then the driver IC will enter the register page.*
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

Default Value

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Restriction -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	N.A.
Partial Mode On, Idle Mode Off, Sleep Out	N.A.
Partial Mode On, Idle Mode On, Sleep Out	N.A.
Sleep In	Yes

7. Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	VDDI,VDDAM	-0.3 ~ +5.5	V
Supply voltage	VCI-AVSS	- 0.3 ~ +6.5	V
Driver supply Voltage	AVDD-AVSS	-0.3 ~ +6.5	V
Driver supply Voltage	AVEE-AVSS	-6.5 ~ +0.3	V
Operating temperature range	TOPR	-30 ~ +75	℃
Storage Temperature range	TSTG	-40 ~ +85	℃
Logic Input voltage range	VIN	-0.3 ~ +4	V
Logic Output voltage range	VO	-0.3 ~ +4	V
Humidity		5% to 95%	%

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 DC CHARACTERISTICS

7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	4.8	V	Note 1
I/O operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.6	V	Note 1
Analog Operating voltage	AVDD	Operating Voltage	GVDDP+0.5		6	V	Note 5
Analog Operating voltage	AVEE	Operating Voltage	-6		GVDDN-0.5	V	Note 6
MIPI Operating voltage	VDDAM	MIPI Supply voltage	1.65	1.8	3.6	V	Note1
Input / Output							
Logic High level input voltage	VIH		0.7VDDI	-	VDDI	V	Note 1, 2
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2
Logic High level output voltage	VOH	IOH = -0.1mA	0.8VDDI	-	VDDI	V	Note 1, 2
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2VDDI	V	Note 1, 2
Logic High level leakage (Except MIPI)	ILIH1	Vin = 0 to VDDI			1	uA	Note 1, 2
Logic Low level leakage (Except MIPI)	ILIIL1	Vin = 0 to VDDI	-1			uA	Note 1, 2
Logic High level leakage MIPI	ILIH2	Vin = 0 to 1. 3 V			10	µA	
Logic Low level leakage MIPI	ILIL2	Vin = 0 to 1. 3 V	-10			µA	
VCOM Operation							
VCOMDC voltage	VCOMDC3	Operating Voltage	-4		+1	V	
Source Driver							
Gamma reference voltage	GVDDP	GVDDP<AVDD-0.3	3.5	-	5.5	V	
	GVDDN	GVDDN>AVEE+0.3	-5.5		-3.5	V	
Output deviation voltage	V,dev1	Sout>=+4.2V, Sout<=+0.8V	-	20	30	mV	Note3
	V,dev2	+0.8V<Sout<+4.2V	-	10	15	mV	
	V,dev3	Sout>=-0.8V, Sout<=-4.2V		20	30	mV	
	V,dev4	-0.8V<Sout<-4.2V		10	15	mV	
Output offset voltage	VOFSET				35	mv	
Power generation							
Internal reference voltage	VREF	Operating Voltage		1.2		V	
Power supply for Digital circuit	VDD			1.62		V	
Power supply for MIPI I/F	VP_HSSI			1.62		V	
Analog power	AVDD		4.5		6	V	
Analog power	AVEE		-6		-4.5	V	
LDO output for GVDDP	AVDDR		3		5.5	V	
LDO output for GVDDN	AVEER		-5.5		-3	V	
LDO output for VGH	VGHO	VGH > VGHO + 0.3V	7		20	V	Note 4
LDO output for VGL	VGLO	VGL < VGLO-0.3V	-4		-18	V	Note 4
1st Booster voltage	VGH	Operating Voltage	2xAVDD		3xAVDD-AVEE	V	
2nd Booster voltage	VGL	Operating Voltage	2*AVEE –AVDD		AVEE – VCI1	V	
3rd Booster voltage or LDO output	VCL	Operating Voltage from pump Circuit or LDO	-3.3		-2.5	V	
Oscillator tolerance	OSC	25℃	-3	-	3	%	
Oscillator tolerance	OSC	75℃~-30℃	-5	-	5	%	

Note 1: VDDI=1.65 to 3.6V, VCI= 2.5 to 4.8V, VDDAM=1.65 to 3.6 V, AVSS=VSS=0V, Ta=-30 to 75 ℃ (to +85 ℃ no damage)
Note 2: When the measurements are performed with LCD module, Measurement Points are like below.
CSX, RDX, WRX, D[23:0], DCX, RESX, SCL, IM[2 : 0] and Test pins
Note 3: Source channel loading= 40pF/channel
Note 4: VCI=3.3V, Ta=25 ℃, No load;
Note 5: for 2-2 power mode,3-power mode and 4-power mode usage only
Note 6: for 3-power mode and 4-power mode usage only

7.2.2 Current Consumption

Three power mode (VDDI + AVDD + AVEE)

Parameter	Symbol	Conditions	Specification									Unit
			MIN			TYP			MAX			
			VDDI	AVDD	AVEE	VDDI	AVDD	AVEE	VDDI	AVDD	AVEE	
Sleep in mode (Note 1) Three power mode (VDDI + AVDD + AVEE)	I_{SPA}	VDDI = VDDAM = 1.8V, AVDD = 5.6V, AVEE = -5.6V, 1920 lines, Ta = 25°	-			75	25	25	200	80	80	uA
Deep standby mode (Note 1) Three power mode (VDDI + AVDD + AVEE)	I_{DST}	VDDI = VDDAM = 1.8V, AVDD = 5.6V, AVEE = -5.6V, Ta = 25°	-			0.2	0.2	0.2	3	3	3	uA

Note. For MIPI interface, the sleep in and deep standby current is only in ULPS mode.

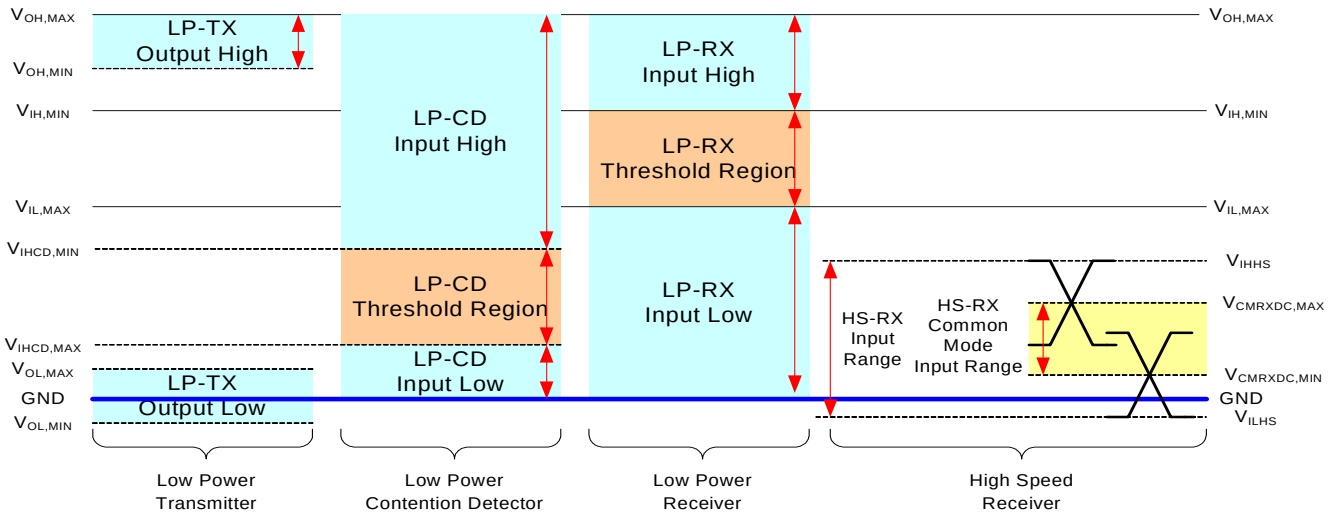
Four power mode (VCI + VDDI + AVDD + AVEE)

Parameter	Symbol	Conditions	Specification												Unit
			MIN				TYP				MAX				
			VDDI	VCI	AVDD	AVEE	VDDI	VCI	AVDD	AVEE	VDDI	VCI	AVDD	AVEE	
Sleep in mode (Note 1) Four power mode (VCI + VDDI + AVDD + AVEE)	I_{SPA}	VDDI = VDDAM = 1.8V, VCI = 3V , AVDD = 5.6V, AVEE = -5.6V, 1920 lines, Ta = 25°	-				75	25	25	25	200	80	80	80	uA
Deep standby mode (Note 1) Four power mode (VCI + VDDI + AVDD + AVEE)	I_{DST}	VDDI = VDDAM = 1.8V, VCI = 3V , AVDD = 5.6V, AVEE = -5.6V, Ta = 25°	-				0.2	0.2	0.2	0.2	3	3	3	3	uA

Note. For MIPI interface, the sleep in and deep standby current is only in ULPS mode.

7.2.3 MIPI DC Characteristics

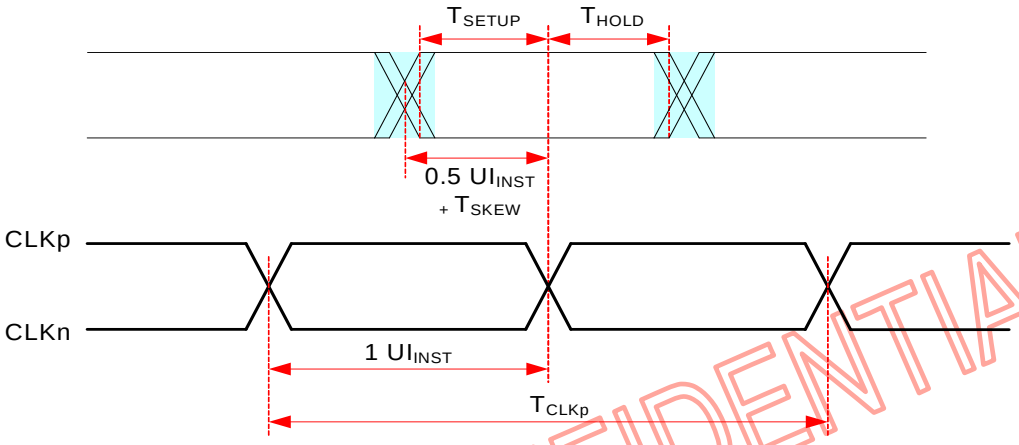
Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.65	1.8	3.6	V
VP_HSSI	High speed / Low power mode operating voltage		1.62		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
|VOD|	HS transmit differential voltage (VOD=VDP-VDN)	140	200	250	mV
V_{IDTH}	Different input high threshold			70	mV
V_{IDTL}	Different input low threshold	-70			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0.0		550	mV
VIH	Logic 1 input threshold	880		VDDAM	mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD,MAX	Logic 0 contention threshold	0.0		200	mV
VILCD,MIN	Logic 1 contention threshold	450		VDDAM	mV



7.3 AC CHARACTERISTICS

7.3.1 MIPI Interface Characteristics

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2,10
Data to Clock Skew [measured at tansmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	3
		-0.2		0.2	UI_{INST}	4
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
Data to Clock Hold Time [measured at reciever]	T_{HOLD}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
20% - 80% rise time and fall time	t_R / t_F	100			ps	9
				0.3	UI_{INST}	7
				0.35	UI_{INST}	8

Note:

1. This value corresponds to a minimum 80 Mbps data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. Total silicon and package delay budget of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

4. Total silicon and package delay budget of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

5. Total setup and hole window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

6. Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

7. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

8. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

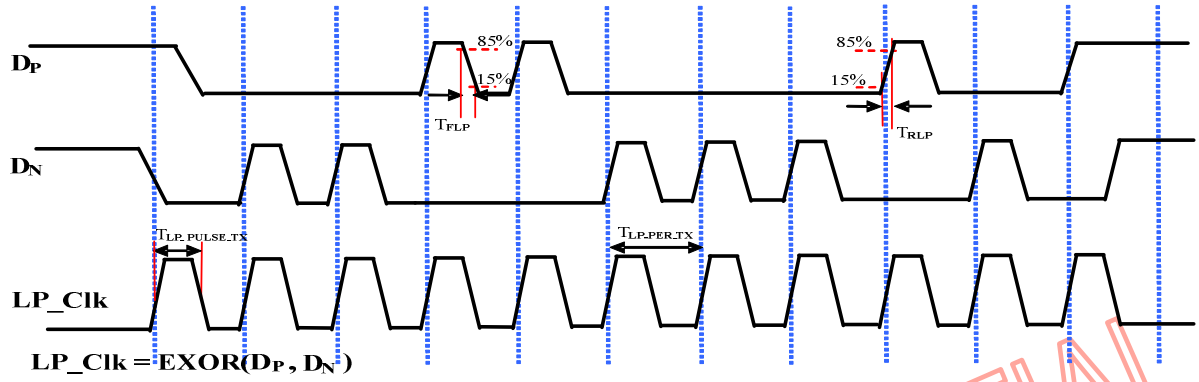
9. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

10. For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for5-6-5.

LP Transmission AC Specification



Parameter		Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time		T_{RLP} / T_{FLP}			25	ns	1
30%-85% rise time and fall time		T_{REOT}			35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40			ns	4
	All other pulses		20			ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90			ns	
Slew Rate@ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30		500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF			30		200	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 20pF			30		150	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 70pF			30		100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}			70	pF	1

Note:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

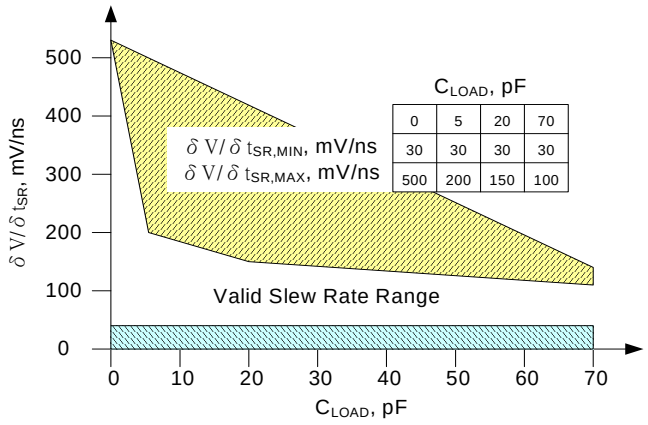
3. Measured as average across any 50 mV segment of the output signal transition.

4. This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.

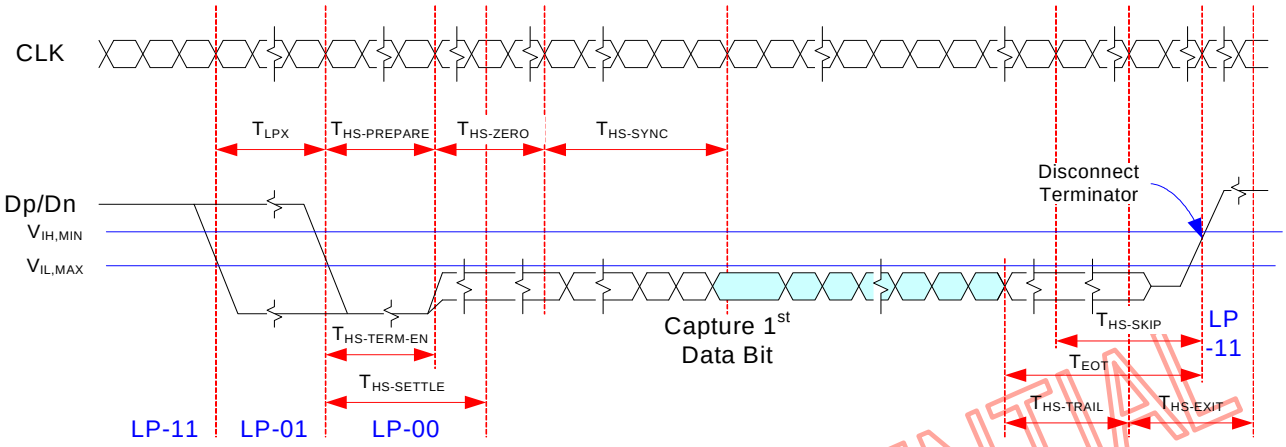
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

6. With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.

7. This value represents a corner point in a piecewise linear curve as bellowed.



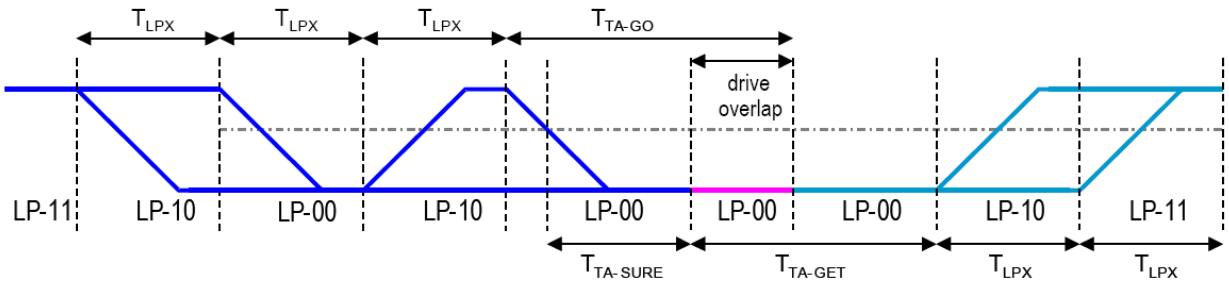
High-Speed Data Transmission in Bursts



Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

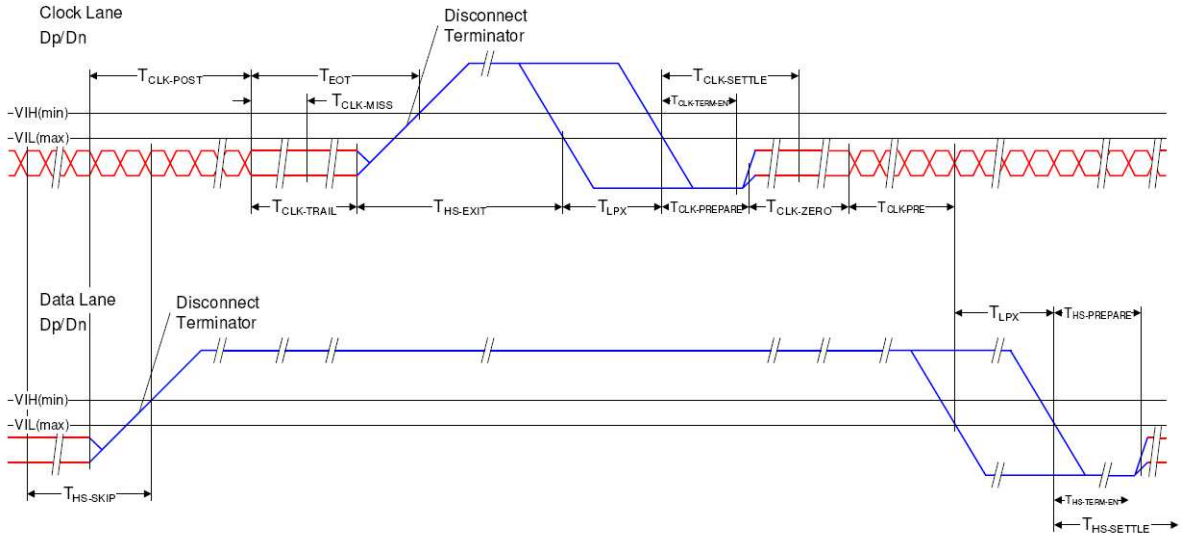
Note:
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode

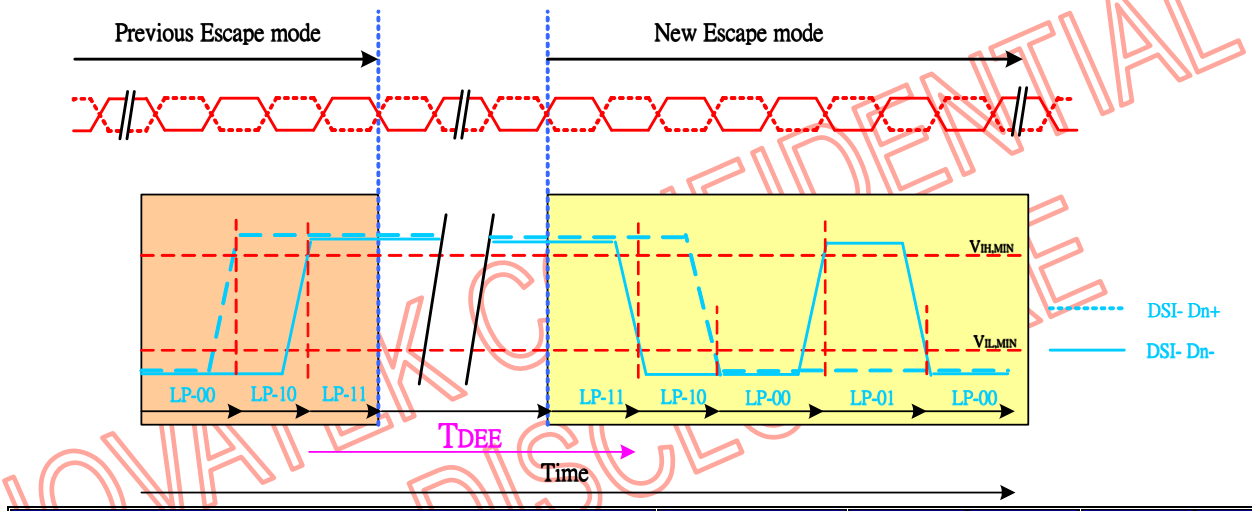


Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+128UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

LP11 timing request between data transformation

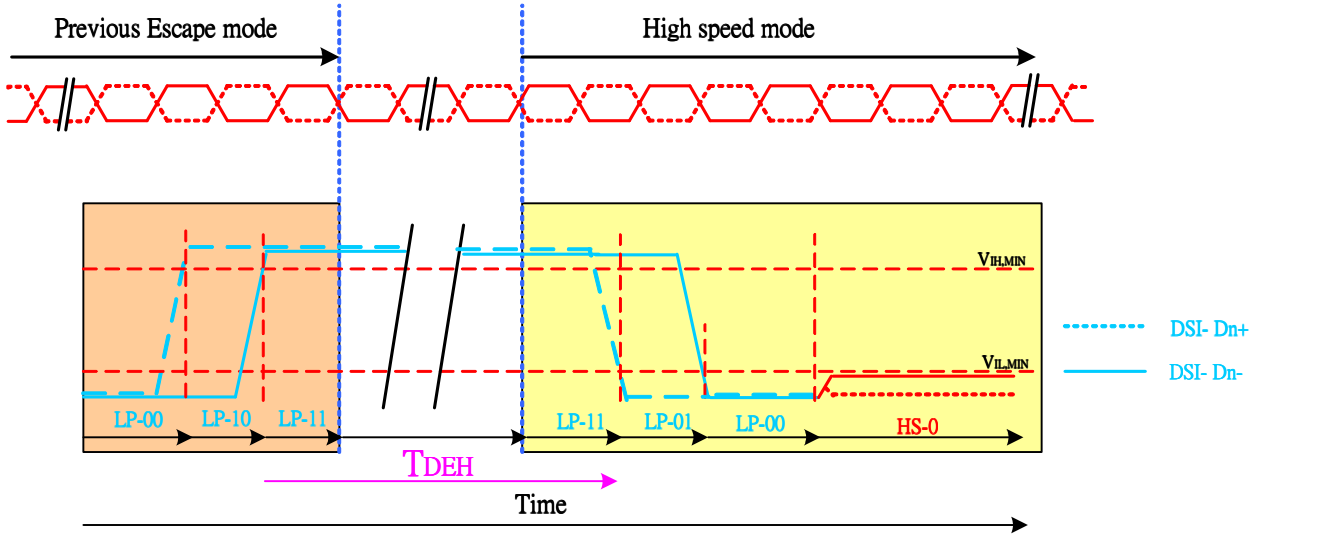
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP – LP, LP – HS, HS – LP, HS – HS, BTA – BTA, LP – BTA, BTA – LP, HS – BTA, and BTA – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP – LP command



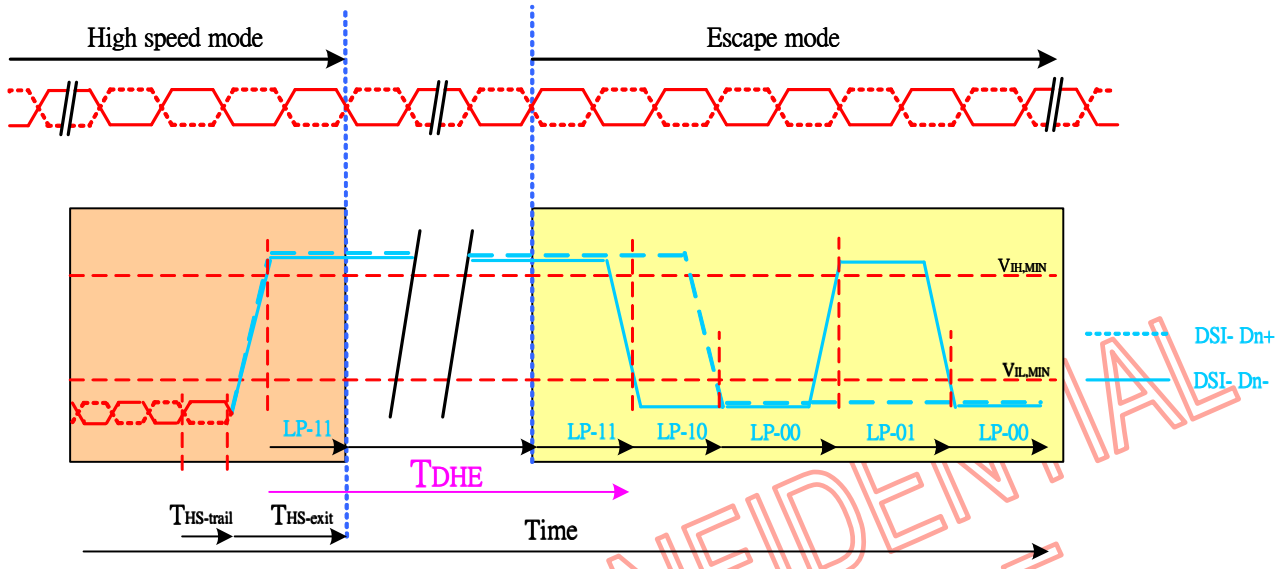
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	100			ns

(2)Timing between LP – HS command



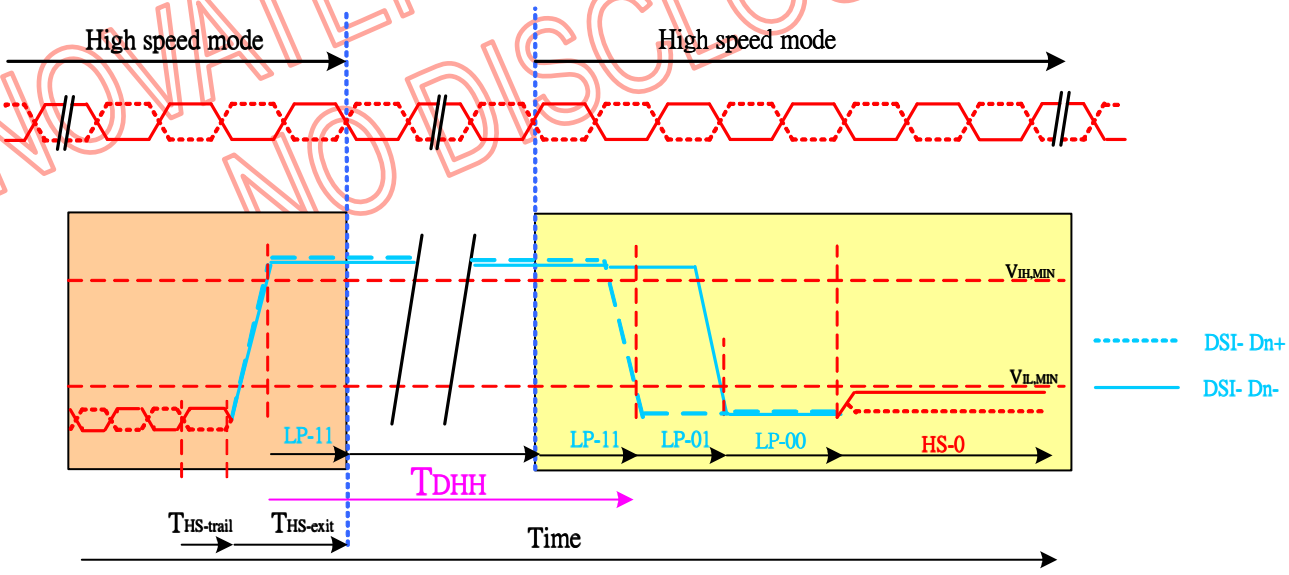
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(100,32UI)			ns

(3)Timing between HS – LP command



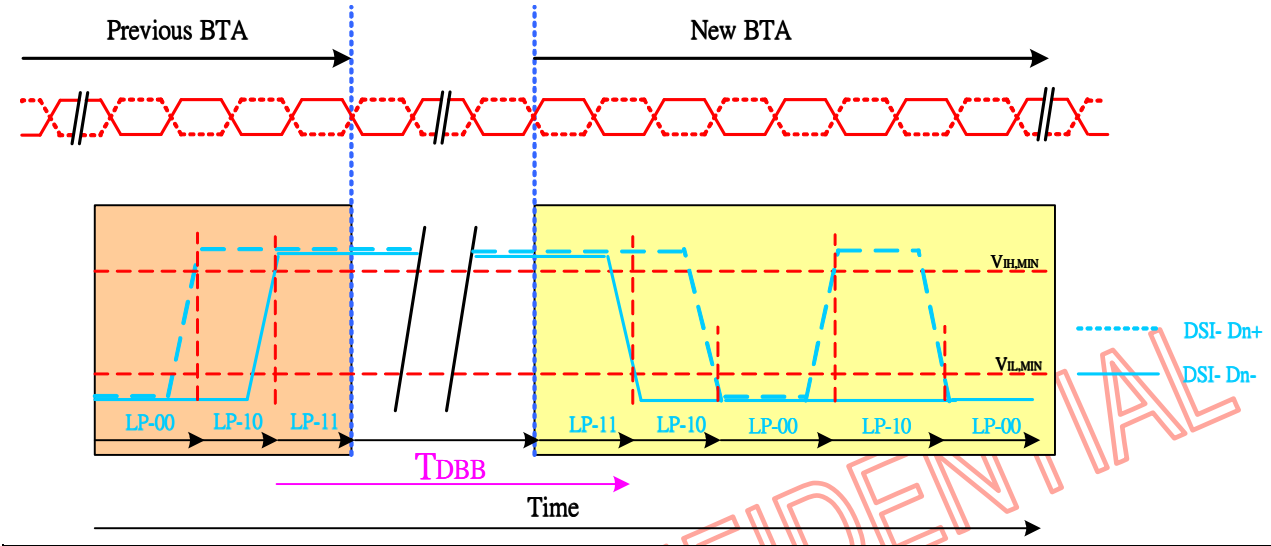
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(100,32UI)			ns

(4)Timing between HS –HS command



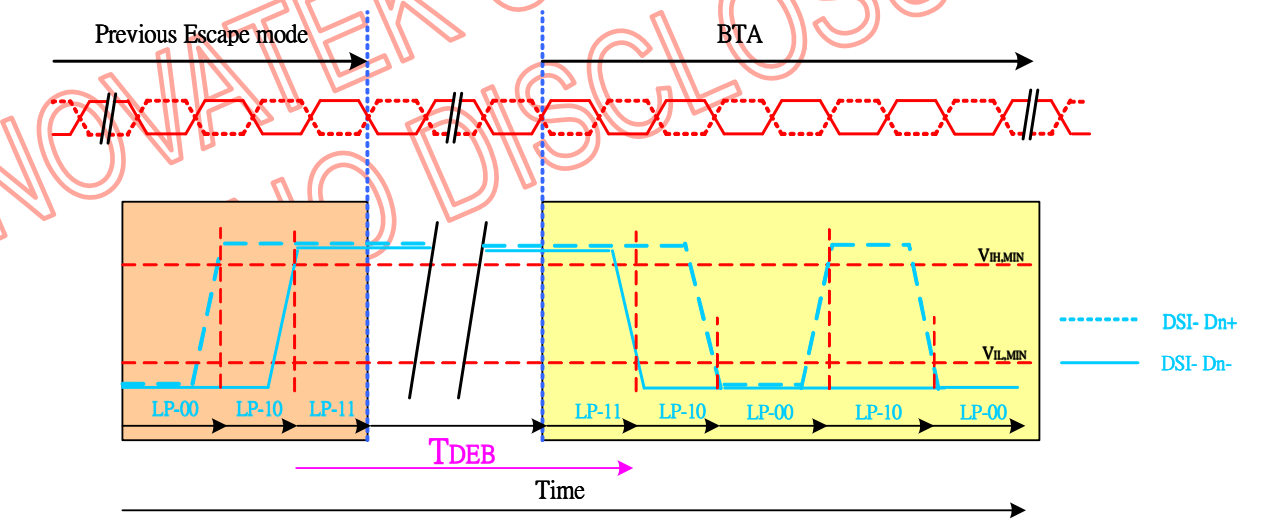
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DHH}	Max(100,32UI)			ns

(5)Timing between BTA – BTA command



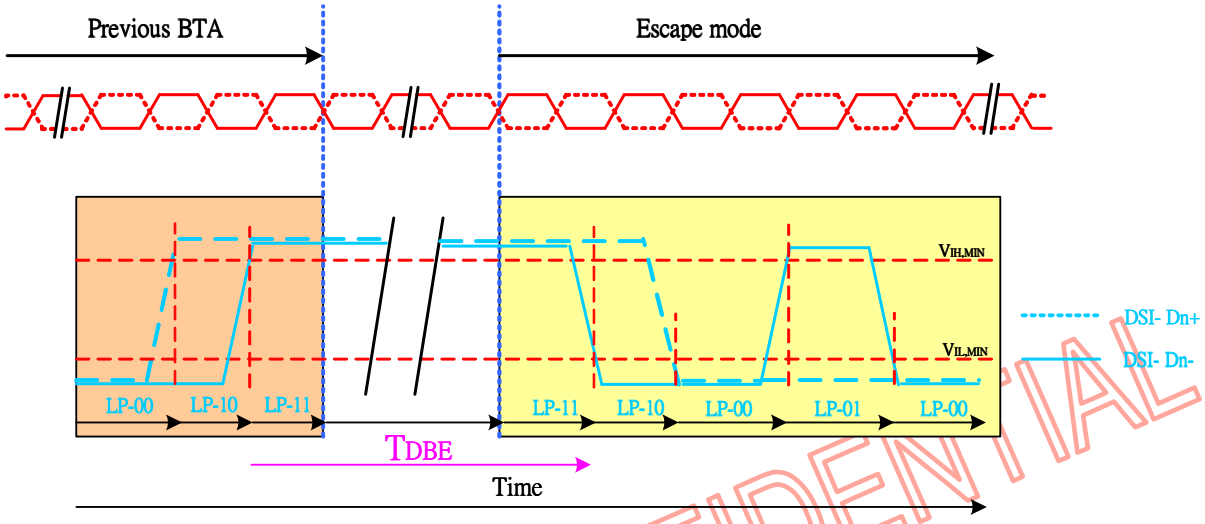
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the new BTA	T_{DBB}	100			ns

(6)Timing between LP– BTA command



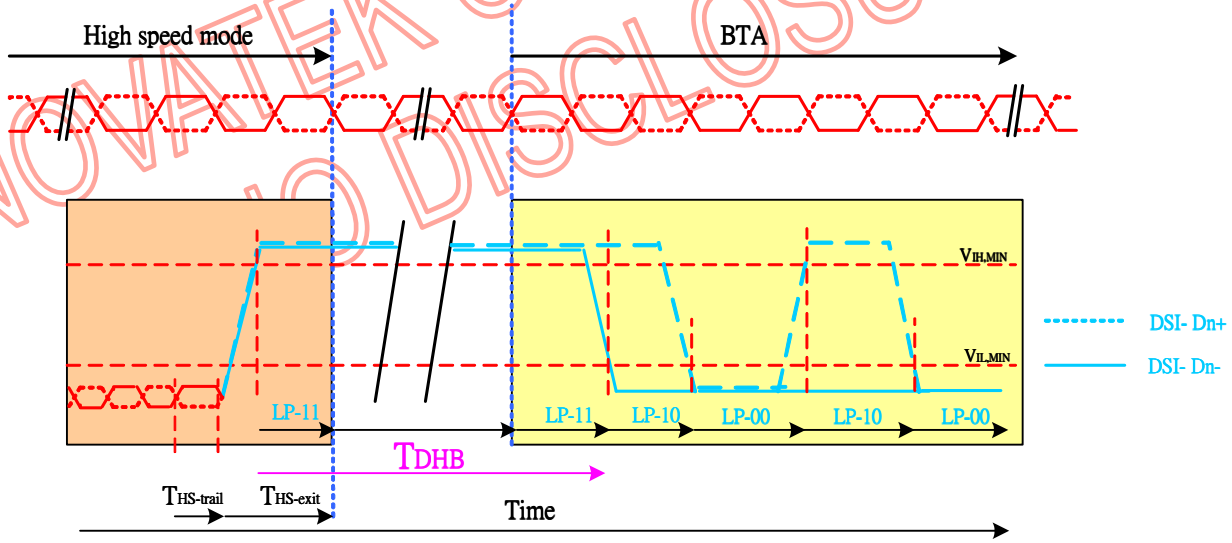
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DEB}	100			ns

(7)Timing between BTA – LP command



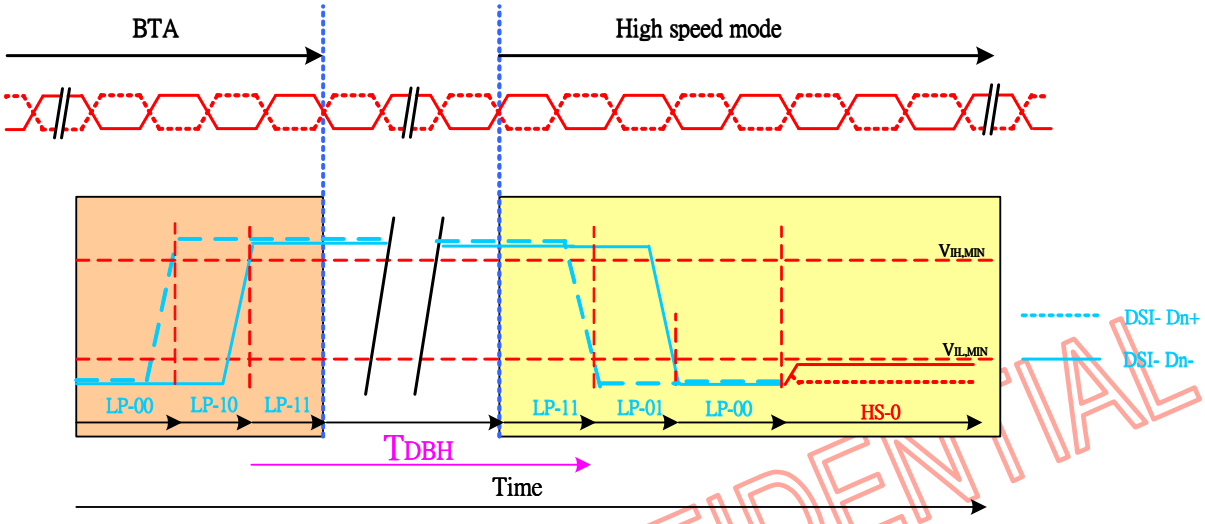
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Escape Mode Entry	T_{DBE}	100			ns

(8)Timing between HS – BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DHB}	Max(100,32UI)			ns

(9)Timing between BTA – HS command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DBH}	Max(100,32UI)			ns

7.3.2 Serial Interface Timing Characteristics

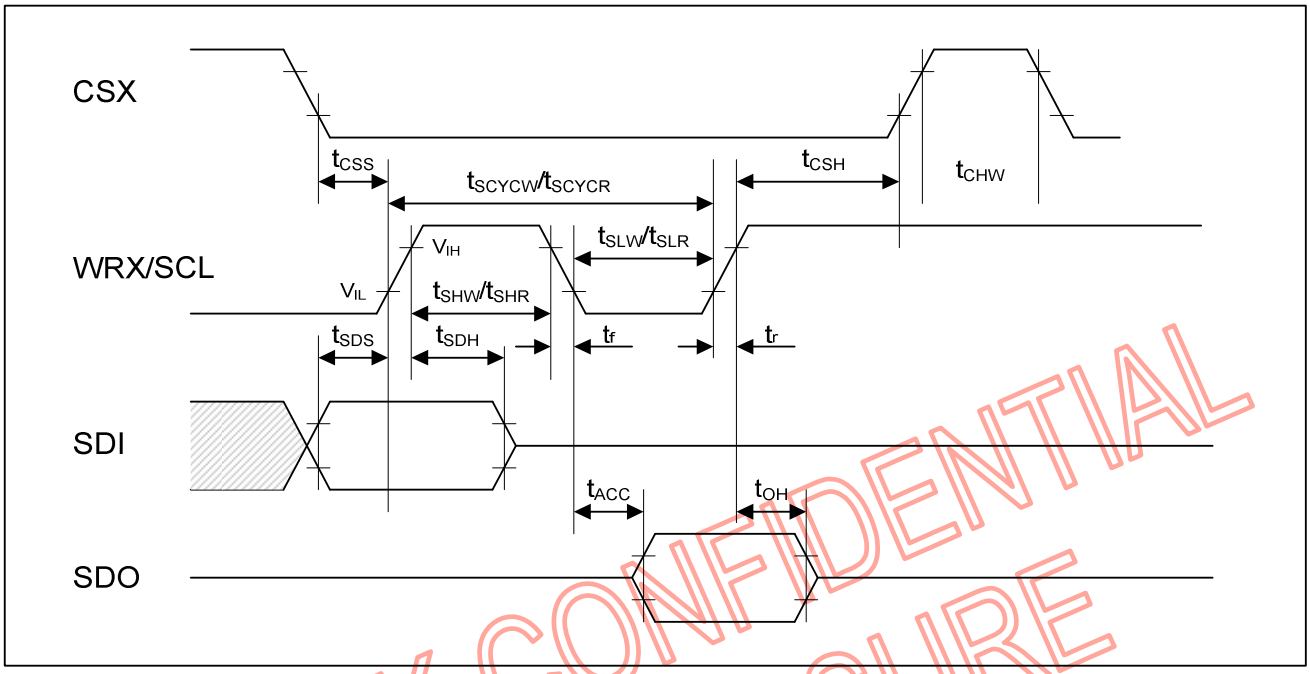


Figure 7.3.2 Serial Interface (9-bits) Operation

VCI= 2.5 V to 4.8 V, VDDI = 1.65V to 3.6V, VDDAM = 1.65V ~ 3.6V

Item	Symbol	Timing Diagram	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	t_{SCYCW}	Figure 7.3.2	100	-	20,000	ns
SCL clock cycle time Read (transmitted)	t_{SCYCR}	Figure 7.3.2	300	-	20,000	ns
SCL “High” pulse width Write (received)	t_{SHW}	Figure 7.3.2	40	-	-	ns
SCL “High” pulse width Read (transmitted)	t_{SHR}	Figure 7.3.2	140	-	-	ns
SCL “Low” pulse width Write (received)	t_{SLW}	Figure 7.3.2	40	-	-	ns
SCL “Low” pulse width Read (transmitted)	t_{SLR}	Figure 7.3.2	140	-	-	ns
SCL clock rise/fall time	t_r, t_f	Figure 7.3.2	-	-	10	ns
Chip select setup time	t_{CSS}	Figure 7.3.2	20	-	-	ns
Chip select hold time	t_{CSH}	Figure 7.3.2	50	-	-	ns
Input data setup time	t_{SDS}	Figure 7.3.2	20	-	-	ns
Input data hold time	t_{SDH}	Figure 7.3.2	20	-	-	ns
Output data access time	t_{ACC}	Figure 7.3.2	-	-	120	ns
Output data hold time	t_{OH}	Figure 7.3.2	5	-	-	ns
Chip deselect “High” pulse width	t_{CHW}	Figure 7.3.2	45	-	-	ns

7.3.3 I2C Bus Characteristics

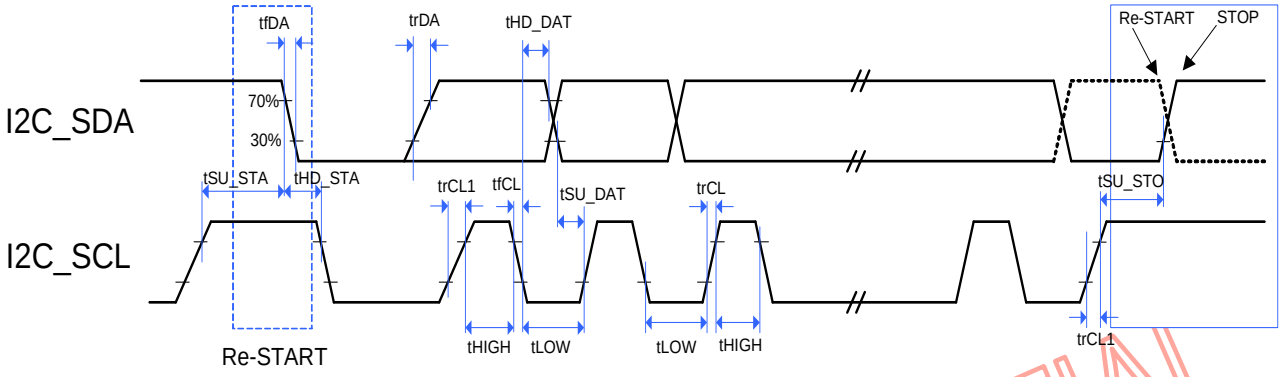


Figure 7.3.3 I2C-Bus Operation

Table 7.3.3 I2C-Bus Timing, VCI = 2.5 V to 4.8 V, VDDI = 1.65V to 3.6V, VDDAM = 1.65V ~ 3.6V

Item (High Speed Mode)	Timing Diagram	Symbol	Min.	Typ.	Max.	Unit
I2C_SCL clock frequency	Figure 7.3.3	Fscl	-	-	3.4	MHz
Hold time for START condition	Figure 7.3.3	t_{HD_STA}	160	-	-	ns
Set-up time for a repeated START condition	Figure 7.3.3	t_{SU_STA}	160	-	-	ns
LOW period of the I2C_SCL clock	Figure 7.3.3	t_{LOW}	160	-	-	ns
HIGH period of the I2C_SCL clock	Figure 7.3.3	t_{HIGH}	60	-	-	ns
Data hold time	Figure 7.3.3	t_{HD_DAT}	-	-	70	ns
Data set-up time	Figure 7.3.3	t_{SU_DAT}	10	-	-	ns
Rise time for I2C_SCL signal	Figure 7.3.3	t_{rCL}	10	-	40	ns
Rise time for I2C_SCL signal l after a repeated START condition and after an acknowledge bit	Figure 7.3.3	t_{rCL1}	10	-	80	ns
Rise time for I2C_SDA signal	Figure 7.3.3	t_{rDA}	10	-	80	ns
Fall time for I2C_SCL signal	Figure 7.3.3	t_{fCL}	10	-	40	ns
Fall time for I2C_SDA signal	Figure 7.3.3	t_{fDA}	10	-	80	ns
Set-up time for STOP condition	Figure 7.3.3	t_{SU_STO}	160	-	-	ns
Pulse width of spikes (must be suppressed by the input filter)	Figure 7.3.3	t_{SP}	-	-	10	ns
Noise margin at the LOW level	Figure 7.3.3	V_{nL}	0.1	-	-	VDDI
Noise margin at the HIGH level	Figure 7.3.3	V_{nH}	0.2	-	-	VDDI

Table 7.3.4 I2C-Bus Timing, VCI = 2.5 V to 4.8 V, VDDI = 1.65V to 3.6V, VDDAM = 1.65V ~ 3.6V

Item (Fast Mode)	Timing Diagram	Symbol	Min.	Typ.	Max.	Unit
I2C_SCL clock frequency	Figure 7.3.3	Fscl	-	-	400	KHz
Hold time for START condition	Figure 7.3.3	t_{HD_STA}	600	-	-	ns
Set-up time for a repeated START condition	Figure 7.3.3	t_{SU_STA}	600	-	-	ns
LOW period of the I2C_SCL clock	Figure 7.3.3	t_{LOW}	1.3	-	-	us
HIGH period of the I2C_SCL clock	Figure 7.3.3	t_{HIGH}	0.6	-	-	us
Data hold time	Figure 7.3.3	t_{HD_DAT}	5	-	70	us
Data set-up time	Figure 7.3.3	t_{SU_DAT}	100	-	-	ns
Rise time for I2C_SCL signal	Figure 7.3.3	t_{rCL}	-	-	300	ns
Rise time for I2C_SCL signal l after a repeated START condition and after an acknowledge bit	Figure 7.3.3	t_{rCL1}	-	-	300	ns
Rise time for I2C_SDA signal	Figure 7.3.3	t_{rDA}	-	-	300	ns
Fall time for I2C_SCL signal	Figure 7.3.3	t_{fCL}	-	-	300	ns
Fall time for I2C_SDA signal	Figure 7.3.3	t_{fDA}	-	-	300	ns
Set-up time for STOP condition	Figure 7.3.3	t_{SU_STO}	600	-	-	ns
Pulse width of spikes (must be suppressed by the input filter)	Figure 7.3.3	t_{SP}	-	-	50	ns
Noise margin at the LOW level	Figure 7.3.3	V_{nL}	0.1	-	-	VDDI
Noise margin at the HIGH level	Figure 7.3.3	V_{nH}	0.2	-	-	VDDI

7.3.4 Reset Timing Characteristics

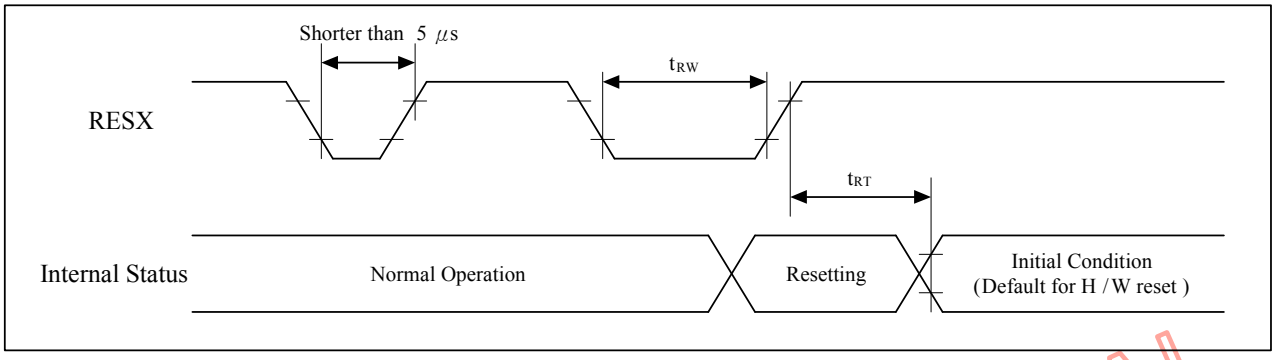


Figure 7.3.4 Reset Operation

Table 7.3.4 Reset Timing Characteristics VCI=2.5~4.8V, VDDI=1.65~3.6V, VDDAM=1.65~3.6V

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10(Note)	-	us
	t_{RT}	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms

Note：

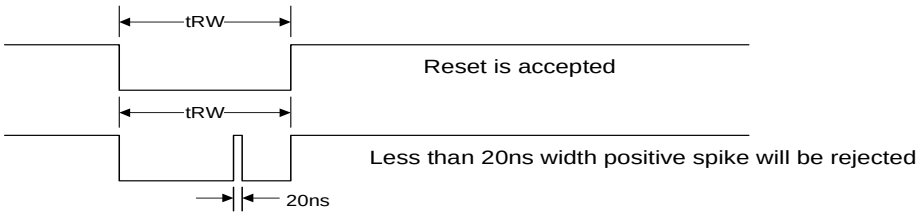
-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.

-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below ：

RESX	Pulse Action
Shorter than 5us	**Reset Rejected**
Longer than 9us	**Reset**
Between 5us and 9us	**Reset Starts**

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below ：



-When Reset applied during Sleep-In Mode.

-When Reset applied during Sleep-Out Mode.

-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.