NOVATEK
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Data Sheet

# *NT39416B*

## 1200CH TFT LCD Source Driver with TCON

***V0.4***

***Preliminary Spec***

## Revise History

| NT39416 Specification Revision History | | | |
|---|---|---|---|
| **Version** | **Content** | **Page** | **Date** |
| 0.0 | New Spec. | All | 2007/12/27 |
| 0.1 | Add Pad Coordinates | 36 | 2008/02/18 |
| 0.2 | Modify Timing Table | 29 | 2008/03/04 |
| 0.3 | Add BIST Pattern<br>Modify UPDN Pin Description<br>Modify RSTB Timing | 50<br>10<br>28 | 2008/03/19 |
| 0.4 | Modify Data Input Format<br>Modify Timing Characteristic | 21<br>22~25 | 2008/04/09 |

# Index

## Features

- Special design for small-sized color TFT LCD source drivers with timing controller
- Integrated 1200 channel source driver
- Supports display resolutions : 800(RGB)x600、800(RGB)x480
- 8-bit resolution 256 gray scale with 2-bits dithering
- Supports TTL 24-bit parallel (RGB) input timing
- Support cascade function with bidirectional shift control (CMOS signal)
- Support single or dual-gate operation mode
- Support Delta or Stripe color filter configuration
- Support stand-by mode for low power consumption
- Support dot inversion driving scheme
- V1 ~ V14 for adjusting Gamma correction
- Output dynamic range: 0.1 ~ AVDD-0.1V
- Power for source driver voltage AVDD: 6.5V ~ 13.5V
- Power for digital interface circuit VDD: 3.0 ~ 3.6V
- Operating frequency: 50 MHz
- COG package



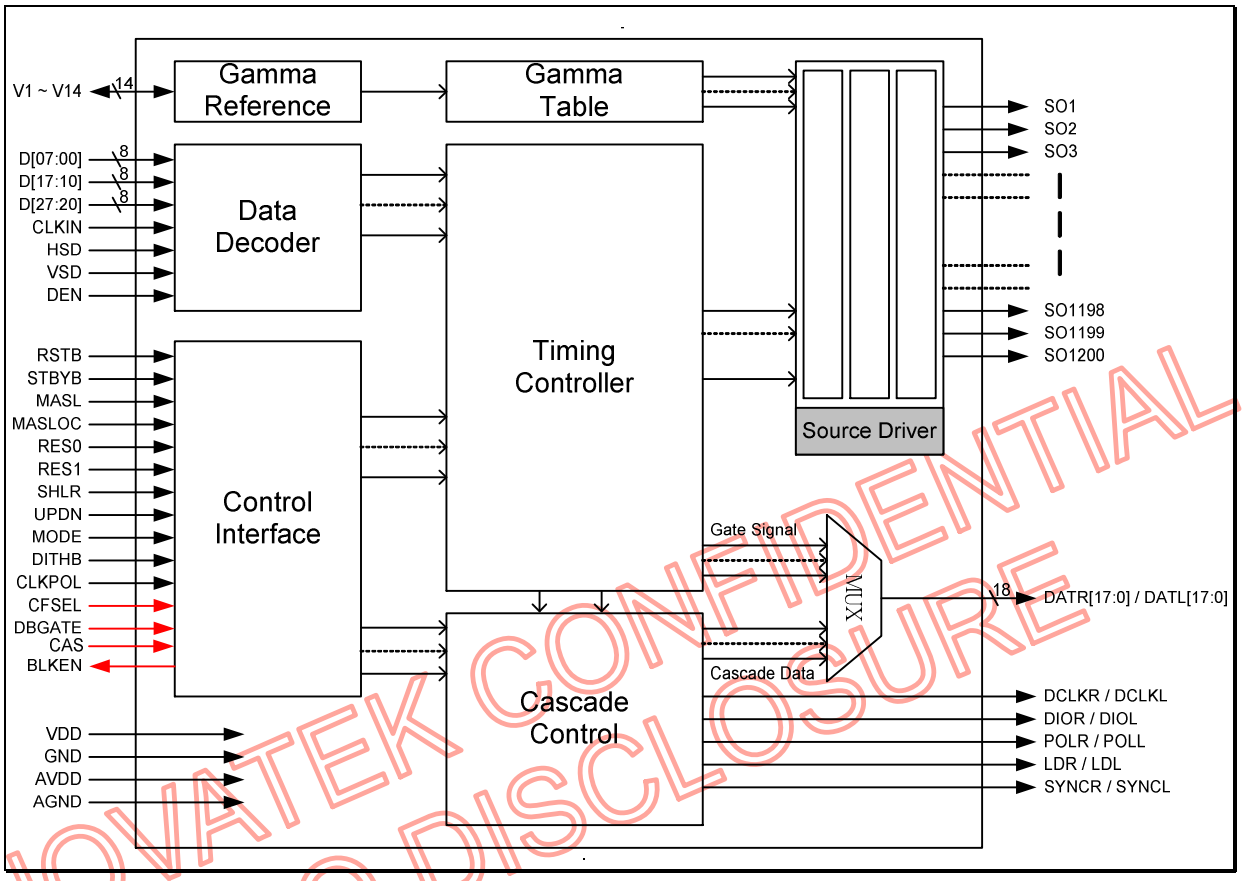
## General Description

NT39416 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. NT39416 integrated source driver, timing controller and pin control Interface.

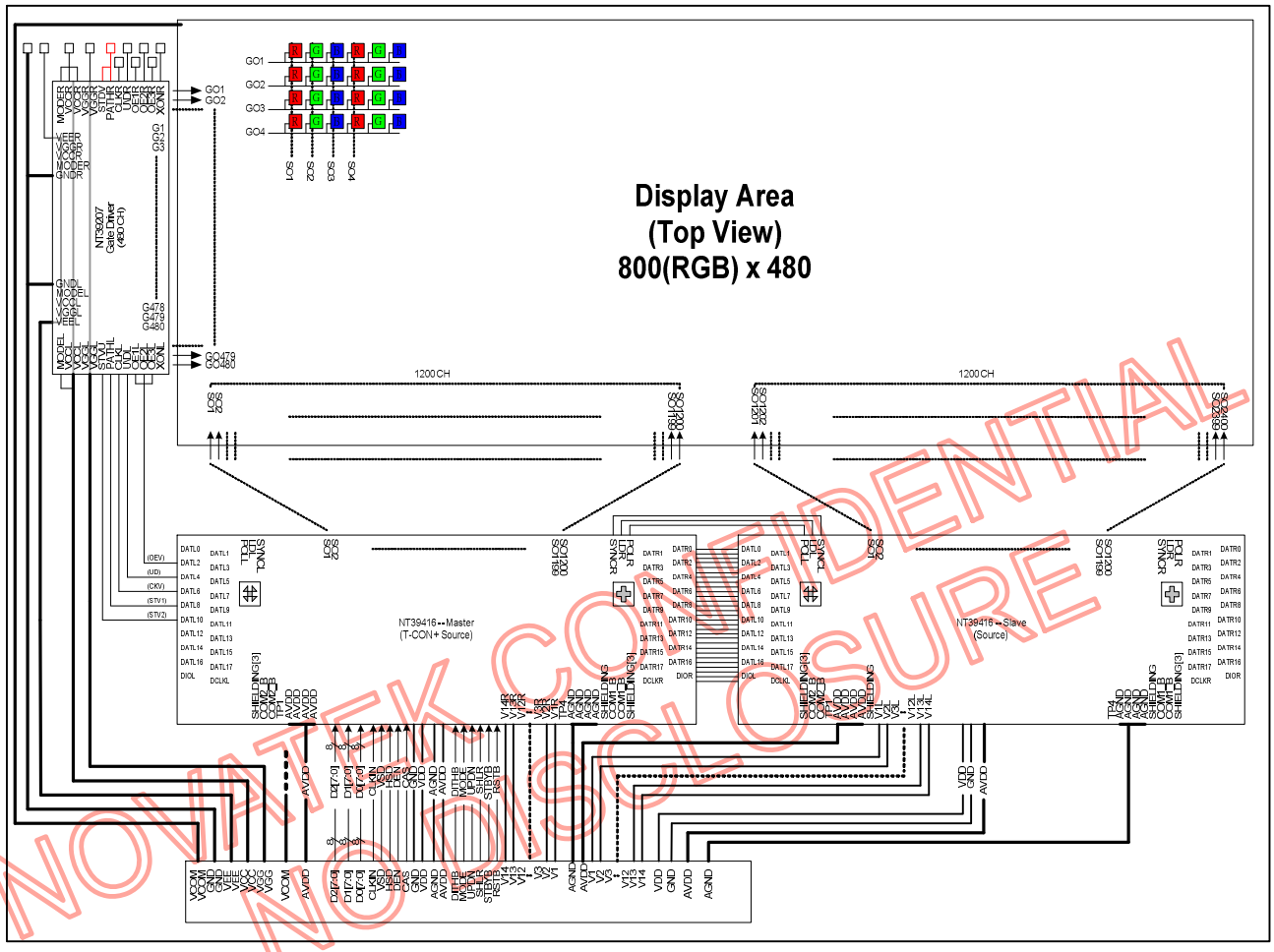
Input timing support TTL digital 24bit parallel RGB data format, and source output support 8-bit resolution 256 gray scale with dithering features. Operating parameters can be set via pin control for all control features. Special circuit architecture is designed for lower power dissipation.

NT39416 support two chip cascade operation mode to reduce the FPC amount and save the cost. Configure able Master and Slave configuration increase the flexibility for different panel design. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

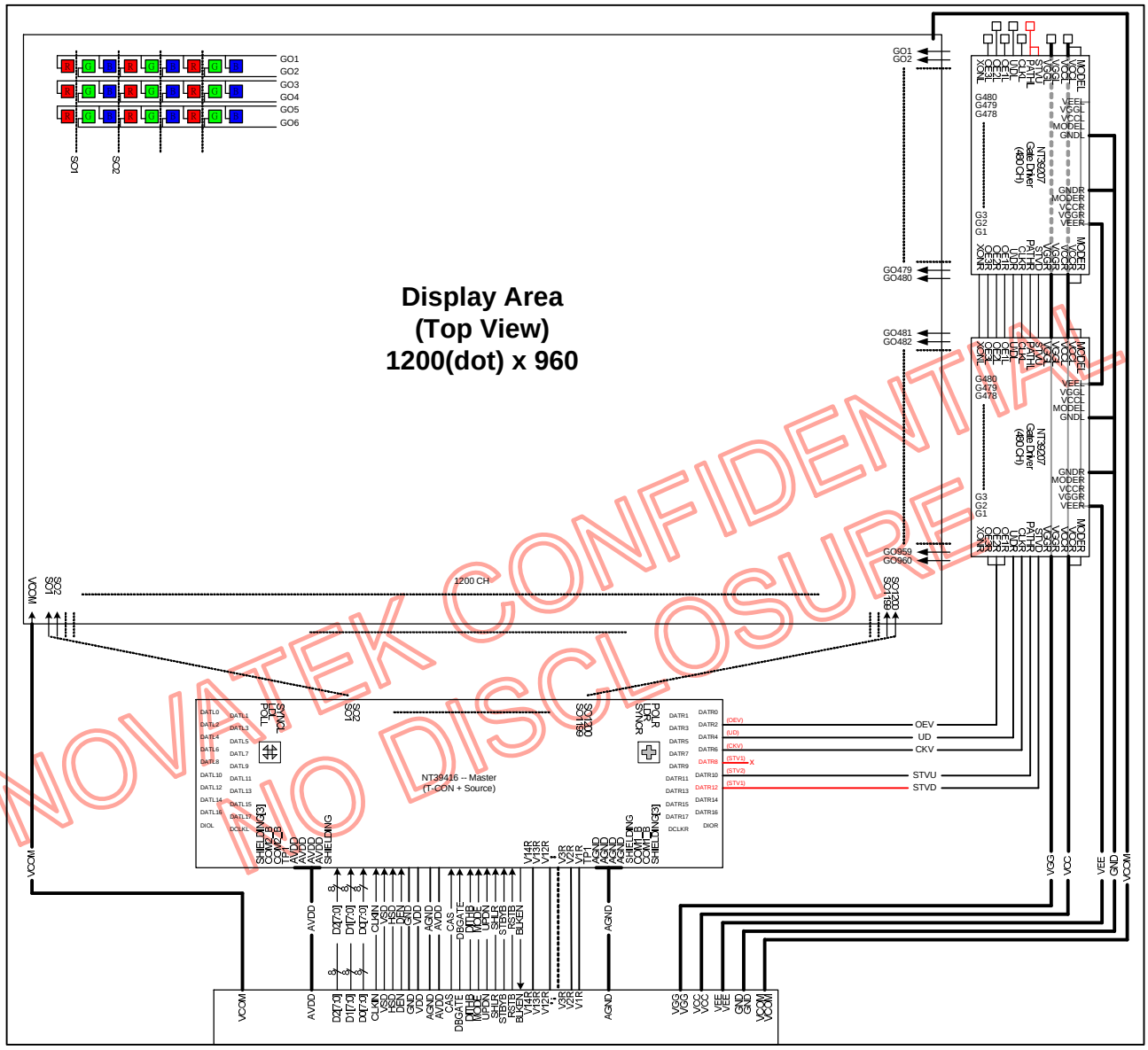
## Function Block Diagram



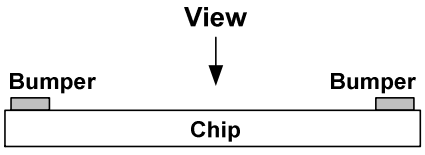
# Application Block Diagram – 2 Chip Cascade



# Application Block Diagram – Dual Gate Application



## Pad Sequence (Bump Side)

# Pad Description

**NT39416 Pad Description:**

| Designation | I/O | Description |
|---|---|---|
| D07~D00<br>D17~D10<br>D27~D20 | I | Parallel data Input. For TTL 24-bit parallel RGB image data input.<br>D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; DIN[27:20] = B[7:0] data.<br>For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND. |
| CLKIN | I | Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge. |
| HSD | I | Horizontal Sync input. Negative polarity. |
| VSD | I | Vertical Sync input. Negative polarity. |
| DEN | I | Data Input Enable. Active High to enable the data input bus under “DE Mode”.<br>Normally pull low. |
| MODE | I | DE / SYNC mode select. Normally pull high<br>H : DE mode.<br>L : HSD/VSD mode. |
| RES[1:0] | I | Display resolution selection.<br>RES[1:0] = “00”, for 800(RGB)*480 display resolution<br>RES[1:0] = “01”, for 800(RGB)*600 display resolution<br>RES[1:0] = “10”, for 400(RGB)*480 display resolution<br>RES[1:0] = “11”, for 400(RGB)*240 display resolution |
| DITHB | I | Dithering function enable control. Normally pull high<br>DITHB = “1”, Disable internal dithering function<br>DITHB = “0”, Enable internal dithering function |
| CLKPOL | I | Input clock edge selection. Normally pull low<br>CLKPOL = “1”, Latch data at CLKIN rising edge.<br>CLKPOL = “0”, Latch data at CLKIN falling edge. (Default) |
| BLKEN | O | Backlight enable control signal for external controller.<br>BLKEN = “1”, Logical control signal to turn on external backlight controller<br>BLKEN = “0”, Turn off external backlight controller<br>Note: Refer to the Power On/Off Sequence for the detail information. |
| CFSEL | I | Color Filter type selection. Normally pull high<br>CFSEL = “1”, Stripe mode. (Default)<br>CFSEL = “0”, Delta mode |
| DBGATE | I | Dual Gate function enables control. Normally pull low<br>DBGATE = “1”, Enable Dual Gate Function.<br>DBGATE = “0”, Disable Dual Gate Function (Default)<br>Note: Cascade function will be disabled under “dual gate” mode!! |
| V1 ~ V14 | I/O | Gamma correction reference voltage. These input voltage must be offered by user.<br>AGND<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< AVDD<br>V2, V6, V9, V13 is disable. Please make sure AVDD-1 ≧ V1. |
| RSTB | I | Global reset pin. Active Low to enter Reset State.<br>Suggest to connecting with an RC reset circuit for stability. Normally pull high. |
| STBYB | I | Standby mode, normally pulled high.<br>STBYB = “1”, normal operation<br>STBYB = “0”, timing controller, source driver will turn off, all output are High-Z |
| MASL | I | Master and Slave Mode selection. Normally pull high.<br>MASL = ”H”, for Master mode. (Default Mode)<br>MASL = ”L”, for Slave mode.<br>Only the Master chip will issue the Gate and Cascade control signal. |

| | | |
|---|---|---|
| MASLOC | I | Master location definition pin. Normally pull low.<br>MASLOC = ”L”, Master locate on right side (Panel top view). (Default Mode)<br>MASLOC = ”H”, Master locate on left side (Panel top view). |
| SHLR | I | Source Right or Left sequence control.<br>SHLR = “L”, shift left: last data = S1←S2←S3.....←S1200 = first data.<br>SHLR = “H”, shift right: first data = S1→S→S3.....→S1200 = last data. |
| UPDN | I | Gate Up or Down scan control. Normally pull low.<br>UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.<br>UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver. |
| BIST | I | Normal Operation/BIST pattern select. Normally pull low<br>BIST = H : BIST(DCLK input is not needed)<br>BIST = L : Normal Operation |
| CAS | I | Cascade function select. Normally pull high.<br>CAS = ”H”, Enable cascade function.<br>CAS = ”L”, Disable cascade function. |
| DATR[17:0] | I/O | Multi function I/O pin.<br>Refer to the Cascade DAT pin mapping table for the detail. |
| DCLKR | I/O | Master and Slave cascade control signal. |
| DIOR | I/O | Master and Slave cascade control signal. |
| POLR | I/O | Master and Slave cascade control signal. |
| LDR | I/O | Master and Slave cascade control signal. |
| SYNCR | I/O | Master and Slave cascade control signal. |
| DATL[17:0] | I/O | Multi function I/O pin.<br>Refer to the Cascade DAT pin mapping table for the detail. |
| DCLKL | I/O | Master and Slave cascade control signal. |
| DIOL | I/O | Master and Slave cascade control signal. |
| POLL | I/O | Master and Slave cascade control signal. |
| LDL | I/O | Master and Slave cascade control signal. |
| SYNCL | I/O | Master and Slave cascade control signal. |
| AVDD | PI | Power supply for analog circuits |
| AGND | PI | Ground pins for analog circuits |
| VDD | PI | Power supply for digital circuits |
| GND | PI | Ground pins for digital circuits |
| SO1~SO1200 | O | Source Driver Output Signals.<br>All outputs will be of unknown values under stand-by mode. |
| ALIGN | M | For assembly alignment. |
| COM1_B<br>COM1_B | S | Internal link together between input side and output side. |
| COM1_T<br>COM2_T | S | Internal link together between input side and output side. |
| TP5~0 | T | Test pin for Novatek only. Float these pins for normal operation. |
| SHIELDING | SH | IC Shielding pads.<br>Those pins are internally connected to the AGND.<br>DO NOT connect to any WOA on the panel. |
| DASHD | SH | Data Bus Shielding pad.<br>Those pins are internally connected to the GND.<br>RECOMMAND to add shielding lines on the FPC to reduce EMI. |
| DUM | D | Dummy pads.<br>Those pins are floating pads. |

**Note:**

**I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,**

**T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, C: Capacitor pin.**

**NT39416 Pass Line Description:**

| Pass Line No: | Pad Name | |
|---|---|---|
| 1 | COM1_B | COM1_T |
| 2 | COM2_B | COM2_T |

## Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

| Pin Name | Wiring resistance value(Ω) | Pin Name | Wiring resistance value(Ω) |
|---|---|---|---|
| VDD | <25 | DCLKR | < 200 & 20 pf |
| AVDD | <5 | DIOR | < 200 & 20 pf |
| GND | <25 | POLR | < 200 & 20 pf |
| AGND | <5 | LDR | < 200 & 20 pf |
| V1~V14 | <20 | SYNCR | < 200 & 20 pf |
| D00~D07 | <200 | DATRL17:0] | < 200 & 20 pf |
| D10~D17 | <200 | DCLKL | < 200 & 20 pf |
| D20~D27 | <200 | DIOL | < 200 & 20 pf |
| DEN | <200 | POLL | < 200 & 20 pf |
| MODE | <1K | LDL | < 200 & 20 pf |
| RES[1:0] | <1K | CASCADE V1~V14 | <50 |
| DITHB | <1K | CLKIN | <50 |
| CLKPOL | <1K | HSD | <200 |
| BLKEN | <1K | VSD | <200 |
| CFSEL | <1K | | |
| DBGATE | <1K | | |
| RSTB | <1K | | |
| MASL | <1K | | |
| MASLOC | <1K | | |
| SHLR | <1K | | |
| UPDN | <1K | | |
| BIST | <1K | | |
| CAS | <1K | | |
| DATR[17:0] | < 200 & 20 pf | | |

## DATR[17:0] / DTAL[17:0] pin mapping Table:

| DATR [17:0] | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "0"<br>CAS = "1" | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "1"<br>CAS = "1" | DBGATE = "0"<br>MASL = "0"<br>MASLOC = "0"<br>CAS = "1" | DBGATE = "0"<br>MASL = "0"<br>MASLOC = "1"<br>CAS = "1" | DBGATE = "1"<br>MASL = "1"<br>MASLOC = "X"<br>CAS = "0" | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "X"<br>RES[1:0]= "1X"<br>CAS = "0" |
|---|---|---|---|---|---|---|
| **Description** | Master for cascade.<br>Master locate on panel right side | Master for cascade.<br>Master locate on panel left side | Slave for cascade.<br>Master locate on panel right side | Slave for cascade.<br>Master locate on panel left side | Dual Gate Mode | Single Source Mode |
| DATR0 | X | DAT0 | DAT0 | X | X | X |
| DATR1 | X | DAT1 | DAT1 | X | X | X |
| DATR2 | OEV | DAT2 | DAT2 | X | OEV | OEV |
| DATR3 | X | DAT3 | DAT3 | X | X | X |
| DATR4 | UD | DAT4 | DAT4 | X | UD | UD |
| DATR5 | X | DAT5 | DAT5 | X | X | X |
| DATR6 | CKV | DAT6 | DAT6 | X | CKV | CKV |
| DATR7 | X | DAT7 | DAT7 | X | X | X |
| DATR8 | STV1 | DAT8 | DAT8 | X | STV1 | STV1 |
| DATR9 | X | DAT9 | DAT9 | X | X | X |
| DATR10 | STV2 | DAT10 | DAT10 | X | STV2 | STV2 |
| DATR11 | X | DAT11 | DAT11 | X | X | X |
| DATR12 | STV1 | DAT12 | DAT12 | X | STV1 | STV1 |
| DATR13 | X | DAT13 | DAT13 | X | X | X |
| DATR14 | X | DAT14 | DAT14 | X | X | X |
| DATR15 | X | DAT15 | DAT15 | X | X | X |
| DATR16 | STBN | DAT16 | DAT16 | X | STBN | STBN |
| DATR17 | X | DAT17 | DAT17 | X | X | X |
| DCLKR | X | DCLK | DCLK | X | X | X |
| DIOR | X | DIO | DIO | X | X | X |
| LDR | X | LD | LD | X | X | X |
| SYNCR | X | SYNC | SYNC | X | X | X |

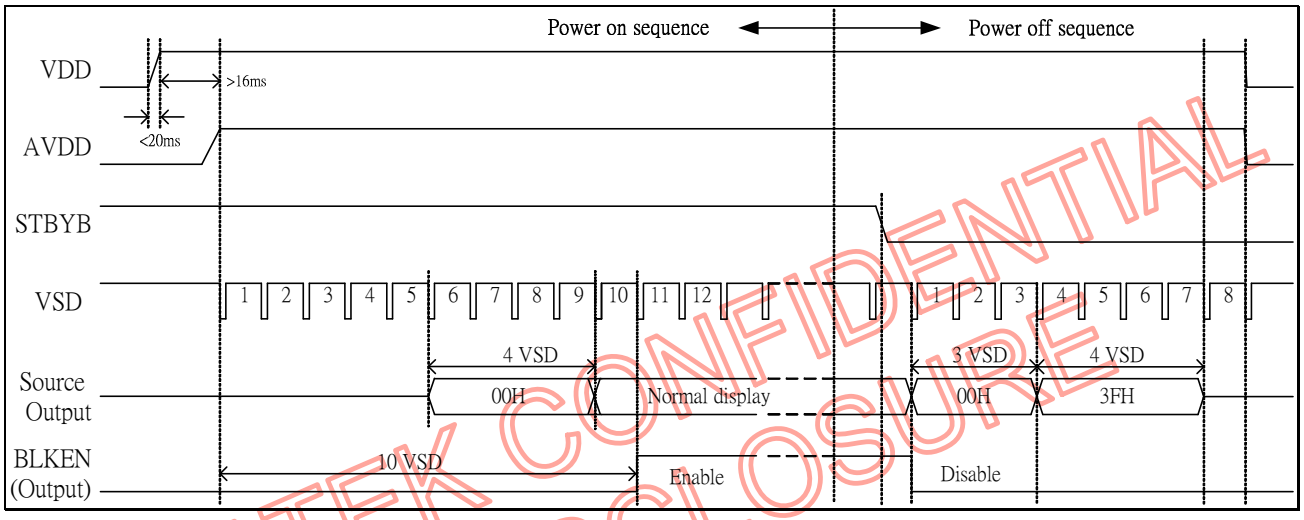
| DATL [17:0] | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "0"<br>CAS = "1" | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "1"<br>CAS = "1" | DBGATE = "0"<br>MASL = "0"<br>MASLOC = "0"<br>CAS = "1" | DBGATE = "0"<br>MASL = "0"<br>MASLOC = "1"<br>CAS = "1" | DBGATE = "1"<br>MASL = "1"<br>MASLOC = "X"<br>CAS = "0" | DBGATE = "0"<br>MASL = "1"<br>MASLOC = "X"<br>RES[1:0]= "1X"<br>CAS = "0" |
|---|---|---|---|---|---|---|
| **Description** | Master for cascade.<br>Master locate on panel right side | Master for cascade.<br>Master locate on panel left side | Slave for cascade.<br>Master locate on panel right side | Slave for cascade.<br>Master locate on panel left side | Dual Gate Mode | Single Source Mode |
| DATL0 | DAT0 | X | X | DAT0 | X | X |
| DATL1 | DAT1 | X | X | DAT1 | X | X |
| DATL2 | DAT2 | OEV | X | DAT2 | OEV | OEV |
| DATL3 | DAT3 | X | X | DAT3 | X | X |
| DATL4 | DAT4 | UD | X | DAT4 | UD | UD |
| DATL5 | DAT5 | X | X | DAT5 | X | X |
| DATL6 | DAT6 | CKV | X | DAT6 | CKV | CKV |
| DATL7 | DAT7 | X | X | DAT7 | X | X |
| DATL8 | DAT8 | STV1 | X | DAT8 | STV1 | STV1 |
| DATL9 | DAT9 | X | X | DAT9 | X | X |
| DATL10 | DAT10 | STV2 | X | DAT10 | STV2 | STV2 |
| DATL11 | DAT11 | X | X | DAT11 | X | X |
| DATL12 | DAT12 | STV1 | X | DAT12 | STV1 | STV1 |
| DATL13 | DAT13 | X | X | DAT13 | X | X |
| DATL14 | DAT14 | X | X | DAT14 | X | X |
| DATL15 | DAT15 | X | X | DAT15 | X | X |
| DATL16 | DAT16 | STBN | X | DAT16 | STBN | STBN |
| DATL17 | DAT17 | X | X | DAT17 | X | X |
| DCLKL | DCLK | X | X | DCLK | X | X |
| DIOL | DIO | X | X | DIO | X | X |
| LDL | LD | X | X | LD | X | X |
| SYNCL | SYNC | X | X | SYNC | X | X |

# Function Description

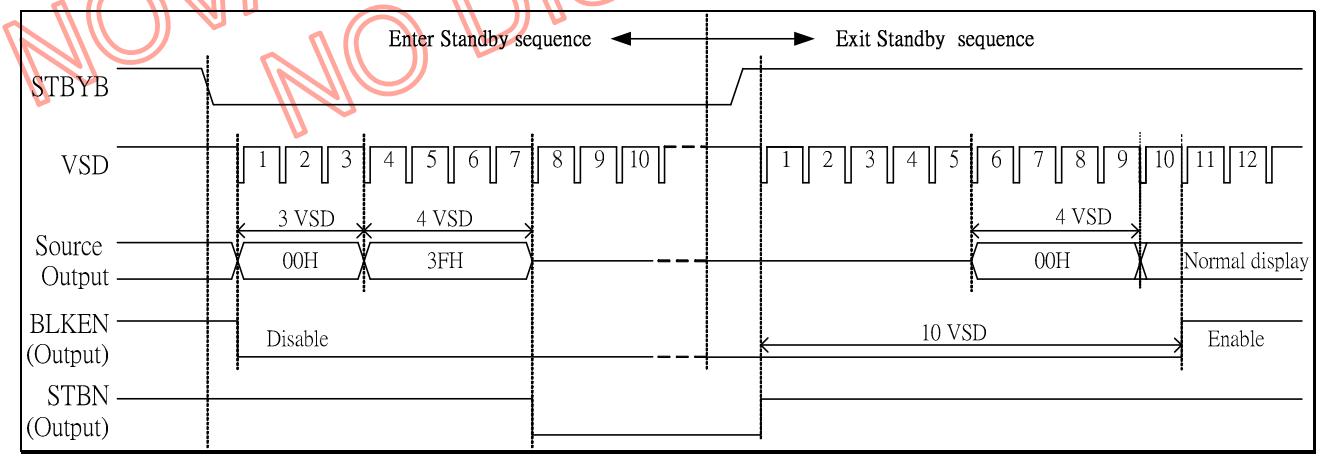
## Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time ($T_{POR}$) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

### Power-On/Off Timing Sequence:




### Enter and Exit Standby Mode Sequence:



## Input Data VS Output Channels

### 1. DBGATE="0", CFSEL="1", Stripe Mode

(1) SHLR="1" , right shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | First data | | | → | Last data | | |
| Odd Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |
| Even Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |

(2) SHLR="0", left shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | Last data | | | ← | First data | | |
| Odd Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |
| Even Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |

### 2. DBGATE="0", CFSEL="0", Delta Mode

(1) SHLR="1" , right shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | First data | | | → | Last data | | |
| Odd Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |
| Even Line | D17~D10 | D27~D20 | D07~D00 | - - - | D17~D10 | D27~D20 | D07~D00 |

(2) SHLR="0", left shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | Last data | | | ← | First data | | |
| Odd Line | D07~D00 | D17~D10 | D27~D20 | - - - | D07~D00 | D17~D10 | D27~D20 |
| Even Line | D17~D10 | D27~D20 | D07~D00 | - - - | D17~D10 | D27~D20 | D07~D00 |

### 3. DBGATE="1", CFSEL="1", Stripe Mode

(1) SHLR="1" , right shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | First data | | | → | Last data | | |
| Odd Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Odd Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Even Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |

(2) SHLR="0", left shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | Last data | | | ← | First data | | |
| Odd Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Odd Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Even Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |

### 4. DBGATE="1", CFSEL="0", Delta Mode

(1) SHLR="1" , right shift

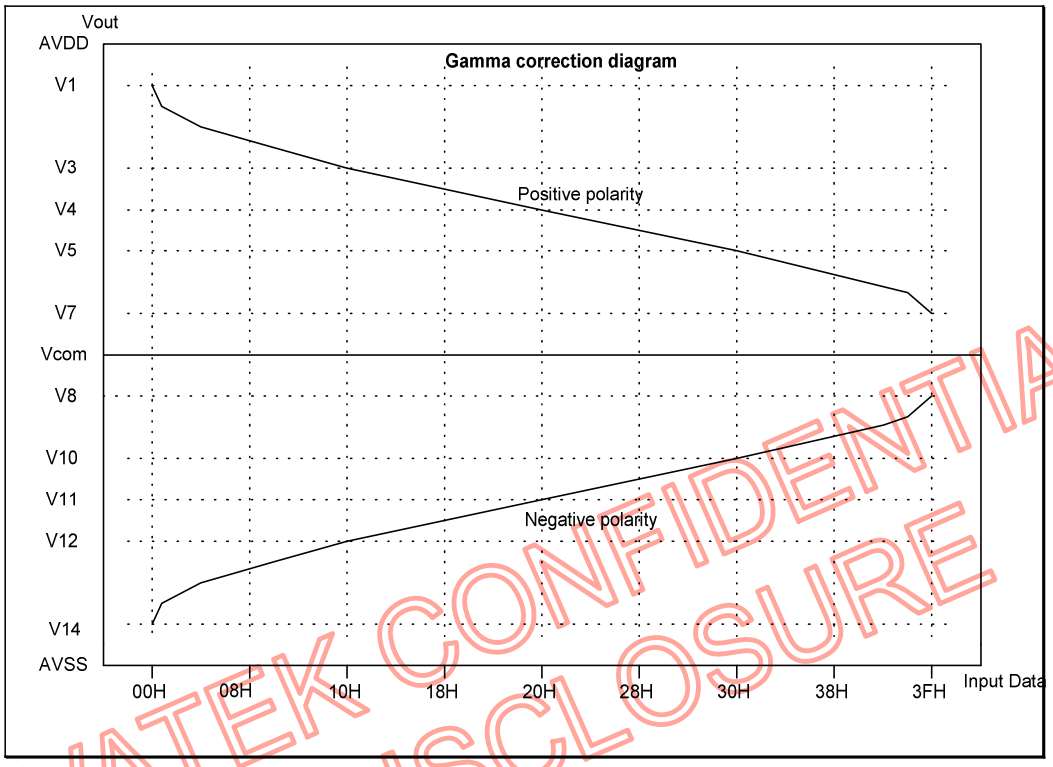
| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | First data | | | → | Last data | | |
| Odd Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Odd Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn+1 | D27~D20 | D17~D10 | D07~D00 | - - - | D27~D20 | D17~D10 | D07~D00 |

(2) SHLR="0", left shift

| Output | SO1 | SO2 | SO3 | - - - | SO1198 | SO1199 | SO1200 |
|---|---|---|---|---|---|---|---|
| Order | Last data | | | ← | First data | | |
| Odd Line /Gn | D07~D00 | D27~D20 | D17~D10 | - - - | D07~D00 | D27~D20 | D17~D10 |
| Odd Line /Gn+1 | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn | D17~D10 | D07~D00 | D27~D20 | - - - | D17~D10 | D07~D00 | D27~D20 |
| Even Line /Gn+1 | D27~D20 | D17~D10 | D07~D00 | - - - | D27~D20 | D17~D10 | D07~D00 |

## Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.




Remark: AVDD-1 ≥ V1 ≥ V3 ≥ V4 ≥ V5 ≥ V7; V8 ≥V10 ≥ V11 ≥ V12 ≥ V14 ≥ AGND+0.1V

## Gamma correction resistor ratio

| Name | Resistor | Name | Resistor |
|---|---|---|---|
| R0 | 6.4 | R32 | 0.8 |
| R1 | 6 | R33 | 0.8 |
| R2 | 5.6 | R34 | 0.8 |
| R3 | 5.2 | R35 | 0.8 |
| R4 | 4.8 | R36 | 0.8 |
| R5 | 4.4 | R37 | 0.8 |
| R6 | 4.4 | R38 | 0.8 |
| R7 | 4 | R39 | 0.8 |
| R8 | 4 | R40 | 0.8 |
| R9 | 3.2 | R41 | 0.8 |
| R10 | 3.2 | R42 | 0.8 |
| R11 | 2.8 | R43 | 0.8 |
| R12 | 2.8 | R44 | 0.8 |
| R13 | 2.8 | R45 | 0.8 |
| R14 | 2.4 | R46 | 0.8 |
| R15 | 2.4 | R47 | 0.8 |
| R16 | 2.4 | R48 | 0.8 |
| R17 | 2 | R49 | 0.8 |
| R18 | 2 | R50 | 0.8 |
| R19 | 2 | R51 | 0.8 |
| R20 | 1.6 | R52 | 0.8 |
| R21 | 1.6 | R53 | 1.2 |
| R22 | 1.6 | R54 | 1.2 |
| R23 | 1.2 | R55 | 1.2 |
| R24 | 1.2 | R56 | 1.6 |
| R25 | 1.2 | R57 | 1.6 |
| R26 | 1.2 | R58 | 2 |
| R27 | 0.8 | R59 | 2 |
| R28 | 0.8 | R60 | 2.4 |
| R29 | 0.8 | R61 | 4 |
| R30 | 0.8 | R62 | 6.4 |
| R31 | 0.8 | | |

V1, V14 →
← V4, V11
V3. V12 →
← V5, V10
V4, V11 →
← V7, V8

## Output Voltage VS Input Data

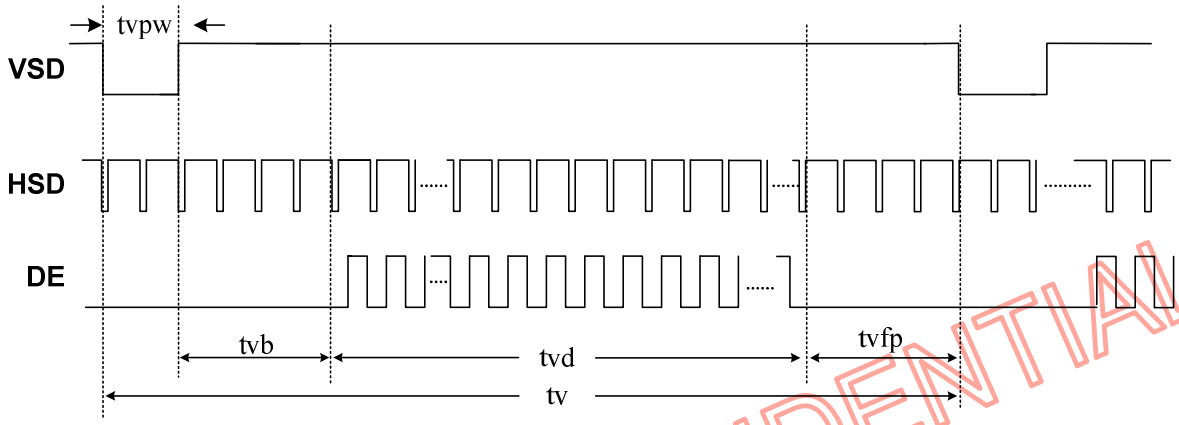
| | Positive polarity Output Voltage | Negative polarity Output Voltage |
|---|---|---|
| **00H** | V1 | V14 |
| **01H** | V3 + ( V1 – V3)X 58 / 64.4 | V14+ ( V12 – V14)X 6.4 / 64.4 |
| **02H** | V3 + ( V1 – V3)X 52 / 64.4 | V14+ ( V12 – V14)X 12.4 / 64.4 |
| **03H** | V3 + ( V1 – V3)X 46.4 / 64.4 | V14+ ( V12 – V14)X 18 / 64.4 |
| **04H** | V3 + ( V1 – V3)X 41.2 / 64.4 | V14+ ( V12 – V14)X 23.2 / 64.4 |
| **05H** | V3 + ( V1 – V3)X 36.4 / 64.4 | V14 + ( V12 – V14)X 28 / 64.4 |
| **06H** | V3 + ( V1 – V3)X 32 / 64.4 | V14 + ( V12 – V14)X 32.4 / 64.4 |
| **07H** | V3 + ( V1 – V3)X 27.6 / 64.4 | V14 + ( V12 – V14)X 36.8 / 64.4 |
| **08H** | V3 + ( V1 – V3)X 23.6 / 64.4 | V14 + ( V12 – V14)X 40.8 / 64.4 |
| **09H** | V3 + ( V1 – V3)X 19.6 / 64.4 | V14 + ( V12 – V14)X 44.8 / 64.4 |
| **0AH** | V3 + ( V1 – V3)X 16.4 / 64.4 | V14 + ( V12 – V14)X 48 / 64.4 |
| **0BH** | V3 + ( V1 – V3)X 13.2 / 64.4 | V14 + ( V12 – V14)X 51.2 / 64.4 |
| **0CH** | V3 + ( V1 – V3)X 10.4 / 64.4 | V14 + ( V12 – V14)X 57 / 64.4 |
| **0DH** | V3 + ( V1 – V3)X 7.6 / 64.4 | V14 + ( V12 – V14)X 56.8 / 64.4 |
| **0EH** | V3 + ( V1 – V3)X 4.8 / 64.4 | V14 + ( V12 – V14)X 59.6 / 64.4 |
| **0FH** | V3 + ( V1 – V3)X 2.4 / 64.4 | V14 + ( V12 – V14)X 62 / 64.4 |
| **10H** | V3 | V12 |
| **11H** | V4 + (V3 – V4) X 19.6 / 22 | V12 + ( V11 – V12)X 2.4 / 22 |
| **12H** | V4 + (V3 – V4) X 17.6 / 22 | V12 + ( V11 – V12)X 4.4 / 22 |
| **13H** | V4 + (V3 – V4) X 15.6 / 22 | V12 + ( V11 – V12)X 6.4 / 22 |
| **14H** | V4 + (V3 – V4) X 13.6 / 22 | V12 + ( V11 – V12)X 8.4 / 22 |
| **15H** | V4 + (V3 – V4) X 12 / 22 | V12 + ( V11 – V12)X 10 / 22 |
| **16H** | V4 + (V3 – V4) X 10.4 / 22 | V12 + ( V11 – V12)X 11.6 / 22 |
| **17H** | V4 + (V3 – V4) X 8.8 / 22 | V12 + ( V11 – V12)X 13.2 / 22 |
| **18H** | V4 + (V3 – V4) X 7.6 / 22 | V12 + ( V11 – V12)X 14.4 / 22 |
| **19H** | V4 + (V3 – V4) X 6.4 / 22 | V12 + ( V11 – V12)X 15.6 / 22 |
| **1AH** | V4 + (V3 – V4) X 5.2 / 22 | V12 + ( V11 – V12)X 16.8 / 22 |
| **1BH** | V4 + (V3 – V4) X 4 / 22 | V12 + ( V11 – V12)X 18 / 22 |
| **1CH** | V4 + (V3 – V4) X 3.2 / 22 | V12 + ( V11 – V12)X 18.8 / 22 |
| **1DH** | V4 + (V3 – V4) X 2.4 / 22 | V12 + ( V11 – V12)X 19.6 / 22 |
| **1EH** | V4 + (V3 – V4) X 1.6 / 22 | V12 + ( V11 – V12)X 20.4 / 22 |
| **1FH** | V4 + (V3 – V4) X 0.8 / 22 | V12 + ( V11 – V12)X 21.2 / 22 |

(continued)

| Data | Positive polarity Output Voltage | Negative polarity Output Voltage |
|---|---|---|
| **20H** | V4 | V11 |
| **21H** | V5 + (V4 – V5) X 12 / 12.8 | V11 + ( V10 – V11) X 0.8 / 12.8 |
| **22H** | V5 + (V4 – V5) X 11.2 / 12.8 | V11 + ( V10 – V11) X 1.6 / 12.8 |
| **23H** | V5 + (V4 – V5) X 10.4 / 12.8 | V11 + ( V10 – V11) X 2.4 / 12.8 |
| **24H** | V5 + (V4 – V5) X 9.6 / 12.8 | V11 + ( V10 – V11) X 3.2 / 12.8 |
| **25H** | V5 + (V4 – V5) X 8.8 / 12.8 | V11 + ( V10 – V11) X 4 / 12.8 |
| **26H** | V5 + (V4 – V5) X 8 / 12.8 | V11 + ( V10 – V11) X 4.8 / 12.8 |
| **27H** | V5 + (V4 – V5) X 7.2 / 12.8 | V11 + ( V10 – V11) X 5.6 / 12.8 |
| **28H** | V5 + (V4 – V5) X 6.4 / 12.8 | V11 + ( V10 – V11) X 6.4 / 12.8 |
| **29H** | V5 + (V4 – V5) X 5.6 / 12.8 | V11 + ( V10 – V11) X 7.2 / 12.8 |
| **2AH** | V5 + (V4 – V5) X 4.8 / 12.8 | V11 + ( V10 – V11) X 8 / 12.8 |
| **2BH** | V5 + (V4 – V5) X 4 / 12.8 | V11 + ( V10 – V11) X 8.8 / 12.8 |
| **2CH** | V5 + (V4 – V5) X 3.2 / 12.8 | V11 + ( V10 – V11) X 9.6 / 12.8 |
| **2DH** | V5 + (V4 – V5) X 2.4 / 12.8 | V11 + ( V10 – V11) X 10.4 / 12.8 |
| **2EH** | V5 + (V4 – V5) X 1.6 / 12.8 | V11 + ( V10 – V11) X 11.2 / 12.8 |
| **2FH** | V5 + (V4 – V5) X 0.8 / 12.8 | V11 + ( V10 – V11) X 12 / 12.8 |
| **30H** | V5 | V10 |
| **31H** | V7 + (V5 – V7) X 26.8 / 27.6 | V10 + ( V8 – V10) X 0.8 / 27.6 |
| **32H** | V7 + (V5 – V7) X 26 / 27.6 | V10 + ( V8 – V10) X 1.6 / 27.6 |
| **33H** | V7 + (V5 – V7) X 25.2 / 27.6 | V10 + ( V8 – V10) X 2.4 / 27.6 |
| **34H** | V7 + (V5 – V7) X 24.4 / 27.6 | V10 + ( V8 – V10) X 3.2 / 27.6 |
| **35H** | V7 + (V5 – V7) X 23.6 / 27.6 | V10 + ( V8 – V10) X 4 / 27.6 |
| **36H** | V7 + (V5 – V7) X 22.4 / 27.6 | V10 + ( V8 – V10) X 5.2 / 27.6 |
| **37H** | V7 + (V5 – V7) X 21.2 / 27.6 | V10 + ( V8 – V10) X 6.4 / 27.6 |
| **38H** | V7 + (V5 – V7) X 20 / 27.6 | V10 + ( V8 – V10) X 7.6 / 27.6 |
| **39H** | V7 + (V5 – V7) X 18.4 / 27.6 | V10 + ( V8 – V10) X 9.2 / 27.6 |
| **3AH** | V7 + (V5 – V7) X 16.8 / 27.6 | V10 + ( V8 – V10) X 10.8 / 27.6 |
| **3BH** | V7 + (V5 – V7) X 14.8 / 27.6 | V10 + ( V8 – V10) X 12.8 / 27.6 |
| **3CH** | V7 + (V5 – V7) X 12.8 / 27.6 | V10 + ( V8 – V10) X 14.8 / 27.6 |
| **3DH** | V7 + (V5 – V7) X 10.4 / 27.6 | V10 + ( V8 – V10) X 17.2 / 27.6 |
| **3EH** | V7 + (V5 – V7) X 6.4 / 27.6 | V10 + ( V8 – V10) X 21.2 / 27.6 |
| **3FH** | V7 | V8 |

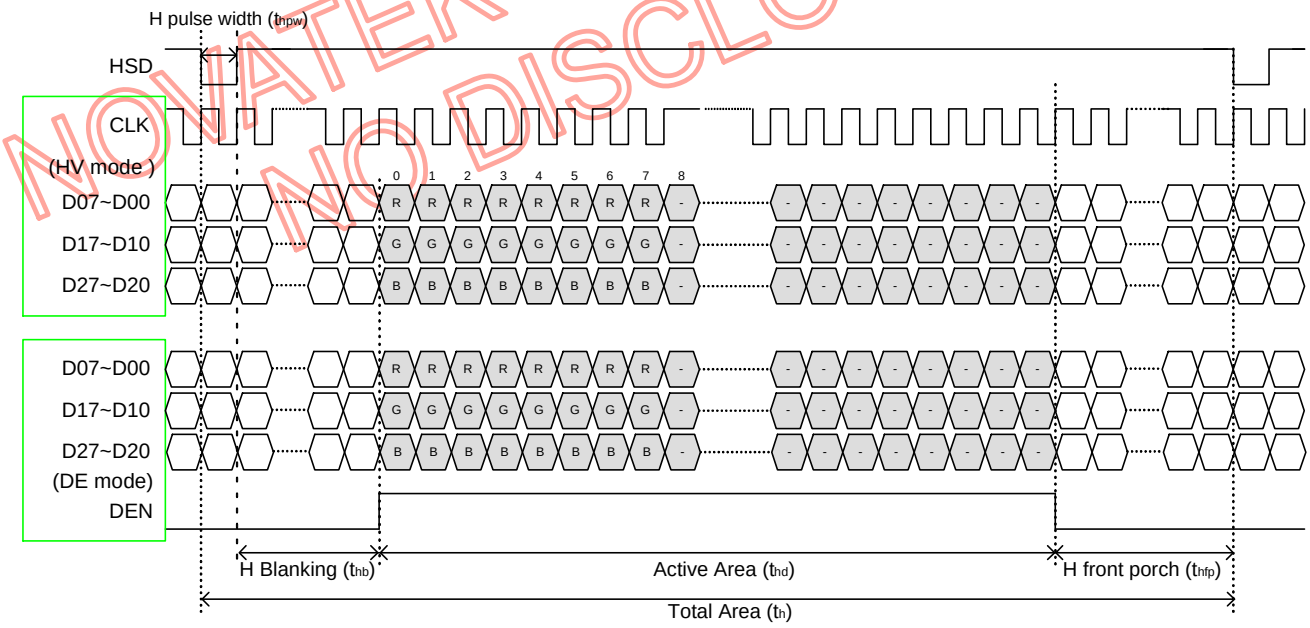
# Data Input Format

### Vertical input timing






### Horizontal input timing



# Timing Characteristic

## For 800x480 panel

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| Horizontal display area | | thd | | 800 | | DCLK | |
| DCLK frequency | | fclk | Min. | Typ. | Max. | | |
| | | | - | 33.3 | 50 | MHz | |
| 1 Horizontal Line | | th | | 928 | | DCLK | |
| HSD pulse width | Min. | thpw | | 1 | | DCLK | thb+thpw=88 DCLK is fixed. |
| | Typ. | | | 48 | | | |
| | Max. | | | - | | | |
| HSD Back Porch (Blanking) | | thb | - | 40 | | | |
| HSD Front Porch | | thfp | - | 40 | | | |

Vertical input timing

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Vertical display area | tvd | | 480 | | H | |
| VSD period time | tv | - | 525 | | H | tvpw+tvb=32H Is fixed |
| VSD pulse width | tvpw | 1 | 3 | | H | |
| VSD Back Porch (Blanking) | tvb | - | 29 | | H | |
| VSD Front Porch | tvfp | - | 13 | | H | |

## For 800x600 panel

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| Horizontal display area | | thd | 800 | | | DCLK | |
| DCLK frequency | | fclk | **Min.** | **Typ.** | **Max.** | | |
| | | | - | 40 | 50 | MHz | |
| 1 Horizontal Line | | th | 1000 | | | DCLK | |
| HSD pulse width | Min. | thpw | 1 | | | | thb+thpw=88 DCLK is fixed. |
| | Typ. | | 48 | | | | |
| | Max. | | - | | | | |
| HSD Back Porch (Blanking) | | thb | - | 40 | | | |
| HSD Front Porch | | thfp | - | 112 | | | |

Vertical input timing

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Vertical display area | tvd | | 600 | | H | |
| VSD period time | tv | - | 660 | | H | tvpw+tvb=39H Is fixed |
| VSD pulse width | tvpw | 1 | 3 | | H | |
| VSD Back Porch (Blanking) | tvb | - | 36 | | H | |
| VSD Front Porch | tvfp | - | 21 | | H | |

## For 400x480 panel

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| Horizontal display area | | thd | 400 | | | DCLK | |
| DCLK frequency | | fclk | **Min.** | **Typ.** | **Max.** | | |
| | | | - | 40 | 50 | MHz | |
| 1 Horizontal Line | | th | 520 | | | DCLK | |
| HSD pulse width | Min. | thpw | 1 | | | | thb+thpw=88 DCLK is fixed. |
| | Typ. | | 48 | | | | |
| | Max. | | - | | | | |
| HSD Back Porch (Blanking) | | thb | - | 40 | | | |
| HSD Front Porch | | thfp | - | 32 | | | |

Vertical input timing

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Vertical display area | tvd | | 480 | | H | |
| VSD period time | tv | - | 525 | | H | tvpw+tvb=32H Is fixed |
| VSD pulse width | tvpw | 1 | 3 | | H | |
| VSD Back Porch (Blanking) | tvb | - | 29 | | H | |
| VSD Front Porch | tvfp | - | 13 | | H | |

## For 400x240 panel

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| Horizontal display area | | thd | 400 | | | DCLK | |
| DCLK frequency | | fclk | **Min.** | **Typ.** | **Max.** | | |
| | | | - | 40 | 50 | MHz | |
| 1 Horizontal Line | | th | 520 | | | DCLK | |
| HSD pulse width | Min. | thpw | 1 | | | | thb+thpw=88 DCLK is fixed. |
| | Typ. | | 48 | | | | |
| | Max. | | - | | | | |
| HSD Back Porch (Blanking) | | thb | - | 40 | | | |
| HSD Front Porch | | thfp | - | 32 | | | |

Vertical input timing

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Vertical display area | tvd | | 240 | | H | |
| VSD period time | tv | - | 270 | | H | tvpw+tvb=17H Is fixed |
| VSD pulse width | tvpw | - | 1 | | H | |
| VSD Back Porch (Blanking) | tvb | - | 16 | | H | |
| VSD Front Porch | tvfp | - | 13 | | H | |

# Absolute Maximum Ratings

## VOLTAGE

(GND = AGND = 0V, TA = 25°C)

| | MIN. | MAX. | UNIT |
|---|---|---|---|
| **Digital Supply Voltage, VDD** | -0.5 | +5.0 | **V** |
| **Analog Supply Voltage, AVDD, V1~V14** | -0.5 | +15.0 | **V** |

## TEMPERATURE

| | MIN. | MAX. | UNIT |
|---|---|---|---|
| **Operating temperature** | -20 | +85 | **°C** |
| **Storage temperature** | -55 | +125 | **°C** |

***Comments**

**Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.**

# Recommended Operating Range

(GND = AGND = 0V, TA = -20 to +85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Digital supply voltage** | **VDD** | 3.0 | 3.3 | 3.6 | **V** |
| **Analog supply voltage** | **AVDD** | 6.5 | -- | 13.5 | **V** |
| **Digital input voltage** | **VIN** | 0 | - | VCC | **V** |

## DC Electrical Characteristics

(VDD= 3.0 to 3.6V, AVDD= 6.5 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Low level input voltage | Vil | 0 | - | 0.3xVDD | V | For the digital circuit |
| High level input voltage | Vih | 0.7xVDD | - | VDD | V | For the digital circuit |
| Input leakage current | Ii | - | - | ±1 | μA | For the digital circuit |
| High level output voltage | Voh | VDD-0.4 | - | - | V | Ioh= -400μA |
| Low level output voltage | Vol | - | - | GND+0.4 | V | Iol= +400μA |
| Pull low/high resistor | Ri | 200K | 250K | 300K | ohm | For the digital input pin @ VDD=3.3V |
| Digital Operation current | Idd | - | 8 (TBD) | 10 (TBD) | mA | Fclk=50 MHz, FLD=48KHz, VDD=3.3V |
| Digital Stand-by current | Ist1 | - | 10 (TBD) | 50 (TBD) | μA | Clock & all functions are stopped |
| Analog Operating Current | Idda | - | 10 (TBD) | 12 (TBD) | mA | No load, Fclk=50MHz, FLD=48KHz @ AVDD=10V,V1=8V, V14=0.4V |
| Analog Stand-by current | Ist2 | - | 10 (TBD) | 50 (TBD) | μA | No load, Clock & all functions are stopped |
| Input level of V1 ~ V7 | Vref1 | 0.4* AVDD | - | AVDD-1 | V | Gamma correction voltage input |
| Input level of V8 ~ V14 | Vref2 | 0.1 | - | 0.6* AVDD | V | Gamma correction voltage input |
| Output Voltage deviation | Vod1 | - | ±20 | ±35 | mV | Vo = AGND+0.1V ~ AGND+0.5V & Vo = AVDD-0.5V ~ AVDD-0.1V |
| Output Voltage deviation | Vod2 | - | ±15 | ±20 | mV | Vo = AGND+0.5V ~ AVDD-0.5V |
| Output Voltage Offset between Chips | Voc | - | - | ±20 | mV | Vo = AGND+0.5V ~ AVDD-0.5V |
| Dynamic Range of Output | Vdr | 0.1 | - | AVDD-0.1 | V | SO1 ~ SO1200 |
| Sinking Current of Outputs | IOLy | 80 | - | - | uA | SO1 ~ SO1200; Vo=0.1V v.s 1.0V , AVDD=13.5V |
| Driving Current of Outputs | IOHy | 80 | - | - | uA | SO1 ~ SO1200; Vo=13.4V v.s 12.5V , AVDD=13.5V |
| Resistance of Gamma Table | Rg | 0.7*Rn | 1.0*Rn | 1.3*Rn | ohm | Rn: Internal gamma resistor |

## AC Electrical Characteristics

(VDD= 3.0 to 3.6V, AVDD= 6.5 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| VDD Power On Slew rate | $T_{POR}$ | - | - | 20 | ms | From 0V to 90% VDD |
| RSTB pulse width | $T_{Rst}$ | 50 | - | - | us | CLKIN = 50MHz |
| CLKIN cycle time | Tcph | 20 | | | ns | |
| CLKIN pulse duty | Tcwh | 40 | 50 | 60 | % | |
| VSD setup time | Tvst | 8 | - | - | ns | |
| VSD hold time | Tvhd | 8 | - | - | ns | |
| HSD setup time | Thst | 8 | - | - | ns | |
| HSD hold time | Thhd | 8 | - | - | ns | |
| Data set-up time | Tdsu | 8 | - | - | ns | D0[7:0], D1[7:0], D2[7:0] to CLKIN |
| Data hold time | Tdhd | 8 | - | - | ns | D0[7:0], D1[7:0], D2[7:0] to CLKIN |
| DE setup time | Tesu | 8 | - | - | ns | |
| DE hold time | Tehd | 8 | - | - | ns | |
| Output stable time | Tsst | - | - | 6 | us | 10% to 90% target voltage.<br>CL=120pF, R=10K ohm |

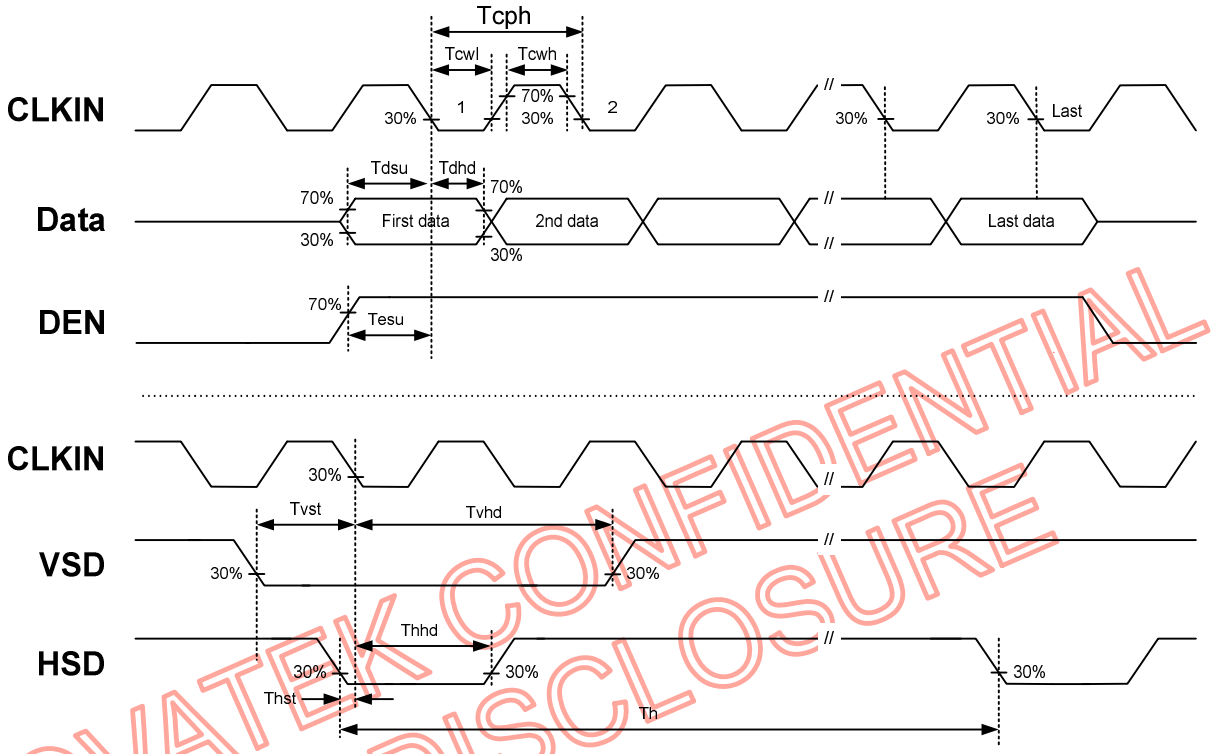
# Timing Table

## Parallel 24-bit RGB Mode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| CLKIN Frequency | Fclk | - | 40 | 50 | MHz | VDD = 3.0V ~3.6V |
| CLKIN Cycle Time | Tclk | 20 | 25 | - | ns | |
| CLKIN Pulse Duty | Tcwh | 40 | 50 | 60 | % | Tclk |
| Time from HSD to Source Output | Thso | - | 64 | - | CLKIN | |
| Time from HSD to LD | Thld | - | 64 | - | CLKIN | |
| Time from HSD to STV | Thstv | - | 2 | - | CLKIN | |
| Time from HSD to CKV | Thckv | - | 20 | - | CLKIN | |
| Time from HSD to OEV | Thoev | - | 4 | - | CLKIN | |
| LD Pulse Width | Twld | - | 10 | - | CLKIN | |
| CKV Pulse Width | Twckv | - | 66 | - | CLKIN | |
| OEV Pulse Width | Twoev | - | 74 | - | CLKIN | |

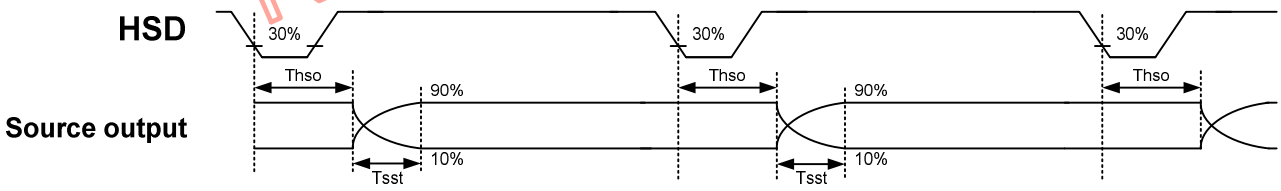
# Timing Diagram

## Input Clock and Data Timing Diagram

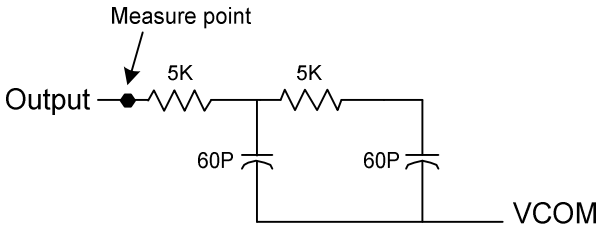




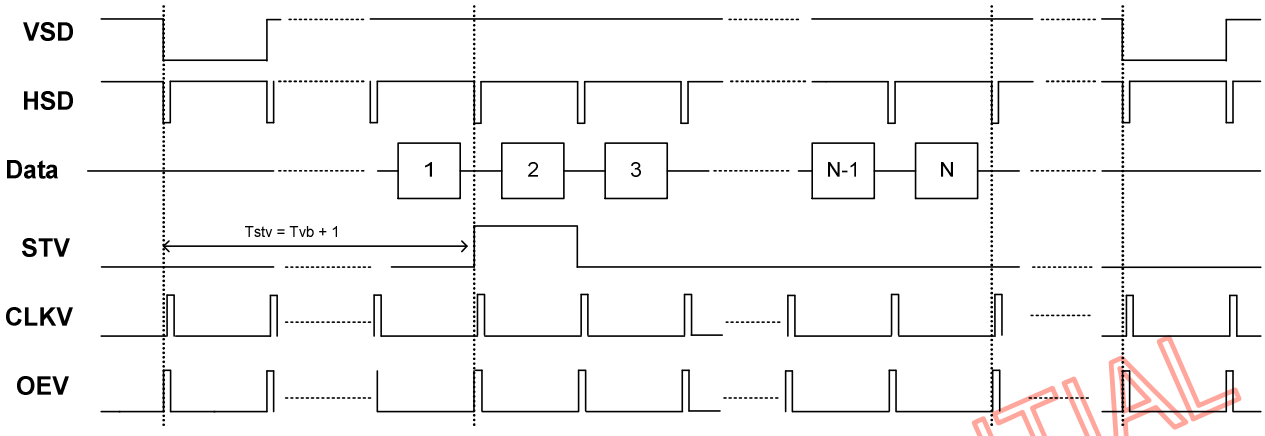

## Source Output Timing Diagram (Cascade)



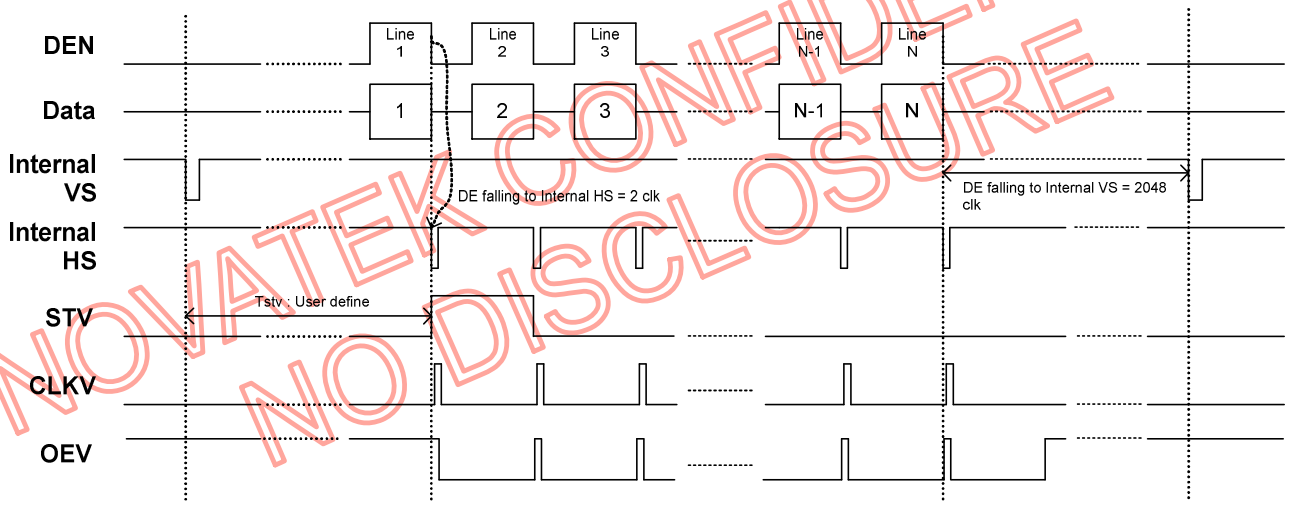

**Output load condition :**



## Vertical Timing Diagram HV (Cascade)

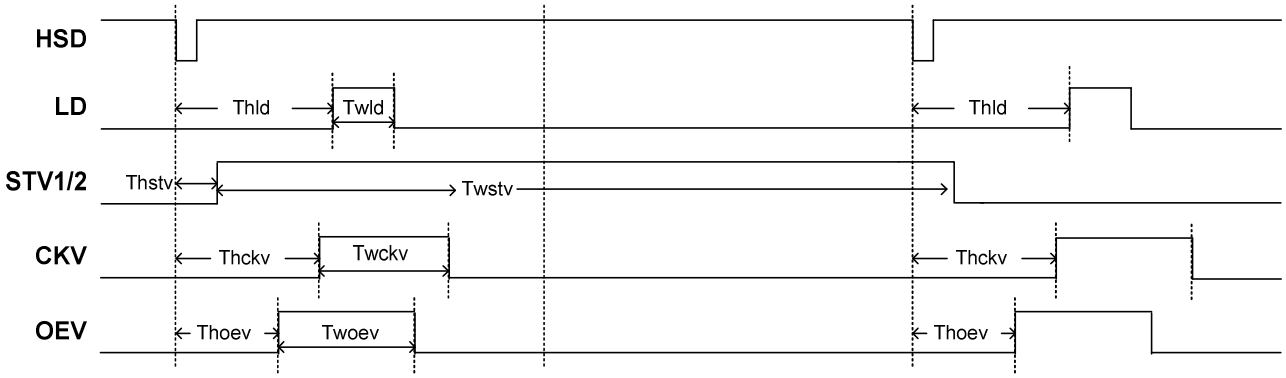



## Vertical Timing Diagram DE (Cascade)

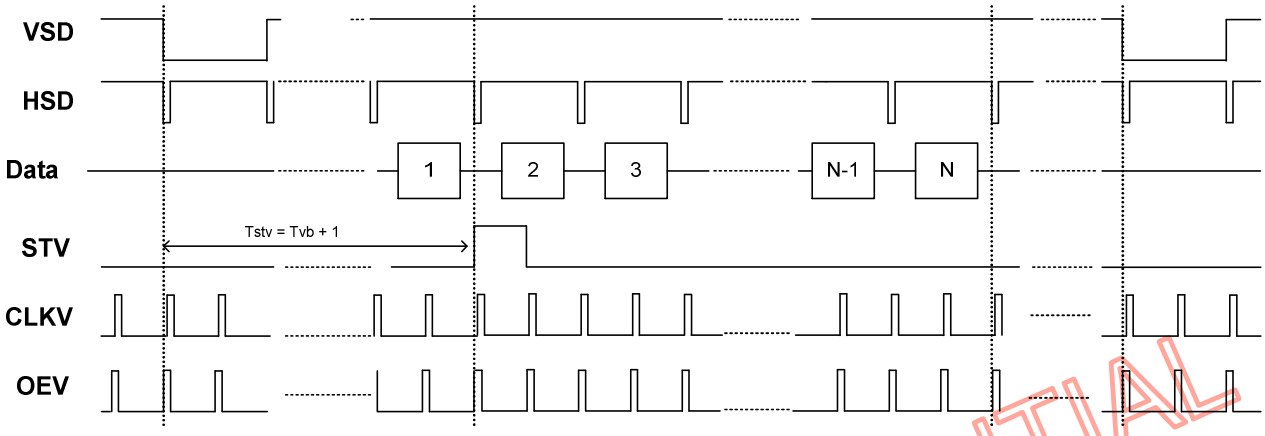




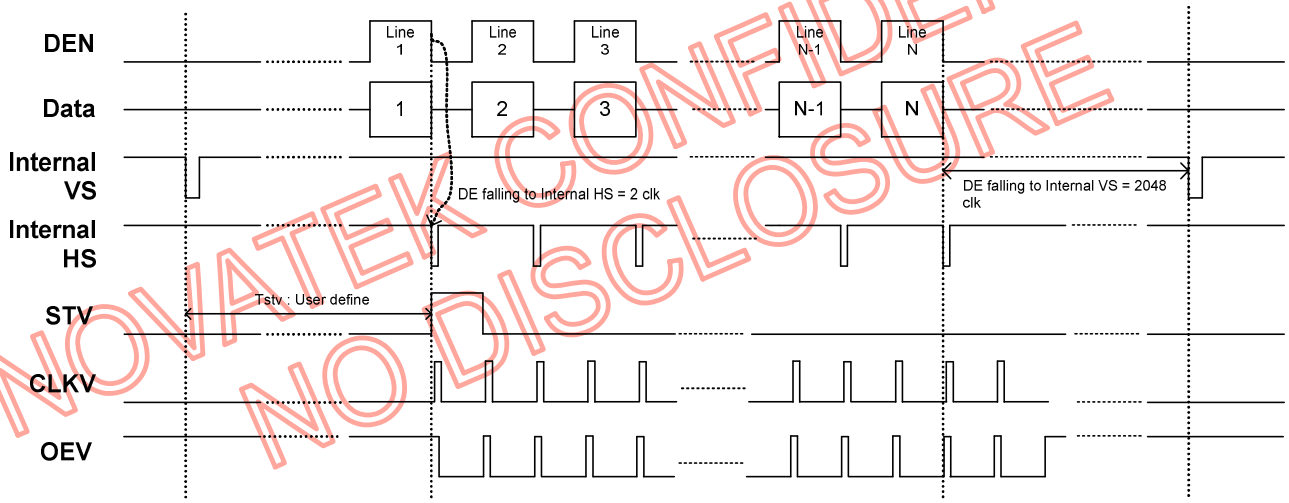

## Gate output timing diagram (Cascade)



## Vertical Timing Diagram HV (Dual Gate)

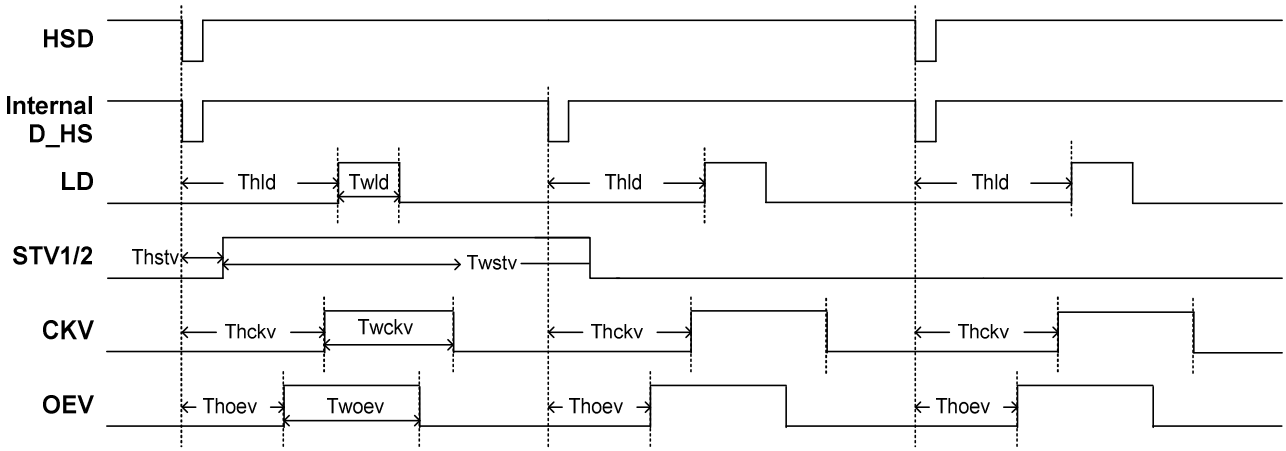



## Vertical Timing Diagram DE (Dual Gate)

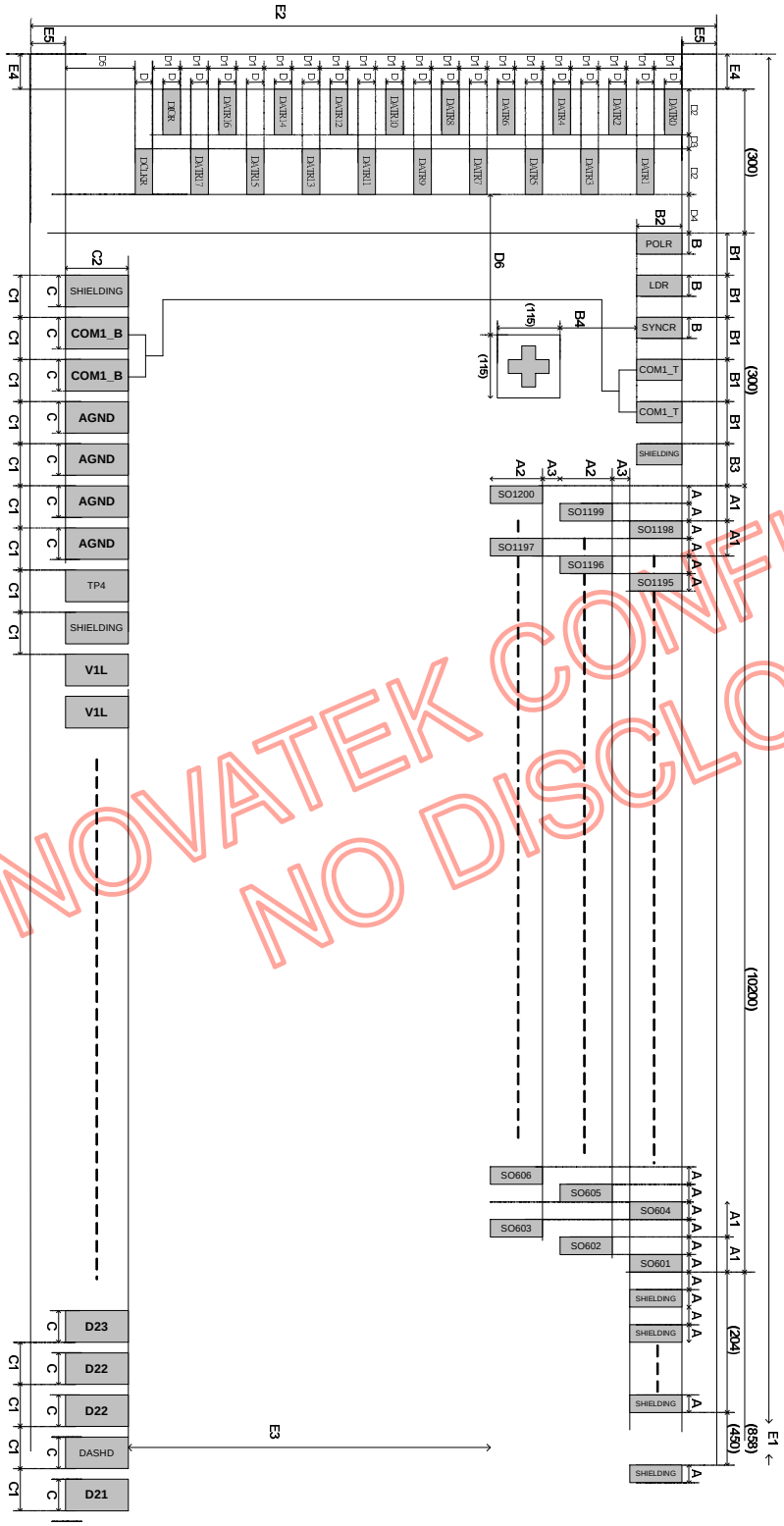


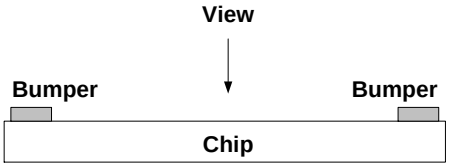



## Gate output timing diagram (Dual Gate)

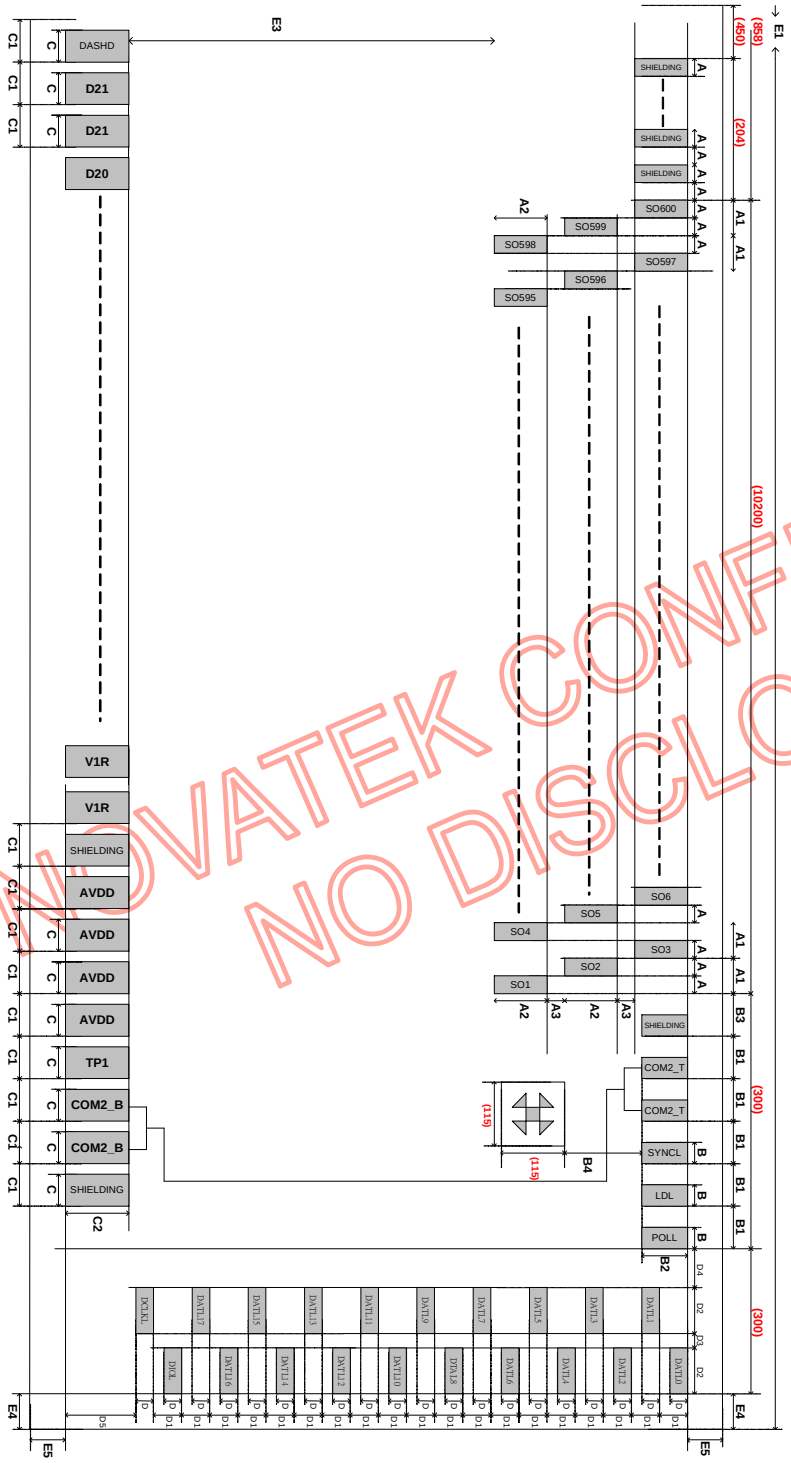


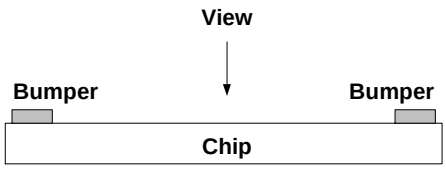
## Pad Outline Dimension 1 (Bump Side)



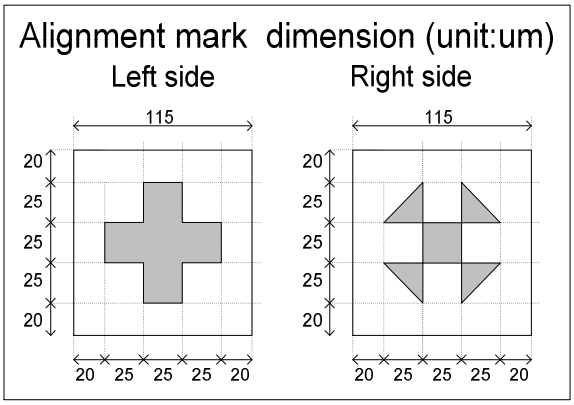



## Pad Outline Dimension 2 (Bump Side)



## Alignment Mark




## Pad Information

| Symbol | Dimension (um) |
|---|---|
| A | 17 |
| A1 | 34 |
| A2 | 110 |
| A3 | 30 |
| | |
| B | 30 |
| B1 | 50 |
| B2 | 70 |
| B3 | 50 |
| B4 | 191.5 |
| C | 65 |
| C1 | 85 |
| C2 | 110 |

| Symbol | Dimension (um) |
|---|---|
| D | 30 |
| D1 | 40 |
| D2 | 100 |
| D3 | 30 |
| D4 | 70 |
| D5 | 34 |
| D6 | 168.5 |
| | |
| E1 | 22572 (max) * |
| E2 | 938 (max) * |
| E3 | 324 |
| E4 | 57(max) |
| E5 | 57(max) |



***Note: Chip dimension includes scribe line.**

# Appendix A: Pad Coordinates

| No | Name | CX | CY |
|---|---|---|---|
| 1 | SHIELDING[69] | -10922.5 | -357 |
| 2 | SHIELDING[70] | -10837.5 | -357 |
| 3 | SHIELDING[1] | -10752.5 | -357 |
| 4 | COM1_B | -10667.5 | -357 |
| 5 | COM1_B | -10582.5 | -357 |
| 6 | AGND | -10497.5 | -357 |
| 7 | AGND | -10412.5 | -357 |
| 8 | AGND | -10327.5 | -357 |
| 9 | AGND | -10242.5 | -357 |
| 10 | TP4 | -10157.5 | -357 |
| 11 | SHIELDING[2] | -10072.5 | -357 |
| 12 | V1R | -9987.5 | -357 |
| 13 | V1R | -9902.5 | -357 |
| 14 | SHIELDING[3] | -9817.5 | -357 |
| 15 | V2R | -9732.5 | -357 |
| 16 | V2R | -9647.5 | -357 |
| 17 | SHIELDING[4] | -9562.5 | -357 |
| 18 | V3R | -9477.5 | -357 |
| 19 | V3R | -9392.5 | -357 |
| 20 | SHIELDING[5] | -9307.5 | -357 |
| 21 | V4R | -9222.5 | -357 |
| 22 | V4R | -9137.5 | -357 |
| 23 | SHIELDING[6] | -9052.5 | -357 |
| 24 | V5R | -8967.5 | -357 |
| 25 | V5R | -8882.5 | -357 |
| 26 | SHIELDING[7] | -8797.5 | -357 |
| 27 | V6R | -8712.5 | -357 |
| 28 | V6R | -8627.5 | -357 |
| 29 | SHIELDING[8] | -8542.5 | -357 |
| 30 | V7R | -8457.5 | -357 |
| 31 | V7R | -8372.5 | -357 |
| 32 | SHIELDING[9] | -8287.5 | -357 |
| 33 | V8R | -8202.5 | -357 |
| 34 | V8R | -8117.5 | -357 |
| 35 | SHIELDING[10] | -8032.5 | -357 |
| 36 | V9R | -7947.5 | -357 |
| 37 | V9R | -7862.5 | -357 |
| 38 | SHIELDING[11] | -7777.5 | -357 |
| 39 | V10R | -7692.5 | -357 |
| 40 | V10R | -7607.5 | -357 |
| 41 | SHIELDING[12] | -7522.5 | -357 |
| 42 | V11R | -7437.5 | -357 |
| 43 | V11R | -7352.5 | -357 |
| 44 | SHIELDING[13] | -7267.5 | -357 |
| 45 | V12R | -7182.5 | -357 |
| 46 | V12R | -7097.5 | -357 |
| 47 | SHIELDIN | -7012.5 | -357 |
| 48 | V13R | -6927.5 | -357 |
| 49 | V13R | -6842.5 | -357 |
| 50 | SHIELDING[15] | -6757.5 | -357 |
| 51 | V14R | -6672.5 | -357 |
| 52 | V14R | -6587.5 | -357 |
| 53 | SHIELDING[16] | -6502.5 | -357 |
| 54 | TP0 | -6417.5 | -357 |
| 55 | SHIELDING[17] | -6332.5 | -357 |
| 56 | SHIELDING[18] | -6247.5 | -357 |
| 57 | SHIELDING[19] | -6162.5 | -357 |
| 58 | SHIELDING[20] | -6077.5 | -357 |
| 59 | TP5 | -5992.5 | -357 |
| 60 | BIST | -5907.5 | -357 |
| 61 | BIST | -5822.5 | -357 |
| 62 | SHIELDING[21] | -5737.5 | -357 |
| 63 | AVDD | -5652.5 | -357 |
| 64 | AVDD | -5567.5 | -357 |
| 65 | AVDD | -5482.5 | -357 |
| 66 | AVDD | -5397.5 | -357 |
| 67 | SHIELDING[22] | -5312.5 | -357 |
| 68 | AGND | -5227.5 | -357 |
| 69 | AGND | -5142.5 | -357 |
| 70 | AGND | -5057.5 | -357 |
| 71 | AGND | -4972.5 | -357 |
| 72 | SHIELDING[23] | -4887.5 | -357 |
| 73 | GND | -4802.5 | -357 |
| 74 | GND | -4717.5 | -357 |
| 75 | GND | -4632.5 | -357 |
| 76 | GND | -4547.5 | -357 |
| 77 | SHIELDING[24] | -4462.5 | -357 |
| 78 | BLKEN | -4377.5 | -357 |
| 79 | BLKEN | -4292.5 | -357 |
| 80 | SHIELDING[25] | -4207.5 | -357 |
| 81 | VDD | -4122.5 | -357 |
| 82 | VDD | -4037.5 | -357 |
| 83 | VDD | -3952.5 | -357 |
| 84 | VDD | -3867.5 | -357 |
| 85 | TP3 | -3782.5 | -357 |
| 86 | DBGATE | -3697.5 | -357 |
| 87 | DBGATE | -3612.5 | -357 |
| 88 | SHIELDING[26] | -3527.5 | -357 |
| 89 | MASL | -3442.5 | -357 |
| 90 | MASL | -3357.5 | -357 |
| 91 | SHIELDING[27] | -3272.5 | -357 |
| 92 | MASLOC | -3187.5 | -357 |
| 93 | MASLOC | -3102.5 | -357 |
| 94 | SHIELDING[28] | -3017.5 | -357 |
| 95 | RES[0] | -2932.5 | -357 |
| 96 | RES[0] | -2847.5 | -357 |
| 97 | SHIELDING[29] | -2762.5 | -357 |
| 98 | SHIELDING[30] | -2677.5 | -357 |
| 99 | RES[1] | -2592.5 | -357 |
| 100 | RES[1] | -2507.5 | -357 |
| 101 | CFSEL | -2422.5 | -357 |
| 102 | CFSEL | -2337.5 | -357 |
| 103 | DASHD[1] | -2252.5 | -357 |
| 104 | VSD | -2167.5 | -357 |
| 105 | VSD | -2082.5 | -357 |
| 106 | DASHD[2] | -1997.5 | -357 |
| 107 | HSD | -1912.5 | -357 |

| | | | |
|---|---|---|---|
| 108 | HSD | -1827.5 | -357 |
| 109 | DASHD[3] | -1742.5 | -357 |
| 110 | DEN | -1657.5 | -357 |
| 111 | DEN | -1572.5 | -357 |
| 112 | DASHD[4] | -1487.5 | -357 |
| 113 | CLKIN | -1402.5 | -357 |
| 114 | CLKIN | -1317.5 | -357 |
| 115 | DASHD[5] | -1232.5 | -357 |
| 116 | D27 | -1147.5 | -357 |
| 117 | D27 | -1062.5 | -357 |
| 118 | D26 | -977.5 | -357 |
| 119 | D26 | -892.5 | -357 |
| 120 | DASHD[6] | -807.5 | -357 |
| 121 | D25 | -722.5 | -357 |
| 122 | D25 | -637.5 | -357 |
| 123 | D24 | -552.5 | -357 |
| 124 | D24 | -467.5 | -357 |
| 125 | DASHD[7] | -382.5 | -357 |
| 126 | D23 | -297.5 | -357 |
| 127 | D23 | -212.5 | -357 |
| 128 | D22 | -127.5 | -357 |
| 129 | D22 | -42.5 | -357 |
| 130 | DASHD[8] | 42.5 | -357 |
| 131 | D21 | 127.5 | -357 |
| 132 | D21 | 212.5 | -357 |
| 133 | D20 | 297.5 | -357 |
| 134 | D20 | 382.5 | -357 |
| 135 | DASHD[9] | 467.5 | -357 |
| 136 | D17 | 552.5 | -357 |
| 137 | D17 | 637.5 | -357 |
| 138 | D16 | 722.5 | -357 |
| 201 | CAS | 6077.5 | -357 |
| 202 | GND | 6162.5 | -357 |
| 203 | GND | 6247.5 | -357 |
| 204 | GND | 6332.5 | -357 |
| 205 | GND | 6417.5 | -357 |
| 206 | TP2 | 6502.5 | -357 |
| 207 | V14L | 6587.5 | -357 |
| 208 | V14L | 6672.5 | -357 |

| | | | |
|---|---|---|---|
| 139 | D16 | 807.5 | -357 |
| 140 | DASHD[10] | 892.5 | -357 |
| 141 | D15 | 977.5 | -357 |
| 142 | D15 | 1062.5 | -357 |
| 143 | D14 | 1147.5 | -357 |
| 144 | D14 | 1232.5 | -357 |
| 145 | DASHD[11] | 1317.5 | -357 |
| 146 | D13 | 1402.5 | -357 |
| 147 | D13 | 1487.5 | -357 |
| 148 | D12 | 1572.5 | -357 |
| 149 | D12 | 1657.5 | -357 |
| 150 | DASHD[12] | 1742.5 | -357 |
| 151 | D11 | 1827.5 | -357 |
| 152 | D11 | 1912.5 | -357 |
| 153 | D10 | 1997.5 | -357 |
| 154 | D10 | 2082.5 | -357 |
| 155 | DASHD[13] | 2167.5 | -357 |
| 156 | D07 | 2252.5 | -357 |
| 157 | D07 | 2337.5 | -357 |
| 158 | D06 | 2422.5 | -357 |
| 159 | D06 | 2507.5 | -357 |
| 160 | DASHD[14] | 2592.5 | -357 |
| 161 | D05 | 2677.5 | -357 |
| 162 | D05 | 2762.5 | -357 |
| 163 | D04 | 2847.5 | -357 |
| 164 | D04 | 2932.5 | -357 |
| 165 | DASHD[15] | 3017.5 | -357 |
| 166 | D03 | 3102.5 | -357 |
| 167 | D03 | 3187.5 | -357 |
| 168 | D02 | 3272.5 | -357 |
| 169 | D02 | 3357.5 | -357 |
| 209 | SHIELDING[38] | 6757.5 | -357 |
| 210 | V13L | 6842.5 | -357 |
| 211 | V13L | 6927.5 | -357 |
| 212 | SHIELDING[39] | 7012.5 | -357 |
| 213 | V12L | 7097.5 | -357 |
| 214 | V12L | 7182.5 | -357 |
| 215 | SHIELDING[40] | 7267.5 | -357 |
| 216 | V11L | 7352.5 | -357 |

| | | | |
|---|---|---|---|
| 170 | DASHD[16] | 3442.5 | -357 |
| 171 | D01 | 3527.5 | -357 |
| 172 | D01 | 3612.5 | -357 |
| 173 | D00 | 3697.5 | -357 |
| 174 | D00 | 3782.5 | -357 |
| 175 | DASHD[17] | 3867.5 | -357 |
| 176 | SHIELDING[31] | 3952.5 | -357 |
| 177 | MODE | 4037.5 | -357 |
| 178 | MODE | 4122.5 | -357 |
| 179 | CLKPOL | 4207.5 | -357 |
| 180 | CLKPOL | 4292.5 | -357 |
| 181 | SHIELDING[32] | 4377.5 | -357 |
| 182 | DITHB | 4462.5 | -357 |
| 183 | DITHB | 4547.5 | -357 |
| 184 | SHIELDING[33] | 4632.5 | -357 |
| 185 | SHLR | 4717.5 | -357 |
| 186 | SHLR | 4802.5 | -357 |
| 187 | SHIELDING[34] | 4887.5 | -357 |
| 188 | UPDN | 4972.5 | -357 |
| 189 | UPDN | 5057.5 | -357 |
| 190 | SHIELDING[35] | 5142.5 | -357 |
| 191 | STBYB | 5227.5 | -357 |
| 192 | STBYB | 5312.5 | -357 |
| 193 | SHIELDING[36] | 5397.5 | -357 |
| 194 | RSTB | 5482.5 | -357 |
| 195 | RSTB | 5567.5 | -357 |
| 196 | SHIELDING[37] | 5652.5 | -357 |
| 197 | VDD | 5737.5 | -357 |
| 198 | VDD | 5822.5 | -357 |
| 199 | VDD | 5907.5 | -357 |
| 200 | VDD | 5992.5 | -357 |
| 217 | V11L | 7437.5 | -357 |
| 218 | SHIELDING[41] | 7522.5 | -357 |
| 219 | V10L | 7607.5 | -357 |
| 220 | V10L | 7692.5 | -357 |
| 221 | SHIELDING[42] | 7777.5 | -357 |
| 222 | V9L | 7862.5 | -357 |
| 223 | V9L | 7947.5 | -357 |
| 224 | SHIELDING[43] | 8032.5 | -357 |

| | | | |
|---|---|---|---|
| 225 | V8L | 8117.5 | -357 |
| 226 | V8L | 8202.5 | -357 |
| 227 | SHIELDING[44] | 8287.5 | -357 |
| 228 | V7L | 8372.5 | -357 |
| 229 | V7L | 8457.5 | -357 |
| 230 | SHIELDING[45] | 8542.5 | -357 |
| 231 | V6L | 8627.5 | -357 |
| 232 | V6L | 8712.5 | -357 |
| 233 | SHIELDING[46] | 8797.5 | -357 |
| 234 | V5L | 8882.5 | -357 |
| 235 | V5L | 8967.5 | -357 |
| 236 | SHIELDING[47] | 9052.5 | -357 |
| 237 | V4L | 9137.5 | -357 |
| 238 | V4L | 9222.5 | -357 |
| 239 | SHIELDING[48] | 9307.5 | -357 |
| 240 | V3L | 9392.5 | -357 |
| 241 | V3L | 9477.5 | -357 |
| 242 | SHIELDING[49] | 9562.5 | -357 |
| 243 | V2L | 9647.5 | -357 |
| 244 | V2L | 9732.5 | -357 |
| 245 | SHIELDING[50] | 9817.5 | -357 |
| 246 | V1L | 9902.5 | -357 |
| 247 | V1L | 9987.5 | -357 |
| 248 | SHIELDING[51] | 10072.5 | -357 |
| 249 | AVDD | 10157.5 | -357 |
| 250 | AVDD | 10242.5 | -357 |
| 251 | AVDD | 10327.5 | -357 |
| 252 | AVDD | 10412.5 | -357 |
| 253 | TP1 | 10497.5 | -357 |
| 254 | COM2_B | 10582.5 | -357 |
| 255 | COM2_B | 10667.5 | -357 |
| 256 | SHIELDING[52] | 10752.5 | -357 |
| 257 | SHIELDING[53] | 10837.5 | -357 |
| 258 | SHIELDING[54] | 10922.5 | -357 |
| 259 | DCLKL | 11049 | -363 |
| 260 | DIOL | 11179 | -323 |
| 261 | DATL[17] | 11049 | -283 |
| 262 | DATL[16] | 11179 | -243 |
| 263 | DATL[15] | 11049 | -203 |
| 264 | DATL[14] | 11179 | -163 |
| 265 | DATL[13] | 11049 | -123 |
| 266 | DATL[12] | 11179 | -83 |
| 267 | DATL[11] | 11049 | -43 |
| 268 | DATL[10] | 11179 | -3 |
| 269 | DATL[9] | 11049 | 37 |
| 270 | DATL[8] | 11179 | 77 |
| 271 | DATL[7] | 11049 | 117 |
| 272 | DATL[6] | 11179 | 157 |
| 273 | DATL[5] | 11049 | 197 |
| 274 | DATL[4] | 11179 | 237 |
| 275 | DATL[3] | 11049 | 277 |
| 276 | DATL[2] | 11179 | 317 |
| 277 | DATL[1] | 11049 | 357 |
| 278 | DATL[0] | 11179 | 397 |
| 279 | POLL | 10914 | 377 |
| 280 | LDL | 10864 | 377 |
| 281 | SYNCL | 10814 | 377 |
| 282 | COM2_T | 10764 | 377 |
| 283 | COM2_T | 10714 | 377 |
| 284 | SHIELDING[55] | 10664 | 377 |
| 285 | SO[1] | 10620.5 | 77 |
| 286 | SO[2] | 10603.5 | 217 |
| 287 | SO[3] | 10586.5 | 357 |
| 288 | SO[4] | 10569.5 | 77 |
| 289 | SO[5] | 10552.5 | 217 |
| 290 | SO[6] | 10535.5 | 357 |
| 291 | SO[7] | 10518.5 | 77 |
| 292 | SO[8] | 10501.5 | 217 |
| 293 | SO[9] | 10484.5 | 357 |
| 294 | SO[10] | 10467.5 | 77 |
| 295 | SO[11] | 10450.5 | 217 |
| 296 | SO[12] | 10433.5 | 357 |
| 297 | SO[13] | 10416.5 | 77 |
| 298 | SO[14] | 10399.5 | 217 |
| 299 | SO[15] | 10382.5 | 357 |
| 300 | SO[16] | 10365.5 | 77 |
| 301 | SO[17] | 10348.5 | 217 |
| 302 | SO[18] | 10331.5 | 357 |
| 303 | SO[19] | 10314.5 | 77 |
| 304 | SO[20] | 10297.5 | 217 |
| 305 | SO[21] | 10280.5 | 357 |
| 306 | SO[22] | 10263.5 | 77 |
| 307 | SO[23] | 10246.5 | 217 |
| 308 | SO[24] | 10229.5 | 357 |
| 309 | SO[25] | 10212.5 | 77 |
| 310 | SO[26] | 10195.5 | 217 |
| 311 | SO[27] | 10178.5 | 357 |
| 312 | SO[28] | 10161.5 | 77 |
| 313 | SO[29] | 10144.5 | 217 |
| 314 | SO[30] | 10127.5 | 357 |
| 315 | SO[31] | 10110.5 | 77 |
| 316 | SO[32] | 10093.5 | 217 |
| 317 | SO[33] | 10076.5 | 357 |
| 318 | SO[34] | 10059.5 | 77 |
| 319 | SO[35] | 10042.5 | 217 |
| 320 | SO[36] | 10025.5 | 357 |
| 321 | SO[37] | 10008.5 | 77 |
| 322 | SO[38] | 9991.5 | 217 |
| 323 | SO[39] | 9974.5 | 357 |
| 324 | SO[40] | 9957.5 | 77 |
| 325 | SO[41] | 9940.5 | 217 |
| 326 | SO[42] | 9923.5 | 357 |
| 327 | SO[43] | 9906.5 | 77 |
| 328 | SO[44] | 9889.5 | 217 |
| 329 | SO[45] | 9872.5 | 357 |
| 330 | SO[46] | 9855.5 | 77 |
| 331 | SO[47] | 9838.5 | 217 |
| 332 | SO[48] | 9821.5 | 357 |
| 333 | SO[49] | 9804.5 | 77 |
| 334 | SO[50] | 9787.5 | 217 |
| 335 | SO[51] | 9770.5 | 357 |
| 336 | SO[52] | 9753.5 | 77 |
| 337 | SO[53] | 9736.5 | 217 |
| 338 | SO[54] | 9719.5 | 357 |

| | | | |
|---|---|---|---|
| 339 | SO[55] | 9702.5 | 77 |
| 340 | SO[56] | 9685.5 | 217 |
| 341 | SO[57] | 9668.5 | 357 |
| 342 | SO[58] | 9651.5 | 77 |
| 343 | SO[59] | 9634.5 | 217 |
| 344 | SO[60] | 9617.5 | 357 |
| 345 | SO[61] | 9600.5 | 77 |
| 346 | SO[62] | 9583.5 | 217 |
| 347 | SO[63] | 9566.5 | 357 |
| 348 | SO[64] | 9549.5 | 77 |
| 349 | SO[65] | 9532.5 | 217 |
| 350 | SO[66] | 9515.5 | 357 |
| 351 | SO[67] | 9498.5 | 77 |
| 352 | SO[68] | 9481.5 | 217 |
| 353 | SO[69] | 9464.5 | 357 |
| 354 | SO[70] | 9447.5 | 77 |
| 355 | SO[71] | 9430.5 | 217 |
| 356 | SO[72] | 9413.5 | 357 |
| 357 | SO[73] | 9396.5 | 77 |
| 358 | SO[74] | 9379.5 | 217 |
| 359 | SO[75] | 9362.5 | 357 |
| 360 | SO[76] | 9345.5 | 77 |
| 361 | SO[77] | 9328.5 | 217 |
| 362 | SO[78] | 9311.5 | 357 |
| 363 | SO[79] | 9294.5 | 77 |
| 364 | SO[80] | 9277.5 | 217 |
| 365 | SO[81] | 9260.5 | 357 |
| 366 | SO[82] | 9243.5 | 77 |
| 367 | SO[83] | 9226.5 | 217 |
| 368 | SO[84] | 9209.5 | 357 |
| 369 | SO[85] | 9192.5 | 77 |
| 370 | SO[86] | 9175.5 | 217 |
| 371 | SO[87] | 9158.5 | 357 |
| 372 | SO[88] | 9141.5 | 77 |
| 373 | SO[89] | 9124.5 | 217 |
| 374 | SO[90] | 9107.5 | 357 |
| 375 | SO[91] | 9090.5 | 77 |
| 376 | SO[92] | 9073.5 | 217 |
| 377 | SO[93] | 9056.5 | 357 |
| 378 | SO[94] | 9039.5 | 77 |
| 379 | SO[95] | 9022.5 | 217 |
| 380 | SO[96] | 9005.5 | 357 |
| 381 | SO[97] | 8988.5 | 77 |
| 382 | SO[98] | 8971.5 | 217 |
| 383 | SO[99] | 8954.5 | 357 |
| 384 | SO[100] | 8937.5 | 77 |
| 385 | SO[101] | 8920.5 | 217 |
| 386 | SO[102] | 8903.5 | 357 |
| 387 | SO[103] | 8886.5 | 77 |
| 388 | SO[104] | 8869.5 | 217 |
| 389 | SO[105] | 8852.5 | 357 |
| 390 | SO[106] | 8835.5 | 77 |
| 391 | SO[107] | 8818.5 | 217 |
| 392 | SO[108] | 8801.5 | 357 |
| 393 | SO[109] | 8784.5 | 77 |
| 394 | SO[110] | 8767.5 | 217 |
| 395 | SO[111] | 8750.5 | 357 |
| 396 | SO[112] | 8733.5 | 77 |
| 397 | SO[113] | 8716.5 | 217 |
| 398 | SO[114] | 8699.5 | 357 |
| 399 | SO[115] | 8682.5 | 77 |
| 400 | SO[116] | 8665.5 | 217 |
| 401 | SO[117] | 8648.5 | 357 |
| 402 | SO[118] | 8631.5 | 77 |
| 403 | SO[119] | 8614.5 | 217 |
| 404 | SO[120] | 8597.5 | 357 |
| 405 | SO[121] | 8580.5 | 77 |
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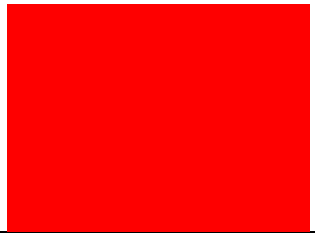
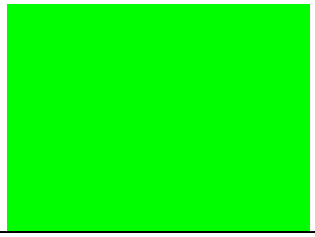
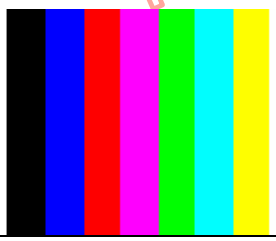
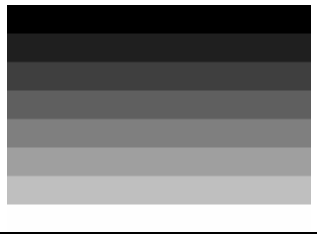
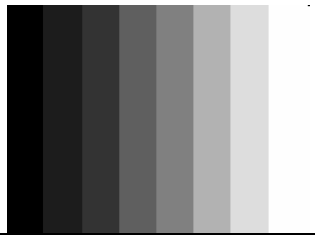
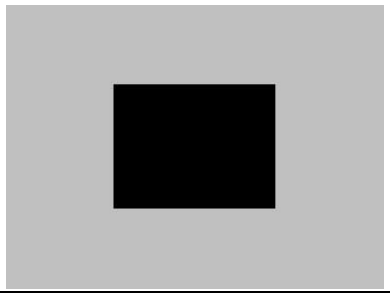
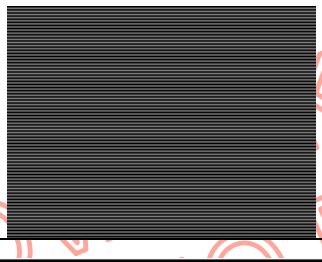
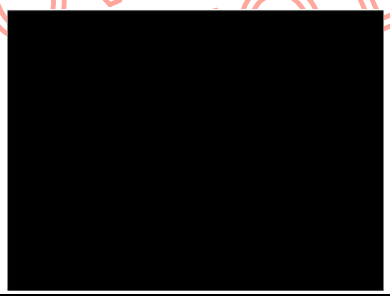
| 1292 | SO[996] | -7152.5 | 77 |
| 1293 | SO[997] | -7169.5 | 357 |
| 1294 | SO[998] | -7186.5 | 217 |
| 1295 | SO[999] | -7203.5 | 77 |
| 1296 | SO[1000] | -7220.5 | 357 |
| 1297 | SO[1001] | -7237.5 | 217 |
| 1298 | SO[1002] | -7254.5 | 77 |
| 1299 | SO[1003] | -7271.5 | 357 |
| 1300 | SO[1004] | -7288.5 | 217 |
| 1301 | SO[1005] | -7305.5 | 77 |
| 1302 | SO[1006] | -7322.5 | 357 |
| 1303 | SO[1007] | -7339.5 | 217 |
| 1304 | SO[1008] | -7356.5 | 77 |
| 1305 | SO[1009] | -7373.5 | 357 |
| 1306 | SO[1010] | -7390.5 | 217 |
| 1307 | SO[1011] | -7407.5 | 77 |
| 1308 | SO[1012] | -7424.5 | 357 |
| 1309 | SO[1013] | -7441.5 | 217 |
| 1310 | SO[1014] | -7458.5 | 77 |
| 1311 | SO[1015] | -7475.5 | 357 |
| 1312 | SO[1016] | -7492.5 | 217 |
| 1313 | SO[1017] | -7509.5 | 77 |
| 1314 | SO[1018] | -7526.5 | 357 |
| 1315 | SO[1019] | -7543.5 | 217 |
| 1316 | SO[1020] | -7560.5 | 77 |
| 1317 | SO[1021] | -7577.5 | 357 |
| 1318 | SO[1022] | -7594.5 | 217 |
| 1319 | SO[1023] | -7611.5 | 77 |
| 1320 | SO[1024] | -7628.5 | 357 |
| 1321 | SO[1025] | -7645.5 | 217 |
| 1322 | SO[1026] | -7662.5 | 77 |
| 1323 | SO[1027] | -7679.5 | 357 |
| 1324 | SO[1028] | -7696.5 | 217 |
| 1325 | SO[1029] | -7713.5 | 77 |
| 1326 | SO[1030] | -7730.5 | 357 |
| 1327 | SO[1031] | -7747.5 | 217 |
| 1328 | SO[1032] | -7764.5 | 77 |
| 1329 | SO[1033] | -7781.5 | 357 |
| 1330 | SO[1034] | -7798.5 | 217 |
| 1331 | SO[1035] | -7815.5 | 77 |
| 1332 | SO[1036] | -7832.5 | 357 |
| 1333 | SO[1037] | -7849.5 | 217 |
| 1334 | SO[1038] | -7866.5 | 77 |
| 1335 | SO[1039] | -7883.5 | 357 |
| 1336 | SO[1040] | -7900.5 | 217 |
| 1337 | SO[1041] | -7917.5 | 77 |
| 1338 | SO[1042] | -7934.5 | 357 |
| 1339 | SO[1043] | -7951.5 | 217 |
| 1340 | SO[1044] | -7968.5 | 77 |
| 1341 | SO[1045] | -7985.5 | 357 |
| 1342 | SO[1046] | -8002.5 | 217 |
| 1343 | SO[1047] | -8019.5 | 77 |
| 1344 | SO[1048] | -8036.5 | 357 |
| 1345 | SO[1049] | -8053.5 | 217 |
| 1346 | SO[1050] | -8070.5 | 77 |
| 1347 | SO[1051] | -8087.5 | 357 |
| 1348 | SO[1052] | -8104.5 | 217 |
| 1349 | SO[1053] | -8121.5 | 77 |
| 1350 | SO[1054] | -8138.5 | 357 |
| 1351 | SO[1055] | -8155.5 | 217 |
| 1352 | SO[1056] | -8172.5 | 77 |
| 1353 | SO[1057] | -8189.5 | 357 |
| 1354 | SO[1058] | -8206.5 | 217 |
| 1355 | SO[1059] | -8223.5 | 77 |
| 1356 | SO[1060] | -8240.5 | 357 |
| 1357 | SO[1061] | -8257.5 | 217 |
| 1358 | SO[1062] | -8274.5 | 77 |
| 1359 | SO[1063] | -8291.5 | 357 |
| 1360 | SO[1064] | -8308.5 | 217 |
| 1361 | SO[1065] | -8325.5 | 77 |
| 1362 | SO[1066] | -8342.5 | 357 |
| 1363 | SO[1067] | -8359.5 | 217 |
| 1364 | SO[1068] | -8376.5 | 77 |

| | | | |
|---|---|---|---|
| 1365 | SO[1069] | -8393.5 | 357 |
| 1366 | SO[1070] | -8410.5 | 217 |
| 1367 | SO[1071] | -8427.5 | 77 |
| 1368 | SO[1072] | -8444.5 | 357 |
| 1369 | SO[1073] | -8461.5 | 217 |
| 1370 | SO[1074] | -8478.5 | 77 |
| 1371 | SO[1075] | -8495.5 | 357 |
| 1372 | SO[1076] | -8512.5 | 217 |
| 1373 | SO[1077] | -8529.5 | 77 |
| 1374 | SO[1078] | -8546.5 | 357 |
| 1375 | SO[1079] | -8563.5 | 217 |
| 1376 | SO[1080] | -8580.5 | 77 |
| 1377 | SO[1081] | -8597.5 | 357 |
| 1378 | SO[1082] | -8614.5 | 217 |
| 1379 | SO[1083] | -8631.5 | 77 |
| 1380 | SO[1084] | -8648.5 | 357 |
| 1381 | SO[1085] | -8665.5 | 217 |
| 1382 | SO[1086] | -8682.5 | 77 |
| 1383 | SO[1087] | -8699.5 | 357 |
| 1384 | SO[1088] | -8716.5 | 217 |
| 1385 | SO[1089] | -8733.5 | 77 |
| 1386 | SO[1090] | -8750.5 | 357 |
| 1387 | SO[1091] | -8767.5 | 217 |
| 1388 | SO[1092] | -8784.5 | 77 |
| 1389 | SO[1093] | -8801.5 | 357 |
| 1390 | SO[1094] | -8818.5 | 217 |
| 1391 | SO[1095] | -8835.5 | 77 |
| 1392 | SO[1096] | -8852.5 | 357 |
| 1393 | SO[1097] | -8869.5 | 217 |
| 1394 | SO[1098] | -8886.5 | 77 |
| 1395 | SO[1099] | -8903.5 | 357 |
| 1396 | SO[1100] | -8920.5 | 217 |
| 1397 | SO[1101] | -8937.5 | 77 |
| 1398 | SO[1102] | -8954.5 | 357 |
| 1399 | SO[1103] | -8971.5 | 217 |
| 1400 | SO[1104] | -8988.5 | 77 |
| 1401 | SO[1105] | -9005.5 | 357 |
| 1402 | SO[1106] | -9022.5 | 217 |
| 1403 | SO[1107] | -9039.5 | 77 |
| 1404 | SO[1108] | -9056.5 | 357 |
| 1405 | SO[1109] | -9073.5 | 217 |
| 1406 | SO[1110] | -9090.5 | 77 |
| 1407 | SO[1111] | -9107.5 | 357 |
| 1408 | SO[1112] | -9124.5 | 217 |
| 1409 | SO[1113] | -9141.5 | 77 |
| 1410 | SO[1114] | -9158.5 | 357 |
| 1411 | SO[1115] | -9175.5 | 217 |
| 1412 | SO[1116] | -9192.5 | 77 |
| 1413 | SO[1117] | -9209.5 | 357 |
| 1414 | SO[1118] | -9226.5 | 217 |
| 1415 | SO[1119] | -9243.5 | 77 |
| 1416 | SO[1120] | -9260.5 | 357 |
| 1417 | SO[1121] | -9277.5 | 217 |
| 1418 | SO[1122] | -9294.5 | 77 |
| 1419 | SO[1123] | -9311.5 | 357 |
| 1420 | SO[1124] | -9328.5 | 217 |
| 1421 | SO[1125] | -9345.5 | 77 |
| 1422 | SO[1126] | -9362.5 | 357 |
| 1423 | SO[1127] | -9379.5 | 217 |
| 1424 | SO[1128] | -9396.5 | 77 |
| 1425 | SO[1129] | -9413.5 | 357 |
| 1426 | SO[1130] | -9430.5 | 217 |
| 1427 | SO[1131] | -9447.5 | 77 |
| 1428 | SO[1132] | -9464.5 | 357 |
| 1429 | SO[1133] | -9481.5 | 217 |
| 1430 | SO[1134] | -9498.5 | 77 |
| 1431 | SO[1135] | -9515.5 | 357 |
| 1432 | SO[1136] | -9532.5 | 217 |
| 1433 | SO[1137] | -9549.5 | 77 |
| 1434 | SO[1138] | -9566.5 | 357 |
| 1435 | SO[1139] | -9583.5 | 217 |
| 1436 | SO[1140] | -9600.5 | 77 |
| 1437 | SO[1141] | -9617.5 | 357 |
| 1438 | SO[1142] | -9634.5 | 217 |
| 1439 | SO[1143] | -9651.5 | 77 |
| 1440 | SO[1144] | -9668.5 | 357 |
| 1441 | SO[1145] | -9685.5 | 217 |
| 1442 | SO[1146] | -9702.5 | 77 |
| 1443 | SO[1147] | -9719.5 | 357 |
| 1444 | SO[1148] | -9736.5 | 217 |
| 1445 | SO[1149] | -9753.5 | 77 |
| 1446 | SO[1150] | -9770.5 | 357 |
| 1447 | SO[1151] | -9787.5 | 217 |
| 1448 | SO[1152] | -9804.5 | 77 |
| 1449 | SO[1153] | -9821.5 | 357 |
| 1450 | SO[1154] | -9838.5 | 217 |
| 1451 | SO[1155] | -9855.5 | 77 |
| 1452 | SO[1156] | -9872.5 | 357 |
| 1453 | SO[1157] | -9889.5 | 217 |
| 1454 | SO[1158] | -9906.5 | 77 |
| 1455 | SO[1159] | -9923.5 | 357 |
| 1456 | SO[1160] | -9940.5 | 217 |
| 1457 | SO[1161] | -9957.5 | 77 |
| 1458 | SO[1162] | -9974.5 | 357 |
| 1459 | SO[1163] | -9991.5 | 217 |
| 1460 | SO[1164] | -10008.5 | 77 |
| 1461 | SO[1165] | -10025.5 | 357 |
| 1462 | SO[1166] | -10042.5 | 217 |
| 1463 | SO[1167] | -10059.5 | 77 |
| 1464 | SO[1168] | -10076.5 | 357 |
| 1465 | SO[1169] | -10093.5 | 217 |
| 1466 | SO[1170] | -10110.5 | 77 |
| 1467 | SO[1171] | -10127.5 | 357 |
| 1468 | SO[1172] | -10144.5 | 217 |
| 1469 | SO[1173] | -10161.5 | 77 |
| 1470 | SO[1174] | -10178.5 | 357 |
| 1471 | SO[1175] | -10195.5 | 217 |
| 1472 | SO[1176] | -10212.5 | 77 |
| 1473 | SO[1177] | -10229.5 | 357 |
| 1474 | SO[1178] | -10246.5 | 217 |
| 1475 | SO[1179] | -10263.5 | 77 |
| 1476 | SO[1180] | -10280.5 | 357 |
| 1477 | SO[1181] | -10297.5 | 217 |
| 1478 | SO[1182] | -10314.5 | 77 |

| | | | |
|---|---|---|---|
| 1479 | SO[1183] | -10331.5 | 357 |
| 1480 | SO[1184] | -10348.5 | 217 |
| 1481 | SO[1185] | -10365.5 | 77 |
| 1482 | SO[1186] | -10382.5 | 357 |
| 1483 | SO[1187] | -10399.5 | 217 |
| 1484 | SO[1188] | -10416.5 | 77 |
| 1485 | SO[1189] | -10433.5 | 357 |
| 1486 | SO[1190] | -10450.5 | 217 |
| 1487 | SO[1191] | -10467.5 | 77 |
| 1488 | SO[1192] | -10484.5 | 357 |
| 1489 | SO[1193] | -10501.5 | 217 |
| 1490 | SO[1194] | -10518.5 | 77 |
| 1491 | SO[1195] | -10535.5 | 357 |
| 1492 | SO[1196] | -10552.5 | 217 |
| 1493 | SO[1197] | -10569.5 | 77 |
| 1494 | SO[1198] | -10586.5 | 357 |
| 1495 | SO[1199] | -10603.5 | 217 |
| 1496 | SO[1200] | -10620.5 | 77 |
| 1497 | SHIELDING[68] | -10664 | 377 |
| 1498 | COM1_T | -10714 | 377 |
| 1499 | COM1_T | -10764 | 377 |
| 1500 | SYNCR | -10814 | 377 |
| 1501 | LDR | -10864 | 377 |
| 1502 | POLR | -10914 | 377 |
| 1503 | DATR[0] | -11179 | 397 |
| 1504 | DATR[1] | -11049 | 357 |
| 1505 | DATR[2] | -11179 | 317 |
| 1506 | DATR[3] | -11049 | 277 |
| 1507 | DATR[4] | -11179 | 237 |
| 1508 | DATR[5] | -11049 | 197 |
| 1509 | DATR[6] | -11179 | 157 |
| 1510 | DATR[7] | -11049 | 117 |
| 1511 | DATR[8] | -11179 | 77 |
| 1512 | DATR[9] | -11049 | 37 |
| 1513 | DATR[10] | -11179 | -3 |
| 1514 | DATR[11] | -11049 | -43 |
| 1515 | DATR[12] | -11179 | -83 |
| 1516 | DATR[13] | -11049 | -123 |
| 1517 | DATR[14] | -11179 | -163 |
| 1518 | DATR[15] | -11049 | -203 |
| 1519 | DATR[16] | -11179 | -243 |
| 1520 | DATR[17] | -11049 | -283 |
| 1521 | DIOR | -11179 | -323 |
| 1522 | DCLKR | -11049 | -363 |

## Appendix B: BIST Pattern

| No. | Pattern | Test function Description | Notice |
|---|---|---|---|
| 1 |  | 1. Color alignment with color filter. | |
| 2 |  | 1. Color alignment with color filter. | |
| 3 |  | 1. Color alignment with color filter. | |
| 4 | Black | | |
| 5 | White | | |
| 6 |  | 1. Customer standard test pattern.<br>2. Color alignment with color filter.<br>3. Driver scan direction. | |
| 7 |  | 1. Customer standard test pattern. | |

| | | | |
|---|---|---|---|
| 8 |  | 1. Customer standard test pattern. | |
| 9 |  | 1. Cross talk??<br>(Vertical cross talk: Belong to Panel issue, Horzontal cross talk: Inversion structure issue( Line inversion), | |
| 10 |  | 1. Chessboard pattern. | |
| 11 |  | 1. Black-Gray(128) flicker pattern | |
| 12 |  | Black background and White circle | |