SC5004

8-Bit 1284-Channel TFT LCD Source Driver with TCON

Product Description

SC5004 is a highly integrated 1284 channel source driver with built-in timing controller and power circuit for color TFT-LCD panels. This driver supports many interfaces and resolutions for industrial or automotive products.

Features

- Timing controller (TCON)
  - Supports standard display resolutions : 640x480, 800x(480/600/1280), 960x540, 1024x(600/768/480), 1280x(480/720/800), 1440x540, 1600x600, 1366x768
  - Supports programmable resolutions for special panel design
  - Supports 18/24-bit parallel (RGB) CMOS input timing
  - Supports 18/24-bit LVDS input timing
  - Supports SPI or I^2C command and burst mode
  - Supports Power on/off white or black pattern selection
  - Supports low temperature compensation driving scheme
  - Supports SC5005 Gate driver DC-DC control
  - Supports Gate driver all on (XON) function
  - Support external 1k bits EEPROM (SII S24CS01A)
  - Support Driver IC feedback signal (DFB) for ASIL
  - Power for logic circuit : 3.0V~3.6V
  - Max. LVDS operating frequency : 80MHz
  - Built-in MTP for customer settings and supports overwrite up to 50 times.
  - Built-In Self Test (BIST) function for no CLK, HS, VS or DE input
  - Built-in input signal missing alarm function

- Source driver (SD)
  - Output : 1284 output channels
  - Supports 1920(RGB)x720 resolution by 5 chips cascade
  - Supports CMOS/RSDS/mini-LVDS (6/8-bit) interface
  - Supports 120MHz high speed RSDS cascade interface
  - True 8 bits R/G/B resolution (16.7M colors)
  - LCD driving voltage : 8.0 ~ 13.5V
  - Built-in digital programmable Gamma curve
  - Supports 1 dot / 1+2 dot / column inversion driving scheme
  - Stagger output PAD with 18um pitch

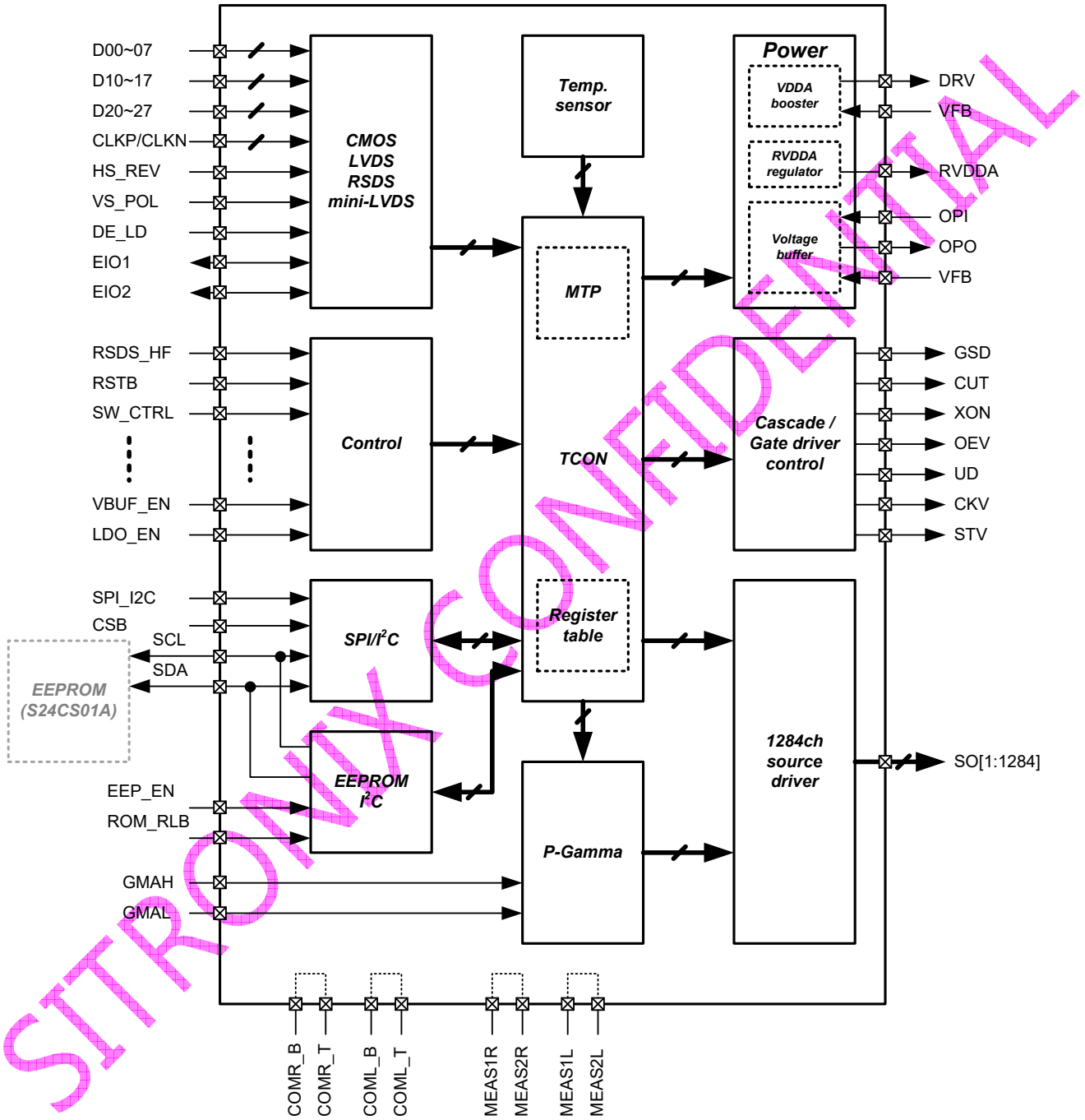
- Power Circuit
  - PWM booster x1 : Generating VDDA voltage (8.0~13.5V) for source driver
  - Voltage buffer x 1 : For panel Vcom voltage
  - LDO x 1 : Generating source driver Gamma reference voltage

- Extreme temperature compensation
  - Built-in a wide range temperature sensor
  - 2nd Gamma curve for better display quality
  - 2nd Power setting for Gamma curve
  - 2nd Gate driving voltage control register
  - Frame reduction function
  - External LCD module heater control
  - Over Heat Protection (OHP)

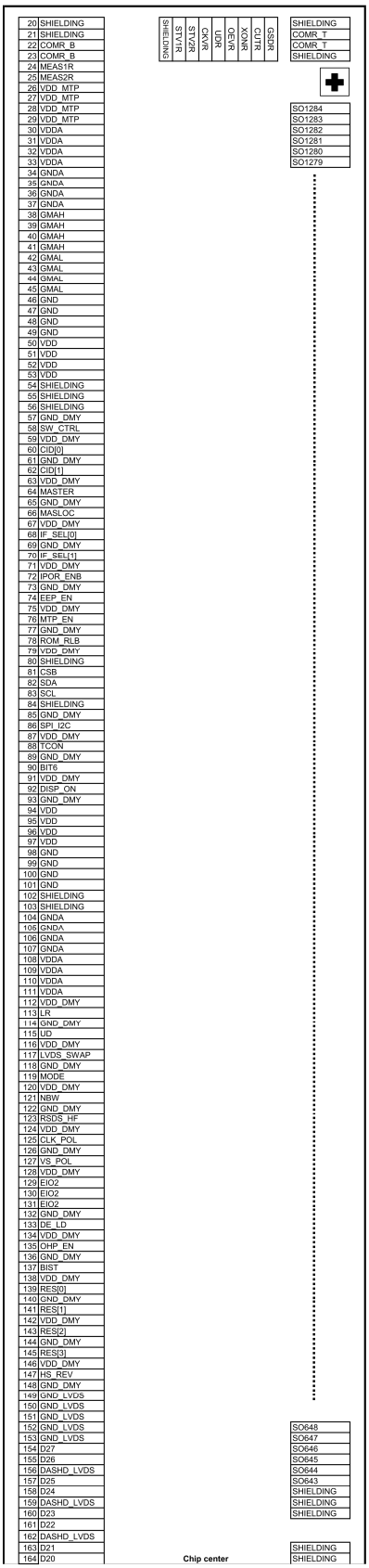
- Programmable Gamma curve
  - User can set Gamma curve via SPI / I^2C or EEPROM

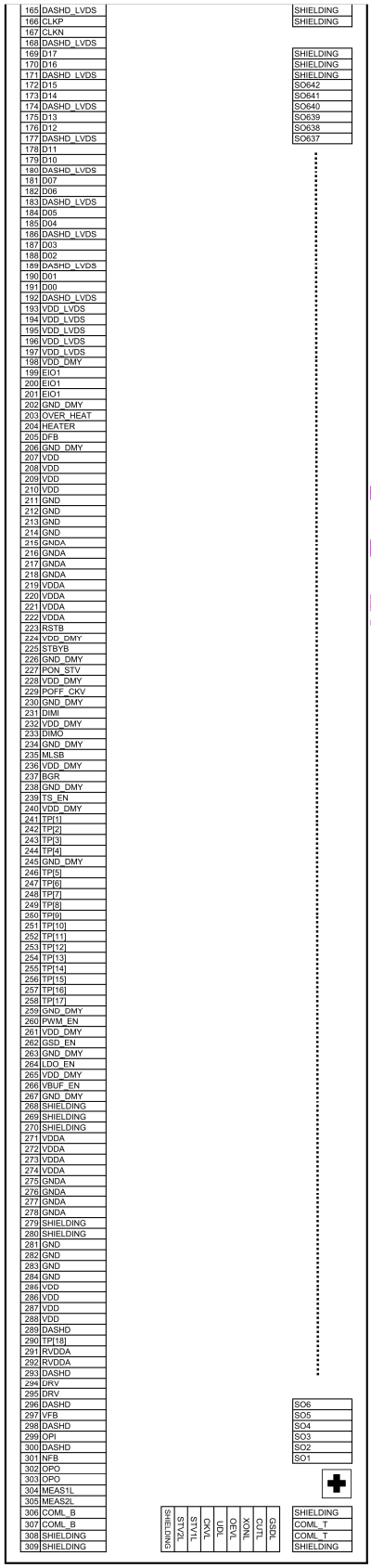
- Programmable resolution in TCON mode
  - User can define any resolution inside SC5004 cascade range (Max=4)
  - $H_{DISP} \leqq 1712$(RGB)
  - $V_{DISP} \leqq 1280$
  - Supports SYNC or DE mode timing

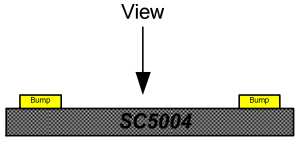
Function Block Diagram



PAD sequence (Bump view)







Pin Description

Power supply pins :

PIN name	I/O	Description
VDD	P	Digital circuit power supply
GND	P	Digital circuit ground
VDD_LVDS	P	LVDS circuit power supply
GND_LVDS	P	LVDS circuit ground
VDDA	P	Source driver analog power supply
GNDA	P	Source driver analog ground
VDD_MTP	P	External power supply for MTP programming

SPI / I²C and EEPROM control pins :

PIN name	I/O	Int. pulled	Description	
CSB	I	H	Chip select signal H : chip not selected (inaccessible) L : chip selected (accessible)	
SCL	I/O	-	Clock signal for SPI, I²C or EEPROM	
SDA	I/O	-	Serial data input of SPI, I²C or EEPROM	
SPI_I2C	I	L	Serial interface selection H : SPI L : I²C	
EEP_EN	I	L	Enable external EEPROM H : enable L : disable	When EEP_EN=1 and MTP_EN=1, SC5004won't loading any data from EEPROM or MTP.
MTP_EN	I	L	Enable internal MTP H : enable L : disable	
ROM_RLB	I	L	EEPROM / MTP periodicity (0.5 second) reload control H : disable L : enable	

Input interface pins :

PIN name	I/O	Int. pulled	Description	
D00~D07	I	-	6/8 bit display data inputs for red color	When IFSEL[1:0]=01 CMOS interface mode and input data is 6 bit format, LSB 2 bits must connect to GND.
D10~D17	I	-	6/8 bit display data inputs for green color	
D20~D27	I	-	6/8 bit display data inputs for blue color	
CLKP	I	-	Pixel clock input	
CLKN	I	-	Pixel clock input	
CLK_POL	I	L	CMOS interface input clock edge selection H : latch data at clock rising edge L : latch data at clock falling edge * This setting only for TCON mode CMOS interface	
EIO1	I/O	-	Start pulse (EIO) for source driver CMOS/RSDS/mini-LVDS mode LR=1, scan direction : EIO1→ SO[1] → SO[2] → ... SO[1284] → EIO2 LR=0, scan direction : EIO2→ SO[1284] → SO[1283] → ... SO[1] → EIO1	
EIO2	I/O	-		
VS_POL	I	L	Frame synchronous signal (VS) for SYNC mode or polarity (POL) for source driver mode	
DE_LD	I	L	Data enable signal (DE) for DE mode or latch signal (LD) for source driver mode	
HS_REV	I	L	When TCON=1 (TCON mode) Line synchronous signal (HS) for SYNC mode	
			When TCON=0 (SD mode) CMOS interface data inverse function H : Inverse (Ex : 00/h→FF/h, 55/h→AA/h and so on) L : Normal	

Control pins (hardware only) :

PIN name	I/O	Int. pulled	Description
TCON	I	H	TCON or Source driver mode selection H : TCON + SD mode L : SD mode
RSDS_HF	I	L	Source driver RSDS interface mode high frequency setting H : 60MHz < f_{RSDS} < 120MHz L : f_{RSDS} < 70MHz
SW_CTRL	I	L	Software pin control function (TCON & SD mode both effective) H : Disable hardware pin control (S/W > H/W) L : Hardware related software bits will be disable (H/W > S/W)
IPOR_ENB	I	L	Internal Power On Reset function control H : Disable L : Enable
PON_STV	I	L	When TCON=1 (TCON mode) : Power on pattern selection, this sequence can be skip by S/W bit “PON_SKIP” H : black L : white
			When TCON=0 (SD mode) : STV input for source driver offset cancellation.
POFF_CKV	I	L	When TCON=1 (TCON mode) : Power off pattern selection H : black L : white
			When TCON=0 (SD mode) : CKV input for GD DC-DC function.
IF_SEL[1:0]	I	LH	See “interface selection table”
CID[1:0] (*)	I	LL	SC5004 TCON mode chip location ID setting, see “Chip arrangement”
MASTER	I	L	SC5004 master chip setting H : master chip L : slave chip (Only master chip can enable internal power circuit and link with SC5005 Gate driver)
MASLOC	I	L	TCON mode :SC5004 master chip location H : master at left side of panel top view L : master at right side of panel top view
			SD mode : Act as CID[2] for internal register or MTP R/W
GSD_EN	I	L	Gate communication interface control. H : enable L : disable (Pure Gate IC mode)
HEATER (*)	O	-	External heater control signal
OVER_HEAT (*)	O	-	Over heat protection flag signal output
DISP_ON(*)	I	L	Display On for external CPU control, polarity can be inverse by register DISPON_POL (address 19, bit 7) and this function also related to NBW setting. H : Black pattern L : Normal display * Recommend connects this pin to GND for general purpose.
DFB (*)	O	-	Driver IC feedback signal
DIMI	I	L	LED backlight dimming input (100 ~ 10kHz)
DIMO (*)	O	-	LED backlight dimming output OHP_EN=L : when TCON=1, on/off sequence controlled by TCON, otherwise DIMO=DIMI. OHP_EN=H : DIMO controlled by BKL_DUTY register setting

Note: (*) means only effective in TCON mode

Control pins (hardware and software) :

PIN name	I/O	Int. pulled	Description
RSTB	I	H	Reset pin H : normal operation L : reset state, suggest to connecting with an RC circuit for stability
STBYB	I	H	Standby mode H : normal operation L : TCON, SD, power circuit and temp sensor will turn off
MODE (*)	I	L	TCON DE or SYNC mode selection H : DE mode L : SYNC mode
BIT6	I	L	Input data format selection H : 6-bit mode L : 8-bit mode
NBW (*)	I	L	Panel type selection H : normally black L : normally white * For SD mode can use HS_REV as NBW function
LR	I	L	SD horizontal shift direction selection H : SO[1] → SO[2] → … SO[1284] L : SO[1284] → SO[1283] → ... SO[1]
BGR (*)	I	L	RGB to BGR data mapping function H : enable (R and B data swap) L : disable
MLSB (*)	I	L	MSB to LSB sequence reverse function (TCON mode CMOS I/F only) H : enable (refer to P.12) L : disable
UD (*)	I	L	GD vertical shift direction selection, actual shift direction depends on GD location (Left or right side on panel)
RES[3:0]	I	HHLH	See “TCON / SD mode source output reference table”
LVDS_SWAP	I	L	LVDS pin sequence swap function, refer to P.12 interface pin mapping table H : Type B L : Type A
TS_EN (*)	I	L	Internal temperature sensor control H : enable L : disable
OHP_EN (*)	I	L	Over heat protection function H : enable L : disable
BIST (*)	I	L	Built-In Self Test function H : enable L : disable
PWM_EN	I	L	VDDA booster control H : enable L : disable
LDO_EN	I	L	RVDDA regulator control H : enable L : disable
VBUF_EN	I	L	Voltage buffer control H : enable L : disable

Note: (*) means only effective in TCON mode

Power circuit pins :

PIN name	I/O	Int. pulled	Description
DRV	O	-	PWM booster driving output
VFB	I	-	PWM booster reference voltage feedback
OPI	I	-	Voltage buffer input
OPO	O	-	Voltage buffer output
NFB	I	-	Voltage buffer negative feedback input (short to OPO in general case)
RVDDA	O	-	LDO voltage output

Gamma correction pins :

PIN name	I/O	Int. pulled	Description
GMAH	I	-	Source driver internal gamma resistor string top voltage
GMAL	I	-	Source driver internal gamma resistor string bottom voltage

Driver and cascade pins :

PIN name	I/O	Int. pulled	Description	
SO[1:1284]	O	-	Source driver voltage output	
XONR/XONL	I/O	-	Gate driver control signal (XON)	When TCON=1, these I/O are cascade signals between IC to IC. (P.22) When TCON=0, if using SC5005 internal DC-DC function then CUT and GSD are Gate driver control signals, see “Cascade & Gate driver connection (P.24~25)”.
OEVR/OEVL	I/O	-	Gate driver control signal (OE)	
UDR/UDL	I/O	-	Gate driver control signal (U_D)	
CKVR/CKVL	I/O	-	Gate driver control signal (CKV)	
CUTR/CUTL	I/O	-	Gate driver control signal (CUT)	
GSDR/GSDL	I/O	-	Gate driver control signal (GSD)	
STV1R/STV1L	I/O	-	Gate driver control signal (STVU)	When TCON=1, STV1 and STV2 must connect with G-IC directly, refer to P.22 “Cascade & Gate driver connection”.
STV2R/STV2L	I/O	-	Gate driver control signal (STVD)	

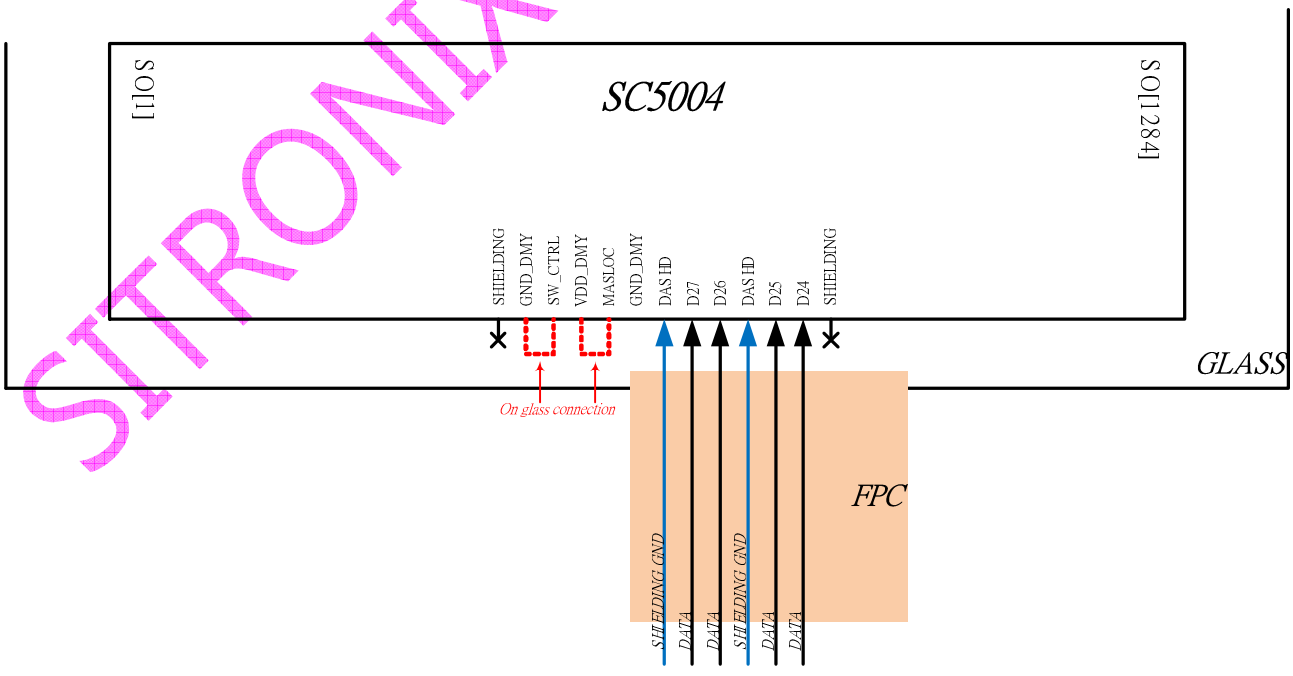
Other pins :

PIN name	I/O	Int. pulled	Description
TP[4:1]	I	L	Test pins, leave it open
TP[18:5]	O	-	Test pins, leave it open
COMR_T	-	-	COMR_T & COMR_B are shorted internally for VCOM connection
COMR_B			
COML_T	-	-	COML_T & COML_B are shorted internally for VCOM connection
COML_B			
MEAS1R/MEAS2R	-	-	MEAS1R and MEAS2R are shorted internally for resistance measurement MEAS1L and MEAS2L are shorted internally for resistance measurement
MEAS1L/MEAS2L	-	-	
SHIELDING	SG	-	Noise shielding PAD, internal connect to GNDA
DASHD	SG	-	Noise shielding PAD, internal connect to GND
VDD_DMY	O	-	For IC on glass setting only, internal connect to VDD.
GND_DMY	O	-	For IC on glass setting only, internal connect to GND.

Note:

I : Input
O : Output
I/O : input/output (Bi-direction)
P : Power
SG : Shielding Ground

SHIELDING, DASHD, VDD_DMY and GND_DMY connection guide :



Recommend wiring resistance value

Function type	Pin name	Wiring resistance value (Ω)
Power supply	VDD	< 10
	VDD_LVDS	
	VDDA	
	GND	
	GND_LVDS	
	GNDA	
	VDD_MTP	
Input interface	EIO1	< 10
	EIO2	
	D00~D07	< 30
	D10~D17	
	D20~D27	
	CLKP	
	CLKN	
	VS_POL	
	DE_LD	
	HS_REV	
	PON_STV	
	POFF_CKV	
SPI / I^2C EEPROM interface	CSB	< 50
	SCL	
	SDA	
Power circuit	VFB	< 100
	OPI	
	NFB	
	DRV	< 10
	OPO	
	RVDDA	
Gamma correction	GMAH	< 10
	GMAL	
Driver and cascade	XONR/XONL	< 150
	OEVR/OEVL	
	UDR/UDL	
	CKVR/CKVL	
	STV1R/STV1L	
	STV2R/STV2L	
	SYNC1R/SYNC1L	
	SYNC2R/SYNC2L	
	GSDR/GSDL	
	CUTR/CUTL	

Function type	Pin name	Wiring resistance value (Ω)
Control	RSTB	< 50
	STBYB	
	SPI_I2C	< 150
	RSDS_HF	
	SW_CTRL	
	IF_SEL[1:0]	
	EEP_EN	
	MTP_EN	
	ROM_RLB	
	CID[1:0]	
	MASTER	
	MASLOC	
	TS_EN	
	DISP_ON	
	OHP_EN	
	CLK_POL	
	MODE	
	BIT8	
	TCON	
	NBW	
	LR	
	UD	
	RES[3:0]	
	LVDS_SWAP	
	IPOR_ENB	
	BIST	
	PWM_EN	
	GSD_EN	
	LDO_EN	
	VBUF_EN	
	OVER_HEAT	
	HEATER	
	DFB	
	BGR	
	MLSB	
	DIMI	
	DIMO	
Others	COMR_B/COML_B	< 10

Interface selection table

IF_SEL[1]	IF_SEL[0]	Interface	Max. pixel frequency
0	0	LVDS	80MHz
0	1	CMOS	60MHz
1	0	RSDS	120MHz
1	1	mini-LVDS	170MHz

Input interface pin mapping table

Pin name	Interface											
	CMOS				LVDS				RSDS		mini-LVDS	
	MLSB=0		MLSB=1		LVDS_SWAP=0		LVDS_SWAP=1		-	-	-	-
	8 bit	6 bit	8 bit	6 bit	8 bit	6 bit	8 bit	6 bit	8 bit	6 bit	8 bit	6 bit
D00	D00	-	D07	-	-	-			D00N	D00N	D0N	D0N
D01	D01	-	D06	-	-	-			D00P	D00P	D0P	D0P
D02	D02	D00	D05	D05	-	-			D01N	D01N	D1N	D1N
D03	D03	D01	D04	D04	-	-			D01P	D01P	D1P	D1P
D04	D04	D02	D03	D03	-	-			D02N	D02N	D2N	D2N
D05	D05	D03	D02	D02	-	-			D02P	D02P	D2P	D2P
D06	D06	D04	D01	D01	-	-			D03N	-	-	-
D07	D07	D05	D00	D00	-	-			D03P	-	-	-
D10	D10	-	D17	-	-	-			D10N	D10N	D3N	D3N
D11	D11	-	D16	-	-	-			D10P	D10P	D3P	D3P
D12	D12	D10	D15	D15	-	-			D11N	D11N	D4N	D4N
D13	D13	D11	D14	D14	-	-			D11P	D11P	D4P	D4P
D14	D14	D12	D13	D13	-	-			D12N	D12N	D5N	D5N
D15	D15	D13	D12	D12	-	-			D12P	D12P	D5P	D5P
D16	D16	D14	D11	D11	-	-			D13N	-	-	-
D17	D17	D15	D10	D10	-	-			D13P	-	-	-
CLKN	-	-	-	-	CLKN	CLKN	D3P	-	CLKN	CLKN	CLKN	CLKN
CLKP	CLK	CLK	CLK	CLK	CLKP	CLKP	D3N	-	CLKP	CLKP	CLKP	CLKP
D20	D20	-	D27	-	D0N	D0N	CLKP	CLKP	D20N	D20N	-	-
D21	D21	-	D26	-	D0P	D0P	CLKN	CLKN	D20P	D20P	-	-
D22	D22	D20	D25	D25	D1N	D1N	D2P	D2P	D21N	D21N	-	-
D23	D23	D21	D24	D24	D1P	D1P	D2N	D2N	D21P	D21P	-	-
D24	D24	D22	D23	D23	D2N	D2N	D1P	D1P	D22N	D22N	-	-
D25	D25	D23	D22	D22	D2P	D2P	D1N	D1N	D22P	D22P	-	-
D26	D26	D24	D21	D21	D3N	-	D0P	D0P	D23N	-	-	-
D27	D27	D25	D20	D20	D3P	-	D0N	D0N	D23P	-	-	-

Resolution and interface quickly reference table

RES[3 :0]	Resolution	SD channel	Min. IC Q'ty	Pixel clock rate @ 60Hz frame rate (unit=MHz)	TCON mode interface		Source driver mode interface		
					CMOS	LVDS	CMOS	RSDS	m-LVDS
0000	1920x720	1152	5	100	-	-	-	●	●
0001	1366x768	1026/1020	4	75	-	●	-	●	●
0010	1280x800	1284/1278	3	73	-	●	-	●	●
0011	800x1280	1200	2	73	-	●	-	●	●
0100	1600x600	1200	4	70	-	●	-	●	●
0101	1280x720	1284/1278	3	66	-	●	-	●	●
0110	1440x540	1080	4	56	●	●	●	●	●
0111	1024x768	1026/1020	3	56	●	●	●	●	●
1000	1280x480	1284/1278	3	45	●	●	●	●	●
1001	1024x600	1026/1020	3	45	●	●	●	●	●
1010	1024x480	1026/1020	3	35	●	●	●	●	●
1011	960x540	960	3	38	●	●	●	●	●
1100	800x600	1200	2	35	●	●	●	●	●
1101	800x480	1200	2	28	●	●	●	●	●
1110	640x480	960	2	22	●	●	●	●	●
1111	Programmable	1284	4(Max)	80 (Max)	●	●	-	-	-

Note:

1. Different resolution with cascade SC5004 quantities will depend on panel size, display interface, FPC layout and external components location …etc.
2. For each application's best solution, please consult with Sitronix.

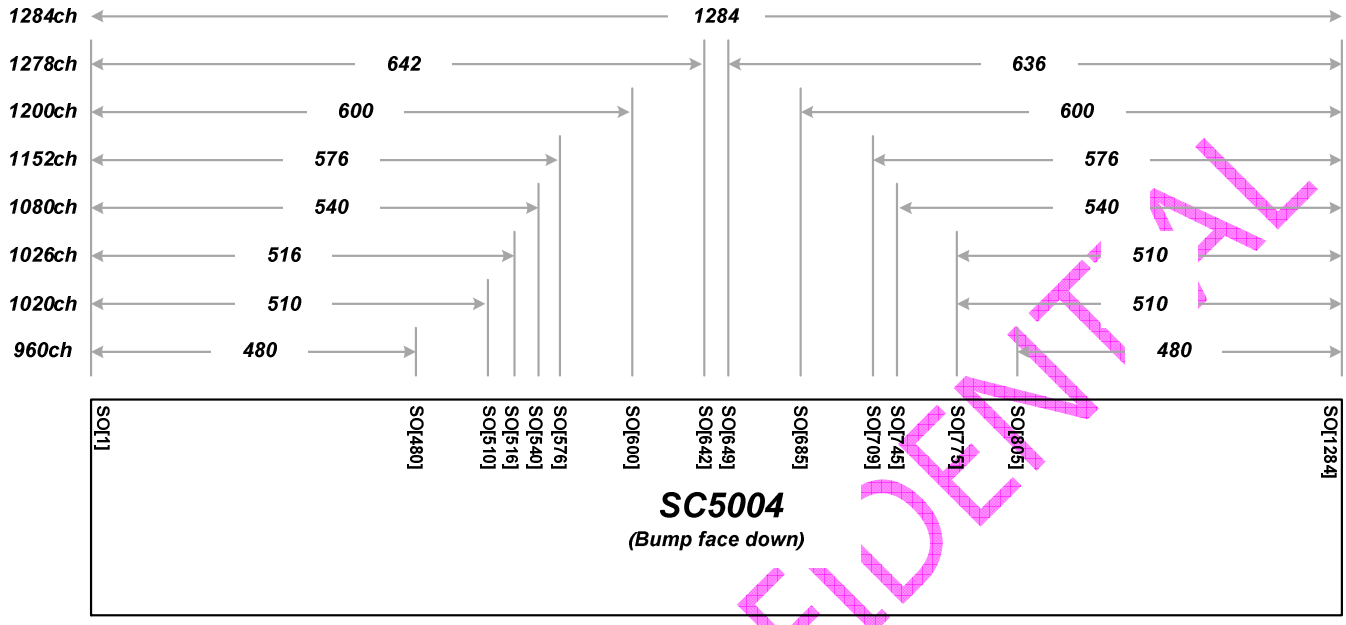
TCON / SD mode source output reference table

Input pin setting							SD channel
TCON	CID[1]	CID[0]	RES[3]	RES[2]	RES[1]	RES[0]	
1	*	*	0	0	0	0	1152
1	0	0	0	0	0	1	1026
1	0	1					1026
1	1	0					1026
1	1	1					1020
1	0	0	0	0	1	0	1278
1	0	1					1278
1	1	0					1284
1	1	1					(1284)
1	*	*	0	0	1	1	1200
1	*	*	0	1	0	0	1200
1	0	0	0	1	0	1	1278
1	0	1					1278
1	1	0					1284
1	1	1					(1284)
1	*	*	0	1	1	0	1080
1	0	0	0	1	1	1	1026
1	0	1					1026
1	1	0					1020
1	1	1					(1020)
1	0	0	1	0	0	0	1278
1	0	1					1278
1	1	0					1284
1	1	1					(1284)
1	0	0	1	0	0	1	1026
1	0	1					1026
1	1	0					1020
1	1	1					(1020)
1	0	0	1	0	1	0	1026
1	0	1					1026
1	1	0					1020
1	1	1					(1020)
1	*	*	1	0	1	1	960
1	*	*	1	1	0	0	1200
1	*	*	1	1	0	1	1200
1	*	*	1	1	1	0	960
1	*	*	1	1	1	1	1284
0	*	*	x	0	0	0	960
0	*	*	x	0	0	1	1020
0	*	*	x	0	1	0	1026
0	*	*	x	0	1	1	1080
0	*	*	x	1	0	0	1152
0	*	*	x	1	0	1	1200
0	*	*	x	1	1	0	1278
0	*	*	x	1	1	1	1284

Note:

1. * means no matter CID[1:0] setting, all output are the same quantity and each IC still needs to set ID[1:0] to identify chip ID.
2. If user want to program each SC5004's register or MTP value then the CID[1:0] must be set correctly.

Resolution and source output relationship



TCON mode specail resolution and source output relationship

1366x768

1026ch	1026ch	1026ch	1020ch
RES[3:0]=0001 CID[1:0]=00	RES[3:0]=0001 CID[1:0]=01	RES[3:0]=0001 CID[1:0]=10	RES[3:0]=0001 CID[1:0]=11

1280x(480/720/800)

1278ch	1278ch	1284ch
RES[3:0]=0010,0101,1000 CID[1:0]=00	RES[3:0]=0010,0101,1000 CID[1:0]=01	RES[3:0]=0010,0101,1000 CID[1:0]=10

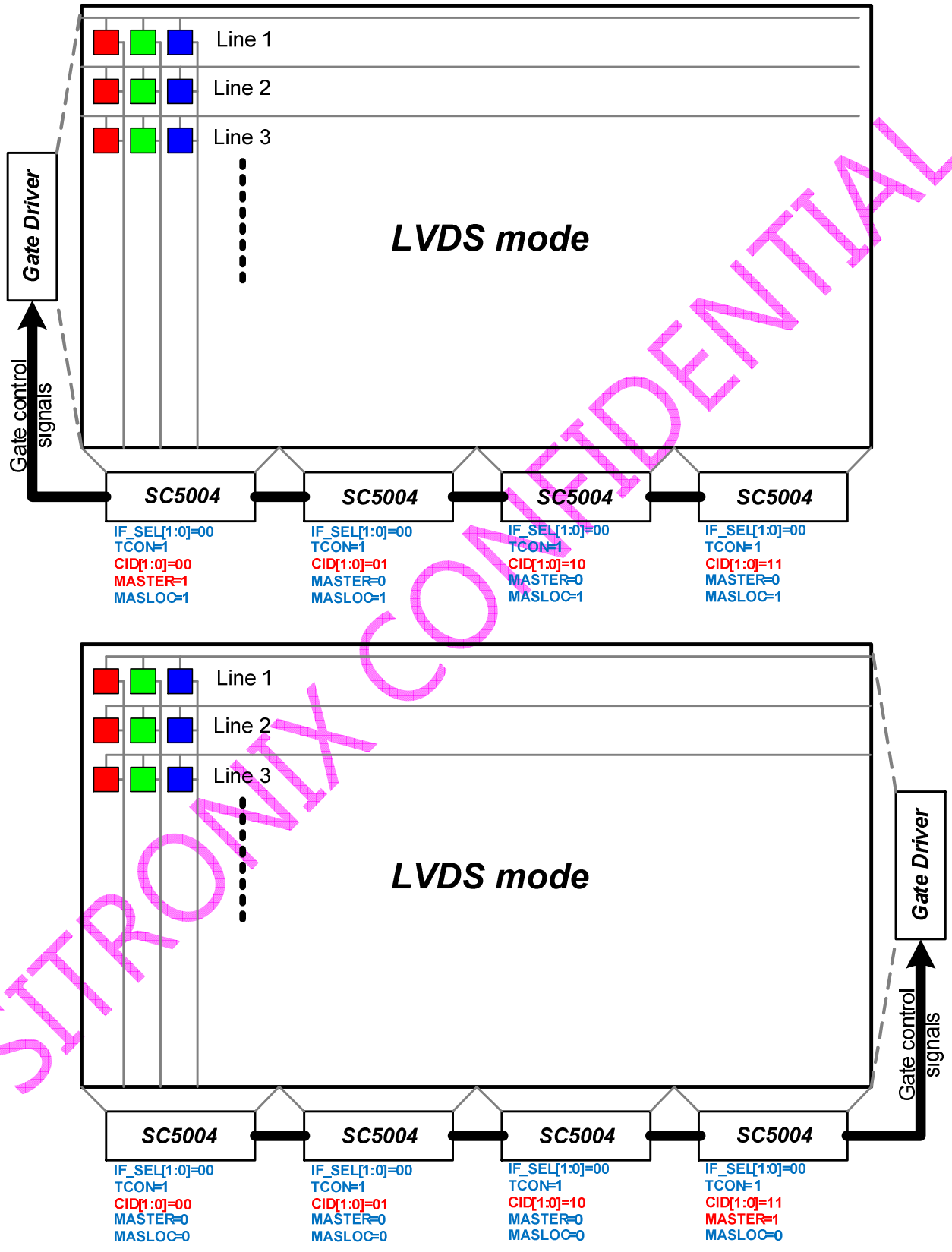
1024x(480/600/768)

1026ch	1026ch	1020ch
RES[3:0]=0111,1001,1010 CID[1:0]=00	RES[3:0]=0111,1001,1010 CID[1:0]=01	RES[3:0]=0111,1001,1010 CID[1:0]=10

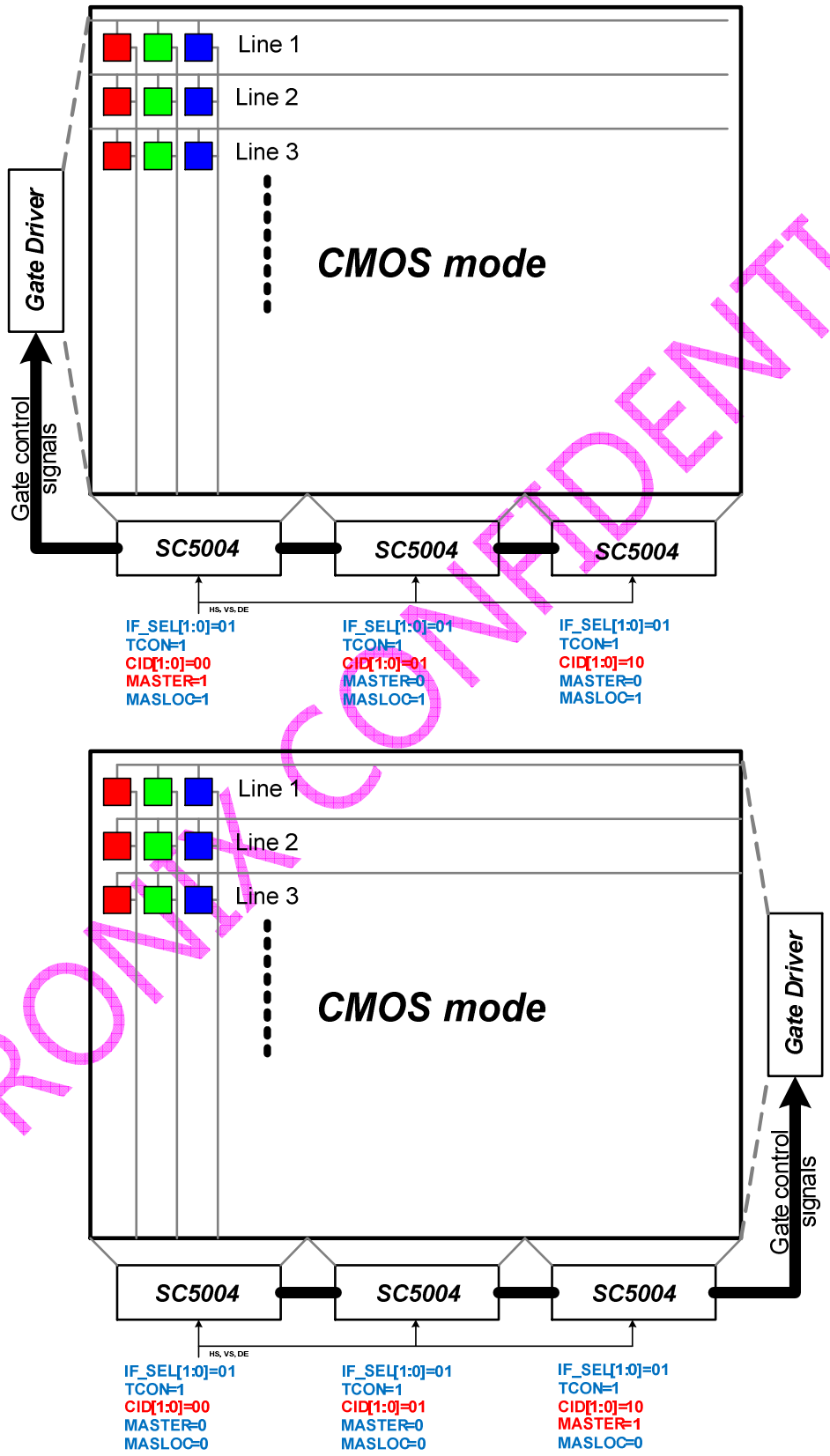
Chip arrangement and scan direction control

Note: UD and LR can be inverse by S/W register 03/h LR_INV and UD_INV (refer to P.86)

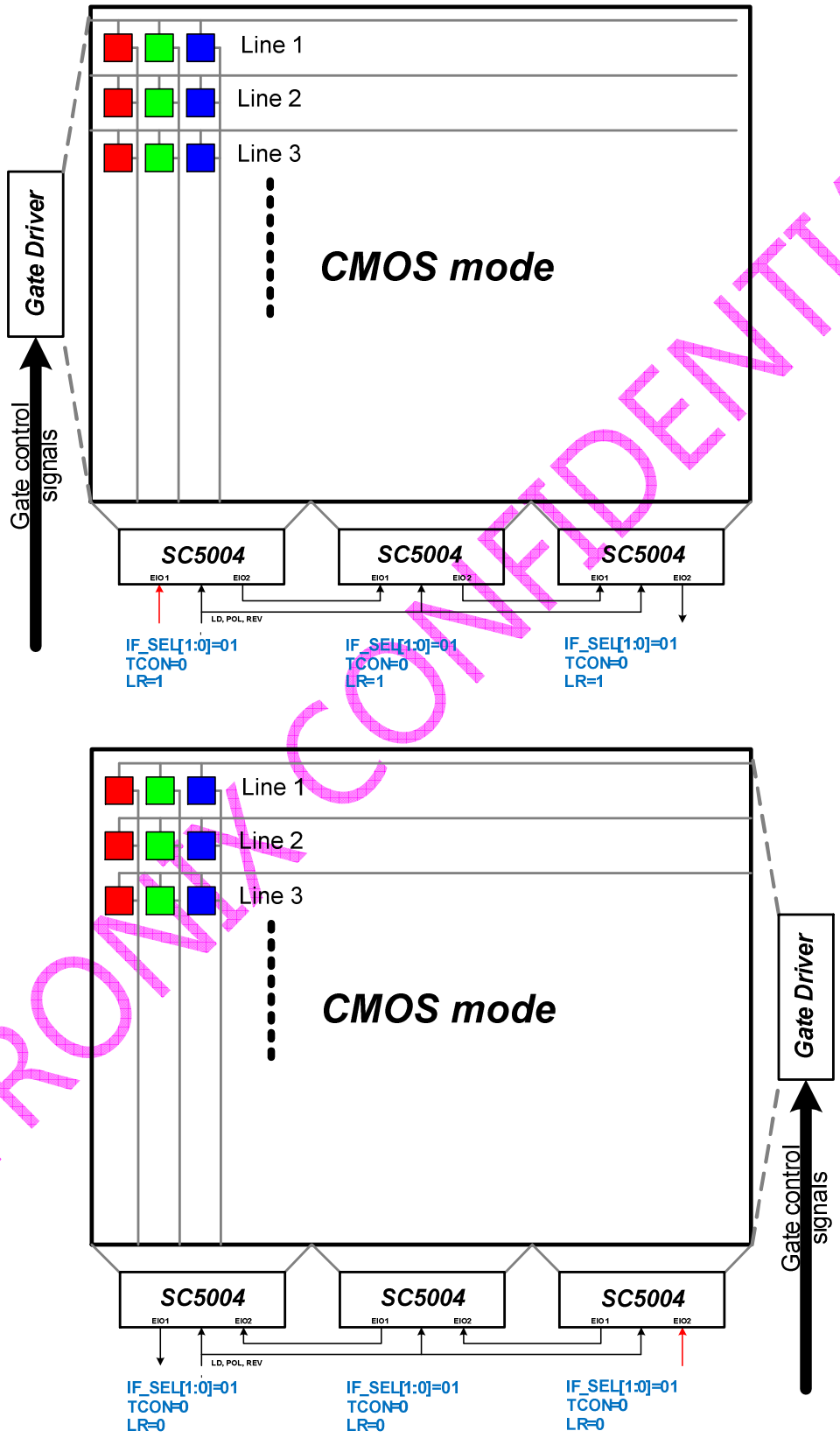
Chip arrangement (TCON LVDS mode)



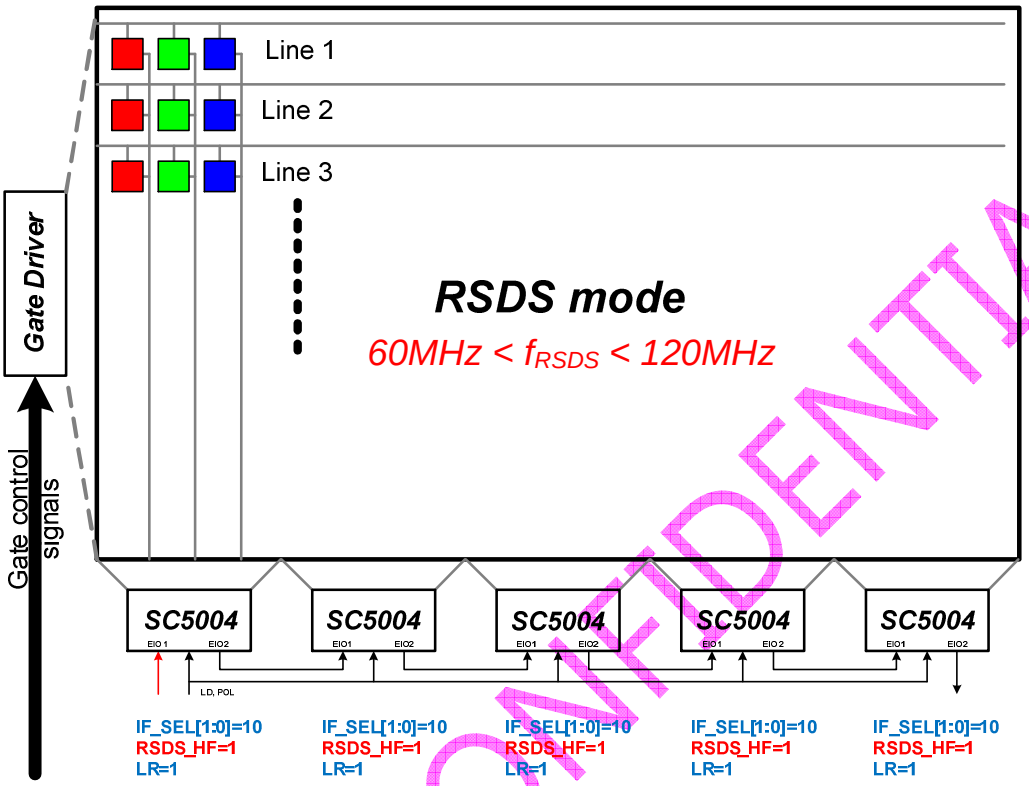
Chip arrangement (TCON CMOS mode)

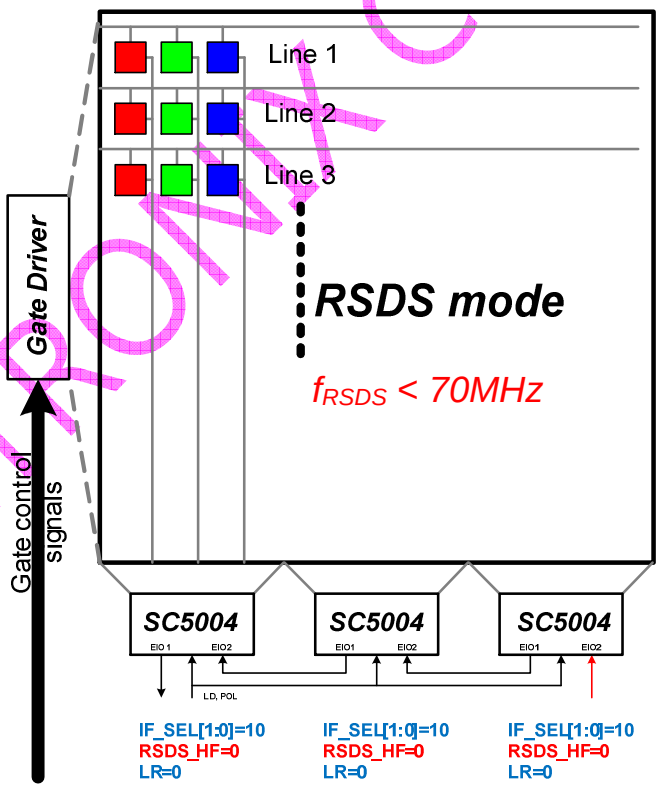


Chip arrangement (SD CMOS mode)

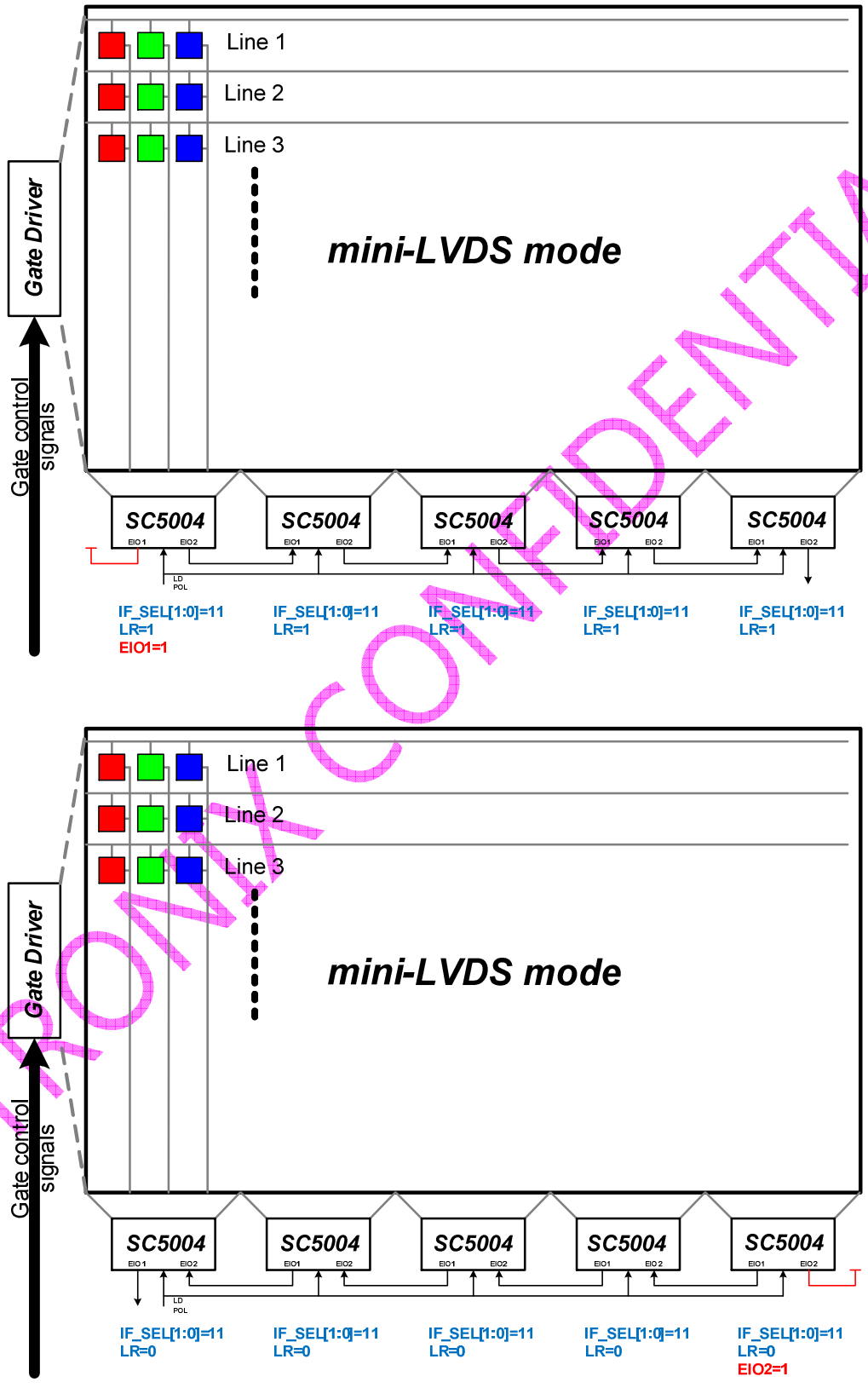


Chip arrangement (SD RSDS mode)



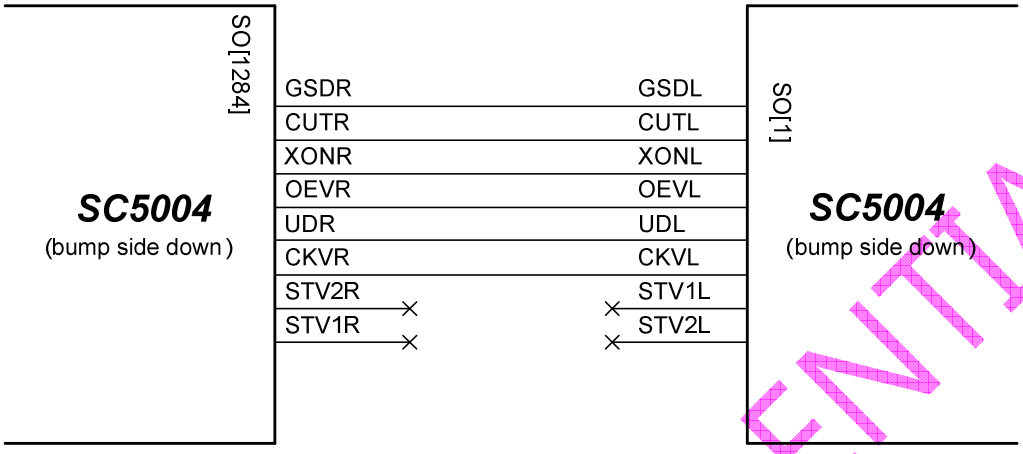


Chip arrangement (SD mini-LVDS mode)

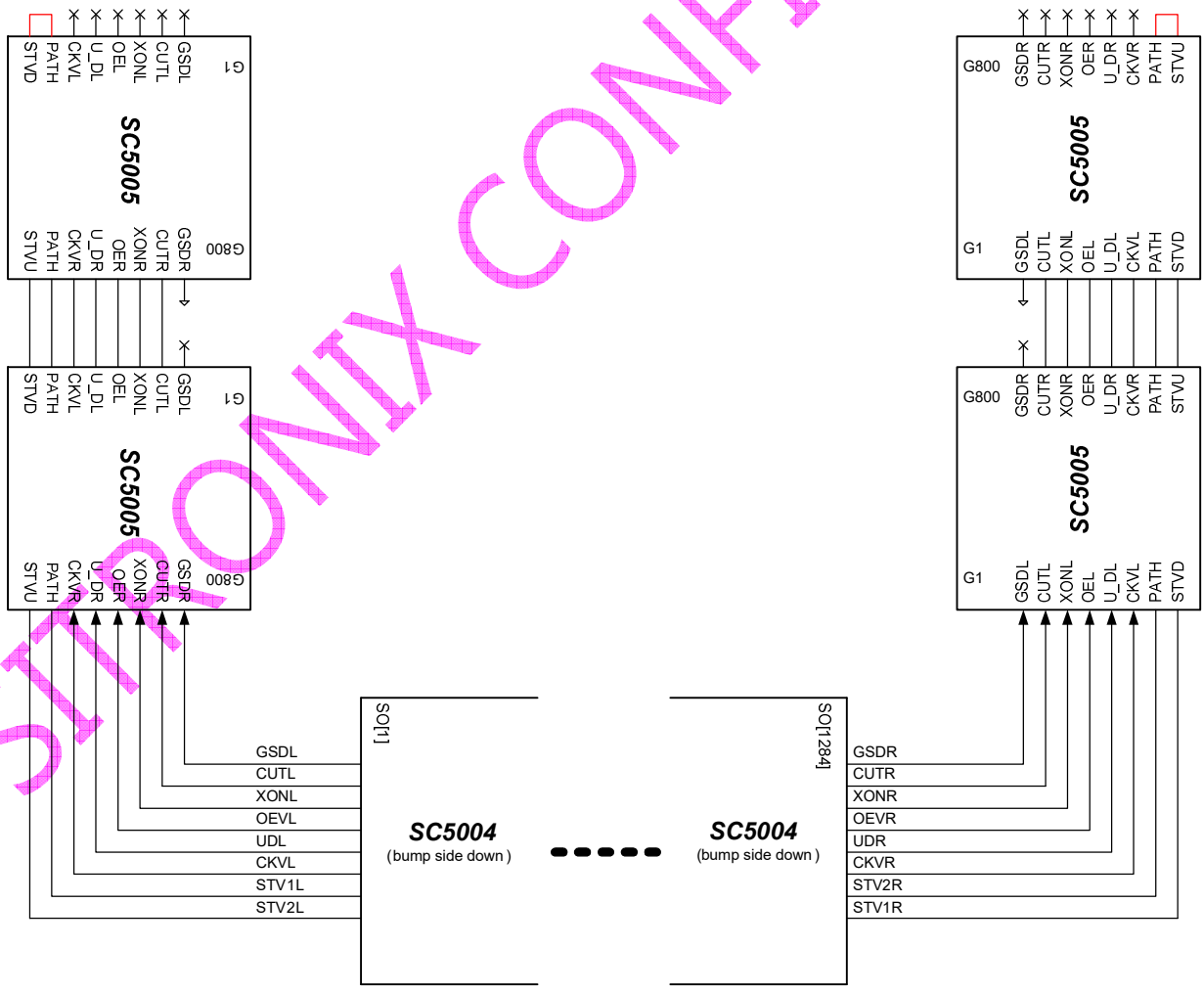


Cascade & Gate driver connection

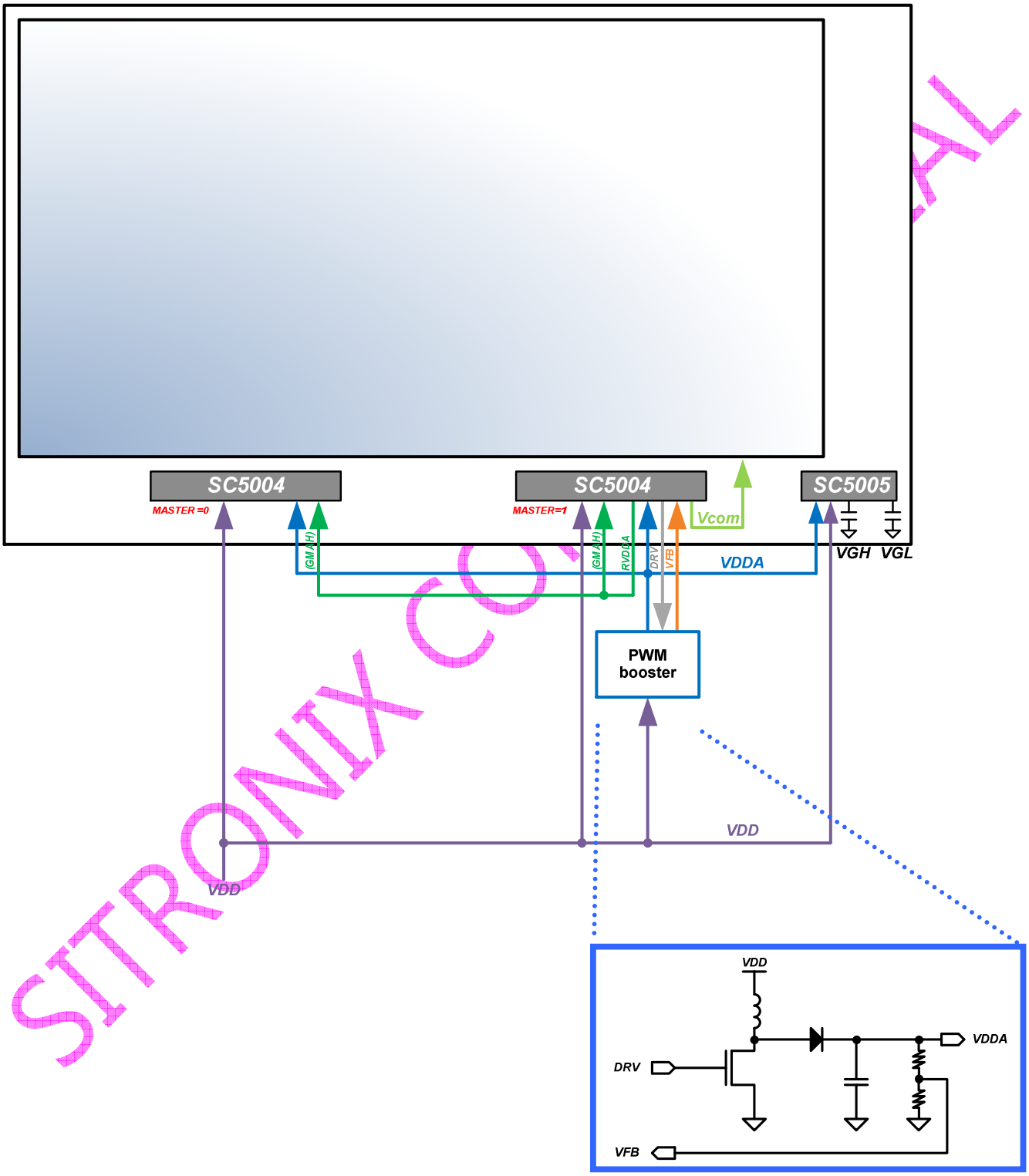
TCON mode SC5004 to SC5004 cascade connection



SC5004 to SC5005 Gate driver connection

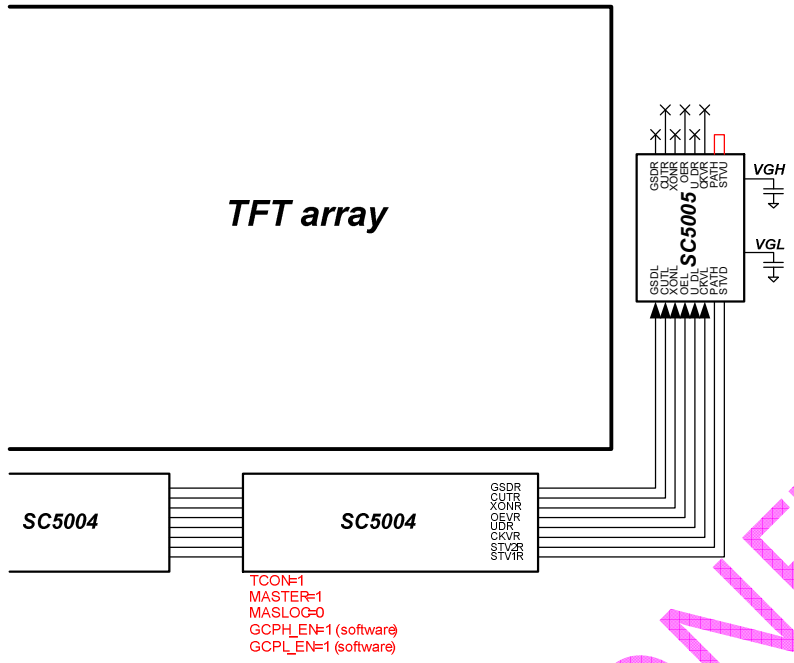


Power & Gate driver connection



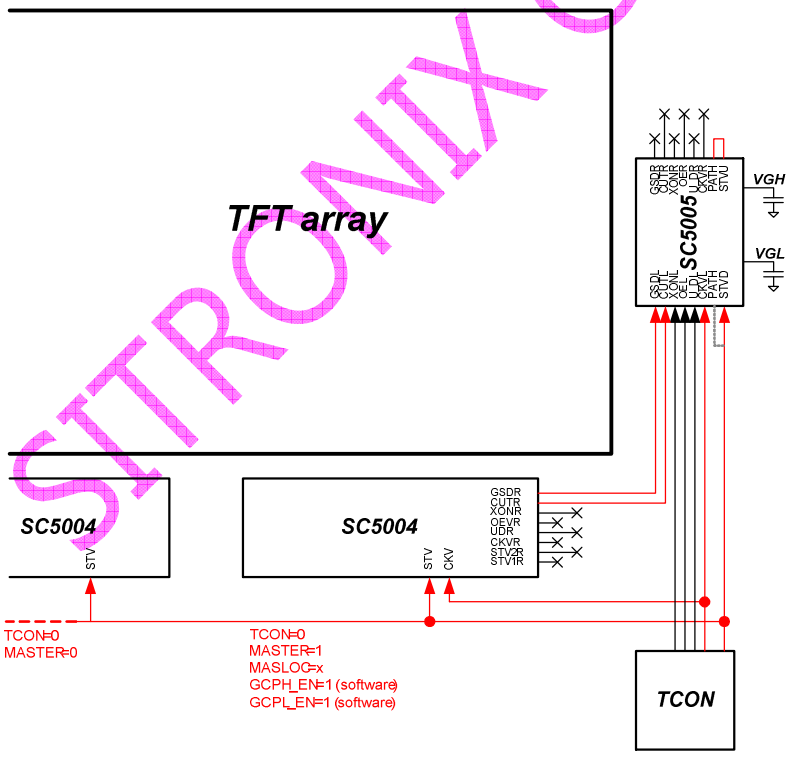
Power & Gate driver connection

TCON + SD mode with Gate driver charge pump connection

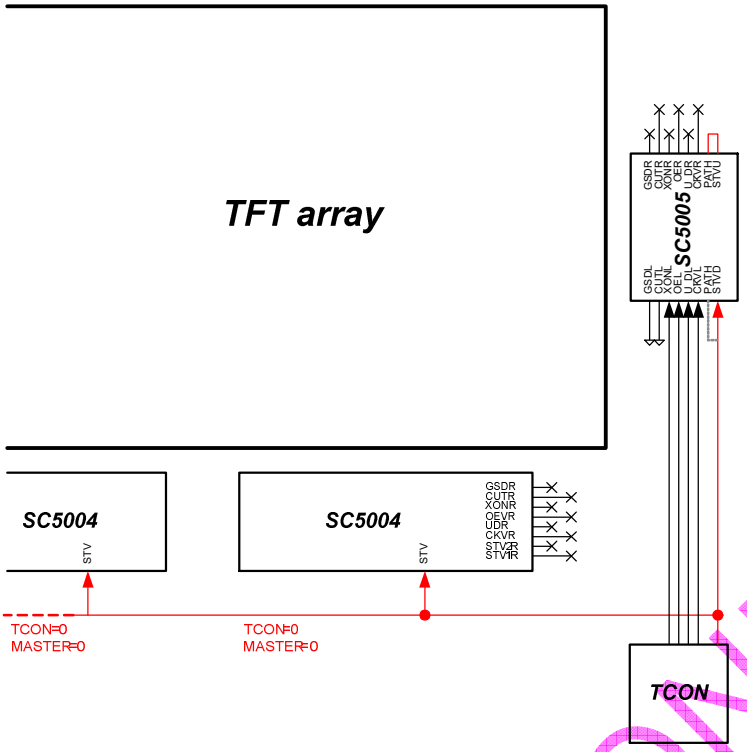


SD mode with Gate driver charge pump connection

(STV signal must connect to each SC5004 SD as offset cancellation control)

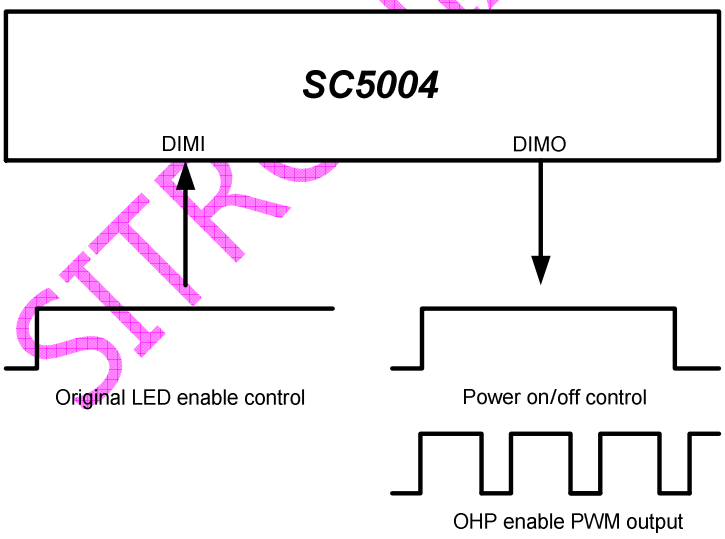


SD mode without Gate driver charge pump connection
(STV signal must connect to each SC5004 SD as offset cancellation control)



LED backlight enable control connection

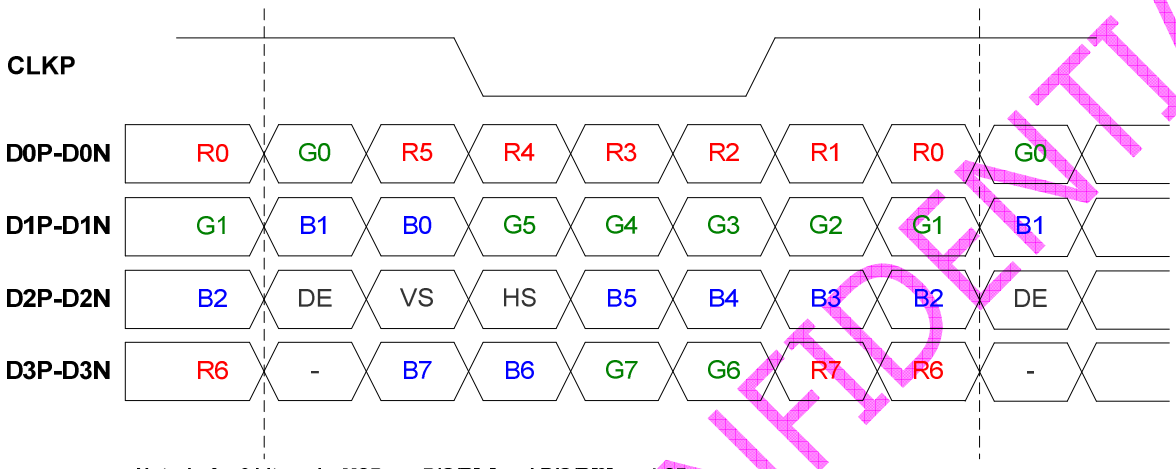
If user wants to adopt SC5004 TCON mode LED backlight power on sequence or enable OHP (Over Heat Protection) function, please follow this connection.



Interface timing

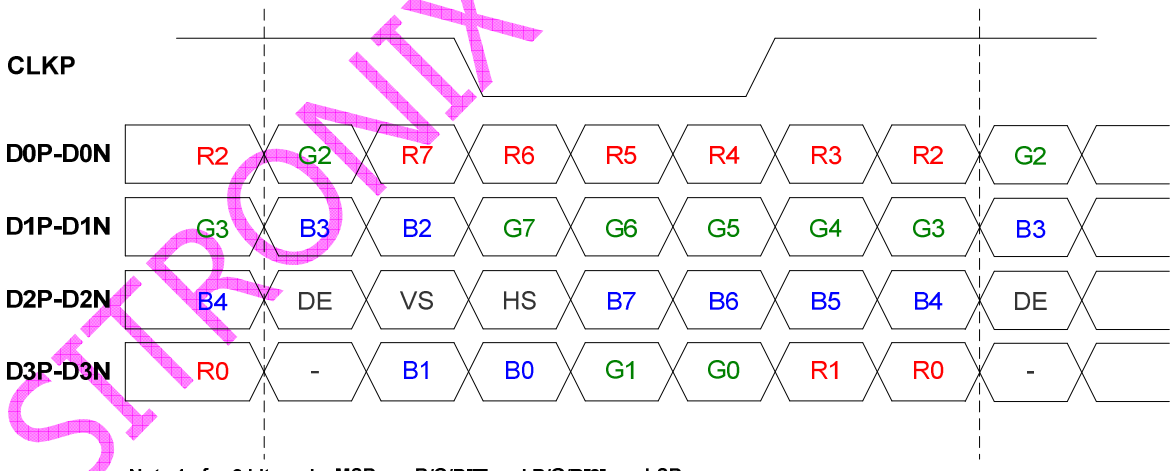
TCON mode LVDS interface data mapping

VESA data mapping



Note 1 : for 6 bit mode, MSB are R/G/B[5] and R/G/B[0] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

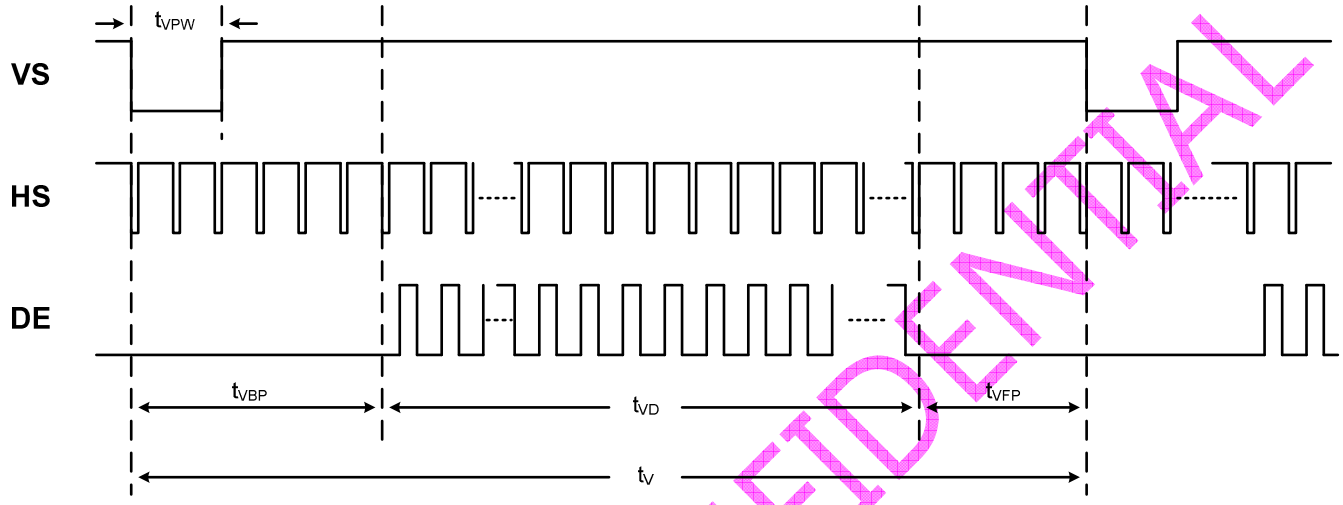
JEIDA data mapping



Note 1 : for 6 bit mode, MSB are R/G/B[7] and R/G/B[2] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

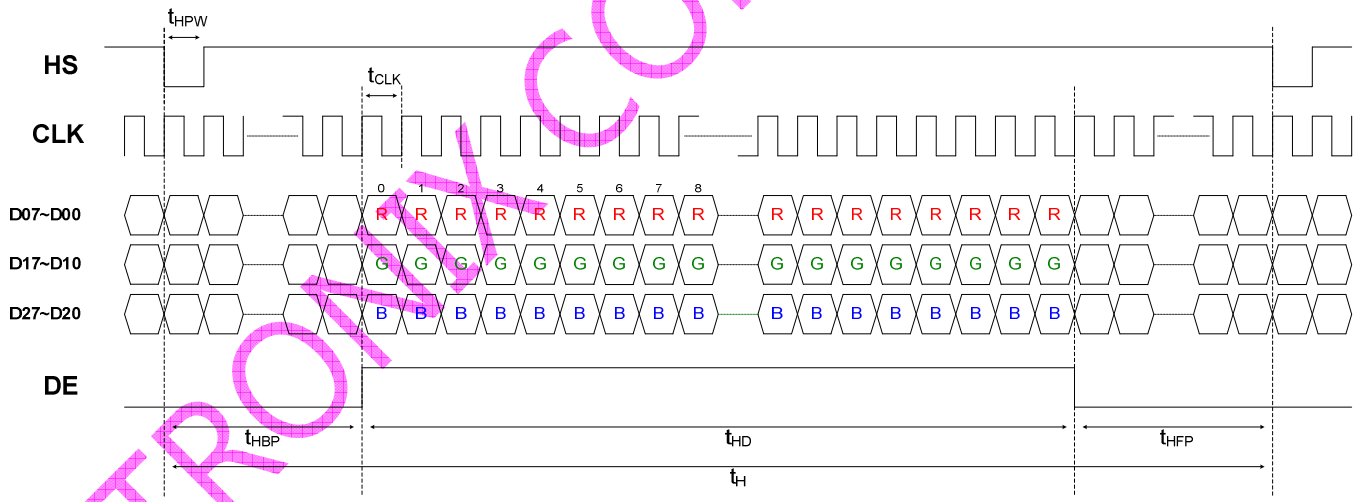
TCON mode CMOS interface

Vertical input timing



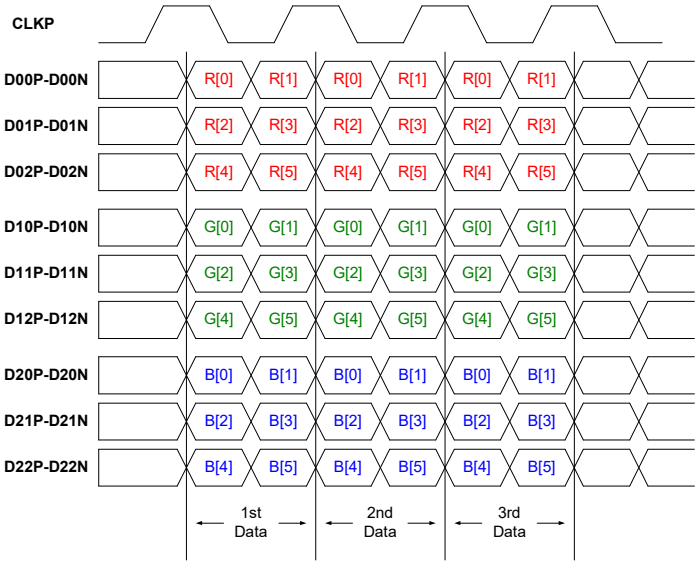
Horizontal input timing

(CLK_POL=L)

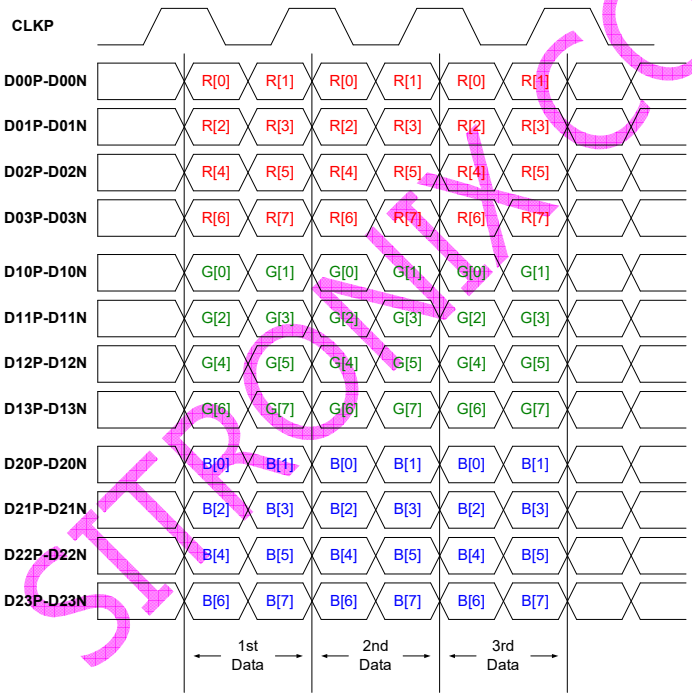


Source driver mode RSDS interface

RSDS 6-Bits Data Mapping

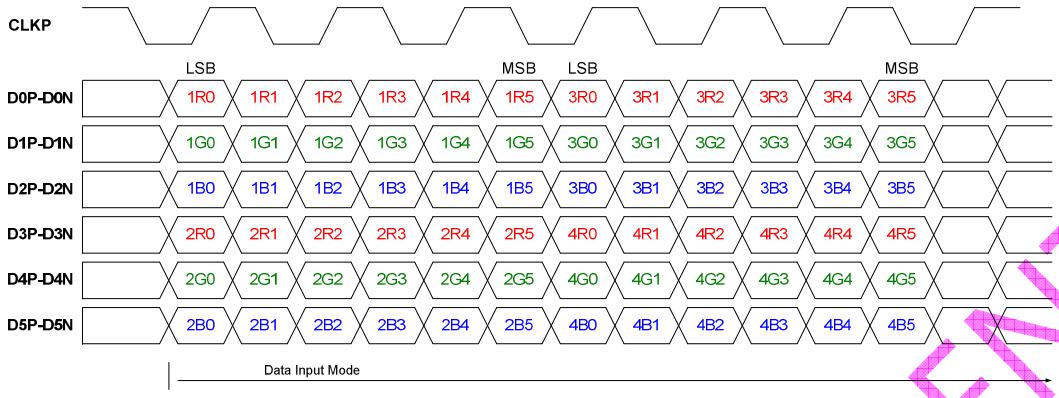


RSDS 8-Bits Data Mapping

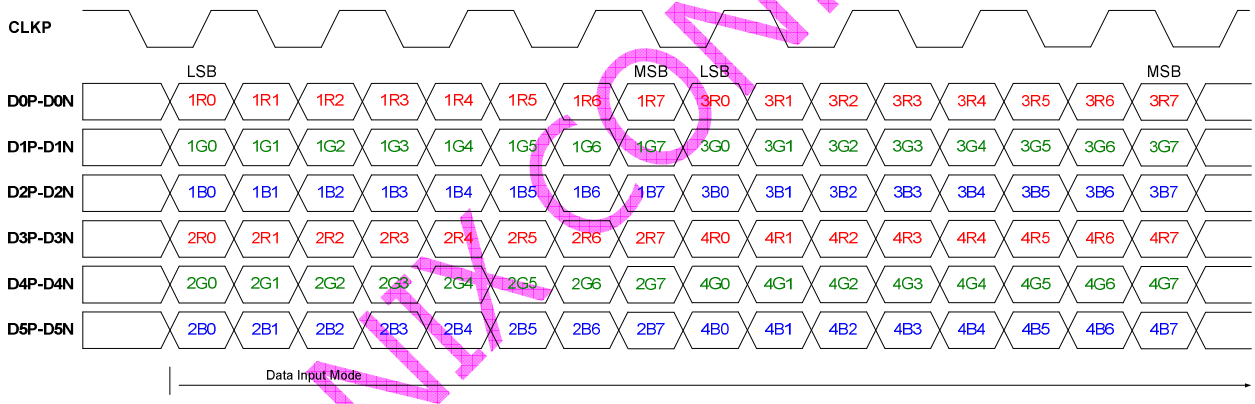


Source driver mode mini-LVDS interface

Mini-LVDS 6-Bits Data Mapping



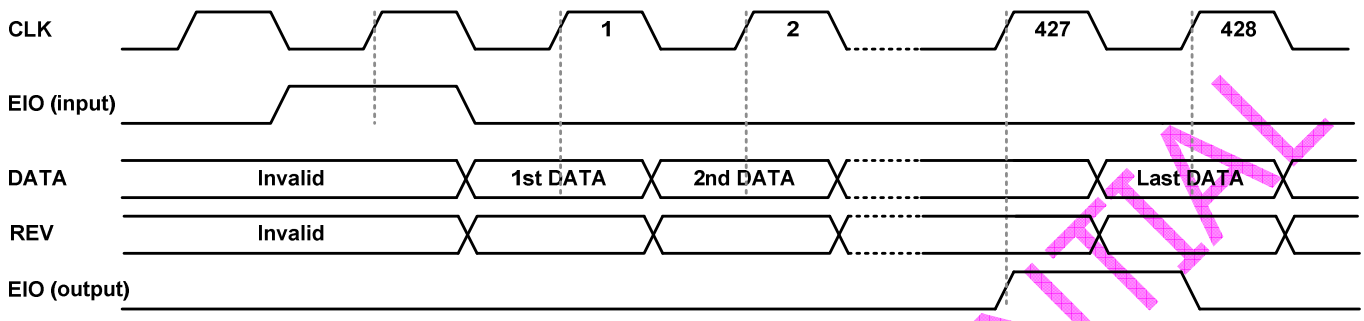
Mini-LVDS 8-Bits Data Mapping



Relationship of mini-LVDS input data and output channel

LR	O1	O2	O3	O4	O5	O6	O7	O8	O9	…	O1276	O1277	O1278	O1279	O1280	O1281	O1282	O1283	O1284
H	1R	1G	1B	2R	2G	2B	3R	3G	3B	…	426R	426G	426B	427R	427G	427B	428R	428G	428B
L	427R	427G	427B	428R	428G	428B	425R	425G	425B	…	4R	4G	4B	1R	1G	1B	2R	2G	2B

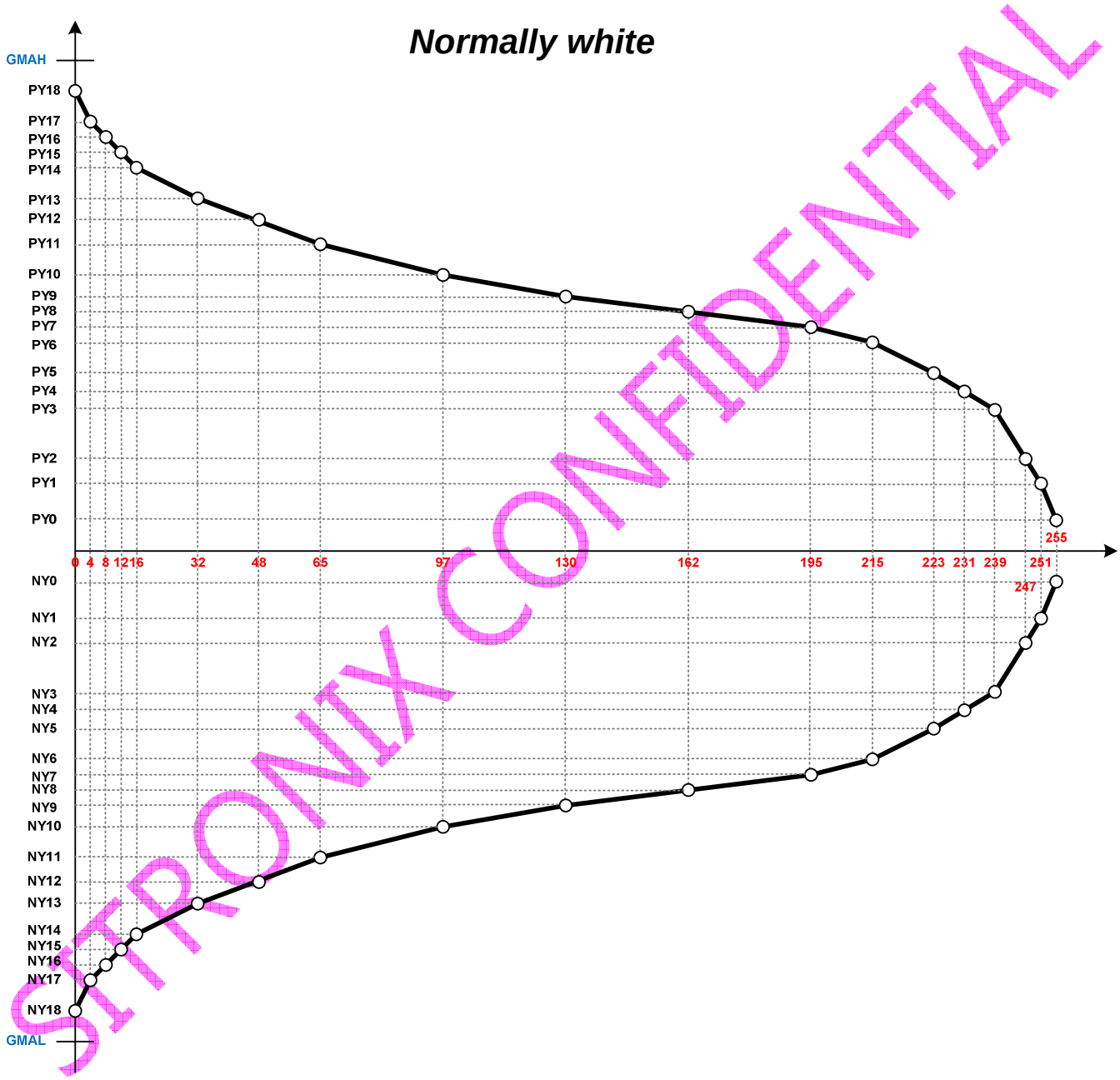
Source driver mode CMOS interface



Note : CLK_POL setting is not available for SD mode CMOS interface

Relationship between Input Data and Output Voltage

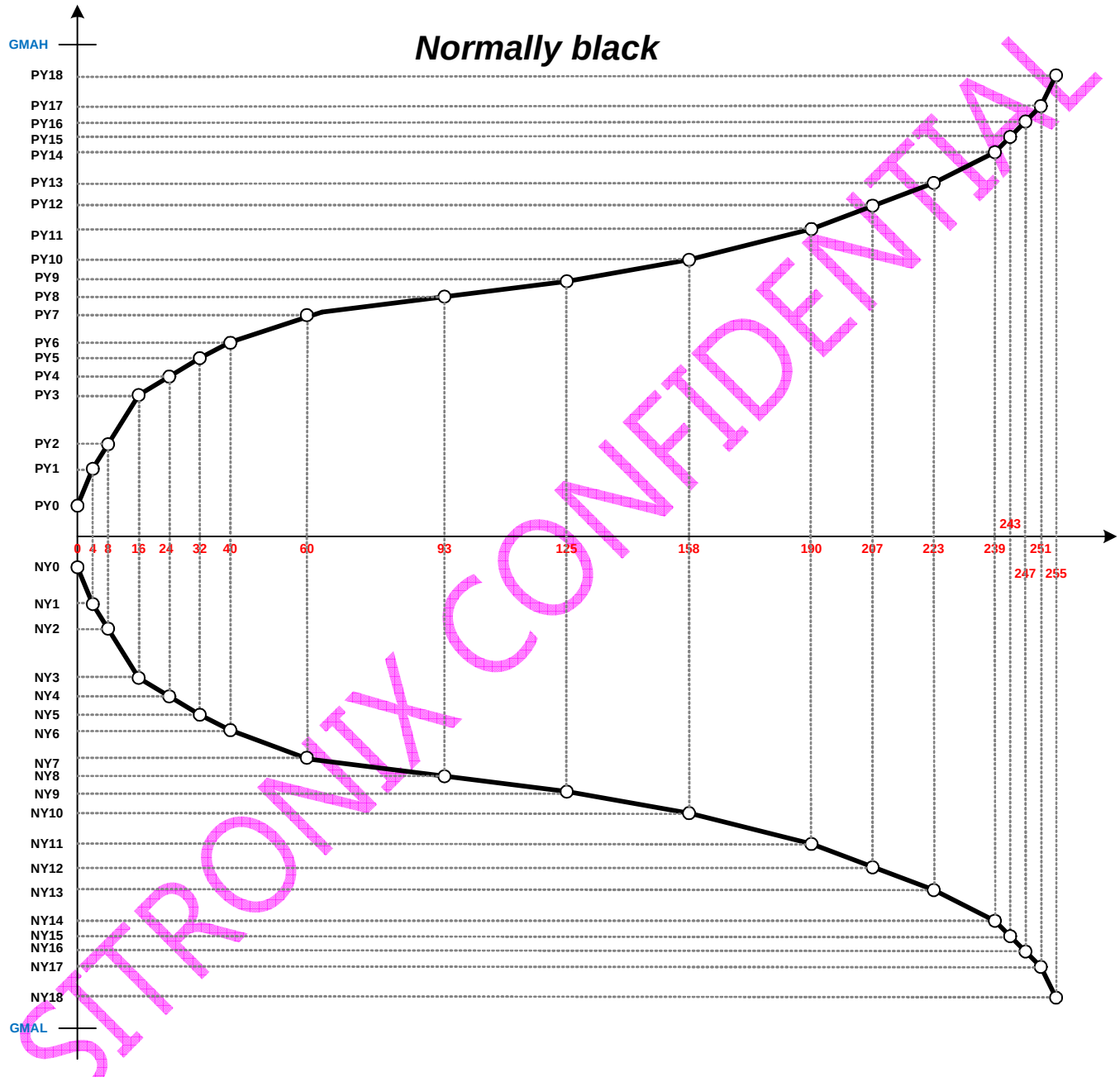
The figure below shows the relationship between the input data and the output voltage with the output polarity. Please refer to "Gamma register and correction voltage mapping table".



Note :

(1) VDDA-2.5V ≦ GMAH ≦ VDDA

(2) GNDA ≦ GMAL ≦ 2.0V

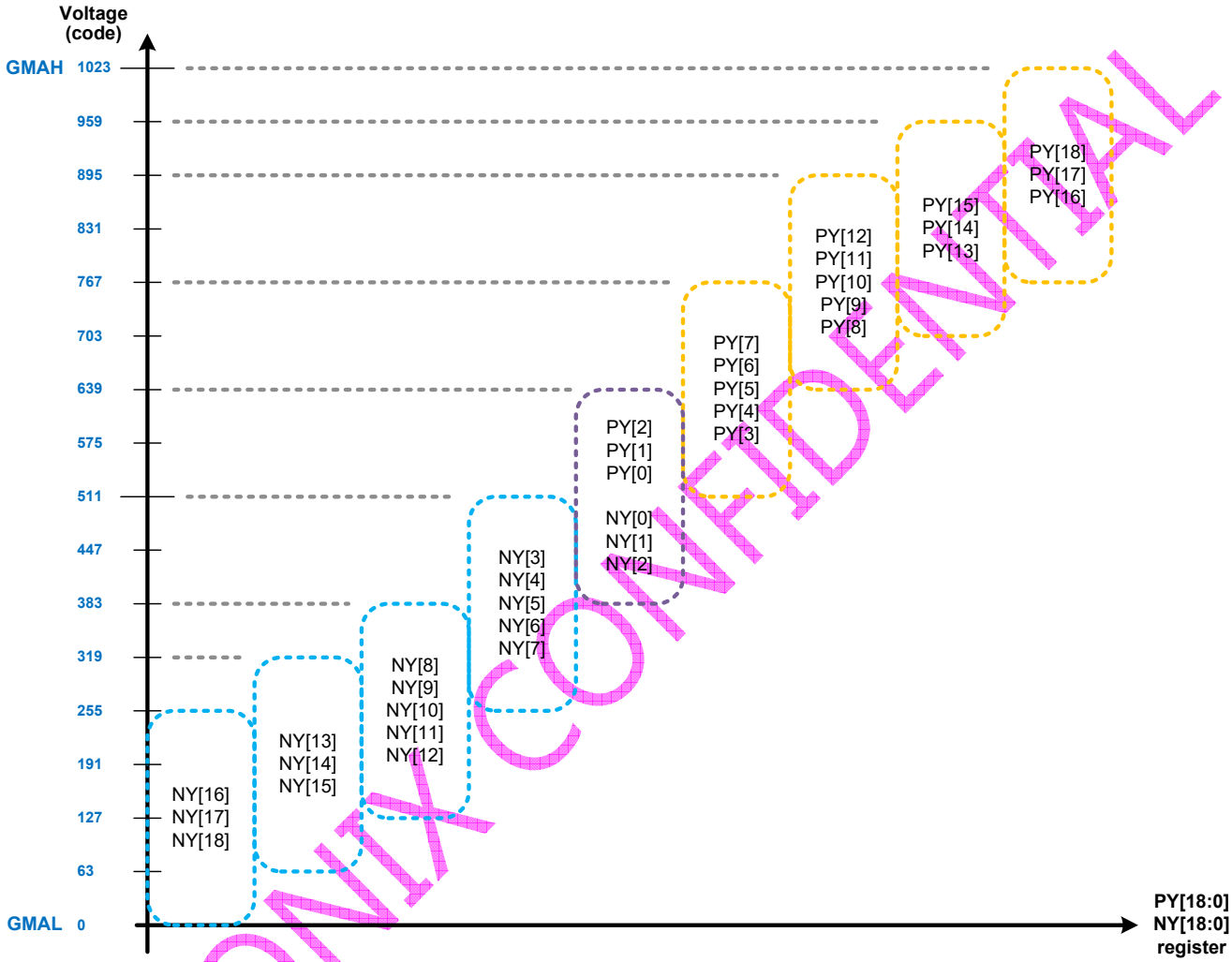


Note :

(1) VDDA-2.5V ≦ GMAH ≦ VDDA

(2) GNDA ≦ GMAL ≦ 2.0V

Gamma register and correction voltage mapping table



Gamma register voltage calculation formula table

Register	Gamma correction voltage
PY[18]	GMAH – [(GMAH-GMAL) / 1023] x (register value + 0)
PY[17]	
PY[16]	
PY[15]	GMAH – [(GMAH-GMAL) / 1023] x (register value + 64)
PY[14]	
PY[13]	
PY[12]	GMAH – [(GMAH-GMAL) / 1023] x (register value + 128)
PY[11]	
PY[10]	
PY[9]	
PY[8]	
PY[7]	GMAH – [(GMAH-GMAL) / 1023] x (register value + 256)
PY[6]	
PY[5]	
PY[4]	
PY[3]	
PY[2]	GMAH – [(GMAH-GMAL) / 1023] x (register value + 384)
PY[1]	
PY[0]	
NY[0]	[(GMAH-GMAL) / 1023] x (register value + 384) + GMAL
NY[1]	
NY[2]	
NY[3]	[(GMAH-GMAL) / 1023] x (register value + 256) + GMAL
NY[4]	
NY[5]	
NY[6]	
NY[7]	
NY[8]	[(GMAH-GMAL) / 1023] x (register value + 128) + GMAL
NY[9]	
NY[10]	
NY[11]	
NY[12]	
NY[13]	[(GMAH-GMAL) / 1023] x (register value + 64) + GMAL
NY[14]	
NY[15]	
NY[16]	[(GMAH-GMAL) / 1023] x (register value + 0) + GMAL
NY[17]	
NY[18]	

Gamma gray code voltage calculation formula table (normally white)

SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
0	0	0	PY[18]	NY[18]
		1	(PY[18]-PY[17]) / 4 x 3 + PY[17]	(NY[18]-NY[17]) / 4 x 3 + NY[17]
		2	(PY[18]-PY[17]) / 4 x 2 + PY[17]	(NY[18]-NY[17]) / 4 x 2 + NY[17]
		3	(PY[18]-PY[17]) / 4 x 1 + PY[17]	(NY[18]-NY[17]) / 4 x 1 + NY[17]
1	1	4	PY[17]	NY[17]
		5	(PY[17]-PY[16]) / 4 x 3 + PY[16]	(NY[17]-NY[16]) / 4 x 3 + NY[16]
		6	(PY[17]-PY[16]) / 4 x 2 + PY[16]	(NY[17]-NY[16]) / 4 x 2 + NY[16]
		7	(PY[17]-PY[16]) / 4 x 1 + PY[16]	(NY[17]-NY[16]) / 4 x 1 + NY[16]
2	2	8	PY[16]	NY[16]
		9	(PY[16]-PY[15]) / 4 x 3 + PY[15]	(NY[16]-NY[15]) / 4 x 3 + NY[15]
		10	(PY[16]-PY[15]) / 4 x 2 + PY[15]	(NY[16]-NY[15]) / 4 x 2 + NY[15]
		11	(PY[16]-PY[15]) / 4 x 1 + PY[15]	(NY[16]-NY[15]) / 4 x 1 + NY[15]
3	3	12	PY[15]	NY[15]
		13	(PY[15]-PY[14]) / 4 x 3 + PY[14]	(NY[15]-NY[14]) / 4 x 3 + NY[14]
		14	(PY[15]-PY[14]) / 4 x 2 + PY[14]	(NY[15]-NY[14]) / 4 x 2 + NY[14]
		15	(PY[15]-PY[14]) / 4 x 1 + PY[14]	(NY[15]-NY[14]) / 4 x 1 + NY[14]
4	4	16	PY[14]	NY[14]
		17	(PY[14]-PY[13]) / 16 x 15 + PY[13]	(NY[14]-NY[13]) / 16 x 15 + NY[13]
		18	(PY[14]-PY[13]) / 16 x 14 + PY[13]	(NY[14]-NY[13]) / 16 x 14 + NY[13]
		19	(PY[14]-PY[13]) / 16 x 13 + PY[13]	(NY[14]-NY[13]) / 16 x 13 + NY[13]
5	5	20	(PY[14]-PY[13]) / 16 x 12 + PY[13]	(NY[14]-NY[13]) / 16 x 12 + NY[13]
		21	(PY[14]-PY[13]) / 16 x 11 + PY[13]	(NY[14]-NY[13]) / 16 x 11 + NY[13]
		22	(PY[14]-PY[13]) / 16 x 10 + PY[13]	(NY[14]-NY[13]) / 16 x 10 + NY[13]
		23	(PY[14]-PY[13]) / 16 x 9 + PY[13]	(NY[14]-NY[13]) / 16 x 9 + NY[13]
6	6	24	(PY[14]-PY[13]) / 16 x 8 + PY[13]	(NY[14]-NY[13]) / 16 x 8 + NY[13]
		25	(PY[14]-PY[13]) / 16 x 7 + PY[13]	(NY[14]-NY[13]) / 16 x 7 + NY[13]
		26	(PY[14]-PY[13]) / 16 x 6 + PY[13]	(NY[14]-NY[13]) / 16 x 6 + NY[13]
		27	(PY[14]-PY[13]) / 16 x 5 + PY[13]	(NY[14]-NY[13]) / 16 x 5 + NY[13]
7	7	28	(PY[14]-PY[13]) / 16 x 4 + PY[13]	(NY[14]-NY[13]) / 16 x 4 + NY[13]
		29	(PY[14]-PY[13]) / 16 x 3 + PY[13]	(NY[14]-NY[13]) / 16 x 3 + NY[13]
		30	(PY[14]-PY[13]) / 16 x 2 + PY[13]	(NY[14]-NY[13]) / 16 x 2 + NY[13]
		31	(PY[14]-PY[13]) / 16 x 1 + PY[13]	(NY[14]-NY[13]) / 16 x 1 + NY[13]
8	8	32	PY[13]	NY[13]
		33	(PY[13]-PY[12]) / 16 x 15 + PY[12]	(NY[13]-NY[12]) / 16 x 15 + NY[12]
		34	(PY[13]-PY[12]) / 16 x 14 + PY[12]	(NY[13]-NY[12]) / 16 x 14 + NY[12]
		35	(PY[13]-PY[12]) / 16 x 13 + PY[12]	(NY[13]-NY[12]) / 16 x 13 + NY[12]
9	9	36	(PY[13]-PY[12]) / 16 x 12 + PY[12]	(NY[13]-NY[12]) / 16 x 12 + NY[12]
		37	(PY[13]-PY[12]) / 16 x 11 + PY[12]	(NY[13]-NY[12]) / 16 x 11 + NY[12]
		38	(PY[13]-PY[12]) / 16 x 10 + PY[12]	(NY[13]-NY[12]) / 16 x 10 + NY[12]
		39	(PY[13]-PY[12]) / 16 x 9 + PY[12]	(NY[13]-NY[12]) / 16 x 9 + NY[12]
10	10	40	(PY[13]-PY[12]) / 16 x 8 + PY[12]	(NY[13]-NY[12]) / 16 x 8 + NY[12]
		41	(PY[13]-PY[12]) / 16 x 7 + PY[12]	(NY[13]-NY[12]) / 16 x 7 + NY[12]
		42	(PY[13]-PY[12]) / 16 x 6 + PY[12]	(NY[13]-NY[12]) / 16 x 6 + NY[12]
		43	(PY[13]-PY[12]) / 16 x 5 + PY[12]	(NY[13]-NY[12]) / 16 x 5 + NY[12]
11	11	44	(PY[13]-PY[12]) / 16 x 4 + PY[12]	(NY[13]-NY[12]) / 16 x 4 + NY[12]
		45	(PY[13]-PY[12]) / 16 x 3 + PY[12]	(NY[13]-NY[12]) / 16 x 3 + NY[12]
		46	(PY[13]-PY[12]) / 16 x 2 + PY[12]	(NY[13]-NY[12]) / 16 x 2 + NY[12]
		47	(PY[13]-PY[12]) / 16 x 1 + PY[12]	(NY[13]-NY[12]) / 16 x 1 + NY[12]
12	12	48	PY[12]	NY[12]
		49	(PY[12]-PY[11]) / 17 x 16 + PY[11]	(NY[12]-NY[11]) / 17 x 16 + NY[11]
		50	(PY[12]-PY[11]) / 17 x 15 + PY[11]	(NY[12]-NY[11]) / 17 x 15 + NY[11]
		51	(PY[12]-PY[11]) / 17 x 14 + PY[11]	(NY[12]-NY[11]) / 17 x 14 + NY[11]
13	13	52	(PY[12]-PY[11]) / 17 x 13 + PY[11]	(NY[12]-NY[11]) / 17 x 13 + NY[11]
		53	(PY[12]-PY[11]) / 17 x 12 + PY[11]	(NY[12]-NY[11]) / 17 x 12 + NY[11]
		54	(PY[12]-PY[11]) / 17 x 11 + PY[11]	(NY[12]-NY[11]) / 17 x 11 + NY[11]
		55	(PY[12]-PY[11]) / 17 x 10 + PY[11]	(NY[12]-NY[11]) / 17 x 10 + NY[11]
14	14	56	(PY[12]-PY[11]) / 17 x 9 + PY[11]	(NY[12]-NY[11]) / 17 x 9 + NY[11]
		57	(PY[12]-PY[11]) / 17 x 8 + PY[11]	(NY[12]-NY[11]) / 17 x 8 + NY[11]
		58	(PY[12]-PY[11]) / 17 x 7 + PY[11]	(NY[12]-NY[11]) / 17 x 7 + NY[11]
		59	(PY[12]-PY[11]) / 17 x 6 + PY[11]	(NY[12]-NY[11]) / 17 x 6 + NY[11]
15	15	60	(PY[12]-PY[11]) / 17 x 5 + PY[11]	(NY[12]-NY[11]) / 17 x 5 + NY[11]
		61	(PY[12]-PY[11]) / 17 x 4 + PY[11]	(NY[12]-NY[11]) / 17 x 4 + NY[11]
		62	(PY[12]-PY[11]) / 17 x 3 + PY[11]	(NY[12]-NY[11]) / 17 x 3 + NY[11]
		63	(PY[12]-PY[11]) / 17 x 2 + PY[11]	(NY[12]-NY[11]) / 17 x 2 + NY[11]

SD mode6 bit gray code	TCON mode6 bit gray code	TCON/SD8 bit gray code	Positive Gamma voltage		Negative Gamma voltage
16		64	(PY[12]-PY[11]) / 17 x 1 + PY[11]		(NY[12]-NY[11]) / 17 x 1 + NY[11]
	16	65	PY[11]		NY[11]
		66	(PY[11]-PY[10]) / 32 x 31 + PY[10]		(NY[11]-NY[10]) / 32 x 31 + NY[10]
		67	(PY[11]-PY[10]) / 32 x 30 + PY[10]		(NY[11]-NY[10]) / 32 x 30 + NY[10]
17		68	(PY[11]-PY[10]) / 32 x 29 + PY[10]		(NY[11]-NY[10]) / 32 x 29 + NY[10]
	17	69	(PY[11]-PY[10]) / 32 x 28 + PY[10]		(NY[11]-NY[10]) / 32 x 28 + NY[10]
		70	(PY[11]-PY[10]) / 32 x 27 + PY[10]		(NY[11]-NY[10]) / 32 x 27 + NY[10]
		71	(PY[11]-PY[10]) / 32 x 26 + PY[10]		(NY[11]-NY[10]) / 32 x 26 + NY[10]
18		72	(PY[11]-PY[10]) / 32 x 25 + PY[10]		(NY[11]-NY[10]) / 32 x 25 + NY[10]
	18	73	(PY[11]-PY[10]) / 32 x 24 + PY[10]		(NY[11]-NY[10]) / 32 x 24 + NY[10]
		74	(PY[11]-PY[10]) / 32 x 23 + PY[10]		(NY[11]-NY[10]) / 32 x 23 + NY[10]
		75	(PY[11]-PY[10]) / 32 x 22 + PY[10]		(NY[11]-NY[10]) / 32 x 22 + NY[10]
19		76	(PY[11]-PY[10]) / 32 x 21 + PY[10]		(NY[11]-NY[10]) / 32 x 21 + NY[10]
	19	77	(PY[11]-PY[10]) / 32 x 20 + PY[10]		(NY[11]-NY[10]) / 32 x 20 + NY[10]
		78	(PY[11]-PY[10]) / 32 x 19 + PY[10]		(NY[11]-NY[10]) / 32 x 19 + NY[10]
		79	(PY[11]-PY[10]) / 32 x 18 + PY[10]		(NY[11]-NY[10]) / 32 x 18 + NY[10]
20		80	(PY[11]-PY[10]) / 32 x 17 + PY[10]		(NY[11]-NY[10]) / 32 x 17 + NY[10]
	20	81	(PY[11]-PY[10]) / 32 x 16 + PY[10]		(NY[11]-NY[10]) / 32 x 16 + NY[10]
		82	(PY[11]-PY[10]) / 32 x 15 + PY[10]		(NY[11]-NY[10]) / 32 x 15 + NY[10]
		83	(PY[11]-PY[10]) / 32 x 14 + PY[10]		(NY[11]-NY[10]) / 32 x 14 + NY[10]
21		84	(PY[11]-PY[10]) / 32 x 13 + PY[10]		(NY[11]-NY[10]) / 32 x 13 + NY[10]
	21	85	(PY[11]-PY[10]) / 32 x 12 + PY[10]		(NY[11]-NY[10]) / 32 x 12 + NY[10]
		86	(PY[11]-PY[10]) / 32 x 11 + PY[10]		(NY[11]-NY[10]) / 32 x 11 + NY[10]
		87	(PY[11]-PY[10]) / 32 x 10 + PY[10]		(NY[11]-NY[10]) / 32 x 10 + NY[10]
22		88	(PY[11]-PY[10]) / 32 x 9 + PY[10]		(NY[11]-NY[10]) / 32 x 9 + NY[10]
	22	89	(PY[11]-PY[10]) / 32 x 8 + PY[10]		(NY[11]-NY[10]) / 32 x 8 + NY[10]
		90	(PY[11]-PY[10]) / 32 x 7 + PY[10]		(NY[11]-NY[10]) / 32 x 7 + NY[10]
		91	(PY[11]-PY[10]) / 32 x 6 + PY[10]		(NY[11]-NY[10]) / 32 x 6 + NY[10]
23		92	(PY[11]-PY[10]) / 32 x 5 + PY[10]		(NY[11]-NY[10]) / 32 x 5 + NY[10]
	23	93	(PY[11]-PY[10]) / 32 x 4 + PY[10]		(NY[11]-NY[10]) / 32 x 4 + NY[10]
		94	(PY[11]-PY[10]) / 32 x 3 + PY[10]		(NY[11]-NY[10]) / 32 x 3 + NY[10]
		95	(PY[11]-PY[10]) / 32 x 2 + PY[10]		(NY[11]-NY[10]) / 32 x 2 + NY[10]
24		96	(PY[11]-PY[10]) / 32 x 1 + PY[10]		(NY[11]-NY[10]) / 32 x 1 + NY[10]
	24	97	PY[10]		NY[10]
		98	(PY[10]-PY[9]) / 33 x 32 + PY[9]		(NY[10]-NY[9]) / 33 x 32 + NY[9]
		99	(PY[10]-PY[9]) / 33 x 31 + PY[9]		(NY[10]-NY[9]) / 33 x 31 + NY[9]
25		100	(PY[10]-PY[9]) / 33 x 30 + PY[9]		(NY[10]-NY[9]) / 33 x 30 + NY[9]
	25	101	(PY[10]-PY[9]) / 33 x 29 + PY[9]		(NY[10]-NY[9]) / 33 x 29 + NY[9]
		102	(PY[10]-PY[9]) / 33 x 28 + PY[9]		(NY[10]-NY[9]) / 33 x 28 + NY[9]
		103	(PY[10]-PY[9]) / 33 x 27 + PY[9]		(NY[10]-NY[9]) / 33 x 27 + NY[9]
26		104	(PY[10]-PY[9]) / 33 x 26 + PY[9]		(NY[10]-NY[9]) / 33 x 26 + NY[9]
	26	105	(PY[10]-PY[9]) / 33 x 25 + PY[9]		(NY[10]-NY[9]) / 33 x 25 + NY[9]
		106	(PY[10]-PY[9]) / 33 x 24 + PY[9]		(NY[10]-NY[9]) / 33 x 24 + NY[9]
		107	(PY[10]-PY[9]) / 33 x 23 + PY[9]		(NY[10]-NY[9]) / 33 x 23 + NY[9]
27		108	(PY[10]-PY[9]) / 33 x 22 + PY[9]		(NY[10]-NY[9]) / 33 x 22 + NY[9]
	27	109	(PY[10]-PY[9]) / 33 x 21 + PY[9]		(NY[10]-NY[9]) / 33 x 21 + NY[9]
		110	(PY[10]-PY[9]) / 33 x 20 + PY[9]		(NY[10]-NY[9]) / 33 x 20 + NY[9]
		111	(PY[10]-PY[9]) / 33 x 19 + PY[9]		(NY[10]-NY[9]) / 33 x 19 + NY[9]
28		112	(PY[10]-PY[9]) / 33 x 18 + PY[9]		(NY[10]-NY[9]) / 33 x 18 + NY[9]
	28	113	(PY[10]-PY[9]) / 33 x 17 + PY[9]		(NY[10]-NY[9]) / 33 x 17 + NY[9]
		114	(PY[10]-PY[9]) / 33 x 16 + PY[9]		(NY[10]-NY[9]) / 33 x 16 + NY[9]
		115	(PY[10]-PY[9]) / 33 x 15 + PY[9]		(NY[10]-NY[9]) / 33 x 15 + NY[9]
29		116	(PY[10]-PY[9]) / 33 x 14 + PY[9]		(NY[10]-NY[9]) / 33 x 14 + NY[9]
	29	117	(PY[10]-PY[9]) / 33 x 13 + PY[9]		(NY[10]-NY[9]) / 33 x 13 + NY[9]
		118	(PY[10]-PY[9]) / 33 x 12 + PY[9]		(NY[10]-NY[9]) / 33 x 12 + NY[9]
		119	(PY[10]-PY[9]) / 33 x 11 + PY[9]		(NY[10]-NY[9]) / 33 x 11 + NY[9]
30		120	(PY[10]-PY[9]) / 33 x 10 + PY[9]		(NY[10]-NY[9]) / 33 x 10 + NY[9]
	30	121	(PY[10]-PY[9]) / 33 x 9 + PY[9]		(NY[10]-NY[9]) / 33 x 9 + NY[9]
		122	(PY[10]-PY[9]) / 33 x 8 + PY[9]		(NY[10]-NY[9]) / 33 x 8 + NY[9]
		123	(PY[10]-PY[9]) / 33 x 7 + PY[9]		(NY[10]-NY[9]) / 33 x 7 + NY[9]
31		124	(PY[10]-PY[9]) / 33 x 6 + PY[9]		(NY[10]-NY[9]) / 33 x 6 + NY[9]
	31	125	(PY[10]-PY[9]) / 33 x 5 + PY[9]		(NY[10]-NY[9]) / 33 x 5 + NY[9]
		126	(PY[10]-PY[9]) / 33 x 4 + PY[9]		(NY[10]-NY[9]) / 33 x 4 + NY[9]
		127	(PY[10]-PY[9]) / 33 x 3 + PY[9]		(NY[10]-NY[9]) / 33 x 3 + NY[9]

SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
32		128	(PY[10]-PY[9]) / 33 x 2 + PY[9]	(NY[10]-NY[9]) / 33 x 2 + NY[9]
		129	(PY[10]-PY[9]) / 33 x 1 + PY[9]	(NY[10]-NY[9]) / 33 x 1 + NY[9]
	32	130	PY[9]	NY[9]
		131	(PY[9]-PY[8]) / 32 x 31 + PY[8]	(NY[9]-NY[8]) / 32 x 31 + NY[8]
33		132	(PY[9]-PY[8]) / 32 x 30 + PY[8]	(NY[9]-NY[8]) / 32 x 30 + NY[8]
		133	(PY[9]-PY[8]) / 32 x 29 + PY[8]	(NY[9]-NY[8]) / 32 x 29 + NY[8]
	33	134	(PY[9]-PY[8]) / 32 x 28 + PY[8]	(NY[9]-NY[8]) / 32 x 28 + NY[8]
		135	(PY[9]-PY[8]) / 32 x 27 + PY[8]	(NY[9]-NY[8]) / 32 x 27 + NY[8]
34		136	(PY[9]-PY[8]) / 32 x 26 + PY[8]	(NY[9]-NY[8]) / 32 x 26 + NY[8]
		137	(PY[9]-PY[8]) / 32 x 25 + PY[8]	(NY[9]-NY[8]) / 32 x 25 + NY[8]
	34	138	(PY[9]-PY[8]) / 32 x 24 + PY[8]	(NY[9]-NY[8]) / 32 x 24 + NY[8]
		139	(PY[9]-PY[8]) / 32 x 23 + PY[8]	(NY[9]-NY[8]) / 32 x 23 + NY[8]
35		140	(PY[9]-PY[8]) / 32 x 22 + PY[8]	(NY[9]-NY[8]) / 32 x 22 + NY[8]
		141	(PY[9]-PY[8]) / 32 x 21 + PY[8]	(NY[9]-NY[8]) / 32 x 21 + NY[8]
	35	142	(PY[9]-PY[8]) / 32 x 20 + PY[8]	(NY[9]-NY[8]) / 32 x 20 + NY[8]
		143	(PY[9]-PY[8]) / 32 x 19 + PY[8]	(NY[9]-NY[8]) / 32 x 19 + NY[8]
36		144	(PY[9]-PY[8]) / 32 x 18 + PY[8]	(NY[9]-NY[8]) / 32 x 18 + NY[8]
		145	(PY[9]-PY[8]) / 32 x 17 + PY[8]	(NY[9]-NY[8]) / 32 x 17 + NY[8]
	36	146	(PY[9]-PY[8]) / 32 x 16 + PY[8]	(NY[9]-NY[8]) / 32 x 16 + NY[8]
		147	(PY[9]-PY[8]) / 32 x 15 + PY[8]	(NY[9]-NY[8]) / 32 x 15 + NY[8]
37		148	(PY[9]-PY[8]) / 32 x 14 + PY[8]	(NY[9]-NY[8]) / 32 x 14 + NY[8]
		149	(PY[9]-PY[8]) / 32 x 13 + PY[8]	(NY[9]-NY[8]) / 32 x 13 + NY[8]
	37	150	(PY[9]-PY[8]) / 32 x 12 + PY[8]	(NY[9]-NY[8]) / 32 x 12 + NY[8]
		151	(PY[9]-PY[8]) / 32 x 11 + PY[8]	(NY[9]-NY[8]) / 32 x 11 + NY[8]
38		152	(PY[9]-PY[8]) / 32 x 10 + PY[8]	(NY[9]-NY[8]) / 32 x 10 + NY[8]
		153	(PY[9]-PY[8]) / 32 x 9 + PY[8]	(NY[9]-NY[8]) / 32 x 9 + NY[8]
	38	154	(PY[9]-PY[8]) / 32 x 8 + PY[8]	(NY[9]-NY[8]) / 32 x 8 + NY[8]
		155	(PY[9]-PY[8]) / 32 x 7 + PY[8]	(NY[9]-NY[8]) / 32 x 7 + NY[8]
39		156	(PY[9]-PY[8]) / 32 x 6 + PY[8]	(NY[9]-NY[8]) / 32 x 6 + NY[8]
		157	(PY[9]-PY[8]) / 32 x 5 + PY[8]	(NY[9]-NY[8]) / 32 x 5 + NY[8]
	39	158	(PY[9]-PY[8]) / 32 x 4 + PY[8]	(NY[9]-NY[8]) / 32 x 4 + NY[8]
		159	(PY[9]-PY[8]) / 32 x 3 + PY[8]	(NY[9]-NY[8]) / 32 x 3 + NY[8]
40		160	(PY[9]-PY[8]) / 32 x 2 + PY[8]	(NY[9]-NY[8]) / 32 x 2 + NY[8]
		161	(PY[9]-PY[8]) / 32 x 1 + PY[8]	(NY[9]-NY[8]) / 32 x 1 + NY[8]
	40	162	PY[8]	NY[8]
		163	(PY[8]-PY[7]) / 33 x 32 + PY[7]	(NY[8]-NY[7]) / 33 x 32 + NY[7]
41		164	(PY[8]-PY[7]) / 33 x 31 + PY[7]	(NY[8]-NY[7]) / 33 x 31 + NY[7]
		165	(PY[8]-PY[7]) / 33 x 30 + PY[7]	(NY[8]-NY[7]) / 33 x 30 + NY[7]
	41	166	(PY[8]-PY[7]) / 33 x 29 + PY[7]	(NY[8]-NY[7]) / 33 x 29 + NY[7]
		167	(PY[8]-PY[7]) / 33 x 28 + PY[7]	(NY[8]-NY[7]) / 33 x 28 + NY[7]
42		168	(PY[8]-PY[7]) / 33 x 27 + PY[7]	(NY[8]-NY[7]) / 33 x 27 + NY[7]
		169	(PY[8]-PY[7]) / 33 x 26 + PY[7]	(NY[8]-NY[7]) / 33 x 26 + NY[7]
	42	170	(PY[8]-PY[7]) / 33 x 25 + PY[7]	(NY[8]-NY[7]) / 33 x 25 + NY[7]
		171	(PY[8]-PY[7]) / 33 x 24 + PY[7]	(NY[8]-NY[7]) / 33 x 24 + NY[7]
43		172	(PY[8]-PY[7]) / 33 x 23 + PY[7]	(NY[8]-NY[7]) / 33 x 23 + NY[7]
		173	(PY[8]-PY[7]) / 33 x 22 + PY[7]	(NY[8]-NY[7]) / 33 x 22 + NY[7]
	43	174	(PY[8]-PY[7]) / 33 x 21 + PY[7]	(NY[8]-NY[7]) / 33 x 21 + NY[7]
		175	(PY[8]-PY[7]) / 33 x 20 + PY[7]	(NY[8]-NY[7]) / 33 x 20 + NY[7]
44		176	(PY[8]-PY[7]) / 33 x 19 + PY[7]	(NY[8]-NY[7]) / 33 x 19 + NY[7]
		177	(PY[8]-PY[7]) / 33 x 18 + PY[7]	(NY[8]-NY[7]) / 33 x 18 + NY[7]
	44	178	(PY[8]-PY[7]) / 33 x 17 + PY[7]	(NY[8]-NY[7]) / 33 x 17 + NY[7]
		179	(PY[8]-PY[7]) / 33 x 16 + PY[7]	(NY[8]-NY[7]) / 33 x 16 + NY[7]
45		180	(PY[8]-PY[7]) / 33 x 15 + PY[7]	(NY[8]-NY[7]) / 33 x 15 + NY[7]
		181	(PY[8]-PY[7]) / 33 x 14 + PY[7]	(NY[8]-NY[7]) / 33 x 14 + NY[7]
	45	182	(PY[8]-PY[7]) / 33 x 13 + PY[7]	(NY[8]-NY[7]) / 33 x 13 + NY[7]
		183	(PY[8]-PY[7]) / 33 x 12 + PY[7]	(NY[8]-NY[7]) / 33 x 12 + NY[7]
46		184	(PY[8]-PY[7]) / 33 x 11 + PY[7]	(NY[8]-NY[7]) / 33 x 11 + NY[7]
		185	(PY[8]-PY[7]) / 33 x 10 + PY[7]	(NY[8]-NY[7]) / 33 x 10 + NY[7]
	46	186	(PY[8]-PY[7]) / 33 x 9 + PY[7]	(NY[8]-NY[7]) / 33 x 9 + NY[7]
		187	(PY[8]-PY[7]) / 33 x 8 + PY[7]	(NY[8]-NY[7]) / 33 x 8 + NY[7]
47		188	(PY[8]-PY[7]) / 33 x 7 + PY[7]	(NY[8]-NY[7]) / 33 x 7 + NY[7]
		189	(PY[8]-PY[7]) / 33 x 6 + PY[7]	(NY[8]-NY[7]) / 33 x 6 + NY[7]
	47	190	(PY[8]-PY[7]) / 33 x 5 + PY[7]	(NY[8]-NY[7]) / 33 x 5 + NY[7]
		191	(PY[8]-PY[7]) / 33 x 4 + PY[7]	(NY[8]-NY[7]) / 33 x 4 + NY[7]

SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
48		192	(PY[8]-PY[7]) / 33 x 3 + PY[7]	(NY[8]-NY[7]) / 33 x 3 + NY[7]
		193	(PY[8]-PY[7]) / 33 x 2 + PY[7]	(NY[8]-NY[7]) / 33 x 2 + NY[7]
		194	(PY[8]-PY[7]) / 33 x 1 + PY[7]	(NY[8]-NY[7]) / 33 x 1 + NY[7]
	48	195	PY[7]	NY[7]
49		196	(PY[7]-PY[6]) / 20 x 19 + PY[6]	(NY[7]-NY[6]) / 20 x 19 + NY[6]
		197	(PY[7]-PY[6]) / 20 x 18 + PY[6]	(NY[7]-NY[6]) / 20 x 18 + NY[6]
		198	(PY[7]-PY[6]) / 20 x 17 + PY[6]	(NY[7]-NY[6]) / 20 x 17 + NY[6]
	49	199	(PY[7]-PY[6]) / 20 x 16 + PY[6]	(NY[7]-NY[6]) / 20 x 16 + NY[6]
50		200	(PY[7]-PY[6]) / 20 x 15 + PY[6]	(NY[7]-NY[6]) / 20 x 15 + NY[6]
		201	(PY[7]-PY[6]) / 20 x 14 + PY[6]	(NY[7]-NY[6]) / 20 x 14 + NY[6]
		202	(PY[7]-PY[6]) / 20 x 13 + PY[6]	(NY[7]-NY[6]) / 20 x 13 + NY[6]
	50	203	(PY[7]-PY[6]) / 20 x 12 + PY[6]	(NY[7]-NY[6]) / 20 x 12 + NY[6]
51		204	(PY[7]-PY[6]) / 20 x 11 + PY[6]	(NY[7]-NY[6]) / 20 x 11 + NY[6]
		205	(PY[7]-PY[6]) / 20 x 10 + PY[6]	(NY[7]-NY[6]) / 20 x 10 + NY[6]
		206	(PY[7]-PY[6]) / 20 x 9 + PY[6]	(NY[7]-NY[6]) / 20 x 9 + NY[6]
	51	207	(PY[7]-PY[6]) / 20 x 8 + PY[6]	(NY[7]-NY[6]) / 20 x 8 + NY[6]
52		208	(PY[7]-PY[6]) / 20 x 7 + PY[6]	(NY[7]-NY[6]) / 20 x 7 + NY[6]
		209	(PY[7]-PY[6]) / 20 x 6 + PY[6]	(NY[7]-NY[6]) / 20 x 6 + NY[6]
		210	(PY[7]-PY[6]) / 20 x 5 + PY[6]	(NY[7]-NY[6]) / 20 x 5 + NY[6]
	52	211	(PY[7]-PY[6]) / 20 x 4 + PY[6]	(NY[7]-NY[6]) / 20 x 4 + NY[6]
53		212	(PY[7]-PY[6]) / 20 x 3 + PY[6]	(NY[7]-NY[6]) / 20 x 3 + NY[6]
		213	(PY[7]-PY[6]) / 20 x 2 + PY[6]	(NY[7]-NY[6]) / 20 x 2 + NY[6]
		214	(PY[7]-PY[6]) / 20 x 1 + PY[6]	(NY[7]-NY[6]) / 20 x 1 + NY[6]
	53	215	PY[6]	NY[6]
54		216	(PY[6]-PY[5]) / 8 x 7 + PY[5]	(NY[6]-NY[5]) / 8 x 7 + NY[5]
		217	(PY[6]-PY[5]) / 8 x 6 + PY[5]	(NY[6]-NY[5]) / 8 x 6 + NY[5]
		218	(PY[6]-PY[5]) / 8 x 5 + PY[5]	(NY[6]-NY[5]) / 8 x 5 + NY[5]
	54	219	(PY[6]-PY[5]) / 8 x 4 + PY[5]	(NY[6]-NY[5]) / 8 x 4 + NY[5]
55		220	(PY[6]-PY[5]) / 8 x 3 + PY[5]	(NY[6]-NY[5]) / 8 x 3 + NY[5]
		221	(PY[6]-PY[5]) / 8 x 2 + PY[5]	(NY[6]-NY[5]) / 8 x 2 + NY[5]
		222	(PY[6]-PY[5]) / 8 x 1 + PY[5]	(NY[6]-NY[5]) / 8 x 1 + NY[5]
	55	223	PY[5]	NY[5]
56		224	(PY[5]-PY[4]) / 8 x 7 + PY[4]	(NY[5]-NY[4]) / 8 x 7 + NY[4]
		225	(PY[5]-PY[4]) / 8 x 6 + PY[4]	(NY[5]-NY[4]) / 8 x 6 + NY[4]
		226	(PY[5]-PY[4]) / 8 x 5 + PY[4]	(NY[5]-NY[4]) / 8 x 5 + NY[4]
	56	227	(PY[5]-PY[4]) / 8 x 4 + PY[4]	(NY[5]-NY[4]) / 8 x 4 + NY[4]
57		228	(PY[5]-PY[4]) / 8 x 3 + PY[4]	(NY[5]-NY[4]) / 8 x 3 + NY[4]
		229	(PY[5]-PY[4]) / 8 x 2 + PY[4]	(NY[5]-NY[4]) / 8 x 2 + NY[4]
		230	(PY[5]-PY[4]) / 8 x 1 + PY[4]	(NY[5]-NY[4]) / 8 x 1 + NY[4]
	57	231	PY[4]	NY[4]
58		232	(PY[4]-PY[3]) / 8 x 7 + PY[3]	(NY[4]-NY[3]) / 8 x 7 + NY[3]
		233	(PY[4]-PY[3]) / 8 x 6 + PY[3]	(NY[4]-NY[3]) / 8 x 6 + NY[3]
		234	(PY[4]-PY[3]) / 8 x 5 + PY[3]	(NY[4]-NY[3]) / 8 x 5 + NY[3]
	58	235	(PY[4]-PY[3]) / 8 x 4 + PY[3]	(NY[4]-NY[3]) / 8 x 4 + NY[3]
59		236	(PY[4]-PY[3]) / 8 x 3 + PY[3]	(NY[4]-NY[3]) / 8 x 3 + NY[3]
		237	(PY[4]-PY[3]) / 8 x 2 + PY[3]	(NY[4]-NY[3]) / 8 x 2 + NY[3]
		238	(PY[4]-PY[3]) / 8 x 1 + PY[3]	(NY[4]-NY[3]) / 8 x 1 + NY[3]
	59	239	PY[3]	NY[3]
60		240	(PY[3]-PY[2]) / 8 x 7 + PY[2]	(NY[3]-NY[2]) / 8 x 7 + NY[2]
		241	(PY[3]-PY[2]) / 8 x 6 + PY[2]	(NY[3]-NY[2]) / 8 x 6 + NY[2]
		242	(PY[3]-PY[2]) / 8 x 5 + PY[2]	(NY[3]-NY[2]) / 8 x 5 + NY[2]
	60	243	(PY[3]-PY[2]) / 8 x 4 + PY[2]	(NY[3]-NY[2]) / 8 x 4 + NY[2]
61		244	(PY[3]-PY[2]) / 8 x 3 + PY[2]	(NY[3]-NY[2]) / 8 x 3 + NY[2]
		245	(PY[3]-PY[2]) / 8 x 2 + PY[2]	(NY[3]-NY[2]) / 8 x 2 + NY[2]
		246	(PY[3]-PY[2]) / 8 x 1 + PY[2]	(NY[3]-NY[2]) / 8 x 1 + NY[2]
	61	247	PY[2]	NY[2]
62		248	(PY[2]-PY[1]) / 4 x 3 + PY[1]	(NY[2]-NY[1]) / 4 x 3 + NY[1]
		249	(PY[2]-PY[1]) / 4 x 2 + PY[1]	(NY[2]-NY[1]) / 4 x 2 + NY[1]
		250	(PY[2]-PY[1]) / 4 x 1 + PY[1]	(NY[2]-NY[1]) / 4 x 1 + NY[1]
	62	251	PY[1]	NY[1]
63		252	(PY[1]-PY[0]) / 4 x 3 + PY[0]	(NY[1]-NY[0]) / 4 x 3 + NY[0]
		253	(PY[1]-PY[0]) / 4 x 2 + PY[0]	(NY[1]-NY[0]) / 4 x 2 + NY[0]
		254	(PY[1]-PY[0]) / 4 x 1 + PY[0]	(NY[1]-NY[0]) / 4 x 1 + NY[0]
	63	255	PY[0]	NY[0]

Gamma gray code voltage calculation formula table (normally black)

SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage				Negative Gamma voltage			
0	0	0	PY[0]				NY[0]			
		1	(PY[0]-PY[1])	/ 4 x	3	+ PY[1]	(NY[0]-NY[1])	/ 4 x	3	+ NY[1]
		2	(PY[0]-PY[1])	/ 4 x	2	+ PY[1]	(NY[0]-NY[1])	/ 4 x	2	+ NY[1]
		3	(PY[0]-PY[1])	/ 4 x	1	+ PY[1]	(NY[0]-NY[1])	/ 4 x	1	+ NY[1]
1	1	4	PY[1]				NY[1]			
		5	(PY[1]-PY[2])	/ 4 x	3	+ PY[2]	(NY[1]-NY[2])	/ 4 x	3	+ NY[2]
		6	(PY[1]-PY[2])	/ 4 x	2	+ PY[2]	(NY[1]-NY[2])	/ 4 x	2	+ NY[2]
		7	(PY[1]-PY[2])	/ 4 x	1	+ PY[2]	(NY[1]-NY[2])	/ 4 x	1	+ NY[2]
2	2	8	PY[2]				NY[2]			
		9	(PY[2]-PY[3])	/ 8 x	7	+ PY[3]	(NY[2]-NY[3])	/ 8 x	7	+ NY[3]
		10	(PY[2]-PY[3])	/ 8 x	6	+ PY[3]	(NY[2]-NY[3])	/ 8 x	6	+ NY[3]
		11	(PY[2]-PY[3])	/ 8 x	5	+ PY[3]	(NY[2]-NY[3])	/ 8 x	5	+ NY[3]
3	3	12	(PY[2]-PY[3])	/ 8 x	4	+ PY[3]	(NY[2]-NY[3])	/ 8 x	4	+ NY[3]
		13	(PY[2]-PY[3])	/ 8 x	3	+ PY[3]	(NY[2]-NY[3])	/ 8 x	3	+ NY[3]
		14	(PY[2]-PY[3])	/ 8 x	2	+ PY[3]	(NY[2]-NY[3])	/ 8 x	2	+ NY[3]
		15	(PY[2]-PY[3])	/ 8 x	1	+ PY[3]	(NY[2]-NY[3])	/ 8 x	1	+ NY[3]
4	4	16	PY[3]				NY[3]			
		17	(PY[3]-PY[4])	/ 8 x	7	+ PY[4]	(NY[3]-NY[4])	/ 8 x	7	+ NY[4]
		18	(PY[3]-PY[4])	/ 8 x	6	+ PY[4]	(NY[3]-NY[4])	/ 8 x	6	+ NY[4]
		19	(PY[3]-PY[4])	/ 8 x	5	+ PY[4]	(NY[3]-NY[4])	/ 8 x	5	+ NY[4]
5	5	20	(PY[3]-PY[4])	/ 8 x	4	+ PY[4]	(NY[3]-NY[4])	/ 8 x	4	+ NY[4]
		21	(PY[3]-PY[4])	/ 8 x	3	+ PY[4]	(NY[3]-NY[4])	/ 8 x	3	+ NY[4]
		22	(PY[3]-PY[4])	/ 8 x	2	+ PY[4]	(NY[3]-NY[4])	/ 8 x	2	+ NY[4]
		23	(PY[3]-PY[4])	/ 8 x	1	+ PY[4]	(NY[3]-NY[4])	/ 8 x	1	+ NY[4]
6	6	24	PY[4]				NY[4]			
		25	(PY[4]-PY[5])	/ 8 x	7	+ PY[5]	(NY[4]-NY[5])	/ 8 x	7	+ NY[5]
		26	(PY[4]-PY[5])	/ 8 x	6	+ PY[5]	(NY[4]-NY[5])	/ 8 x	6	+ NY[5]
		27	(PY[4]-PY[5])	/ 8 x	5	+ PY[5]	(NY[4]-NY[5])	/ 8 x	5	+ NY[5]
7	7	28	(PY[4]-PY[5])	/ 8 x	4	+ PY[5]	(NY[4]-NY[5])	/ 8 x	4	+ NY[5]
		29	(PY[4]-PY[5])	/ 8 x	3	+ PY[5]	(NY[4]-NY[5])	/ 8 x	3	+ NY[5]
		30	(PY[4]-PY[5])	/ 8 x	2	+ PY[5]	(NY[4]-NY[5])	/ 8 x	2	+ NY[5]
		31	(PY[4]-PY[5])	/ 8 x	1	+ PY[5]	(NY[4]-NY[5])	/ 8 x	1	+ NY[5]
8	8	32	PY[5]				NY[5]			
		33	(PY[5]-PY[6])	/ 8 x	7	+ PY[6]	(NY[5]-NY[6])	/ 8 x	7	+ NY[6]
		34	(PY[5]-PY[6])	/ 8 x	6	+ PY[6]	(NY[5]-NY[6])	/ 8 x	6	+ NY[6]
		35	(PY[5]-PY[6])	/ 8 x	5	+ PY[6]	(NY[5]-NY[6])	/ 8 x	5	+ NY[6]
9	9	36	(PY[5]-PY[6])	/ 8 x	4	+ PY[6]	(NY[5]-NY[6])	/ 8 x	4	+ NY[6]
		37	(PY[5]-PY[6])	/ 8 x	3	+ PY[6]	(NY[5]-NY[6])	/ 8 x	3	+ NY[6]
		38	(PY[5]-PY[6])	/ 8 x	2	+ PY[6]	(NY[5]-NY[6])	/ 8 x	2	+ NY[6]
		39	(PY[5]-PY[6])	/ 8 x	1	+ PY[6]	(NY[5]-NY[6])	/ 8 x	1	+ NY[6]
10	10	40	PY[6]				NY[6]			
		41	(PY[6]-PY[7])	/ 20 x	19	+ PY[7]	(NY[6]-NY[7])	/ 20 x	19	+ NY[7]
		42	(PY[6]-PY[7])	/ 20 x	18	+ PY[7]	(NY[6]-NY[7])	/ 20 x	18	+ NY[7]
		43	(PY[6]-PY[7])	/ 20 x	17	+ PY[7]	(NY[6]-NY[7])	/ 20 x	17	+ NY[7]
11	11	44	(PY[6]-PY[7])	/ 20 x	16	+ PY[7]	(NY[6]-NY[7])	/ 20 x	16	+ NY[7]
		45	(PY[6]-PY[7])	/ 20 x	15	+ PY[7]	(NY[6]-NY[7])	/ 20 x	15	+ NY[7]
		46	(PY[6]-PY[7])	/ 20 x	14	+ PY[7]	(NY[6]-NY[7])	/ 20 x	14	+ NY[7]
		47	(PY[6]-PY[7])	/ 20 x	13	+ PY[7]	(NY[6]-NY[7])	/ 20 x	13	+ NY[7]
12	12	48	(PY[6]-PY[7])	/ 20 x	12	+ PY[7]	(NY[6]-NY[7])	/ 20 x	12	+ NY[7]
		49	(PY[6]-PY[7])	/ 20 x	11	+ PY[7]	(NY[6]-NY[7])	/ 20 x	11	+ NY[7]
		50	(PY[6]-PY[7])	/ 20 x	10	+ PY[7]	(NY[6]-NY[7])	/ 20 x	10	+ NY[7]
		51	(PY[6]-PY[7])	/ 20 x	9	+ PY[7]	(NY[6]-NY[7])	/ 20 x	9	+ NY[7]
13	13	52	(PY[6]-PY[7])	/ 20 x	8	+ PY[7]	(NY[6]-NY[7])	/ 20 x	8	+ NY[7]
		53	(PY[6]-PY[7])	/ 20 x	7	+ PY[7]	(NY[6]-NY[7])	/ 20 x	7	+ NY[7]
		54	(PY[6]-PY[7])	/ 20 x	6	+ PY[7]	(NY[6]-NY[7])	/ 20 x	6	+ NY[7]
		55	(PY[6]-PY[7])	/ 20 x	5	+ PY[7]	(NY[6]-NY[7])	/ 20 x	5	+ NY[7]
14	14	56	(PY[6]-PY[7])	/ 20 x	4	+ PY[7]	(NY[6]-NY[7])	/ 20 x	4	+ NY[7]
		57	(PY[6]-PY[7])	/ 20 x	3	+ PY[7]	(NY[6]-NY[7])	/ 20 x	3	+ NY[7]
		58	(PY[6]-PY[7])	/ 20 x	2	+ PY[7]	(NY[6]-NY[7])	/ 20 x	2	+ NY[7]
		59	(PY[6]-PY[7])	/ 20 x	1	+ PY[7]	(NY[6]-NY[7])	/ 20 x	1	+ NY[7]
15	15	60	PY[7]				NY[7]			
		61	(PY[7]-PY[8])	/ 33 x	32	+ PY[8]	(NY[7]-NY[8])	/ 33 x	32	+ NY[8]
		62	(PY[7]-PY[8])	/ 33 x	31	+ PY[8]	(NY[7]-NY[8])	/ 33 x	31	+ NY[8]
		63	(PY[7]-PY[8])	/ 33 x	30	+ PY[8]	(NY[7]-NY[8])	/ 33 x	30	+ NY[8]

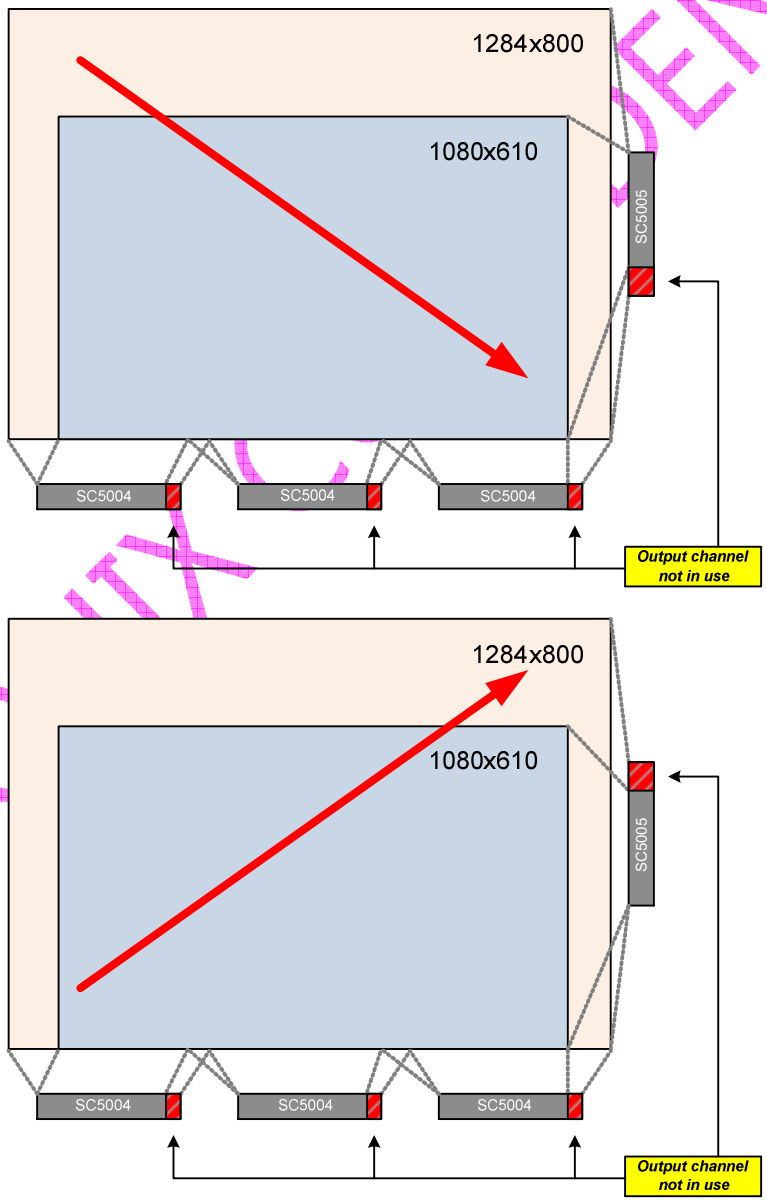
SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
16		64	(PY[7]-PY[8]) / 33 x 29 + PY[8]	(NY[7]-NY[8]) / 33 x 29 + NY[8]
	16	65	(PY[7]-PY[8]) / 33 x 28 + PY[8]	(NY[7]-NY[8]) / 33 x 28 + NY[8]
		66	(PY[7]-PY[8]) / 33 x 27 + PY[8]	(NY[7]-NY[8]) / 33 x 27 + NY[8]
		67	(PY[7]-PY[8]) / 33 x 26 + PY[8]	(NY[7]-NY[8]) / 33 x 26 + NY[8]
17		68	(PY[7]-PY[8]) / 33 x 25 + PY[8]	(NY[7]-NY[8]) / 33 x 25 + NY[8]
	17	69	(PY[7]-PY[8]) / 33 x 24 + PY[8]	(NY[7]-NY[8]) / 33 x 24 + NY[8]
		70	(PY[7]-PY[8]) / 33 x 23 + PY[8]	(NY[7]-NY[8]) / 33 x 23 + NY[8]
		71	(PY[7]-PY[8]) / 33 x 22 + PY[8]	(NY[7]-NY[8]) / 33 x 22 + NY[8]
18		72	(PY[7]-PY[8]) / 33 x 21 + PY[8]	(NY[7]-NY[8]) / 33 x 21 + NY[8]
	18	73	(PY[7]-PY[8]) / 33 x 20 + PY[8]	(NY[7]-NY[8]) / 33 x 20 + NY[8]
		74	(PY[7]-PY[8]) / 33 x 19 + PY[8]	(NY[7]-NY[8]) / 33 x 19 + NY[8]
		75	(PY[7]-PY[8]) / 33 x 18 + PY[8]	(NY[7]-NY[8]) / 33 x 18 + NY[8]
19		76	(PY[7]-PY[8]) / 33 x 17 + PY[8]	(NY[7]-NY[8]) / 33 x 17 + NY[8]
	19	77	(PY[7]-PY[8]) / 33 x 16 + PY[8]	(NY[7]-NY[8]) / 33 x 16 + NY[8]
		78	(PY[7]-PY[8]) / 33 x 15 + PY[8]	(NY[7]-NY[8]) / 33 x 15 + NY[8]
		79	(PY[7]-PY[8]) / 33 x 14 + PY[8]	(NY[7]-NY[8]) / 33 x 14 + NY[8]
20		80	(PY[7]-PY[8]) / 33 x 13 + PY[8]	(NY[7]-NY[8]) / 33 x 13 + NY[8]
	20	81	(PY[7]-PY[8]) / 33 x 12 + PY[8]	(NY[7]-NY[8]) / 33 x 12 + NY[8]
		82	(PY[7]-PY[8]) / 33 x 11 + PY[8]	(NY[7]-NY[8]) / 33 x 11 + NY[8]
		83	(PY[7]-PY[8]) / 33 x 10 + PY[8]	(NY[7]-NY[8]) / 33 x 10 + NY[8]
21		84	(PY[7]-PY[8]) / 33 x 9 + PY[8]	(NY[7]-NY[8]) / 33 x 9 + NY[8]
	21	85	(PY[7]-PY[8]) / 33 x 8 + PY[8]	(NY[7]-NY[8]) / 33 x 8 + NY[8]
		86	(PY[7]-PY[8]) / 33 x 7 + PY[8]	(NY[7]-NY[8]) / 33 x 7 + NY[8]
		87	(PY[7]-PY[8]) / 33 x 6 + PY[8]	(NY[7]-NY[8]) / 33 x 6 + NY[8]
22		88	(PY[7]-PY[8]) / 33 x 5 + PY[8]	(NY[7]-NY[8]) / 33 x 5 + NY[8]
	22	89	(PY[7]-PY[8]) / 33 x 4 + PY[8]	(NY[7]-NY[8]) / 33 x 4 + NY[8]
		90	(PY[7]-PY[8]) / 33 x 3 + PY[8]	(NY[7]-NY[8]) / 33 x 3 + NY[8]
		91	(PY[7]-PY[8]) / 33 x 2 + PY[8]	(NY[7]-NY[8]) / 33 x 2 + NY[8]
23		92	(PY[7]-PY[8]) / 33 x 1 + PY[8]	(NY[7]-NY[8]) / 33 x 1 + NY[8]
	23	93	PY[8]	NY[8]
		94	(PY[8]-PY[9]) / 32 x 31 + PY[9]	(NY[8]-NY[9]) / 32 x 31 + NY[9]
		95	(PY[8]-PY[9]) / 32 x 30 + PY[9]	(NY[8]-NY[9]) / 32 x 30 + NY[9]
24		96	(PY[8]-PY[9]) / 32 x 29 + PY[9]	(NY[8]-NY[9]) / 32 x 29 + NY[9]
	24	97	(PY[8]-PY[9]) / 32 x 28 + PY[9]	(NY[8]-NY[9]) / 32 x 28 + NY[9]
		98	(PY[8]-PY[9]) / 32 x 27 + PY[9]	(NY[8]-NY[9]) / 32 x 27 + NY[9]
		99	(PY[8]-PY[9]) / 32 x 26 + PY[9]	(NY[8]-NY[9]) / 32 x 26 + NY[9]
25		100	(PY[8]-PY[9]) / 32 x 25 + PY[9]	(NY[8]-NY[9]) / 32 x 25 + NY[9]
	25	101	(PY[8]-PY[9]) / 32 x 24 + PY[9]	(NY[8]-NY[9]) / 32 x 24 + NY[9]
		102	(PY[8]-PY[9]) / 32 x 23 + PY[9]	(NY[8]-NY[9]) / 32 x 23 + NY[9]
		103	(PY[8]-PY[9]) / 32 x 22 + PY[9]	(NY[8]-NY[9]) / 32 x 22 + NY[9]
26		104	(PY[8]-PY[9]) / 32 x 21 + PY[9]	(NY[8]-NY[9]) / 32 x 21 + NY[9]
	26	105	(PY[8]-PY[9]) / 32 x 20 + PY[9]	(NY[8]-NY[9]) / 32 x 20 + NY[9]
		106	(PY[8]-PY[9]) / 32 x 19 + PY[9]	(NY[8]-NY[9]) / 32 x 19 + NY[9]
		107	(PY[8]-PY[9]) / 32 x 18 + PY[9]	(NY[8]-NY[9]) / 32 x 18 + NY[9]
27		108	(PY[8]-PY[9]) / 32 x 17 + PY[9]	(NY[8]-NY[9]) / 32 x 17 + NY[9]
	27	109	(PY[8]-PY[9]) / 32 x 16 + PY[9]	(NY[8]-NY[9]) / 32 x 16 + NY[9]
		110	(PY[8]-PY[9]) / 32 x 15 + PY[9]	(NY[8]-NY[9]) / 32 x 15 + NY[9]
		111	(PY[8]-PY[9]) / 32 x 14 + PY[9]	(NY[8]-NY[9]) / 32 x 14 + NY[9]
28		112	(PY[8]-PY[9]) / 32 x 13 + PY[9]	(NY[8]-NY[9]) / 32 x 13 + NY[9]
	28	113	(PY[8]-PY[9]) / 32 x 12 + PY[9]	(NY[8]-NY[9]) / 32 x 12 + NY[9]
		114	(PY[8]-PY[9]) / 32 x 11 + PY[9]	(NY[8]-NY[9]) / 32 x 11 + NY[9]
		115	(PY[8]-PY[9]) / 32 x 10 + PY[9]	(NY[8]-NY[9]) / 32 x 10 + NY[9]
29		116	(PY[8]-PY[9]) / 32 x 9 + PY[9]	(NY[8]-NY[9]) / 32 x 9 + NY[9]
	29	117	(PY[8]-PY[9]) / 32 x 8 + PY[9]	(NY[8]-NY[9]) / 32 x 8 + NY[9]
		118	(PY[8]-PY[9]) / 32 x 7 + PY[9]	(NY[8]-NY[9]) / 32 x 7 + NY[9]
		119	(PY[8]-PY[9]) / 32 x 6 + PY[9]	(NY[8]-NY[9]) / 32 x 6 + NY[9]
30		120	(PY[8]-PY[9]) / 32 x 5 + PY[9]	(NY[8]-NY[9]) / 32 x 5 + NY[9]
	30	121	(PY[8]-PY[9]) / 32 x 4 + PY[9]	(NY[8]-NY[9]) / 32 x 4 + NY[9]
		122	(PY[8]-PY[9]) / 32 x 3 + PY[9]	(NY[8]-NY[9]) / 32 x 3 + NY[9]
		123	(PY[8]-PY[9]) / 32 x 2 + PY[9]	(NY[8]-NY[9]) / 32 x 2 + NY[9]
31		124	(PY[8]-PY[9]) / 32 x 1 + PY[9]	(NY[8]-NY[9]) / 32 x 1 + NY[9]
	31	125	PY[9]	NY[9]
		126	(PY[9]-PY[10]) / 33 x 32 + PY[10]	(NY[9]-NY[10]) / 33 x 32 + NY[10]
		127	(PY[9]-PY[10]) / 33 x 31 + PY[10]	(NY[9]-NY[10]) / 33 x 31 + NY[10]

SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
32		128	(PY[9]-PY[10]) / 33 x 30 + PY[10]	(NY[9]-NY[10]) / 33 x 30 + NY[10]
		129	(PY[9]-PY[10]) / 33 x 29 + PY[10]	(NY[9]-NY[10]) / 33 x 29 + NY[10]
	32	130	(PY[9]-PY[10]) / 33 x 28 + PY[10]	(NY[9]-NY[10]) / 33 x 28 + NY[10]
		131	(PY[9]-PY[10]) / 33 x 27 + PY[10]	(NY[9]-NY[10]) / 33 x 27 + NY[10]
33		132	(PY[9]-PY[10]) / 33 x 26 + PY[10]	(NY[9]-NY[10]) / 33 x 26 + NY[10]
		133	(PY[9]-PY[10]) / 33 x 25 + PY[10]	(NY[9]-NY[10]) / 33 x 25 + NY[10]
	33	134	(PY[9]-PY[10]) / 33 x 24 + PY[10]	(NY[9]-NY[10]) / 33 x 24 + NY[10]
		135	(PY[9]-PY[10]) / 33 x 23 + PY[10]	(NY[9]-NY[10]) / 33 x 23 + NY[10]
34		136	(PY[9]-PY[10]) / 33 x 22 + PY[10]	(NY[9]-NY[10]) / 33 x 22 + NY[10]
		137	(PY[9]-PY[10]) / 33 x 21 + PY[10]	(NY[9]-NY[10]) / 33 x 21 + NY[10]
	34	138	(PY[9]-PY[10]) / 33 x 20 + PY[10]	(NY[9]-NY[10]) / 33 x 20 + NY[10]
		139	(PY[9]-PY[10]) / 33 x 19 + PY[10]	(NY[9]-NY[10]) / 33 x 19 + NY[10]
35		140	(PY[9]-PY[10]) / 33 x 18 + PY[10]	(NY[9]-NY[10]) / 33 x 18 + NY[10]
		141	(PY[9]-PY[10]) / 33 x 17 + PY[10]	(NY[9]-NY[10]) / 33 x 17 + NY[10]
	35	142	(PY[9]-PY[10]) / 33 x 16 + PY[10]	(NY[9]-NY[10]) / 33 x 16 + NY[10]
		143	(PY[9]-PY[10]) / 33 x 15 + PY[10]	(NY[9]-NY[10]) / 33 x 15 + NY[10]
36		144	(PY[9]-PY[10]) / 33 x 14 + PY[10]	(NY[9]-NY[10]) / 33 x 14 + NY[10]
		145	(PY[9]-PY[10]) / 33 x 13 + PY[10]	(NY[9]-NY[10]) / 33 x 13 + NY[10]
	36	146	(PY[9]-PY[10]) / 33 x 12 + PY[10]	(NY[9]-NY[10]) / 33 x 12 + NY[10]
		147	(PY[9]-PY[10]) / 33 x 11 + PY[10]	(NY[9]-NY[10]) / 33 x 11 + NY[10]
37		148	(PY[9]-PY[10]) / 33 x 10 + PY[10]	(NY[9]-NY[10]) / 33 x 10 + NY[10]
		149	(PY[9]-PY[10]) / 33 x 9 + PY[10]	(NY[9]-NY[10]) / 33 x 9 + NY[10]
	37	150	(PY[9]-PY[10]) / 33 x 8 + PY[10]	(NY[9]-NY[10]) / 33 x 8 + NY[10]
		151	(PY[9]-PY[10]) / 33 x 7 + PY[10]	(NY[9]-NY[10]) / 33 x 7 + NY[10]
38		152	(PY[9]-PY[10]) / 33 x 6 + PY[10]	(NY[9]-NY[10]) / 33 x 6 + NY[10]
		153	(PY[9]-PY[10]) / 33 x 5 + PY[10]	(NY[9]-NY[10]) / 33 x 5 + NY[10]
	38	154	(PY[9]-PY[10]) / 33 x 4 + PY[10]	(NY[9]-NY[10]) / 33 x 4 + NY[10]
		155	(PY[9]-PY[10]) / 33 x 3 + PY[10]	(NY[9]-NY[10]) / 33 x 3 + NY[10]
39		156	(PY[9]-PY[10]) / 33 x 2 + PY[10]	(NY[9]-NY[10]) / 33 x 2 + NY[10]
		157	(PY[9]-PY[10]) / 33 x 1 + PY[10]	(NY[9]-NY[10]) / 33 x 1 + NY[10]
	39	158	PY[10]	NY[10]
		159	(PY[10]-PY[11]) / 32 x 31 + PY[11]	(NY[10]-NY[11]) / 32 x 31 + NY[11]
40		160	(PY[10]-PY[11]) / 32 x 30 + PY[11]	(NY[10]-NY[11]) / 32 x 30 + NY[11]
		161	(PY[10]-PY[11]) / 32 x 29 + PY[11]	(NY[10]-NY[11]) / 32 x 29 + NY[11]
	40	162	(PY[10]-PY[11]) / 32 x 28 + PY[11]	(NY[10]-NY[11]) / 32 x 28 + NY[11]
		163	(PY[10]-PY[11]) / 32 x 27 + PY[11]	(NY[10]-NY[11]) / 32 x 27 + NY[11]
41		164	(PY[10]-PY[11]) / 32 x 26 + PY[11]	(NY[10]-NY[11]) / 32 x 26 + NY[11]
		165	(PY[10]-PY[11]) / 32 x 25 + PY[11]	(NY[10]-NY[11]) / 32 x 25 + NY[11]
	41	166	(PY[10]-PY[11]) / 32 x 24 + PY[11]	(NY[10]-NY[11]) / 32 x 24 + NY[11]
		167	(PY[10]-PY[11]) / 32 x 23 + PY[11]	(NY[10]-NY[11]) / 32 x 23 + NY[11]
42		168	(PY[10]-PY[11]) / 32 x 22 + PY[11]	(NY[10]-NY[11]) / 32 x 22 + NY[11]
		169	(PY[10]-PY[11]) / 32 x 21 + PY[11]	(NY[10]-NY[11]) / 32 x 21 + NY[11]
	42	170	(PY[10]-PY[11]) / 32 x 20 + PY[11]	(NY[10]-NY[11]) / 32 x 20 + NY[11]
		171	(PY[10]-PY[11]) / 32 x 19 + PY[11]	(NY[10]-NY[11]) / 32 x 19 + NY[11]
43		172	(PY[10]-PY[11]) / 32 x 18 + PY[11]	(NY[10]-NY[11]) / 32 x 18 + NY[11]
		173	(PY[10]-PY[11]) / 32 x 17 + PY[11]	(NY[10]-NY[11]) / 32 x 17 + NY[11]
	43	174	(PY[10]-PY[11]) / 32 x 16 + PY[11]	(NY[10]-NY[11]) / 32 x 16 + NY[11]
		175	(PY[10]-PY[11]) / 32 x 15 + PY[11]	(NY[10]-NY[11]) / 32 x 15 + NY[11]
44		176	(PY[10]-PY[11]) / 32 x 14 + PY[11]	(NY[10]-NY[11]) / 32 x 14 + NY[11]
		177	(PY[10]-PY[11]) / 32 x 13 + PY[11]	(NY[10]-NY[11]) / 32 x 13 + NY[11]
	44	178	(PY[10]-PY[11]) / 32 x 12 + PY[11]	(NY[10]-NY[11]) / 32 x 12 + NY[11]
		179	(PY[10]-PY[11]) / 32 x 11 + PY[11]	(NY[10]-NY[11]) / 32 x 11 + NY[11]
45		180	(PY[10]-PY[11]) / 32 x 10 + PY[11]	(NY[10]-NY[11]) / 32 x 10 + NY[11]
		181	(PY[10]-PY[11]) / 32 x 9 + PY[11]	(NY[10]-NY[11]) / 32 x 9 + NY[11]
	45	182	(PY[10]-PY[11]) / 32 x 8 + PY[11]	(NY[10]-NY[11]) / 32 x 8 + NY[11]
		183	(PY[10]-PY[11]) / 32 x 7 + PY[11]	(NY[10]-NY[11]) / 32 x 7 + NY[11]
46		184	(PY[10]-PY[11]) / 32 x 6 + PY[11]	(NY[10]-NY[11]) / 32 x 6 + NY[11]
		185	(PY[10]-PY[11]) / 32 x 5 + PY[11]	(NY[10]-NY[11]) / 32 x 5 + NY[11]
	46	186	(PY[10]-PY[11]) / 32 x 4 + PY[11]	(NY[10]-NY[11]) / 32 x 4 + NY[11]
		187	(PY[10]-PY[11]) / 32 x 3 + PY[11]	(NY[10]-NY[11]) / 32 x 3 + NY[11]
47		188	(PY[10]-PY[11]) / 32 x 2 + PY[11]	(NY[10]-NY[11]) / 32 x 2 + NY[11]
		189	(PY[10]-PY[11]) / 32 x 1 + PY[11]	(NY[10]-NY[11]) / 32 x 1 + NY[11]
	47	190	PY[11]	NY[11]
		191	(PY[11]-PY[12]) / 17 x 16 + PY[12]	(NY[11]-NY[12]) / 17 x 16 + NY[12]

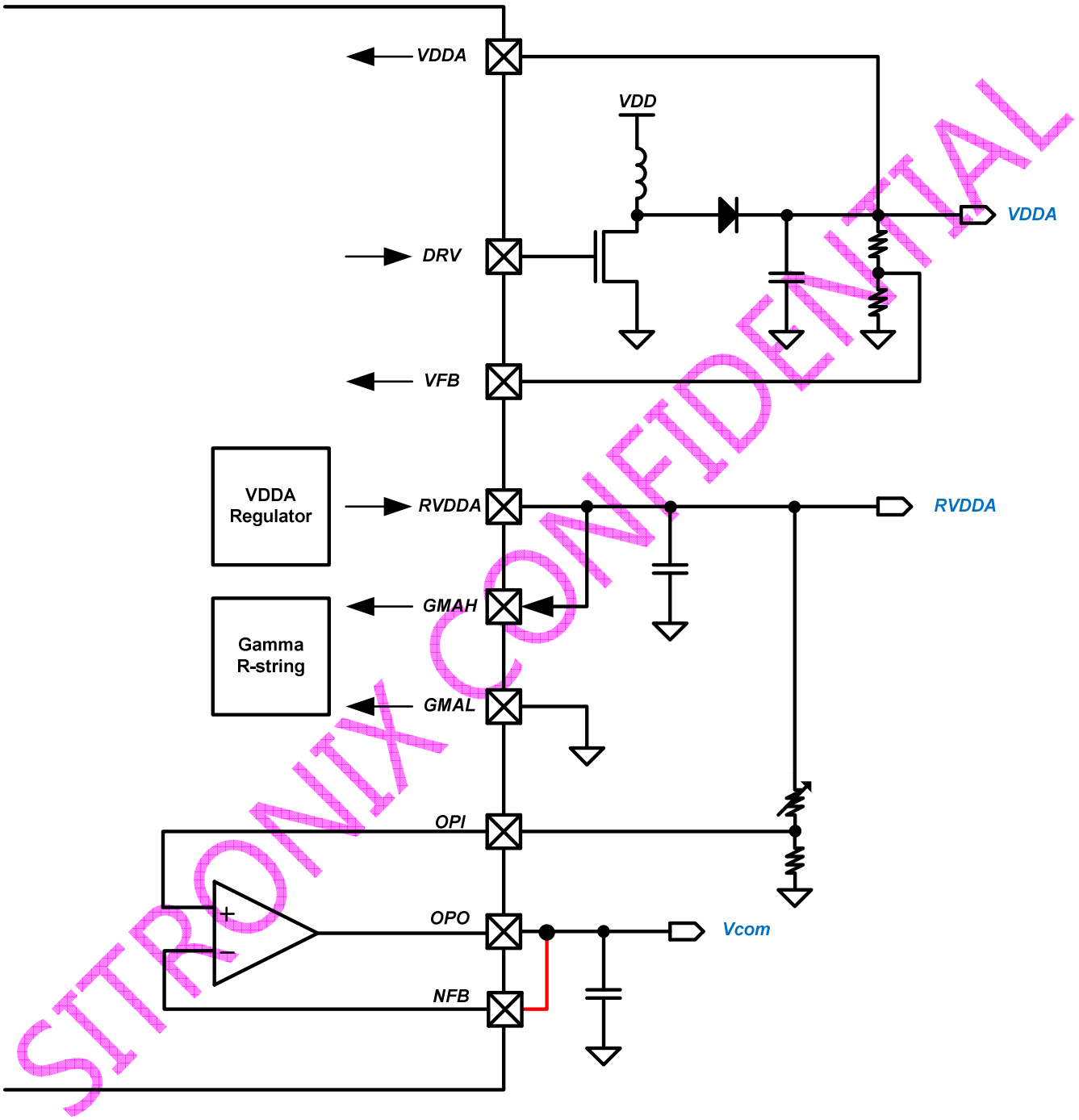
SD mode 6 bit gray code	TCON mode 6 bit gray code	TCON/SD 8 bit gray code	Positive Gamma voltage	Negative Gamma voltage
48		192	(PY[11]-PY[12]) / 17 x 15 + PY[12]	(NY[11]-NY[12]) / 17 x 15 + NY[12]
		193	(PY[11]-PY[12]) / 17 x 14 + PY[12]	(NY[11]-NY[12]) / 17 x 14 + NY[12]
		194	(PY[11]-PY[12]) / 17 x 13 + PY[12]	(NY[11]-NY[12]) / 17 x 13 + NY[12]
	48	195	(PY[11]-PY[12]) / 17 x 12 + PY[12]	(NY[11]-NY[12]) / 17 x 12 + NY[12]
49		196	(PY[11]-PY[12]) / 17 x 11 + PY[12]	(NY[11]-NY[12]) / 17 x 11 + NY[12]
		197	(PY[11]-PY[12]) / 17 x 10 + PY[12]	(NY[11]-NY[12]) / 17 x 10 + NY[12]
		198	(PY[11]-PY[12]) / 17 x 9 + PY[12]	(NY[11]-NY[12]) / 17 x 9 + NY[12]
	49	199	(PY[11]-PY[12]) / 17 x 8 + PY[12]	(NY[11]-NY[12]) / 17 x 8 + NY[12]
50		200	(PY[11]-PY[12]) / 17 x 7 + PY[12]	(NY[11]-NY[12]) / 17 x 7 + NY[12]
		201	(PY[11]-PY[12]) / 17 x 6 + PY[12]	(NY[11]-NY[12]) / 17 x 6 + NY[12]
		202	(PY[11]-PY[12]) / 17 x 5 + PY[12]	(NY[11]-NY[12]) / 17 x 5 + NY[12]
	50	203	(PY[11]-PY[12]) / 17 x 4 + PY[12]	(NY[11]-NY[12]) / 17 x 4 + NY[12]
51		204	(PY[11]-PY[12]) / 17 x 3 + PY[12]	(NY[11]-NY[12]) / 17 x 3 + NY[12]
		205	(PY[11]-PY[12]) / 17 x 2 + PY[12]	(NY[11]-NY[12]) / 17 x 2 + NY[12]
		206	(PY[11]-PY[12]) / 17 x 1 + PY[12]	(NY[11]-NY[12]) / 17 x 1 + NY[12]
	51	207	PY[12]	(NY[11]-NY[12])
52		208	(PY[12]-PY[13]) / 16 x 15 + PY[13]	(NY[12]-NY[13]) / 16 x 15 + NY[13]
		209	(PY[12]-PY[13]) / 16 x 14 + PY[13]	(NY[12]-NY[13]) / 16 x 14 + NY[13]
		210	(PY[12]-PY[13]) / 16 x 13 + PY[13]	(NY[12]-NY[13]) / 16 x 13 + NY[13]
	52	211	(PY[12]-PY[13]) / 16 x 12 + PY[13]	(NY[12]-NY[13]) / 16 x 12 + NY[13]
53		212	(PY[12]-PY[13]) / 16 x 11 + PY[13]	(NY[12]-NY[13]) / 16 x 11 + NY[13]
		213	(PY[12]-PY[13]) / 16 x 10 + PY[13]	(NY[12]-NY[13]) / 16 x 10 + NY[13]
		214	(PY[12]-PY[13]) / 16 x 9 + PY[13]	(NY[12]-NY[13]) / 16 x 9 + NY[13]
	53	215	(PY[12]-PY[13]) / 16 x 8 + PY[13]	(NY[12]-NY[13]) / 16 x 8 + NY[13]
54		216	(PY[12]-PY[13]) / 16 x 7 + PY[13]	(NY[12]-NY[13]) / 16 x 7 + NY[13]
		217	(PY[12]-PY[13]) / 16 x 6 + PY[13]	(NY[12]-NY[13]) / 16 x 6 + NY[13]
		218	(PY[12]-PY[13]) / 16 x 5 + PY[13]	(NY[12]-NY[13]) / 16 x 5 + NY[13]
	54	219	(PY[12]-PY[13]) / 16 x 4 + PY[13]	(NY[12]-NY[13]) / 16 x 4 + NY[13]
55		220	(PY[12]-PY[13]) / 16 x 3 + PY[13]	(NY[12]-NY[13]) / 16 x 3 + NY[13]
		221	(PY[12]-PY[13]) / 16 x 2 + PY[13]	(NY[12]-NY[13]) / 16 x 2 + NY[13]
		222	(PY[12]-PY[13]) / 16 x 1 + PY[13]	(NY[12]-NY[13]) / 16 x 1 + NY[13]
	55	223	PY[13]	NY[13]
56		224	(PY[13]-PY[14]) / 16 x 15 + PY[14]	(NY[13]-NY[14]) / 16 x 15 + NY[14]
		225	(PY[13]-PY[14]) / 16 x 14 + PY[14]	(NY[13]-NY[14]) / 16 x 14 + NY[14]
		226	(PY[13]-PY[14]) / 16 x 13 + PY[14]	(NY[13]-NY[14]) / 16 x 13 + NY[14]
	56	227	(PY[13]-PY[14]) / 16 x 12 + PY[14]	(NY[13]-NY[14]) / 16 x 12 + NY[14]
57		228	(PY[13]-PY[14]) / 16 x 11 + PY[14]	(NY[13]-NY[14]) / 16 x 11 + NY[14]
		229	(PY[13]-PY[14]) / 16 x 10 + PY[14]	(NY[13]-NY[14]) / 16 x 10 + NY[14]
		230	(PY[13]-PY[14]) / 16 x 9 + PY[14]	(NY[13]-NY[14]) / 16 x 9 + NY[14]
	57	231	(PY[13]-PY[14]) / 16 x 8 + PY[14]	(NY[13]-NY[14]) / 16 x 8 + NY[14]
58		232	(PY[13]-PY[14]) / 16 x 7 + PY[14]	(NY[13]-NY[14]) / 16 x 7 + NY[14]
		233	(PY[13]-PY[14]) / 16 x 6 + PY[14]	(NY[13]-NY[14]) / 16 x 6 + NY[14]
		234	(PY[13]-PY[14]) / 16 x 5 + PY[14]	(NY[13]-NY[14]) / 16 x 5 + NY[14]
	58	235	(PY[13]-PY[14]) / 16 x 4 + PY[14]	(NY[13]-NY[14]) / 16 x 4 + NY[14]
59		236	(PY[13]-PY[14]) / 16 x 3 + PY[14]	(NY[13]-NY[14]) / 16 x 3 + NY[14]
		237	(PY[13]-PY[14]) / 16 x 2 + PY[14]	(NY[13]-NY[14]) / 16 x 2 + NY[14]
		238	(PY[13]-PY[14]) / 16 x 1 + PY[14]	(NY[13]-NY[14]) / 16 x 1 + NY[14]
	59	239	PY[14]	NY[14]
60		240	(PY[14]-PY[15]) / 4 x 3 + PY[15]	(NY[14]-NY[15]) / 4 x 3 + NY[15]
		241	(PY[14]-PY[15]) / 4 x 2 + PY[15]	(NY[14]-NY[15]) / 4 x 2 + NY[15]
		242	(PY[14]-PY[15]) / 4 x 1 + PY[15]	(NY[14]-NY[15]) / 4 x 1 + NY[15]
	60	243	PY[15]	NY[15]
61		244	(PY[15]-PY[16]) / 4 x 3 + PY[16]	(NY[15]-NY[16]) / 4 x 3 + NY[16]
		245	(PY[15]-PY[16]) / 4 x 2 + PY[16]	(NY[15]-NY[16]) / 4 x 2 + NY[16]
		246	(PY[15]-PY[16]) / 4 x 1 + PY[16]	(NY[15]-NY[16]) / 4 x 1 + NY[16]
	61	247	PY[16]	NY[16]
62		248	(PY[16]-PY[17]) / 4 x 3 + PY[17]	(NY[16]-NY[17]) / 4 x 3 + NY[17]
		249	(PY[16]-PY[17]) / 4 x 2 + PY[17]	(NY[16]-NY[17]) / 4 x 2 + NY[17]
		250	(PY[16]-PY[17]) / 4 x 1 + PY[17]	(NY[16]-NY[17]) / 4 x 1 + NY[17]
	62	251	PY[17]	NY[17]
63		252	(PY[17]-PY[18]) / 4 x 3 + PY[18]	(NY[17]-NY[18]) / 4 x 3 + NY[18]
		253	(PY[17]-PY[18]) / 4 x 2 + PY[18]	(NY[17]-NY[18]) / 4 x 2 + NY[18]
		254	(PY[17]-PY[18]) / 4 x 1 + PY[18]	(NY[17]-NY[18]) / 4 x 1 + NY[18]
	63	255	PY[18]	NY[18]

Programmable resolution mode

1. User can set any resolution inside (Max.= 4) SC5004 cascade range and input timing supports SYNC or DE mode.
2. In programmable resolution mode the image scan direction must be fixed (uni-direction) because of some source and gate driver output channels will be ignored. Please make sure scan direction is correct before panel start to layout.
3. There still has some limitations as below :
   (1) H_{TOTAL} x V_{TOTAL} ≦ 1.3 Mega
   (2) H_{DISP} x V_{DISP} ≦ 1.1 Mega
   (3) H_{DISP} ≦ 1712(RGB)
   (4) V_{DISP} ≦ 1280



SC5004 application power circuit (sketch)



Note:

1. Above figure is just a sketch for using SC5004 whole internal DC-DC circuit case.
2. Each module application needs different design, so please consult with Sitronix for detail information.

Liquid crystal response time under low temperature

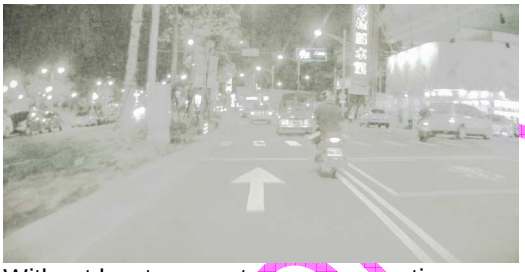
According to liquid crystal response time became very slow under low temperature environment and LCD module usually design as dash board or GPS display in automotive, if the LCD information is not easy to read out when car on the road, it may cause serious safety problem.

Moving GPS map became blur under low temperature

Without low temperature compensation

With low temperature compensation

Night vision image shows poor contrast under low temperature



Without low temperature compensation

With low temperature compensation

Temperature sensor

SC5004 built in a wide range temperature sensor and provide several kinds of low temperature compensation method to improve LCD display performance under low temperature, user can set SC5004 low temperature compensation parameters to improve liquid crystal response time too slow affect and get better display quality without additional cost.

Temperature sensor range : -40~127^{O}C (temperature > 95 ^{O}C characteristic can't be guaranteed)
Temperature sensor accuracy : < +/-4 ^{O}C

Note : Low temp compensation (TEMP1~3[5:0]) range : -40 ~ 71 ^{O}C
Over heat protection (TEMP4~5[5:0]) range : 96 ~127 ^{O}C

TEMP1~5[5:0] : threshold temperature value

TEMP1~5[5:0]	Temperature (^{O}C)
000000	-40 ~ -37
000001	-36 ~ -33
000010	-32 ~ -29
000011	-28 ~ -25
000100	-24 ~ -21
000101	-20 ~ -17
000110	-16 ~ -13
000111	-12 ~ -9
001000	-8 ~ -5
001001	-4 ~ -1
001010	0 ~ 3
001011	4 ~ 7
001100	8 ~ 11
001101	12 ~ 15
001110	16 ~ 19
001111	20 ~ 23
010000	24 ~ 27
010001	28 ~ 31
010010	32 ~ 35
010011	36 ~ 39
010100	40 ~ 43
010101	44 ~ 47
010110	48 ~ 51
010111	52 ~ 55
011000	56 ~ 59
011001	60 ~ 63
011010	64 ~ 67
011011	68 ~ 71
011100	72 ~ 75
011101	76 ~ 79
011110	80 ~ 83
011111	84 ~ 87
100000	88 ~ 91
100001	92 ~ 95
100010	96 ~ 99
100011	100 ~ 103
100100	104 ~ 107
100101	108 ~ 111
100110	112 ~ 115
100111	116 ~ 119
101000	120 ~123
101001	124 ~ 127
101010 | 111111	127 up

Over heat protection

For LCD module over heat problem, user can enable Over Heat Protection (OHP) function to suppress LCD backlight strength or shut down SC5004+SC5005 DC-DC power, but this protection temperature range is over 95^{O}C, please notice that it's already out of SC5004 guaranteed accuracy range.
Setting of OHP register : there are 5 registers (OH_PD, TEMP5[5:0], TEMP4[5:0], FC[7:0], BKL_DUTY[1:0]) and two H/W enable pin (TS_EN and OHP_EN) for OHP function, TEMP4 is OHP start and TEMP5 is end temperature, BKL_DUTY is LED backlight enable duty cycle control register.

OH_PD : over heat power down control.
H : enable
L : disable (default)

TS_EN : temperature sensor enable control
H : enable
L : disable (default)

OHP_EN : over heat protection enable control
H : enable
L : disable (default)

Timer (FC[7:0]) : temperature sensor sampling period, user can set frame counter FC[7:0] from 1 to 255 and this value will be multiple 4 times (4~1020) automatically.

BKL_DUTY[1:0] : LED backlight enable duty cycle setting

BKL_DUTY[1:0]	Enable duty cycle
00	12.5%
01	25% (default)
10	50%
11	100%

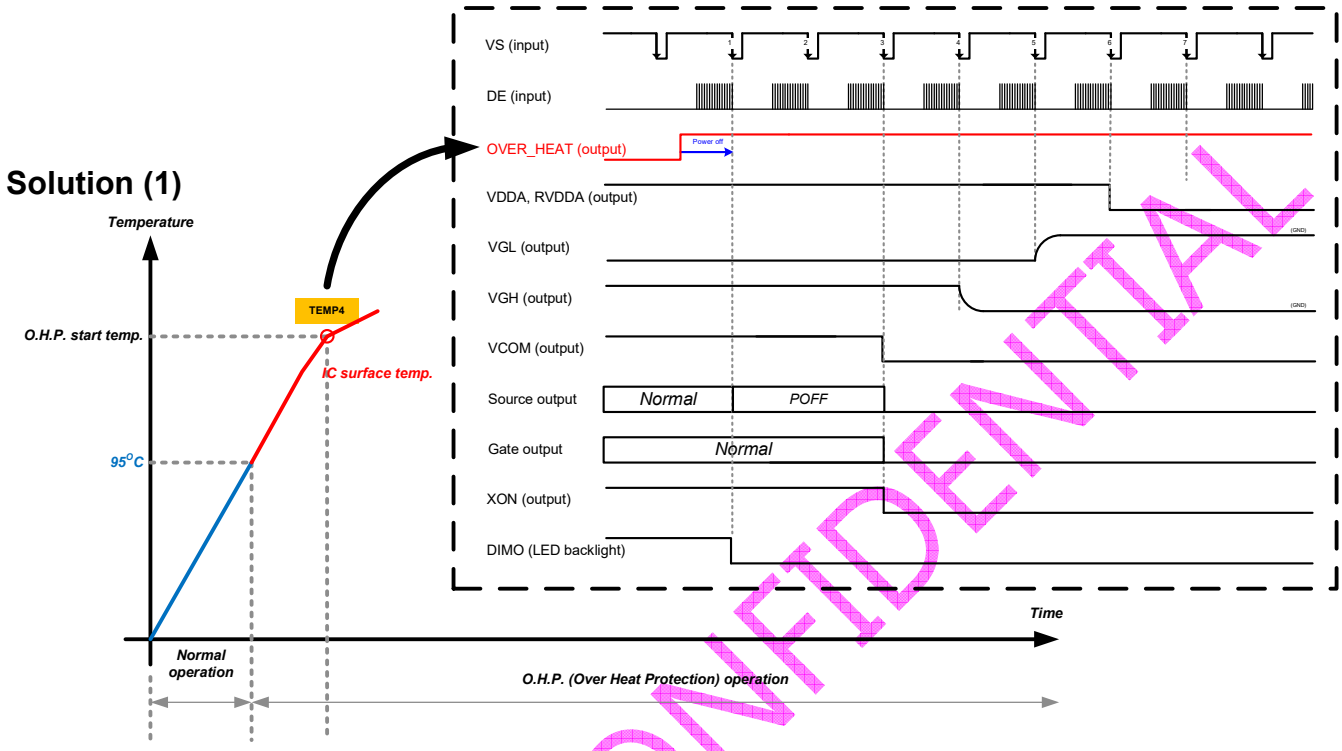
There are 2 different solutions for over heat protection.

Solution (1) : TS_EN=H, OHP_EN=H, OH_PD=H
When master IC internal temperature sensor reading > TEMP4, then master IC will shut down self DC-DC (VDDA, RVDDA, VCOM) and gate driver SC5005 DC-DC (VGL, VGH) immediately and force OVER_HEAT output pin to be high as an alarm signal. User must input reset signal to return to normal operation.

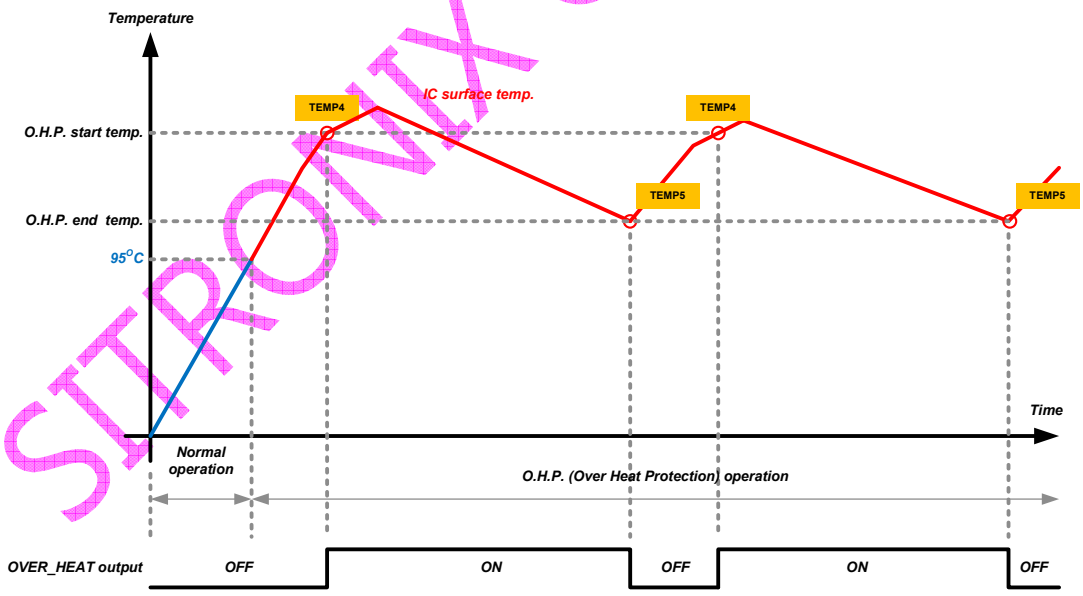
Solution (2) : TS_EN=H, OHP_EN=H, OH_PD=L
In this case, SC5004 will change DIMO output duty cycle to suppress LCD backlight and force OVER_HEAT output pin to be high till temperature sensor reading down to TEMP5 then back to normal operation again.

Note : TEMP4[5:0] and TEMP5[5:0] register value should not be overlap, for hysteresis reason TEMP4[5:0] should higher than TEMP5[5:0] at least 2 levels or above (> 8^{O}C).

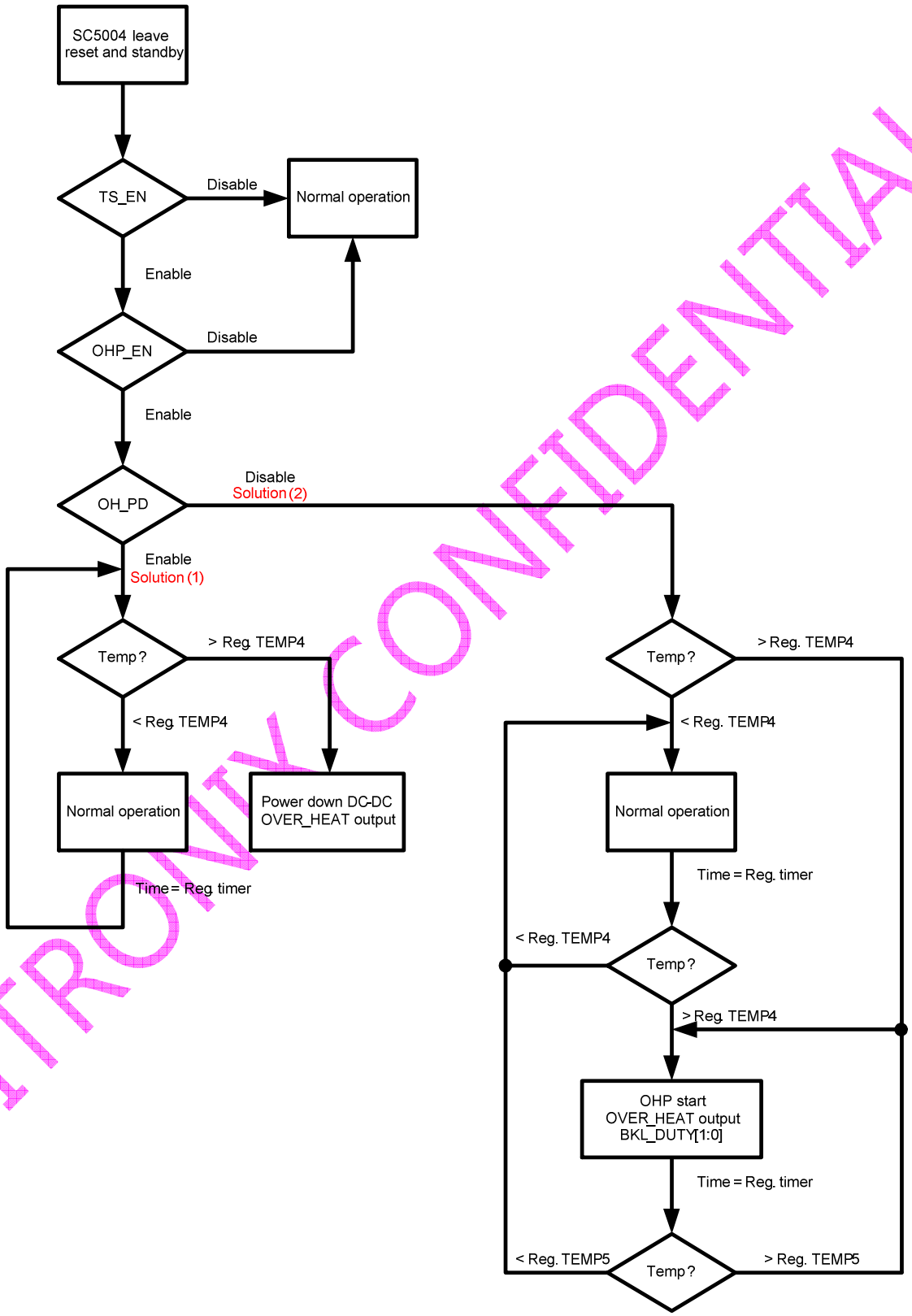
Solution (1)



Solution (2)



Over heat protection flow



Low temperature compensation flow

When user enabled SC5004 temperature sensor and low temperature compensation control then there are 3 kinds of threshold temperature and 1 timer parameters must be set.

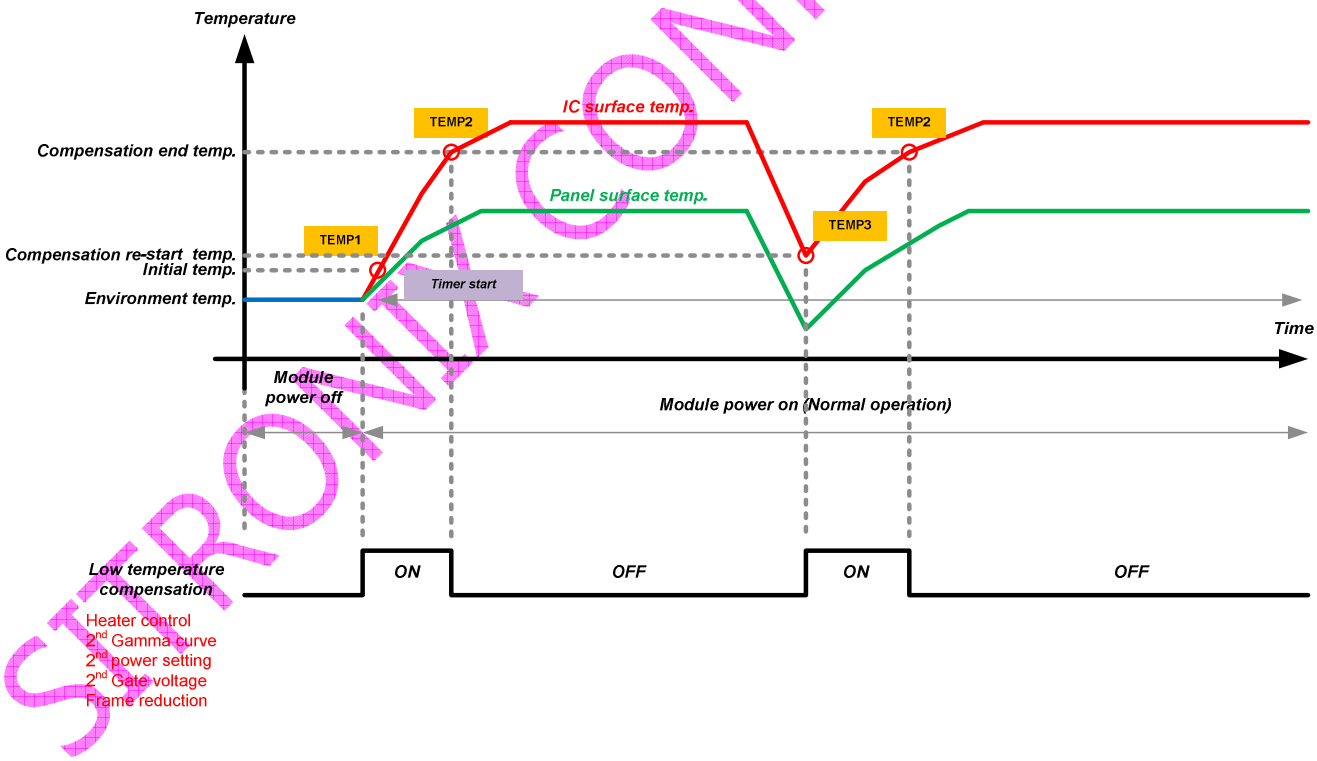
TEMP1[5:0] : initial temperature, when system power on LCD panel surface temperature and SC5004 IC are very close to each other. User can decide low temperature compensation start point by this register.

TEMP2[5:0] : compensation end temperature, there will be a offset temperature between LCD panel surface and SC5004 IC after a period of time, so user should set a ending temperature.

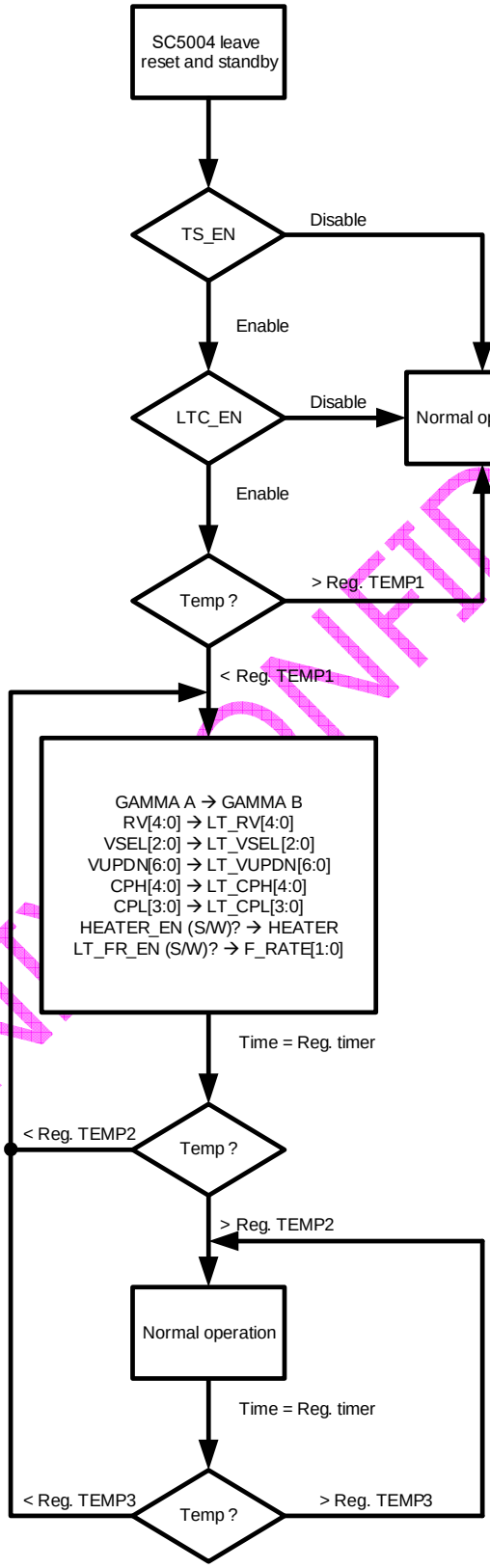
TEMP3[5:0] : compensation re-start temperature, if the environment cooling speed is higher than LCD panel self-heating slope then we need to re-start compensation again.

Timer (FC[7:0]) : temperature sensor sampling period, user can set frame counter FC[7:0] from 1 to 255 and this value will be multiple 4 times (4~1020) automatically.

Note : TEMP2[5:0] and TEMP1[5:0],TEMP3[5:0] register value should not be overlap, for hysteresis reason TEMP2[5:0] should higher than TEMP1[5:0] and TEMP3[5:0] at least 2 levels or above (> 8^{O}C).

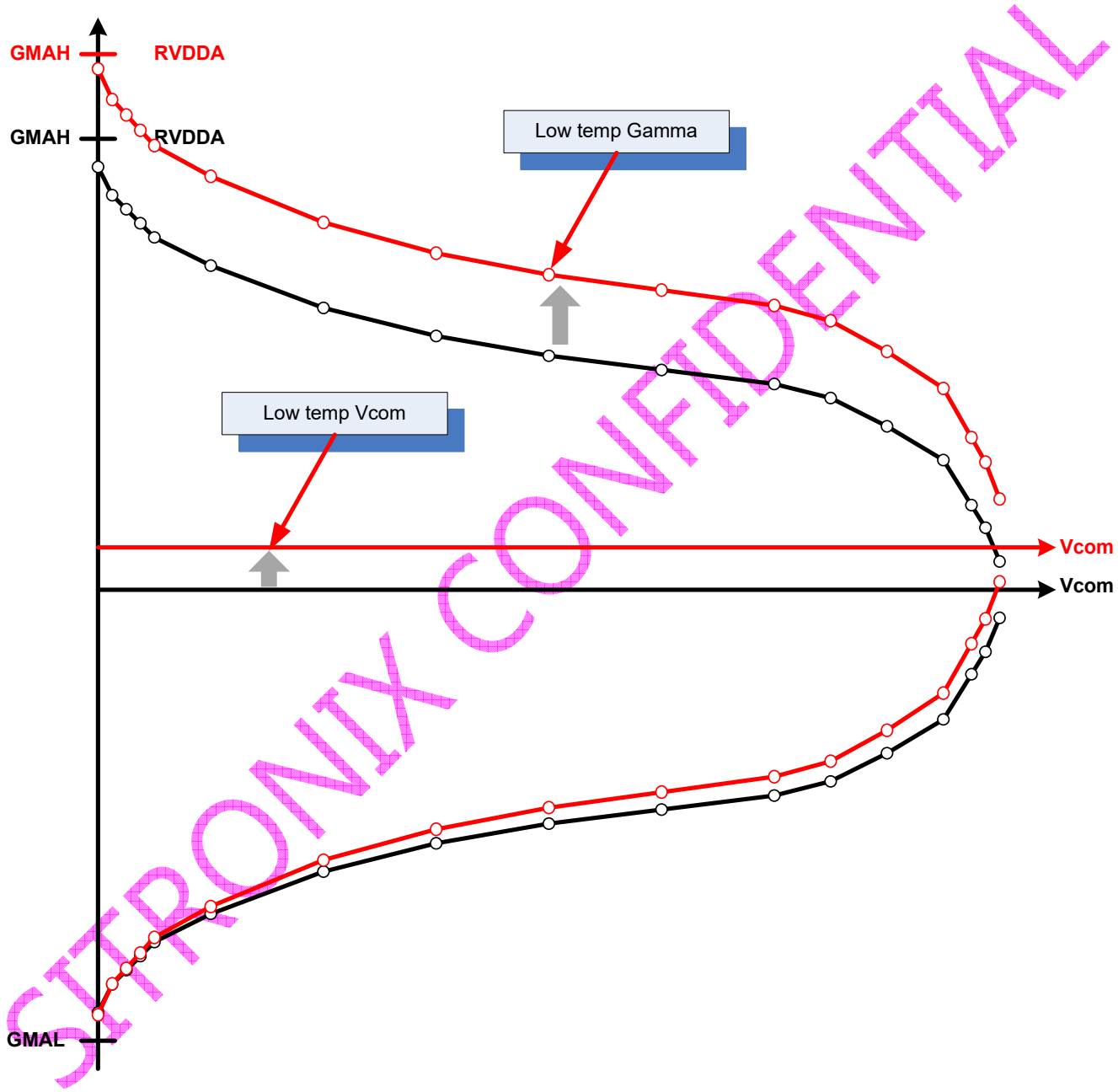


Low temperature compensation flow



Vcom voltage and Gamma curve

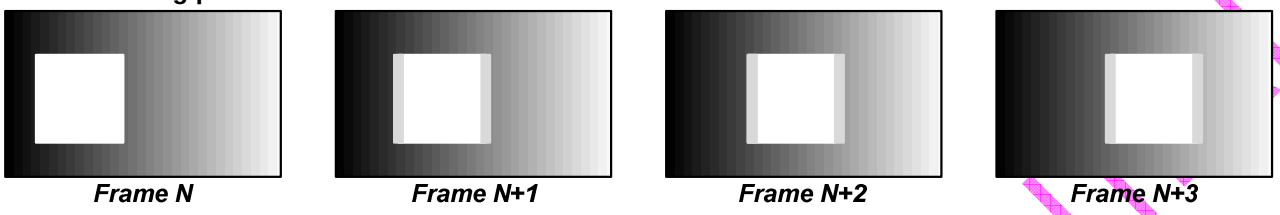
Under low temperature condition SC5004 provide another Gamma curve and power related register parameters, user can fine tune each parameter (LT_RV[4:0], LT_VSEL[2:0], LT_VUPDN[6:0]) to improve image quality.



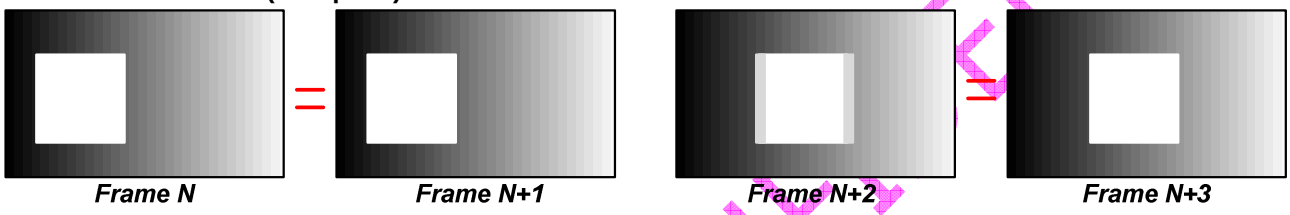
Frame reduction

Under low temperature liquid crystal response time will from 10ms up to 300ms or more, that means moving pictures will become blur and moving text is very hard to read out. SC5004 built in a frame reduction function that can hold moving pictures for more than one frame, it's very helpful for information reading, such as GPS map or car information display purpose.

Normal moving picture



With frame reduction (1/2 speed)



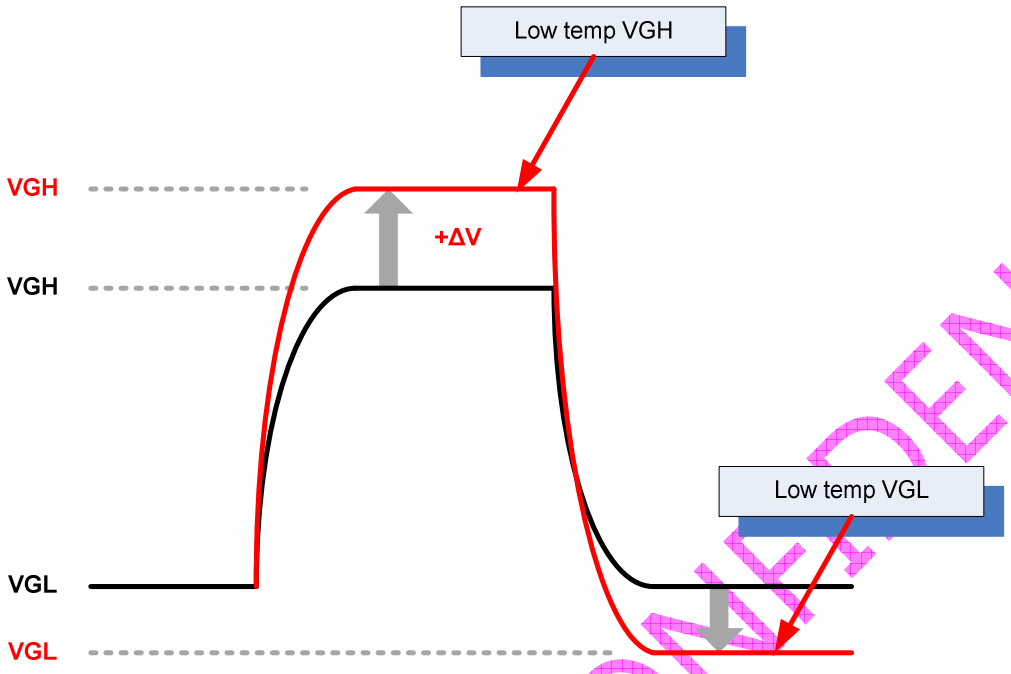
LT_FR_EN : S/W Low temperature frame reduction enable control (10/h)
H : enable
L : disable (default)

F_RATE[1:0] : Frame rate reduction speed setting

F_RATE[1:0]	Frame rate speed
00	1/2 (default)
01	1/3
10	1/4
11	1/8

VGH & VGL for TFT gate driver voltage

Because of TFT Vth voltage varies with temperature, user can fine tune TFT Gate driving voltage through SC5004 (LT_CPH[4:0] and LT_CPL[3:0]) register settings.



Heater control

SC5004 can output a heater control signal with temperature sensor function enable, it provide another solution to deal with LCD module under low temperature problem.

HEATER_EN : S/W heater enable control output (0B/h)
H : enable
L : disable (default)

SC5005 Gate driver VGH & VGL voltage control

When SC5004 with SC5005 gate driver as one set driver for LCD panel, user can enable SC5005 internal DC-DC circuit to generate VGH and VGL voltage and voltage level is selectable by SC5004 register settings.

CPH_EN : VGH charge pump enable contorl
H : enable
L : disable (default)

CPH[4:0] : VGH voltage setting

CPH[4:0]	VGH voltage
00000	14.5V
00001	15.0V
00010	15.5V
00011	16.0V
00100	16.5V
00101	17.0V
00110	17.5V
00111	18.0V
01000	18.5V
01001	19.0V
01010	19.5V
01011	20.0V
01100	20.5V
01101	21.0V
01110	21.5V
01111	22.0V
10000	22.5V
10001	23.0V (default)
10010	23.5V
10011	24.0V
10100	24.5V
10101	25.0V
10110	25.5V
10111	26.0V
11000	26.5V
11001	27.0V
11010	27.5V
11011	28.0V
11100	28.5V
11101	29.0V
11110	29.5V
11111	30.0V

Note : Before CPH_EN set to H (enable VGH charge pump), CPL_EN must set to H first.

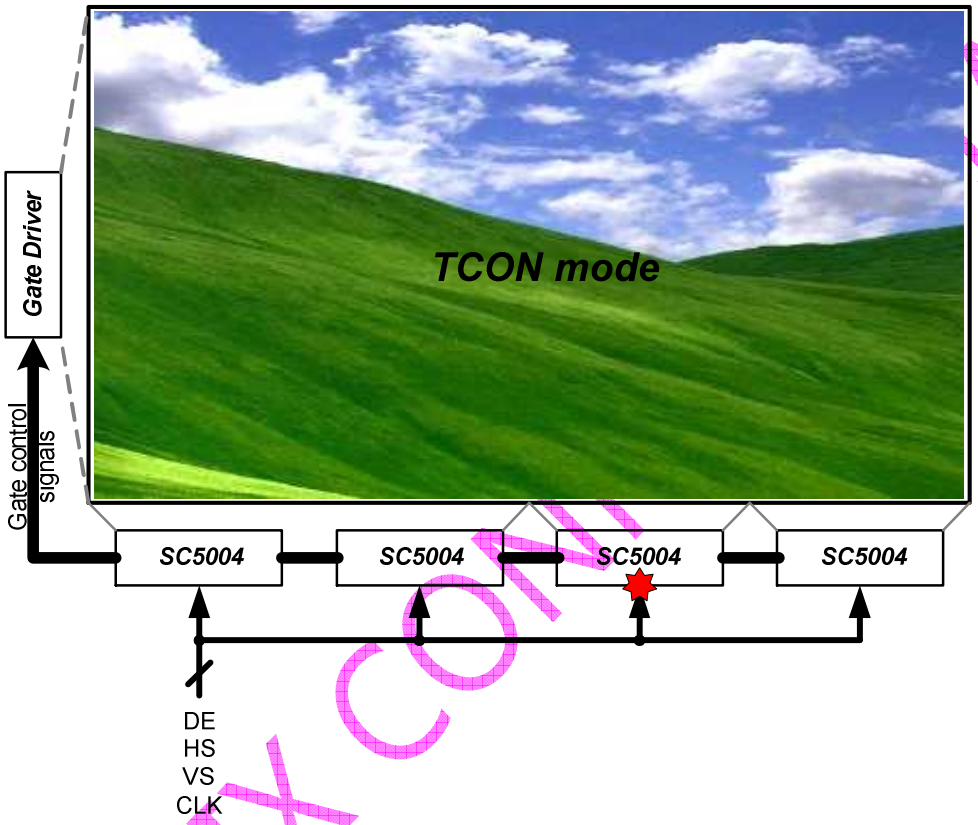
CPL_EN : VGL charge pump enable control
H : enable
L : disable (default)

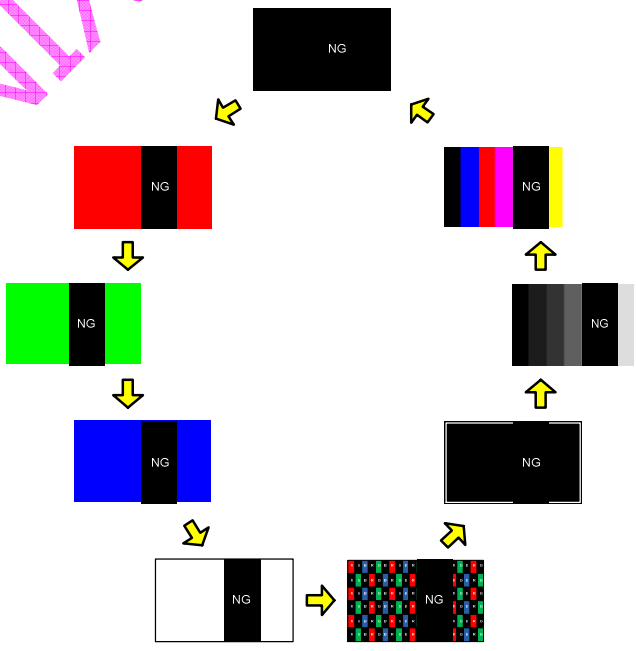
CPL[3:0] : VGL voltage setting

CPL[3:0]	VGL voltage
0000	-3.0V
0001	-3.5V
0010	-4.0V
0011	-4.5V
0100	-5.0V
0101	-5.5V
0110	-6.0V
0111	-6.5V
1000	-7.0V (default)
1001	-7.5V
1010	-8.0V
1011	-8.5V
1100	-9.0V
1101	-9.5V
1110	-10.0V
1111	-10.5V

Input signal missing alarm mode

When SC5004 set as TCON mode and enable MISS_DET register (01/h, bit7) each SC5004 IC will auto detecting CLK and video synchronism signal DE, HS, VS. SC5004 detects CLK and DE in de mode. SC5004 detects CLK, HS and VS in sync mode. If any of these control inputs missing then all SC5004 will auto run BIST pattern (every pattern keep 2 seconds) and failure IC will always be black pattern to remind user abnormal status.



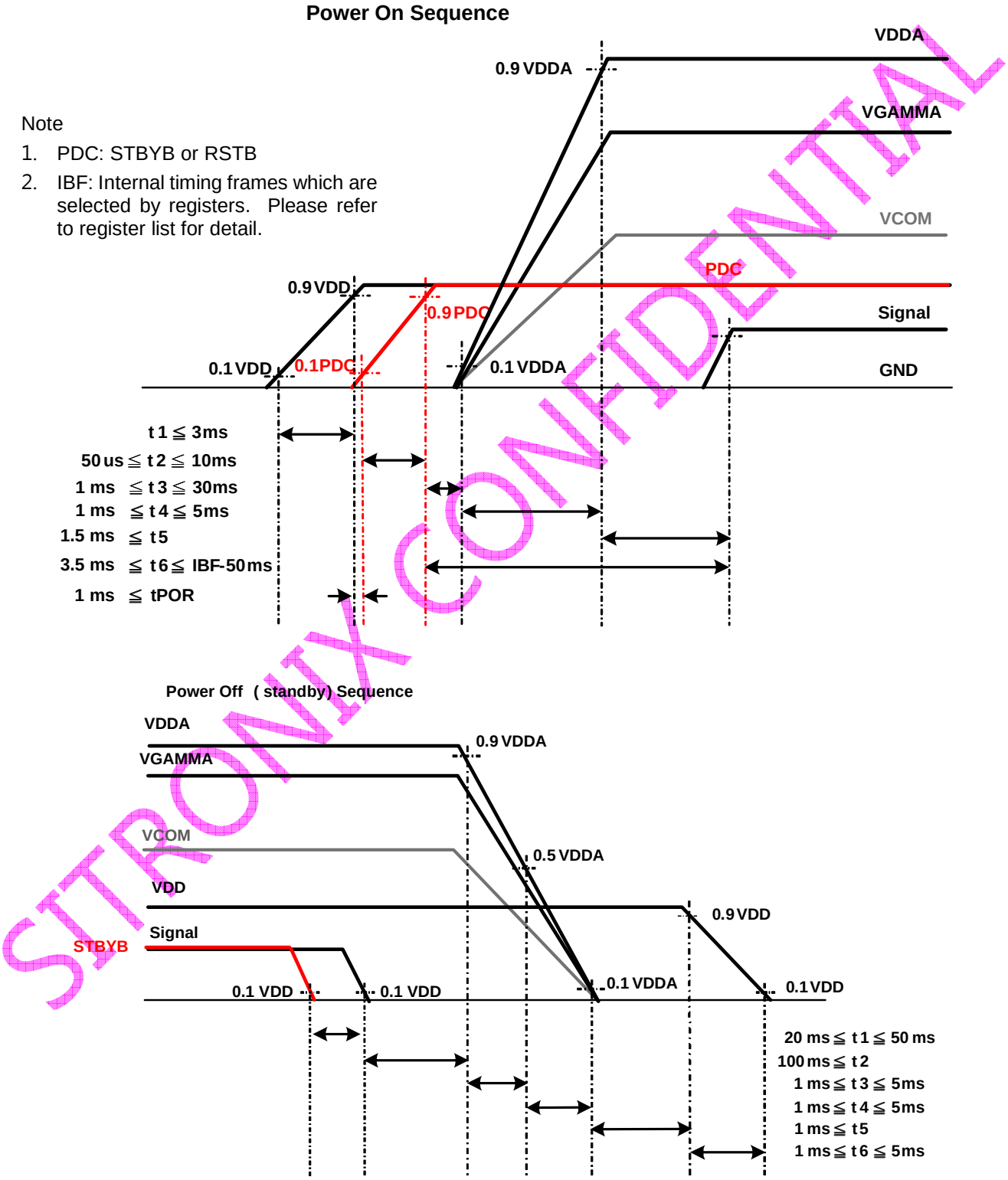


Power on/off sequence without using internal DC-DC

When STSC5004's Tcon mode is selected, and customers don't want to enable STSC5004 internal power circuit to generate all voltages, In order to prevent IC damage from abnormal power on or off sequence, please follow below timings.

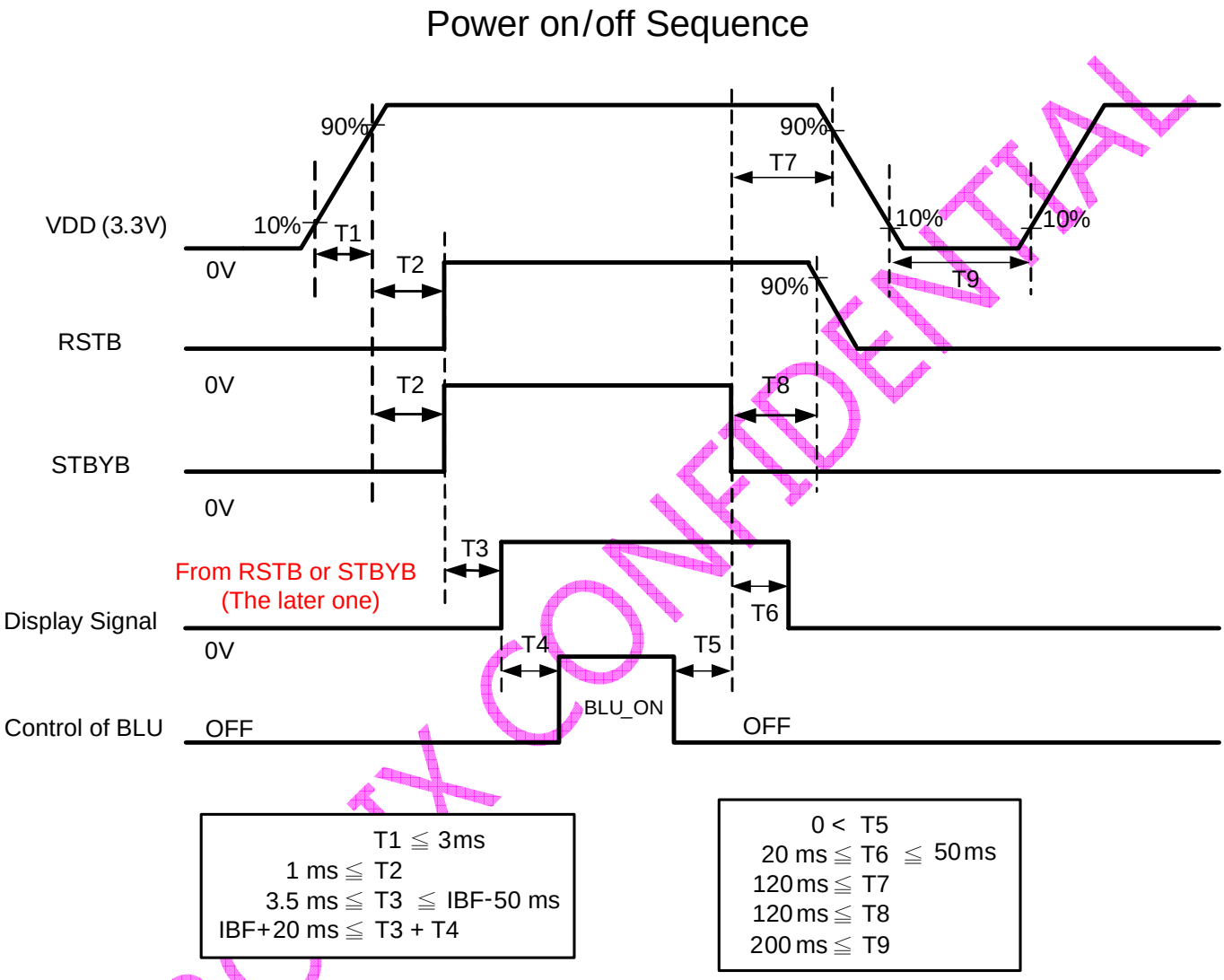
Note

1. PDC: STBYB or RSTB
2. IBF: Internal timing frames which are selected by registers. Please refer to register list for detail.



Power on/off sequence for TFT-LCD module

For TFT-LCD module, please follow below timings to prevent IC damage from abnormal power on or off sequence.

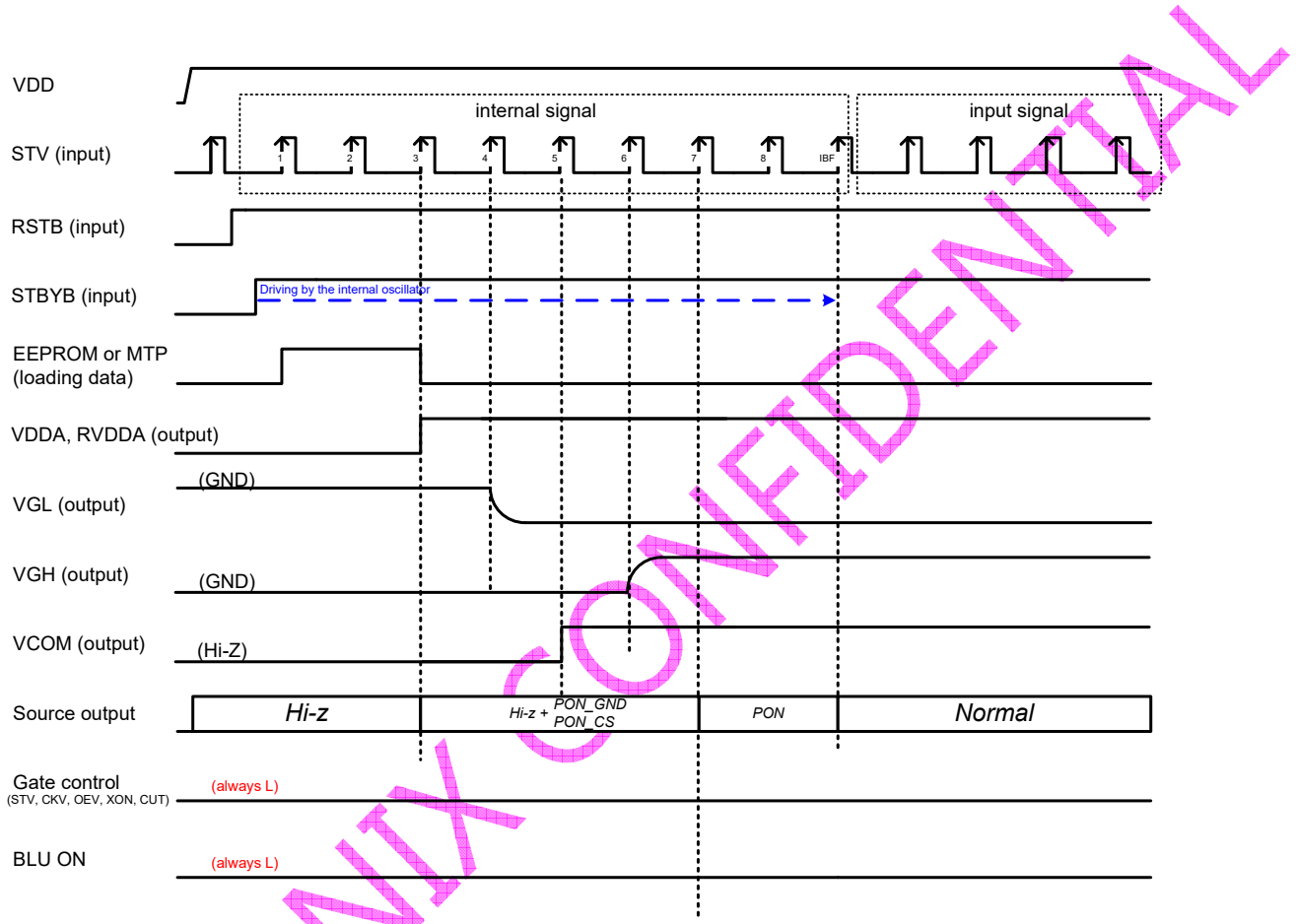


For continuously power off and on, please make sure the external VDD, VGH & VGL are discharged completely before you restart it.

Note that IBF is STSC5004's internal timing frames, selected by registers. Please refer to register list for detail.

SD mode with internal DC-DC power on sequence

When STSC5004 use as a pure source driver with internal power circuit to generate all voltages (MASTER, PWM_EN, LDO_EN, VBUF_EN, CPH_EN and CPL_EN all are H), the power on and off sequence will automatically follow below sequence.



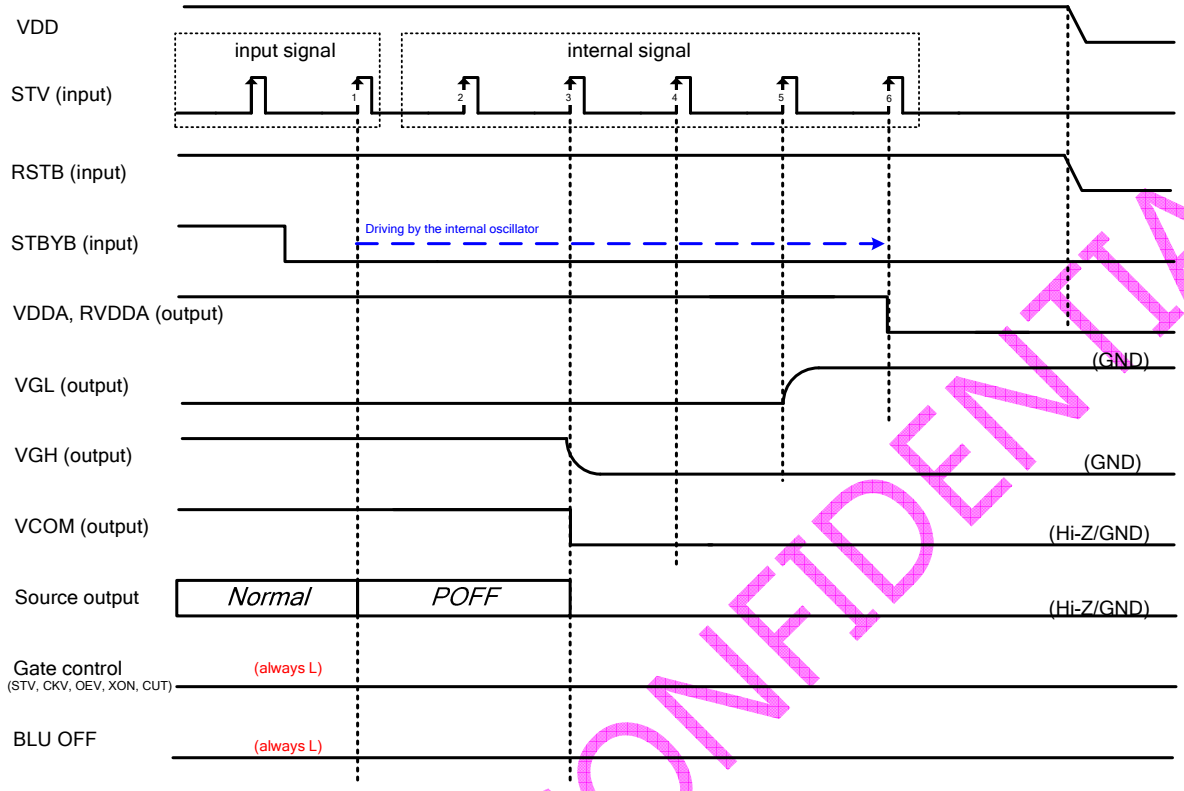
Note:

1. PON_GND, PON_CS, PON, XON function are register settings.
2. Initial IBF (IBF are registers) frames driven by STSC5004's internal oscillator, please make sure all input signals are ready and stable for 50 ms before IBF finishes.
3. IBF and frames:

   IBF: Options for initial internal timing frames.

IB10F	IB79F	Frame
0	0	3
0	1	79
1	0	10
1	1	79

SD mode with internal DC-DC power off sequence

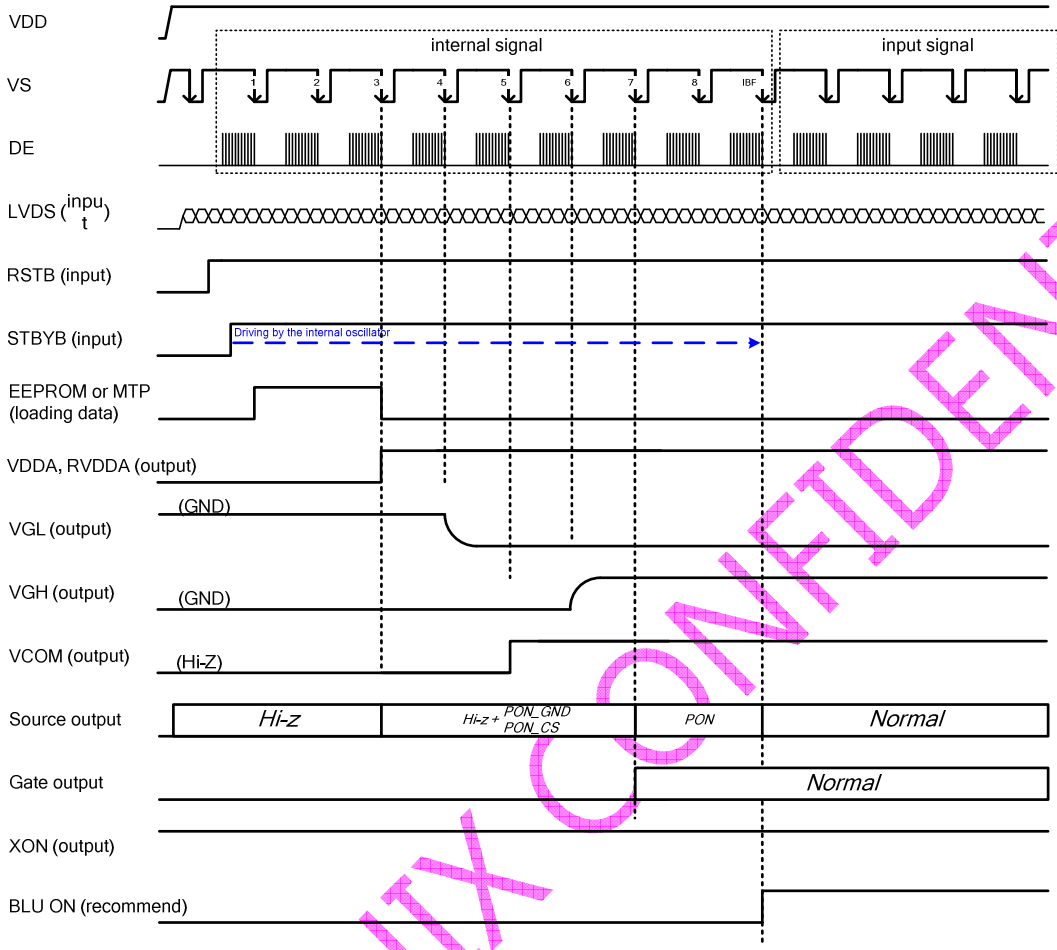


Note :

1. P_OFF is a register setting.
2. After STBYB from H→L 20ms all sequence driving by internal oscillator, don't need external signals.

TCON mode with internal DC-DC power on sequence

When STSC5004 and ST5084 all power control default settings were enabled (PWM_EN, LDO_EN, CPH_EN, CPL_EN and VBUF_EN), the power on and off sequence will automatically follow below sequence.



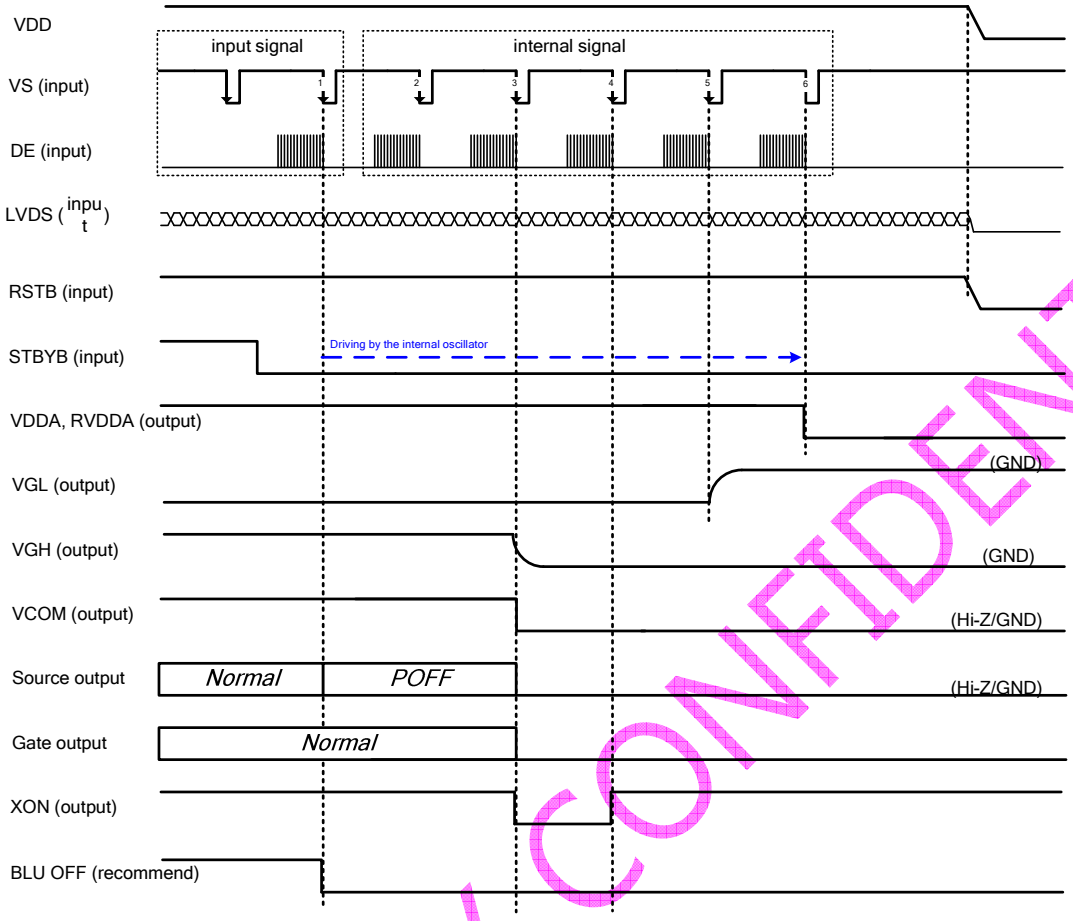
Note :

1. PON_GND, PON_CS, PON, XON function are register settings.
2. Initial IBF (IBF are registers) frames driven by STSC5004's internal oscillator, please make sure all input signals are ready and stable for 50 ms before IBF finishes.
3. IBF and frames:

IBF: Options for initial internal timing frames.

IB10F	IB79F	Frame
0	0	3
0	1	79
1	0	10
1	1	79

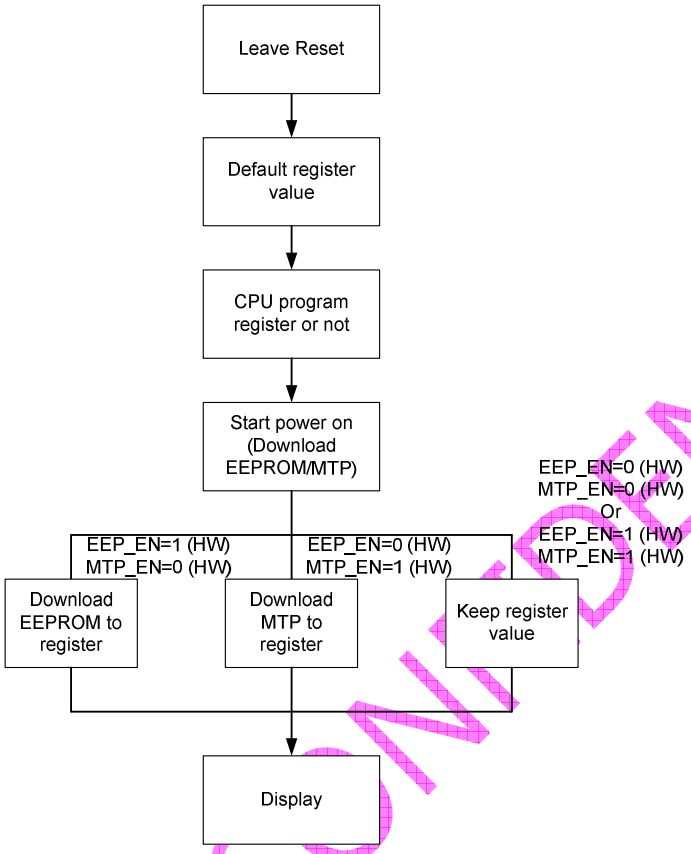
TCON mode with internal DC-DC power off sequence



Note :

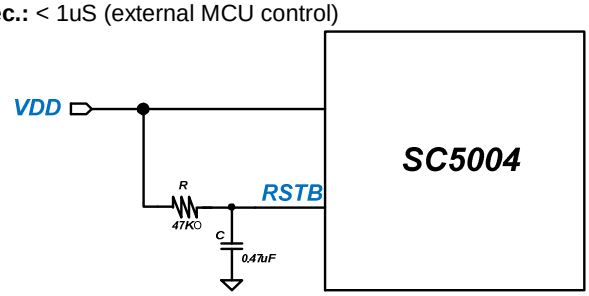
1. P_OFF is a register setting.
2. After STBYB from H→L 20ms all sequence driving by internal oscillator, don't need external signals.

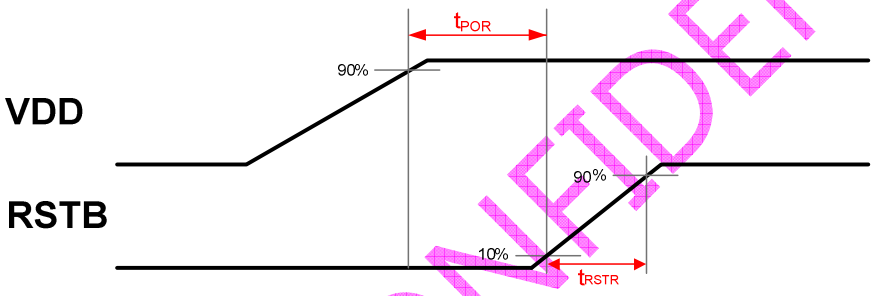
Register value of power on sequence



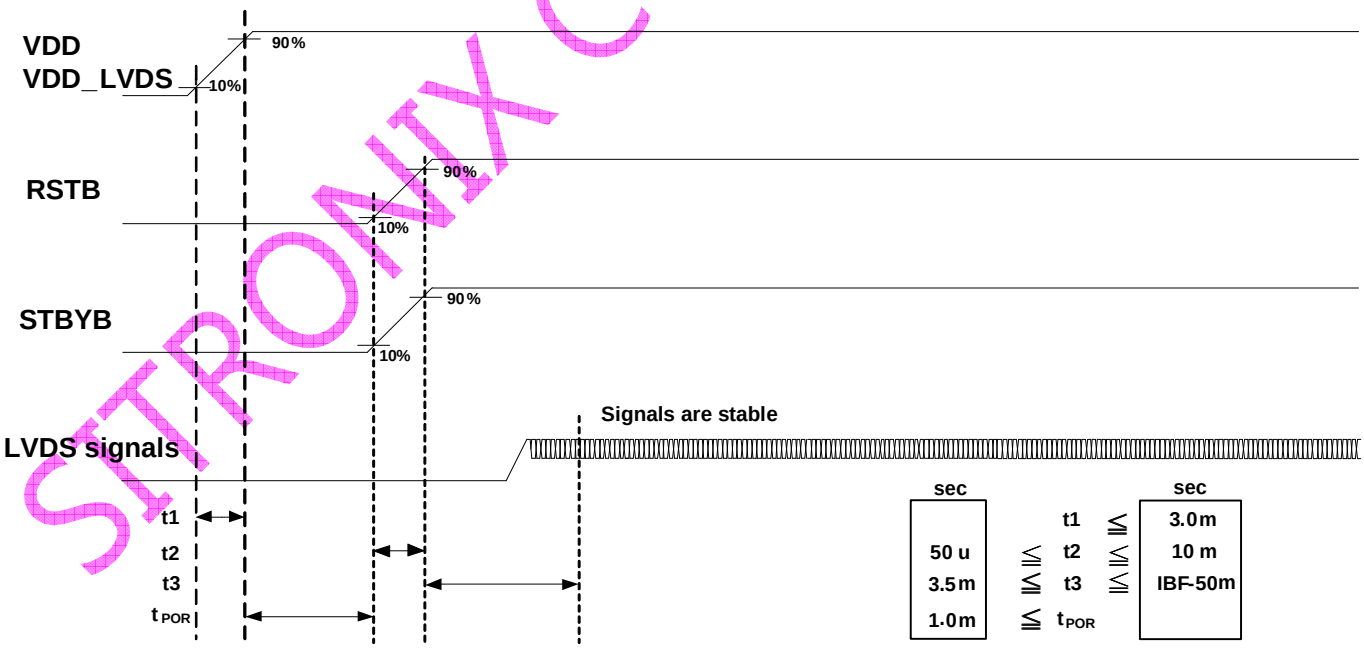
Recommend power on reset timing

We recommend connecting an external RC circuit with RSTB pin for digital circuit initial state stability.
Recommend : 47kΩ + 0.47uF or external MCU control, t_{POR} > 1ms
t_{RSTR} max. timing spec.: < 1uS (external MCU control)





The relationship between LVDS signals and RSTB / STBYB



Please keep LVDS frequency the same and do not stop LVDS signals during power on period.

Timing Characteristic

Input timing

1366x768 (RES[3:0] = 0001)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	64.3	68.6	73.7	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1366	1366	1366	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1386	1416	1446	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	40	82	t_H	$t_{VBP} + t_{VFP}$
Vertical back porch	t_{VBP}	2	2	82- t_{VFP}	t_H	
Vertical display area	t_{VD}	768	768	768	t_H	
Vertical front porch	t_{VFP}	3	38	80	t_H	
Vertical period	t_V	773	808	850	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1280x800 (RES[3:0] = 0010)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	68.4	71.9	78.1	Mhz	
Horizontal blanking time	t_{HBT}	136	144	164	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal back porch	t_{HBP}	5	5	164- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1280	1280	1280	t_{CLK}	
Horizontal front porch	t_{HFP}	131	139	159	t_{CLK}	
Horizontal period	t_H	1416	1424	1444	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	42	101	t_H	$t_{VBP} + t_{VFP}$
Vertical back porch	t_{VBP}	2	2	101- t_{VFP}	t_H	
Vertical display area	t_{VD}	800	800	800	t_H	
Vertical front porch	t_{VFP}	3	40	99	t_H	
Vertical period	t_V	805	842	901	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

800x1280 (RES[3:0] = 0011)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	63.2	68.6	76.0	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	800	800	800	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	820	850	880	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	66	161	t_H	$t_{VBP} + t_{VFP}$
Vertical back porch	t_{VBP}	2	2	161- t_{VFP}	t_H	
Vertical display area	t_{VD}	1280	1280	1280	t_H	
Vertical front porch	t_{VFP}	3	64	159	t_H	
Vertical period	t_V	1285	1346	1441	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1600x600 (RES[3:0] = 0100)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	58.8	62.6	68.6	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1600	1600	1600	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1620	1650	1680	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	32	81	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	81- t_{VFP}	t_H	
Vertical display area	t_{VD}	600	600	600	t_H	
Vertical front porch	t_{VFP}	3	30	79	t_H	
Vertical period	t_V	605	632	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1280x720 (RES[3:0] = 0101)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	61.0	64.1	69.4	Mhz	
Horizontal blanking time	t_{HBT}	122	130	164	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	164- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1280	1280	1280	t_{CLK}	
Horizontal front porch	t_{HFP}	117	125	159	t_{CLK}	
Horizontal period	t_H	1402	1410	1444	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	38	81	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	81- t_{VFP}	t_H	
Vertical display area	t_{VD}	720	720	720	t_H	
Vertical front porch	t_{VFP}	3	36	79	t_H	
Vertical period	t_V	725	758	801	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1440x540 (RES[3:0] = 0110)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	47.7	50.9	62.1	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1440	1440	1440	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1460	1490	1520	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	29	141	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	141- t_{VFP}	t_H	
Vertical display area	t_{VD}	540	540	540	t_H	
Vertical front porch	t_{VFP}	3	27	139	t_H	
Vertical period	t_V	545	569	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1024x768 (RES[3:0] = 0111)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	52.3	55.0	61.5	Mhz	
Horizontal blanking time	t_{HBT}	104	110	180	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	180- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1024	1024	1024	t_{CLK}	
Horizontal front porch	t_{HFP}	99	105	175	t_{CLK}	
Horizontal period	t_H	1128	1134	1204	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	40	83	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	83- t_{VFP}	t_H	
Vertical display area	t_{VD}	768	768	768	t_H	
Vertical front porch	t_{VFP}	3	38	81	t_H	
Vertical period	t_V	773	808	851	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1280x480 (RES[3:0] = 1000)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	37.8	40.4	55.6	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1280	1280	1280	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1300	1330	1360	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	26	201	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	201- t_{VFP}	t_H	
Vertical display area	t_{VD}	480	480	480	t_H	
Vertical front porch	t_{VFP}	3	24	199	t_H	
Vertical period	t_V	485	506	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1024x600 (RES[3:0] = 1001)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	37.9	40.7	45.1	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1024	1024	1024	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1044	1074	1104	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	32	81	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	81- t_{VFP}	t_H	
Vertical display area	t_{VD}	600	600	600	t_H	
Vertical front porch	t_{VFP}	3	30	79	t_H	
Vertical period	t_V	605	632	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

1024x480 (RES[3:0] = 1010)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	30.4	32.6	45.1	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	1024	1024	1024	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	1044	1074	1104	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	26	201	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	201- t_{VFP}	t_H	
Vertical display area	t_{VD}	480	480	480	t_H	
Vertical front porch	t_{VFP}	3	24	199	t_H	
Vertical period	t_V	485	506	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

960x540 (RES[3:0] = 1011)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	32.0	34.5	42.5	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	960	960	960	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	980	1010	1040	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	29	141	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	141- t_{VFP}	t_H	
Vertical display area	t_{VD}	540	540	540	t_H	
Vertical front porch	t_{VFP}	3	27	139	t_H	
Vertical period	t_V	545	569	681	t_H	
Vertical l pulse width	t_{VPW}	1	1	128	t_H	

800x600 (RES[3:0] = 1100)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	29.8	32.2	36.0	Mhz	
Horizontal blanking time	t_{HBT}	20	50	80	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	80- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	800	800	800	t_{CLK}	
Horizontal front porch	t_{HFP}	15	45	75	t_{CLK}	
Horizontal period	t_H	820	850	880	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	32	81	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	81- t_{VFP}	t_H	
Vertical display area	t_{VD}	600	600	600	t_H	
Vertical front porch	t_{VFP}	3	30	79	t_H	
Vertical period	t_V	605	632	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

800x480 (RES[3:0] = 1101)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	25.9	27.6	48.7	Mhz	
Horizontal blanking time	t_{HBT}	90	110	304	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	304- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	800	800	800	t_{CLK}	
Horizontal front porch	t_{HFP}	85	105	299	t_{CLK}	
Horizontal period	t_H	890	910	1104	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	26	255	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	255- t_{VFP}	t_H	
Vertical display area	t_{VD}	480	480	480	t_H	
Vertical front porch	t_{VFP}	3	24	253	t_H	
Vertical period	t_V	485	506	735	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

640x480 (RES[3:0] = 1110)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	21.2	23.4	32.9	Mhz	
Horizontal blanking time	t_{HBT}	90	130	164	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	5	5	164- t_{HFP}	t_{CLK}	
Horizontal display area	t_{HD}	640	640	640	t_{CLK}	
Horizontal front porch	t_{HFP}	85	125	159	t_{CLK}	
Horizontal period	t_H	730	770	804	t_{CLK}	
Horizontal pulse width	t_{HPW}	1	1	256	t_{CLK}	
Vertical blanking time	t_{VBT}	5	26	201	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	2	2	201- t_{VFP}	t_H	
Vertical display area	t_{VD}	480	480	480	t_H	
Vertical front porch	t_{VFP}	3	24	199	t_H	
Vertical period	t_V	485	506	681	t_H	
Vertical pulse width	t_{VPW}	1	1	128	t_H	

The 3-Wire Serial Peripheral Interface

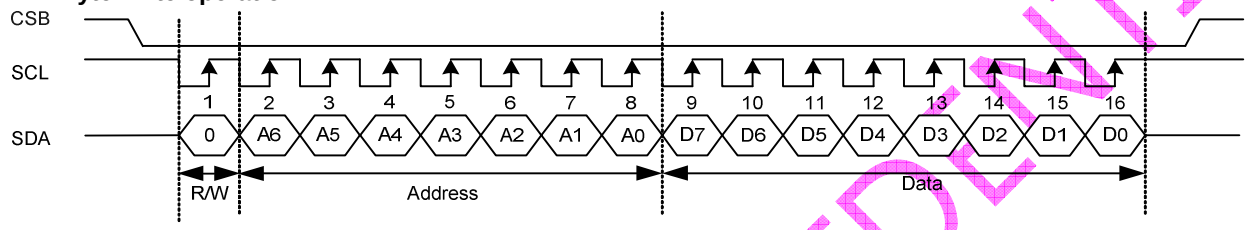
SC5004 supports serial peripheral interface (SPI) to set internal registers. SC5004 is a slave. 3-Wire communication can be bi-directional controlled by the “R/W” bit.

Under write operation, R/W bit equals to “0” and master gives address and data.

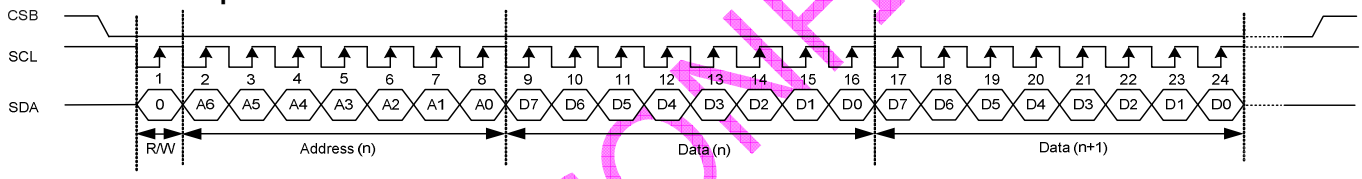
Under read operation, R/W bit equals to “1” and master gives address. SC5004 will return the data value. The returned data should be latched at the rising edge of SCL by external controller. During read operation, master should float SDA pin under “Data phase”.

SC5004 also supports burst read/write mode to saving program timing. Master only gives one time R/W and address when burst mode. Then SC5004 will auto increase address to read/write internal register.

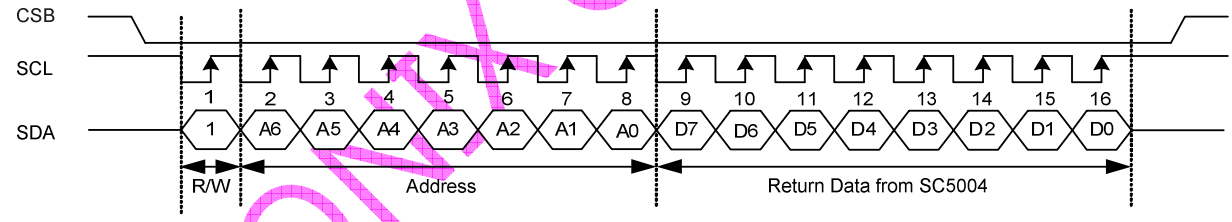
Byte write operation



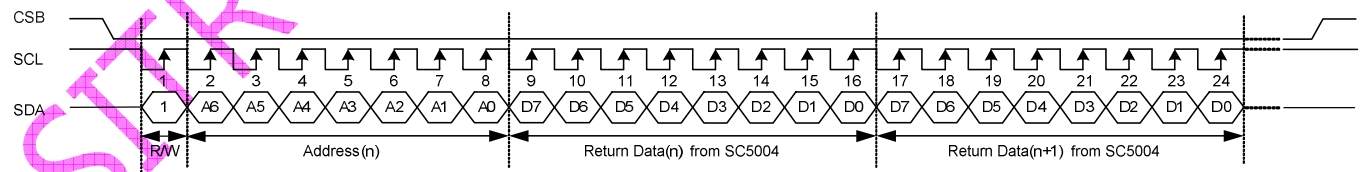
Burst write operation



Byte read operation



Burst read operation



The 2-Wire Serial Interface (I²C)

SC5004 supports 2-Wire Serial Interface (I²C) to set internal registers. SC5004 is a slave and the slave address is fixed to 0111000.

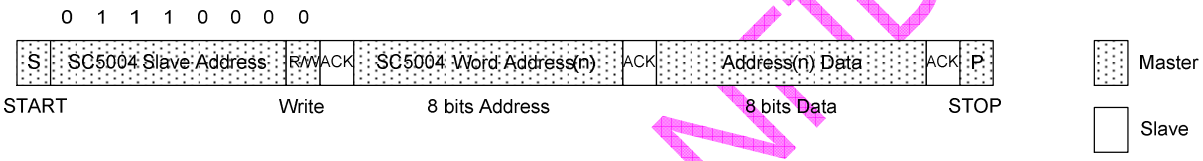
Byte write: Master gives START condition, SC5004 slave address 7bits (0111000) and R/W=0 bit to inform SC5004 that master want to do write operation. SC5004 reply the first acknowledgement. Then master gives 8 bits address data to select which internal register. SC5004 reply the second acknowledgement if the register address is valid. Master goes to give 8 bits data for the internal register value. SC5004 reply the third acknowledgement. Master gives STOP condition at last.

Burst write: As Byte write, master gives more 8 bits data value. SC5004 will auto increase address to save data into internal register.

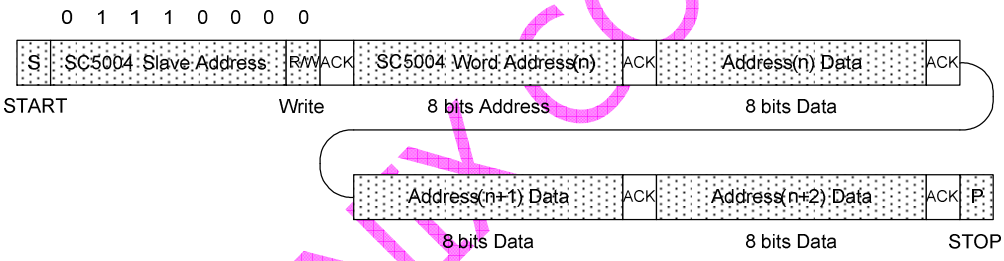
Byte read: Master gives start condition, SC5004 slave address 7bits (0111000) and R/W=0 bit to inform SC5004 that master want to do write operation. SC5004 reply the first acknowledgement. Then master gives 8 bits address data to select which internal register. SC5004 reply the second acknowledgement if the register address is valid. Then without STOP condition, master gives another START condition, SC5004 slave address 7bits (0111000) and R/W=1 bit to inform SC5004 that master want to do read operation. SC5004 reply the third acknowledgement and 8 bits data of internal register value. Master reply the no acknowledgement of read data. Then STOP condition.

Burst read: When master receives data from SC5004 and give an acknowledgement, SC5004 will go to reply data until SC5004 receives no acknowledgement.

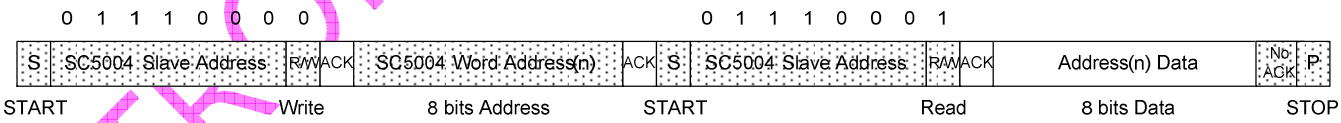
Byte write



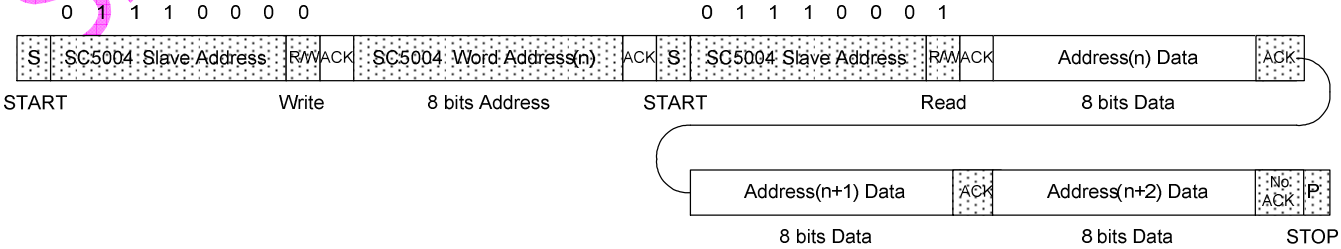
Burst write



Byte read



Burst read



Note : SC5004 8 bits word address MSB will be ignored, no matter 0 or 1.

SC5004 supports SPI/I²C interface to program internal register. It also supports download EEPROM value to internal register with I²C interface.

SPI/I²C/EEPROM related hardware(HW) and software(SW) settings

Hardware setting:

SPI_I2C: SPI or I2C serial interface selection, H=SPI, L=I²C
CID[1:0]: SC5004 chip ID settings
CSB: chip select pin of SPI interface input
SCL: serial clock input/output
SDA: serial data input/output
EEP_EN: EEPROM enable
ROM_RLB: SC5004 periodicities reload EEPROM or MTP data (0.5 second)

Software setting:

WALL: write all chips
AID : Active ID

SC5004 supports external 1K bits EEPROM (ex. SII S24CS01A).

A[2:0]: SII S24CS01A EEPROM address input, must fix to **110**

8-Pin SOP(JEDEC)
Top view

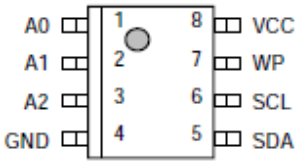


Figure 1

S-24CS01AFJ-TBH-U
S-24CS02AFJ-TBH-U
S-24CS04AFJ-TBH-U

Table 1

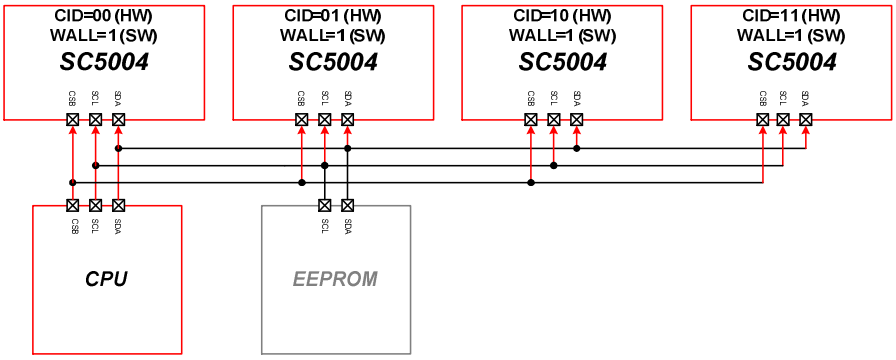
Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*1)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protect input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

*1. Connect to GND or V_{CC}.

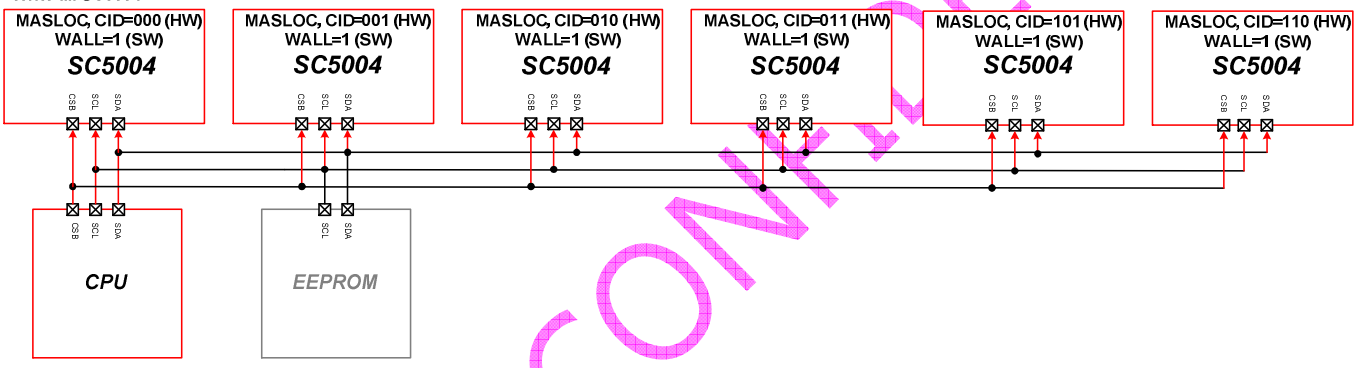
Note : Maximum cascade SC5004 chips are 4

SPI/I²C/EEPROM usage guide as below figures

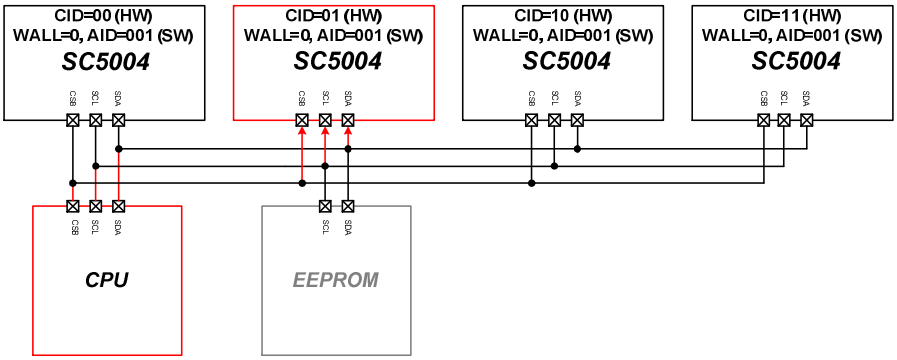
Tcon Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Write all SC5004



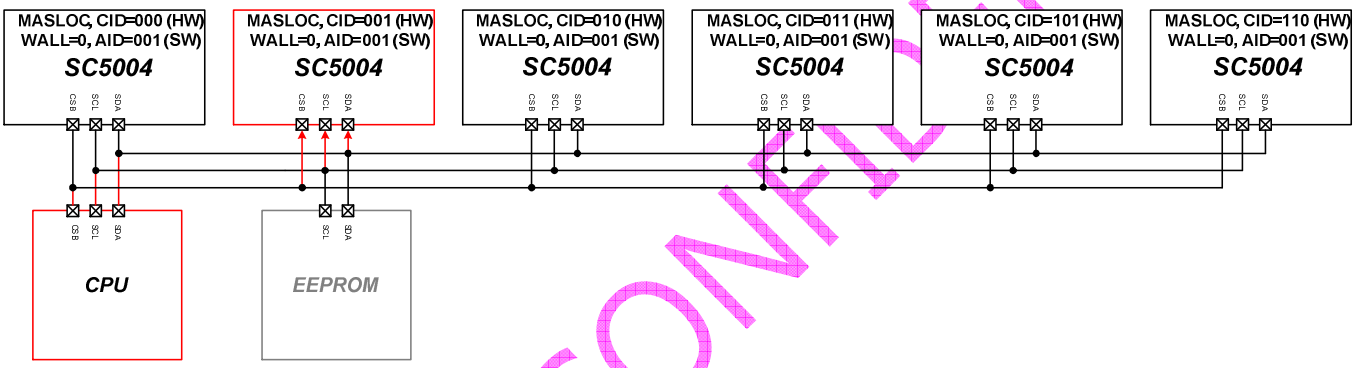
Source Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Write all SC5004



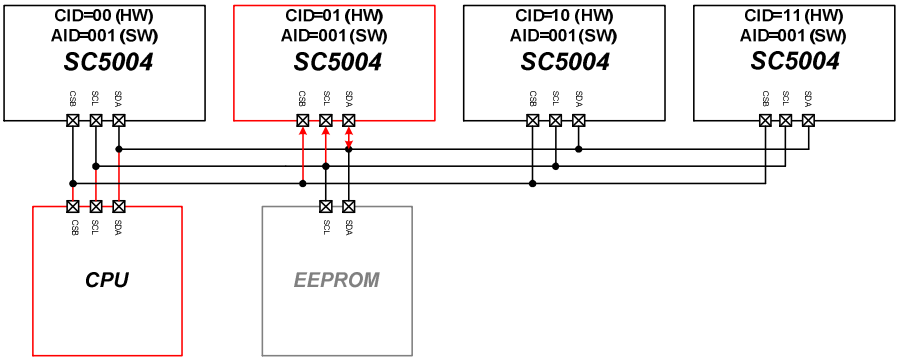
Tcon Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Write one SC5004



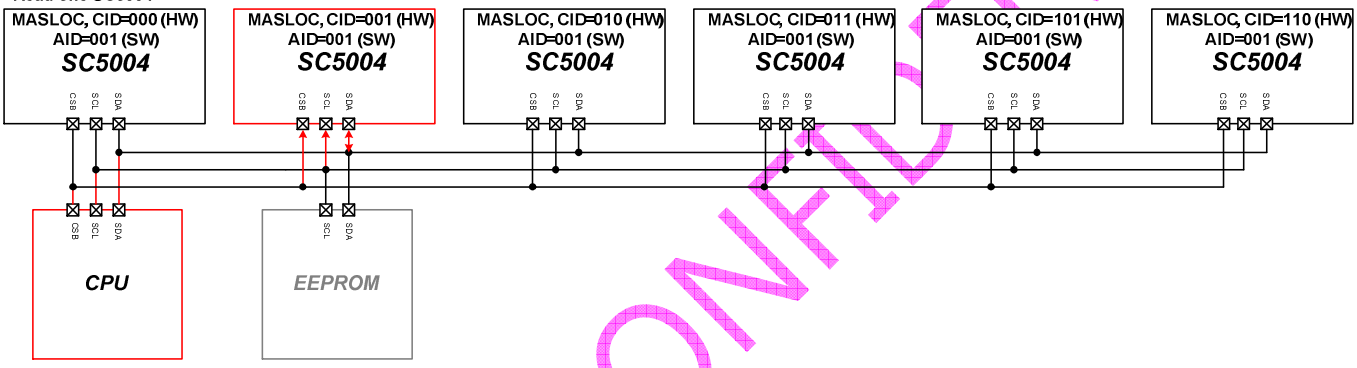
Source Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Write one SC5004



Tcon Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Read one SC5004

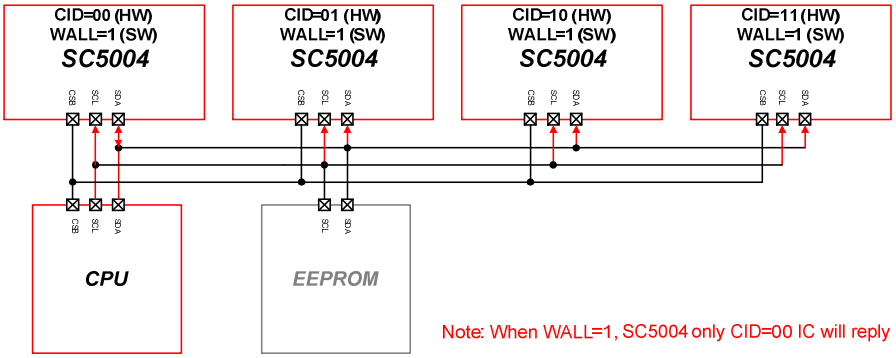


Source Mode:
SPI_I2C=1, CPU program SC5004 with SPI
Read one SC5004



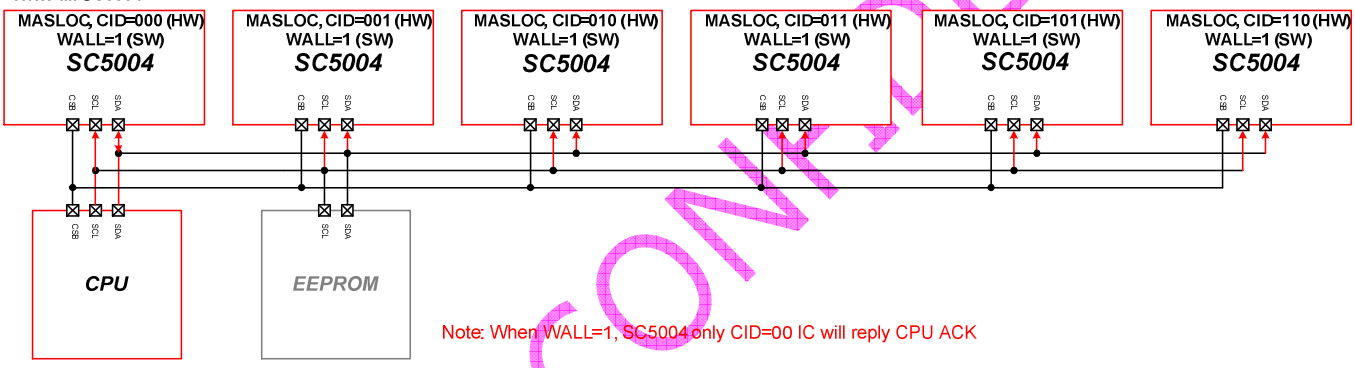
SPI/I²C/EEPROM usage guide as below figures

Tcon Mode:
SPI_I2C=0, CPU program SC5004 with I²C
Write all SC5004



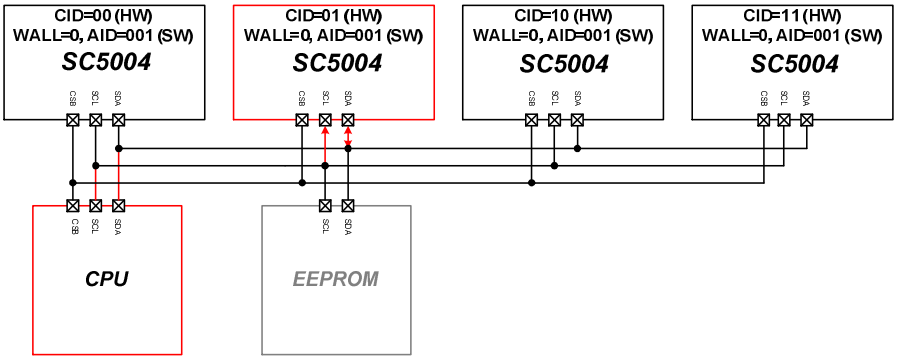
Note: When WALL=1, SC5004 only CID=00 IC will reply CPU ACK

Source Mode:
SPI_I2C=0, CPU program SC5004 with I²C
Write all SC5004

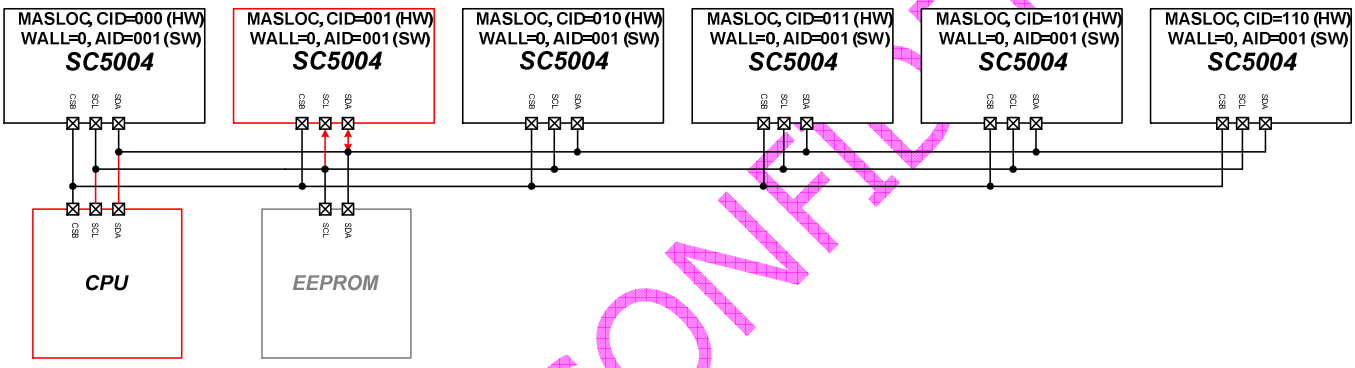


Note: When WALL=1, SC5004 only CID=00 IC will reply CPU ACK

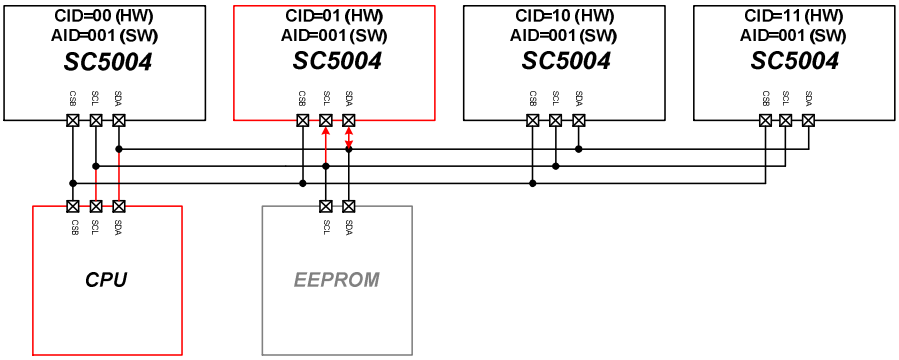
Tcon Mode:
SPI_I2C=0,CPU program SC5004 with I²C
Write one SC5004



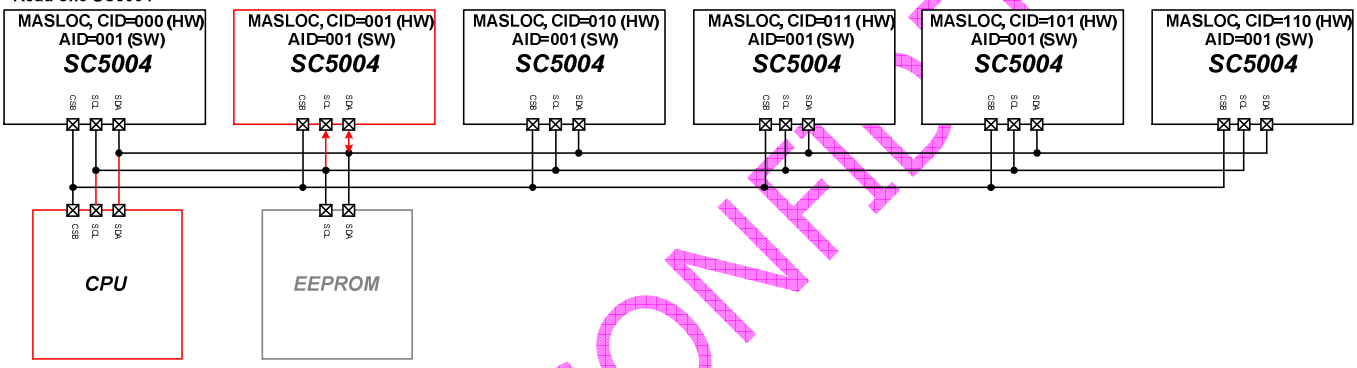
Source Mode:
SPI_I2C=0,CPU program SC5004 with I²C
Write one SC5004



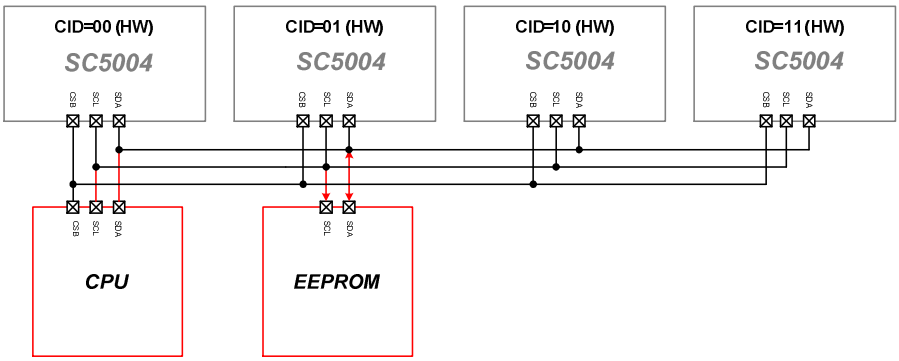
Tcon Mode:
SPI_I2C=0, CPU program SC5004 with I²C
Read one SC5004



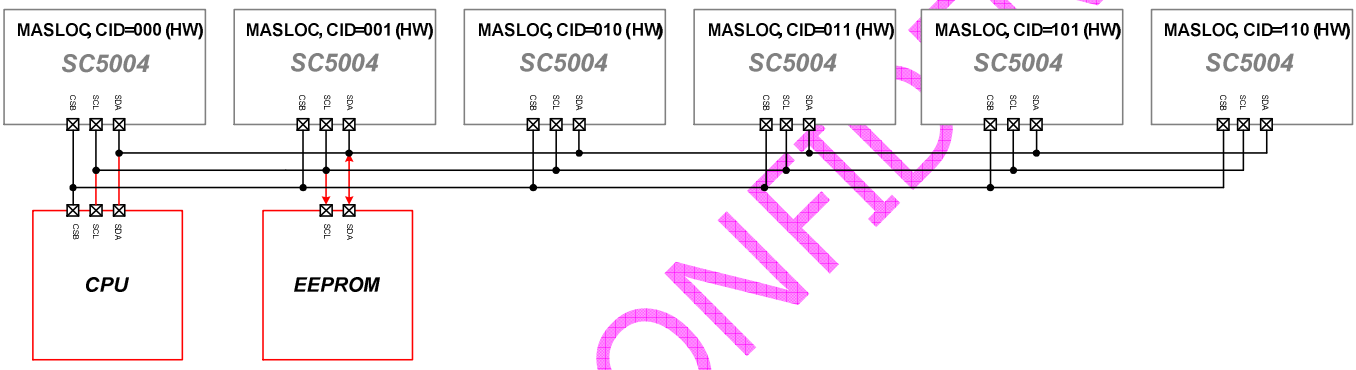
Source Mode:
SPI_I2C=0, CPU program SC5004 with I²C
Read one SC5004



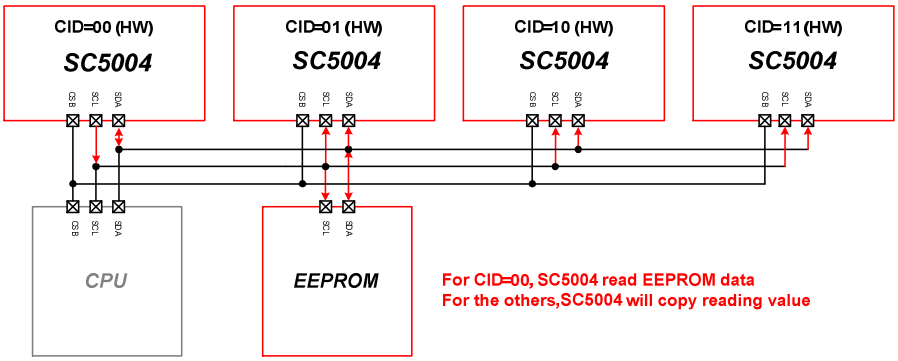
Tcon Mode:
CPU program EEPROM



Source Mode:
CPU program EEPROM

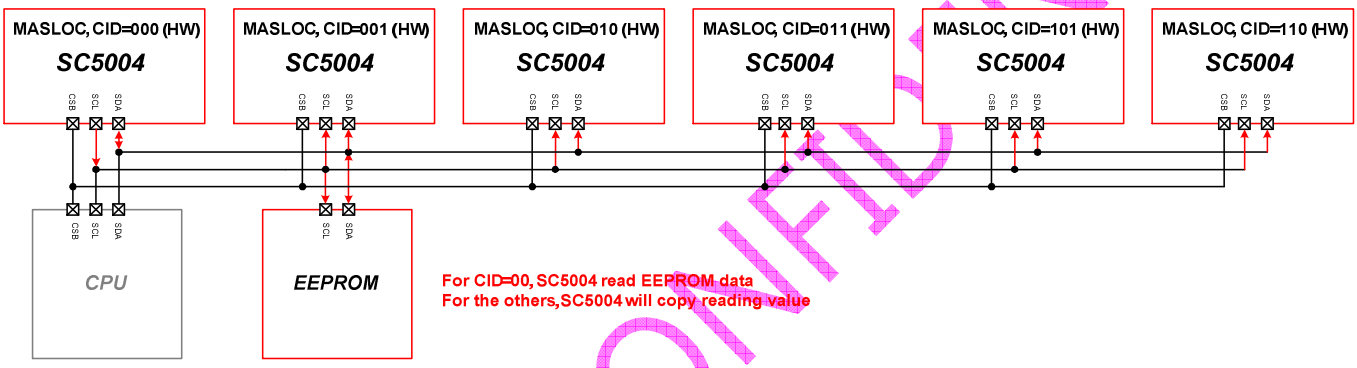


Tcon Mode:
SC5004 read EEPROM



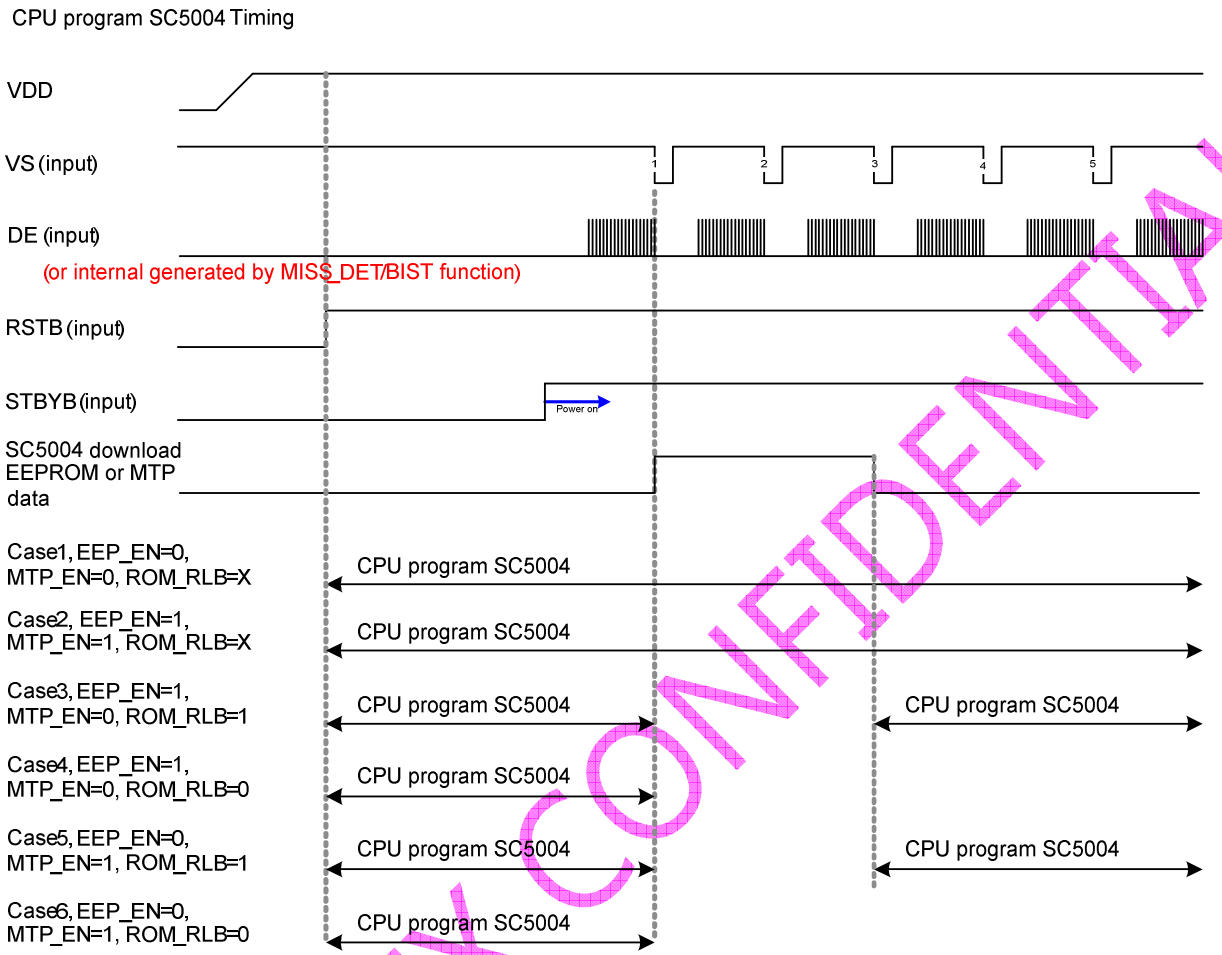
For CID=00, SC5004 read EEPROM data
For the others,SC5004 will copy reading value

Source Mode:
SC5004 read EEPROM

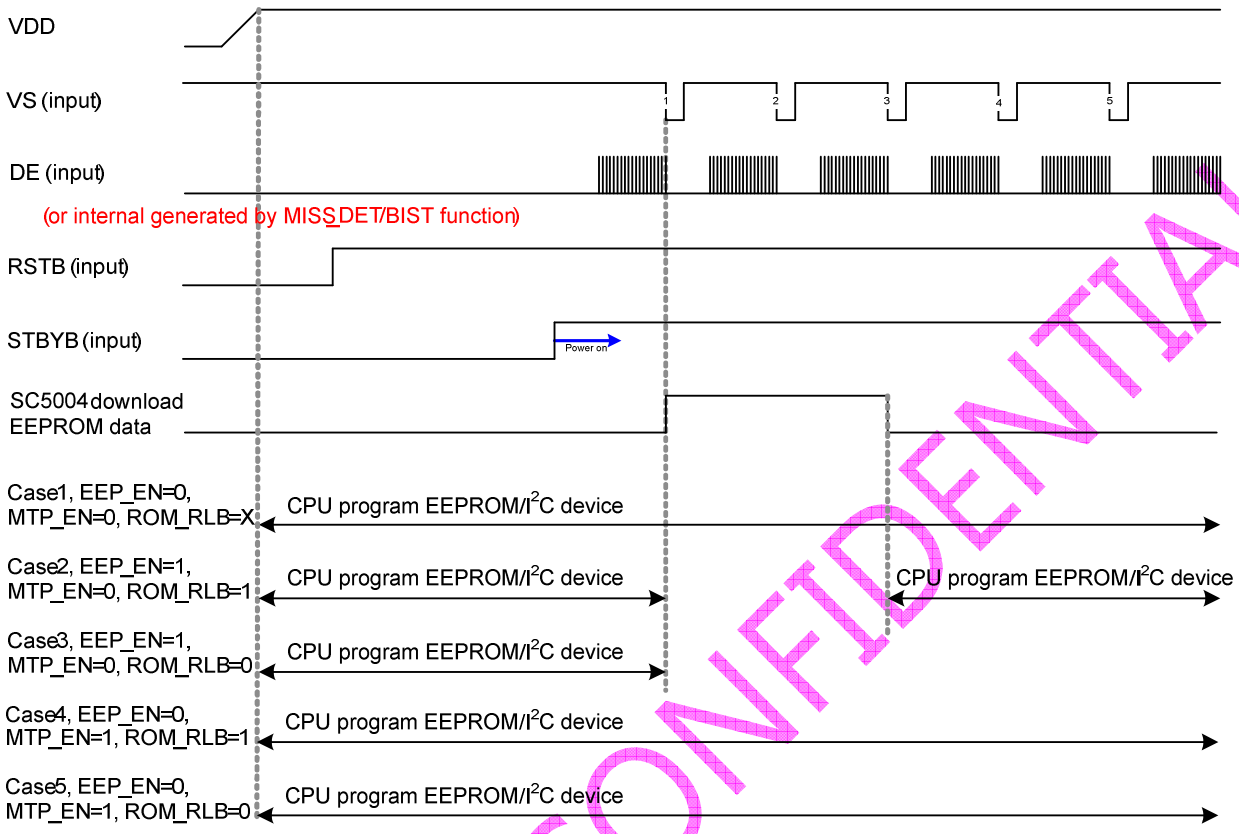


For CID=00, SC5004 read EEPROM data
For the others,SC5004 will copy reading value

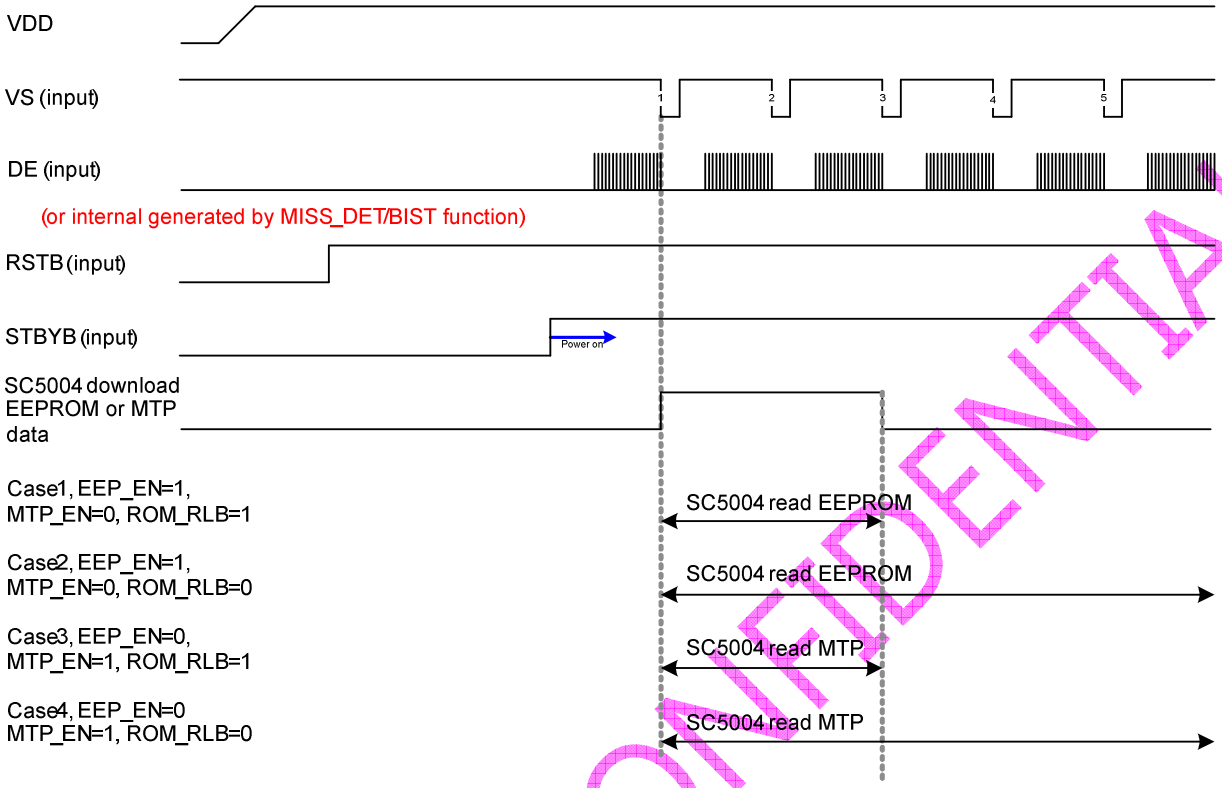
SPI/I²C/EEPROM operation sequence as below figure



CPU program EEPROM/I²C device Timing



SC5004 read EEPROM or MTP



Register List

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
00					WALL	AID[2]	AID[1]	AID[0]
					1	0	0	0

WALL: SPI/I^{2}C write all chips. 1 : enable, 0 : disable

AID[2:0]: Active ID

TCON mode：

When WALL=0, SPI/I^{2}C write/read depends on CID[1:0] and AID[2:0].

AID[1:0]=000：Write/Read CID=00 chip.

AID[1:0]=001：Write/Read CID=01 chip.

AID[1:0]=010：Write/Read CID=10 chip.

AID[1:0]=011：Write/Read CID=11 chip.

SD mode：

When WALL=0, SPI/I^{2}C write/read depends on MASLOC, CID[1:0] and AID[2:0].

AID[2:0]=000：Write/Read {MASLOC, CID} =000 chip.

AID[2:0]=001：Write/Read {MASLOC, CID} =001 chip.

AID[2:0]=010：Write/Read {MASLOC, CID} =010 chip.

AID[2:0]=011：Write/Read {MASLOC, CID} =011 chip.

AID[2:0]=100：Inhibition

AID[2:0]=101：Write/Read {MASLOC, CID} =101 chip.

AID[2:0]=110：Write/Read {MASLOC, CID} =110 chip.

AID[2:0]=111：Inhibition

Note: MASLOC act as CID[2] pin in SD mode

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
01	MISS_DET	BIST	LR	UD	STBYB	RSTB	CLK_POL	MODE
	1	0	1	0	1	1	0	1

MISS_DET: Signal missing detection mode. (only effective in TCON mode) 1: Enable, 0: Disable

BIST: BIST mode.

1: Enable (Pattern depends on BIST_PAT[3:0] setting)

0: Disable

LR: Source driver Left/Right scan sequence

0: Shift left, Last data=S1<-S2<-S3….<-S1284=First data

1: Shift right, First data=S1->S2->S3….->S1284=Last data (default)

UD: Gate UP or Down scan selection

0: STV2 output vertical start pulse and UD pin output logical “0” to Gate driver (default)

1: STV1 output vertical start pulse and UD pin output logical “1” to Gate driver

STBYB: Standby mode. 1: normal mode, 0 : standby mode.

RSTB: Global reset. 1: normal, 0: reset (Reading from EEPROM or MTP, this bit will be skipping)

CLK_POL: Clock polarity (TCON CMOS interface mode only)

1: latch data at clock rising edge.

0: latch data at clock falling edge.

MODE: DE or SYNC mode. 1: DE mode, 0: SYNC mode

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
02	P_ON	P_OFF	NBW	PON_SKIP	RES[3]	RES[2]	RES[1]	RES[0]
	0	0	0	1	1	1	0	1

P_ON: Power on pattern. 1: black, 0: white

P_OFF: Power off pattern. 1: black, 0: white

NBW: Panel type. 1: normally black, 0: normally white

PON_SKIP: PON pattern skip function. 1: skip, 0: display pattern depend on P_ON bit or PON_STV pin setting (Refer to Page.59, 61)

RES[3:0]: Resolution. See “resolution and interface selection table”

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
03	MLSB	BGR	JEIDA	BIT6	INV[1]	INV[0]	LR_INV	UD_INV
	0	0	0	0	0	0	0	0

MLSB: MSB to LSB sequence reverse control. 1: reverse, 0: normal. (refer to P.12)

BGR: Input data RGB to BGR mapping control. 1: BGR, 0: RGB.

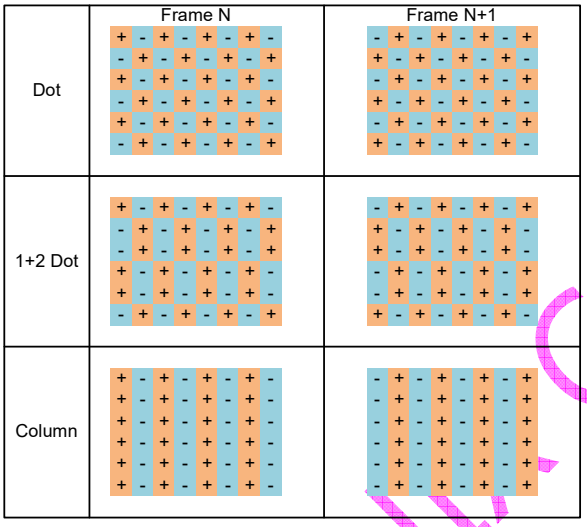
JEIDA: LVDS data format. 1: JEIDA, 0: VESA

BIT6: Input data format selection. 1:6-bit mode, 0:8-bit mode

INV[1:0]: Inversion selection. 00: dot, 01: 1+2dot, 1x: column

LR_INV: LR inverse. 0: normal, 1: inverse

UD_INV: UD inverse. 0: normal, 1: inverse



Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
04	OH_PD	XON_EN	PWM_EN	LDO_EN	VBUF_EN	OVP_EN	VB_TYPE	RESERVE
	0	0	0	0	0	0	0	0

OH_PD : Over heat power down. 1: enable (power down master IC DC-DC), 0: disable (DIMO + BKL_DUTY[1:0])

XON_EN : Gate driver XON control. 1: enable (follow SC5004 power off sequence), 0: disable

PWM_EN: VDDA booster control. 1: Enable, 0: Disable

LDO_EN: RVDDA regulator control. 1: Enable, 0: Disable

VBUF_EN: Voltage buffer control. 1: Enable, 0: Disable

OVP_EN: Over voltage protection. 1: Enable, 0: Disable

VB_TYPE: Voltage buffer type. 1: analog, 0: digital

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
05	FB_SEL[1]	CKVRP[2]	CKVRP[1]	CKVRP[0]	FB_SEL[0]	CKVFP[2]	CKVFP[1]	CKVFP[0]
	0	1	0	0	0	1	1	0

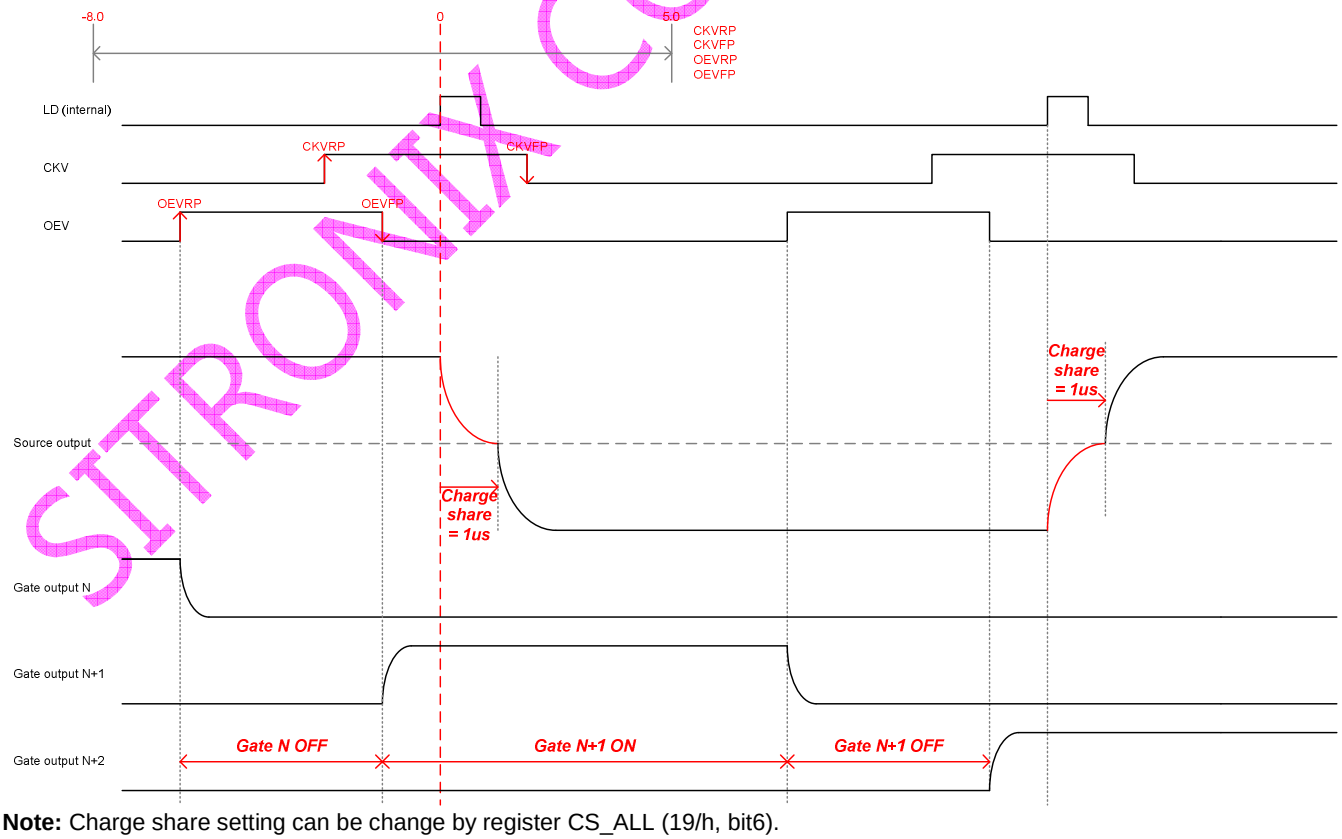
FB_SEL[1:0] : DFB pin feedback signal selection.

CKVRP[2:0] : Gate clock CKV rising position timing control.

CKVRP[2:0]	Time [uS]
000	-5.5
001	-4.5
010	-3.5
011	-2.5
100	-1.5(default)
101	-0.5
110	-0.5
111	-0.5

CKVFP[2:0] : Gate clock CKV falling position timing control.

CKVFP[2:0]	Time [uS]
000	-2
001	-1
010	0
011	1
100	2
101	3
110	4(default)
111	5



Note: Charge share setting can be change by register CS_ALL (19/h, bit6).

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
06	OEVRP[3]	OEVRP[2]	OEVRP[1]	OEVRP[0]	OEVFP[3]	OEVFP[2]	OEVFP[1]	OEVFP[0]
	1	1	0	0	0	1	1	1

OEVRP[3:0]: Gate OEV rising position control

OEVRP[3:0]	Time [uS]
0000	-8
0001	-7.5
0010	-7
0011	-6.5
0100	-6
0101	-5.5
0110	-5
0111	-4.5
1000	-4
1001	-3.5
1010	-3
1011	-2.5
1100	-2(default)
1101	-1.5
1110	-1
1111	-0.5

OEVFP[3:0]: Gate OEV falling position control

OEVFP[3:0]	Time [uS]
0000	-5
0001	-4
0010	-3
0011	-2
0100	2
0101	3
0110	4
0111	5(default)
1000	-5.5
1001	-4.5
1010	-3.5
1011	-2.5
1100	2.5
1101	3.5
1110	4.5
1111	5.5

Note :

1. CKVRP,CKVFP,OEVRP,OEVFP timing base is 0.5 or 1.0us @ 60hz frame rate condition, this varies with different frame rate.
2. Typical charge share timing in TCON mode is 1us and varies with different frame rate.

<<Example>>

Frame rate +10%, than 1uS will be -10% → 0.9uS
Frame rate -10%, than 1uS will be +10% → 1.1uS

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
07	GCPH_EN	GCPL_EN	GCPH_X3	CPH[4]	CPH[3]	CPH[2]	CPH[1]	CPH[0]
	0	0	1	1	0	0	0	1

GCPH_EN: VGH charge pump enable control. 1: Enable, 0: Disable

GCPL_EN: VGL charge pump enable control. 1: Enable, 0: Disable

GCPH_X3: VGH charge pump maximun rating control. 1 : VDDAx3, 0 : VDDAx2

CPH[4:0] : VGH voltage setting

CPH[3:0]	VGH voltage
00000	14.5V
00001	15.0V
00010	15.5V
00011	16.0V
00100	16.5V
00101	17.0V
00110	17.5V
00111	18.0V
01000	18.5V
01001	19.0V
01010	19.5V
01011	20.0V
01100	20.5V
01101	21.0V
01110	21.5V
01111	22.0V
10000	22.5V
10001	23.0V (default)
10010	23.5V
10011	24.0V
10100	24.5V
10101	25.0V
10110	25.5V
10111	26.0V
11000	26.5V
11001	27.0V
11010	27.5V
11011	28.0V
11100	28.5V
11101	29.0V
11110	29.5V
11111	30.0V

Note : Charge pump generating VGH/VGL voltage accuracy ≦+/-200mV

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
08	CPL[3]	CPL[2]	CPL[1]	CPL[0]		VSEL[2]	VSEL[1]	VSEL[0]
	1	0	0	0		0	1	0

CPL[3:0]: VGL voltage setting

CPL[3:0]	VGL voltage
0000	-3.0V
0001	-3.5V
0010	-4.0V
0011	-4.5V
0100	-5.0V
0101	-5.5V
0110	-6.0V
0111	-6.5V
1000	-7.0V (default)
1001	-7.5V
1010	-8.0V
1011	-8.5V
1100	-9.0V
1101	-9.5V
1110	-10.0V
1111	-10.5V

Note : Charge pump generating VGH/VGL voltage accuracy ≤+/-200mV

VSEL[2:0]: Vcom voltage selection

VSEL[2:0]	Vcom voltage
000	3.5
001	4
010	4.5 (default)
011	5
100	5.5
101	6
110	6.5
111	7

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
09			RV[5]	RV[4]	RV[3]	RV[2]	RV[1]	RV[0]
			1	0	0	0	0	1

RV[4:0]: RVDDA voltage selection

RV[5:0]	RVDDA voltage
000000	7.1
000001	7.2
000010	7.3
000011	7.4
000100	7.5
000101	7.6
000110	7.7
000111	7.8
001000	7.9
001001	8.0
001010	8.1
001011	8.2
001100	8.3
001101	8.4
001110	8.5
001111	8.6
010000	8.7
010001	8.8
010010	8.9
010011	9.0
010100	9.1
010101	9.2
010110	9.3
010111	9.4
011000	9.5
011001	9.6
011010	9.7
011011	9.8
011100	9.9
011101	10.0
011110	10.1
011111	10.2

RV[5:0]	RVDDA voltage
100000	10.3
100001	10.4 (default)
100010	10.5
100011	10.6
100100	10.7
100101	10.8
100110	10.9
100111	11.0
101000	11.1
101001	11.2
101010	11.3
101011	11.4
101100	11.5
101101	11.6
101110	11.7
101111	11.8
110000	11.9
110001	12.0
110010	12.1
110011	12.2
110100	12.3
110101	12.4
110110	12.5
110111	12.6
111000	12.7
111001	12.8
111010	12.9
111011	13.0
111100	13.1 (*)
111101	13.2 (*)
111110	13.3 (*)
111111	13.4 (*)

Note :

1. RVDDA LDO regulator operation range limitation is VDDA-2.5 ≦ RVDDA ≦ VDDA-0.5V (Max. = 13.0V)
2. (*) 13.1~13.4 voltage range can't be guaranteed.

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0A		VUPDN[6]	VUPDN[5]	VUPDN[4]	VUPDN[3]	VUPDN[2]	VUPDN[1]	VUPDN[0]
		1	0	0	0	0	0	0

VUPDN[6:0]: Vcom voltage fine tune (up/down)

VUPDN[6:0]	Vcom voltage
0000000	-320mv
0000001	-315mv
0000010	-310mv
|	|
0111111	-5mv
1000000	0 (default)
1000001	+5mv
|	|
1111101	+305mv
1111110	+310mv
1111111	+315mv

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0B	DE_POL	VS_POL	HS_POL	TS_EN	LTC_EN	GAMMA	HEATER_EN	OHP_EN
	0	0	0	0	0	0	0	0

DE_POL: DE input signal polarity inverse control. 1 : inverse, 0 : normal

VS_POL: VS input signal polarity inverse control. 1 : inverse, 0 : normal

HS_POL: HS input signal polarity inverse control. 1 : inverse, 0 : normal

TS_EN: Internal temperature sensor control. 1 : enable, 0 : disable

LTC_EN: Low temperature compensation function. 1 : enable, 0 : disable

GAMMA: Gamma curve selection :
0: Display with Gamma set A
1: Display with Gamma set B
When low temperature compensation activated, GAMMA will switch A and B automatically and don't care this bit setting.

HEATER_EN: Heater flag output enable control. 1 : enable, 0 : disable

OHP_EN: Over heat protection

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0C	LT_VSEL[2]	LT_VSEL [1]	LT_VSEL [0]	LT_CPH[4]	LT_CPH[3]	LT_CPH[2]	LT_CPH[1]	LT_CPH[0]
	0	1	0	1	0	0	0	1

LT_VSEL[2:0]: Low temperature Vcom voltage selection

LT_VSEL[2:0]	Vcom voltage
000	3.5
001	4
010	4.5 (default)
011	5
100	5.5
101	6
110	6.5
111	7

LT_CPH[4:0]: Low temperature VGH voltage setting

LT_CPH[4:0]	VGH voltage
00000	14.5V
00001	15.0V
00010	15.5V
00011	16.0V
00100	16.5V
00101	17.0V
00110	17.5V
00111	18.0V
01000	18.5V
01001	19.0V
01010	19.5V
01011	20.0V
01100	20.5V
01101	21.0V
01110	21.5V
01111	22.0V
10000	22.5V
10001	23.0V (default)
10010	23.5V
10011	24.0V
10100	24.5V
10101	25.0V
10110	25.5V
10111	26.0V
11000	26.5V
11001	27.0V
11010	27.5V
11011	28.0V
11100	28.5V
11101	29.0V
11110	29.5V
11111	30.0V

Note : Charge pump generating VGH/VGL voltage accuracy ≦+/-200mV

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0D			LT_RV[5]	LT_RV[4]	LT_RV[3]	LT_RV[2]	LT_RV[1]	LT_RV[0]
			1	0	0	0	0	1

LT_RV[5:0]: Low temperature RVDDA voltage selection

LT_RV[5:0]	RVDDA voltage
000000	7.1
000001	7.2
000010	7.3
000011	7.4
000100	7.5
000101	7.6
000110	7.7
000111	7.8
001000	7.9
001001	8.0
001010	8.1
001011	8.2
001100	8.3
001101	8.4
001110	8.5
001111	8.6
010000	8.7
010001	8.8
010010	8.9
010011	9.0
010100	9.1
010101	9.2
010110	9.3
010111	9.4
011000	9.5
011001	9.6
011010	9.7
011011	9.8
011100	9.9
011101	10.0
011110	10.1
011111	10.2

LT_RV[5:0]	RVDDA voltage
100000	10.3
100001	10.4 (default)
100010	10.5
100011	10.6
100100	10.7
100101	10.8
100110	10.9
100111	11.0
101000	11.1
101001	11.2
101010	11.3
101011	11.4
101100	11.5
101101	11.6
101110	11.7
101111	11.8
110000	11.9
110001	12.0
110010	12.1
110011	12.2
110100	12.3
110101	12.4
110110	12.5
110111	12.6
111000	12.7
111001	12.8
111010	12.9
111011	13.0
111100	13.1
111101	13.2
111110	13.3
111111	13.4

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0E	IBF10F	LT_VUPDN [6]	LT_VUPDN [5]	LT_VUPDN [4]	LT_VUPDN [3]	LT_VUPDN [2]	LT_VUPDN [1]	LT_VUPDN[0]
	1	1	0	0	0	0	0	0

IBF10F: Power on internal frame numbers:

IB10F	IB79F	Frame
0	0	3
0	1	79
1	0	10
1	1	79

LT_VUPDN[6:0]: Low temperature Vcom voltage fine tune (up/down)

LT_VUPDN[6:0]	Vcom voltage
0000000	-320mv
0000001	-315mv
0000010	-310mv
|	|
0111111	-5mv
1000000	0 (default)
1000001	+5mv
|	|
1111101	+305mv
1111110	+310mv
1111111	+315mv

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0F	LT_CPL[3]	LT_CPL[2]	LT_CPL[1]	LT_CPL[0]	TRES[1]	TRES[0]	BKL_DUTY[1]	BKL_DUTY[0]
	1	0	0	0	0	0	0	1

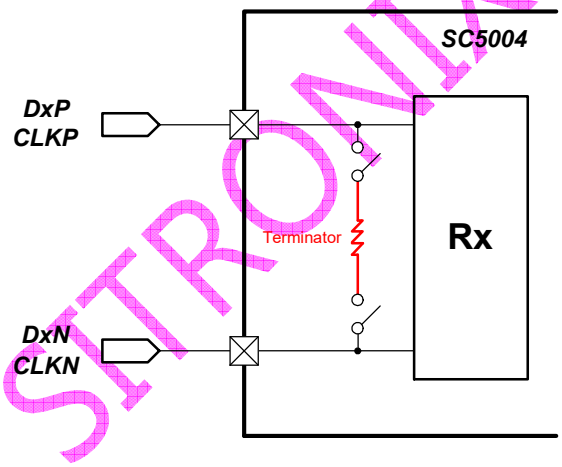
LT_CPL[3:0]: Low temperature VGL voltage setting

LT_CPL[3:0]	VGL voltage
0000	-3.0V
0001	-3.5V
0010	-4.0V
0011	-4.5V
0100	-5.0V
0101	-5.5V
0110	-6.0V
0111	-6.5V
1000	-7.0V (default)
1001	-7.5V
1010	-8.0V
1011	-8.5V
1100	-9.0V
1101	-9.5V
1110	-10.0V
1111	-10.5V

Note: Charge pump generating VGH/VGL voltage accuracy ≦+/-200mV

TRES[1:0] : Termination resistor setting for LVDS, RSDS and mini-LVDS differential input D0[7:0], D1[7:0], D2[7:0], CLKP and CLKN .

TRES[1:0]	Resistance
00	Open (default)
01	200 Ω
10	200 Ω
11	100 Ω



BKL_DUTY[1:0] : LED backlight enable duty cycle setting

BKL_DUTY[1:0]	Enable duty cycle
00	12.5%
01	25% (default)
10	50%
11	100%

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
10	IBF79F	LT_FR_EN	F_RATE[1]	F_RATE[0]	BIST_PAT[3]	BIST_PAT[2]	BIST_PAT[1]	BIST_PAT[0]
	0	0	0	0	1	1	1	1

IBF79F: Power on internal frame numbers:

IB10F	IB79F	Frame
0	0	3
0	1	79
1	0	10
1	1	79

LT_FR_EN : Low temperature frame reduction enable control :
1 : Enable
0 : Disable (default)

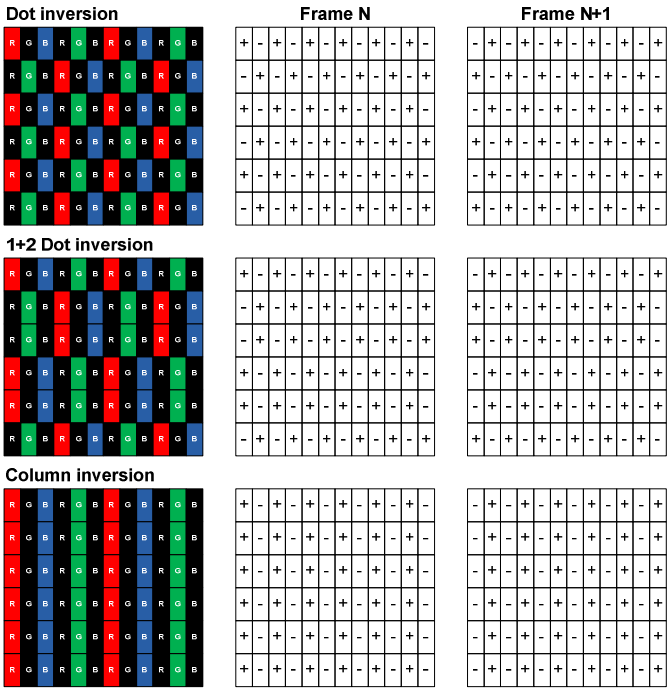
F_RATE[1:0] : Frame rate reduction speed setting

F_RATE[1:0]	Frame rate speed
00	1/2 (default)
01	1/3
10	1/4
11	1/8

BIST_PAT[3:0]:

BIST_PAT[3:0]	pattern
0000	Black
0001	Red
0010	Green
0011	Blue
0100	White
0101	Flicker
0110	Border
0111	Gray
1000	8 color bar
Other	Auto run

Note: flicker pattern depends on inversion type setting (INV[1:0])



Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
11		CPF[2]	CPF[1]	CPF[0]	MASK_GATE	PWMF[2]	PWMF[1]	PWMF[0]
		0	1	1	0	1	0	0

CPF[2:0]: SC5005 Gate driver charge pump clock frequency adjustment

CPF[2:0]	Clock frequency
000	300khz
001	330khz
010	375khz
011	500khz (default)
100	625khz
101	750khz
110	875khz
111	950khz

MASK_GATE: If there are some input noise let TCON unstable, TCON suspend Gate driver control signals or not.
1: Enable
0: Disable (default)

PWMF[2:0]: SC5004 VDDA PWM booster clock frequency adjustment

PWMF[2:0]	Clock frequency
000	180 khz
001	360 khz
010	540 khz
011	720 khz
100	900 khz (default)
101	1080 khz
110	1260 khz
111	1440 khz

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
12	PROGV[7]	PROGV[6]	PROGV[5]	PROGV[4]	PROGV[3]	PROGV[2]	PROGV[1]	PROGV[0]
	0	1	0	1	0	1	1	0
13	PROGH[7]	PROGH[6]	PROGH[5]	PROGH[4]	PROGH[3]	PROGH[2]	PROGH[1]	PROGH[0]
	1	1	1	0	0	0	0	0
14		PROGH[10]	PROGH9]	PROGH[8]		PROGV[10]	PROGV[9]	PROGV[8]
		0	0	1		0	1	1

PROGV[10:0]: Vertical resolution of programmable mode. V range is 1~1280.

PROGH[10:0]: Horizontal resolution of programmable mode. H range is 1~1712.

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
15	MPORCH							HBP[8]
	0							0
16	HBP[7]	HBP[6]	HBP[5]	HBP[4]	HBP[3]	HBP[2]	HBP[1]	HBP[0]
	0	0	0	0	0	1	0	1
17	VBP[7]	VBP[6]	VBP[5]	VBP[4]	VBP[3]	VBP[2]	VBP[1]	VBP[0]
	0	0	0	0	0	0	1	0

MPORCH: Manual setting back porch for SYNC mode. If t_{VBP} is not equal to the typical value 2 or t_{HBP} is not equal to the typical value 5 in the timing characteristic, need to set MPORCH to 1. And set the VBP[7:0] and HBP[8:0] to the correct value.
VBP[7:0]: Vertical back porch setting. Range is 2~255.
HBP[8:0]: Horizontal back porch setting. Range is 5~511.

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
18	VB_ACT	VB_DATA	TEMP1[5]	TEMP1[4]	TEMP1[3]	TEMP1[2]	TEMP1[1]	TEMP1[0]
	0	0	0	0	0	0	1	1

VB_ACT: V blanking period SO[1:1284] continuous active driving and change output polarity.
1: Enable
0: Disable (default)

VB_DATA: V blanking period SO[1:1284] output data code selection.
1: FF/h
0: 00/h (default)

Note: V blanking period display color reference table

NBW	VB_DATA	Color
0	0	Black
0	1	White
1	0	White
1	1	Black

TEMP1[5:0]: initial temperature setting (-28~-25 ^{O}C)

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
19	DISPON_POL	CS_ALL	TEMP2[5]	TEMP2[4]	TEMP2[3]	TEMP2[2]	TEMP2[1]	TEMP2[0]
	1	0	0	0	1	0	0	1

DISPON_POL : This register setting works with DISP_ON (H/W) pin.

DISPON_POL	DISP_ON	SD output color
0	0	Black/White set by PON
0	1	Normal display
1	0	Normal display
1	1	Black/White set by PON

CS_ALL : 1: Always do charge share function at each line.
0: Only do charge share function when POL is changing.

TEMP2[5:0]: compensation end temperature (-4~-1 ^{O}C)

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1A	MAX_DUTY[1]	MAX_DUTY[0]	TEMP3[5]	TEMP3[4]	TEMP3[3]	TEMP3[2]	TEMP3[1]	TEMP3[0]
	0	1	0	0	0	0	1	1

MAX_DUTY[1:0] : PWM max duty cycle control.

MAX_DUTY[1:0]	Percentage
00	70%
01	75% (default)
10	80%
11	85%

TEMP3[5:0]: compensation re-start temperature (-28~-25 ^{O}C)

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1B	OPDRV[1]	OPDRV[0]	TEMP4[5]	TEMP4[4]	TEMP4[3]	TEMP4[2]	TEMP4[1]	TEMP4[0]
	1	0	1	0	0	1	0	1

OPDRV[1:0] : Source OpAmp bias driving ability

OPDRV[1:0]	Driving ability
00	Ultra low
01	Low
10	Normal (default)
11	Strong

TEMP4[5:0]: over heat protection start temperature (108~111 ^{O}C)

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1C	PON_GND	PON_CS	TEMP5[5]	TEMP5[4]	TEMP5[3]	TEMP5[2]	TEMP5[1]	TEMP5[0]
	0	0	1	0	0	0	1	0

PON_GND: Power on period all source output short to GND. 1: Enable, 0: Disable
(Refer to Page.59, 61)

PON_CS: Power on period all source output doing charge share. 1: Enable, 0: Disable
(Refer to Page.59, 61)

TEMP5[5:0]: over heat protection end temperature (96~99 ^{O}C)

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1D	ST[7]	ST[6]	ST[5]	ST[4]	ST[3]	ST[2]	ST[1]	ST[0]
	1	1	1	1	1	1	1	1

ST[7:0]: sensor temperature, 00/h means -40 ^{O}C (accuracy < +/- 4 ^{O}C)
If TS_EN=0, ST[7:0] default value is FF/h, otherwise measure temperature will be ST[7:0] (DEC) - 40 ^{O}C

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1E	FC[7]	FC[6]	FC[5]	FC[4]	FC[3]	FC[2]	FC[1]	FC[0]
	0	0	0	0	0	0	0	0

FC[7:0]: Frame Counter. Count frame to reload temperature sensor value. Register value 0~1 mapping to 4 frames. Register value 2~255 is mapping to 8~1020, each step is 4.

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
1F	RESERVE[7]	RESERVE[6]	RESERVE[5]	RESERVE[4]	RESERVE[3]	RESERVE[2]	RESERVE[1]	RESERVE[0]
	0	0	0	0	0	0	0	0

RESERVE[7:0]: Reserved register

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
20	PYA0[7]	PYA0[6]	PYA0[5]	PYA0[4]	PYA0[3]	PYA0[2]	PYA0[1]	PYA0[0]
	0	1	1	0	1	1	1	1
21	PYA1[7]	PYA1[6]	PYA1[5]	PYA1[4]	PYA1[3]	PYA1[2]	PYA1[1]	PYA1[0]
	0	0	1	1	1	0	1	1
22	PYA2[7]	PYA2[6]	PYA2[5]	PYA2[4]	PYA2[3]	PYA2[2]	PYA2[1]	PYA2[0]
	0	0	1	0	0	1	1	0
23	PYA3[7]	PYA3[6]	PYA3[5]	PYA3[4]	PYA3[3]	PYA3[2]	PYA3[1]	PYA3[0]
	0	1	1	1	1	1	1	1
24	PYA4[7]	PYA4[6]	PYA4[5]	PYA4[4]	PYA4[3]	PYA4[2]	PYA4[1]	PYA4[0]
	0	1	0	1	1	0	1	0
25	PYA5[7]	PYA5[6]	PYA5[5]	PYA5[4]	PYA5[3]	PYA5[2]	PYA5[1]	PYA5[0]
	0	0	1	1	1	1	0	1
26	PYA6[7]	PYA6[6]	PYA6[5]	PYA6[4]	PYA6[3]	PYA6[2]	PYA6[1]	PYA6[0]
	0	0	1	0	1	0	0	1
27	PYA7[7]	PYA7[6]	PYA7[5]	PYA7[4]	PYA7[3]	PYA7[2]	PYA7[1]	PYA7[0]
	0	0	0	0	1	0	1	0
28	PYA8[7]	PYA8[6]	PYA8[5]	PYA8[4]	PYA8[3]	PYA8[2]	PYA8[1]	PYA8[0]
	0	1	1	0	0	0	1	1
29	PYA9[7]	PYA9[6]	PYA9[5]	PYA9[4]	PYA9[3]	PYA9[2]	PYA9[1]	PYA9[0]
	0	1	0	0	1	0	0	1
2A	PYA10[7]	PYA10[6]	PYA10[5]	PYA10[4]	PYA10[3]	PYA10[2]	PYA10[1]	PYA10[0]
	0	0	1	0	1	0	1	1
2B	PYA11[7]	PYA11[6]	PYA11[5]	PYA11[4]	PYA11[3]	PYA11[2]	PYA11[1]	PYA11[0]
	0	0	0	1	0	1	0	0
2C	PYA12[7]	PYA12[6]	PYA12[5]	PYA12[4]	PYA12[3]	PYA12[2]	PYA12[1]	PYA12[0]
	0	0	0	0	0	1	1	1
2D	PYA13[7]	PYA13[6]	PYA13[5]	PYA13[4]	PYA13[3]	PYA13[2]	PYA13[1]	PYA13[0]
	0	0	1	1	1	0	0	1
2E	PYA14[7]	PYA14[6]	PYA14[5]	PYA14[4]	PYA14[3]	PYA14[2]	PYA14[1]	PYA14[0]
	0	0	1	0	0	1	1	0
2F	PYA15[7]	PYA15[6]	PYA15[5]	PYA15[4]	PYA15[3]	PYA15[2]	PYA15[1]	PYA15[0]
	0	0	0	1	1	1	1	1
30	PYA16[7]	PYA16[6]	PYA16[5]	PYA16[4]	PYA16[3]	PYA16[2]	PYA16[1]	PYA16[0]
	0	1	0	1	0	1	0	0
31	PYA17[7]	PYA17[6]	PYA17[5]	PYA17[4]	PYA17[3]	PYA17[2]	PYA17[1]	PYA17[0]
	0	1	0	0	0	1	1	0
32	PYA18[7]	PYA18[6]	PYA18[5]	PYA18[4]	PYA18[3]	PYA18[2]	PYA18[1]	PYA18[0]
	0	0	1	0	0	0	1	0
33	NYA0[7]	NYA0[6]	NYA0[5]	NYA0[4]	NYA0[3]	NYA0[2]	NYA0[1]	NYA0[0]
	0	1	1	0	1	1	1	1
34	NYA1[7]	NYA1[6]	NYA1[5]	NYA1[4]	NYA1[3]	NYA1[2]	NYA1[1]	NYA1[0]
	0	0	1	1	1	0	1	1
35	NYA2[7]	NYA2[6]	NYA2[5]	NYA2[4]	NYA2[3]	NYA2[2]	NYA2[1]	NYA2[0]
	0	0	1	0	0	1	1	0
36	NYA3[7]	NYA3[6]	NYA3[5]	NYA3[4]	NYA3[3]	NYA3[2]	NYA3[1]	NYA3[0]
	0	1	1	1	1	1	1	1
37	NYA4[7]	NYA4[6]	NYA4[5]	NYA4[4]	NYA4[3]	NYA4[2]	NYA4[1]	NYA4[0]
	0	1	0	1	1	0	1	0
38	NYA5[7]	NYA5[6]	NYA5[5]	NYA5[4]	NYA5[3]	NYA5[2]	NYA5[1]	NYA5[0]
	0	0	1	1	1	1	0	1
39	NYA6[7]	NYA6[6]	NYA6[5]	NYA6[4]	NYA6[3]	NYA6[2]	NYA6[1]	NYA6[0]
	0	0	1	0	1	0	0	1
3A	NYA7[7]	NYA7[6]	NYA7[5]	NYA7[4]	NYA7[3]	NYA7[2]	NYA7[1]	NYA7[0]
	0	0	0	0	1	0	1	0

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
3B	NYA8[7]	NYA8[6]	NYA8[5]	NYA8[4]	NYA8[3]	NYA8[2]	NYA8[1]	NYA8[0]
	0	1	1	0	0	0	1	1
3C	NYA9[7]	NYA9[6]	NYA9[5]	NYA9[4]	NYA9[3]	NYA9[2]	NYA9[1]	NYA9[0]
	0	1	0	0	1	0	0	1
3D	NYA10[7]	NYA10[6]	NYA10[5]	NYA10[4]	NYA10[3]	NYA10[2]	NYA10[1]	NYA10[0]
	0	0	1	0	1	0	1	1
3E	NYA11[7]	NYA11[6]	NYA11[5]	NYA11[4]	NYA11[3]	NYA11[2]	NYA11[1]	NYA11[0]
	0	0	0	1	0	1	0	0
3F	NYA12[7]	NYA12[6]	NYA12[5]	NYA12[4]	NYA12[3]	NYA12[2]	NYA12[1]	NYA12[0]
	0	0	0	0	0	1	1	1
40	NYA13[7]	NYA13[6]	NYA13[5]	NYA13[4]	NYA13[3]	NYA13[2]	NYA13[1]	NYA13[0]
	0	0	1	1	1	0	0	1
41	NYA14[7]	NYA14[6]	NYA14[5]	NYA14[4]	NYA14[3]	NYA14[2]	NYA14[1]	NYA14[0]
	0	0	1	0	0	1	1	0
42	NYA15[7]	NYA15[6]	NYA15[5]	NYA15[4]	NYA15[3]	NYA15[2]	NYA15[1]	NYA15[0]
	0	0	0	1	1	1	1	1
43	NYA16[7]	NYA16[6]	NYA16[5]	NYA16[4]	NYA16[3]	NYA16[2]	NYA16[1]	NYA16[0]
	0	1	0	1	0	1	0	0
44	NYA17[7]	NYA17[6]	NYA17[5]	NYA17[4]	NYA17[3]	NYA17[2]	NYA17[1]	NYA17[0]
	0	1	0	0	0	1	1	0
45	NYA18[7]	NYA18[6]	NYA18[5]	NYA18[4]	NYA18[3]	NYA18[2]	NYA18[1]	NYA18[0]
	0	0	1	0	0	0	1	0
46	PYB0[7]	PYB0[6]	PYB0[5]	PYB0[4]	PYB0[3]	PYB0[2]	PYB0[1]	PYB0[0]
	0	1	1	0	1	1	1	1
47	PYB1[7]	PYB1[6]	PYB1[5]	PYB1[4]	PYB1[3]	PYB1[2]	PYB1[1]	PYB1[0]
	0	0	1	1	1	0	1	1
48	PYB2[7]	PYB2[6]	PYB2[5]	PYB2[4]	PYB2[3]	PYB2[2]	PYB2[1]	PYB2[0]
	0	0	1	0	0	1	1	0
49	PYB3[7]	PYB3[6]	PYB3[5]	PYB3[4]	PYB3[3]	PYB3[2]	PYB3[1]	PYB3[0]
	0	1	1	1	1	1	1	1
4A	PYB4[7]	PYB4[6]	PYB4[5]	PYB4[4]	PYB4[3]	PYB4[2]	PYB4[1]	PYB4[0]
	0	1	0	1	1	0	1	0
4B	PYB5[7]	PYB5[6]	PYB5[5]	PYB5[4]	PYB5[3]	PYB5[2]	PYB5[1]	PYB5[0]
	0	0	1	1	1	1	0	1
4C	PYB6[7]	PYB6[6]	PYB6[5]	PYB6[4]	PYB6[3]	PYB6[2]	PYB6[1]	PYB6[0]
	0	0	1	0	1	0	0	1
4D	PYB7[7]	PYB7[6]	PYB7[5]	PYB7[4]	PYB7[3]	PYB7[2]	PYB7[1]	PYB7[0]
	0	0	0	0	1	0	1	0
4E	PYB8[7]	PYB8[6]	PYB8[5]	PYB8[4]	PYB8[3]	PYB8[2]	PYB8[1]	PYB8[0]
	0	1	1	0	0	0	1	1
4F	PYB9[7]	PYB9[6]	PYB9[5]	PYB9[4]	PYB9[3]	PYB9[2]	PYB9[1]	PYB9[0]
	0	1	0	0	1	0	0	1
50	PYB10[7]	PYB10[6]	PYB10[5]	PYB10[4]	PYB10[3]	PYB10[2]	PYB10[1]	PYB10[0]
	0	0	1	0	1	0	1	1
51	PYB11[7]	PYB11[6]	PYB11[5]	PYB11[4]	PYB11[3]	PYB11[2]	PYB11[1]	PYB11[0]
	0	0	0	1	0	1	0	0
52	PYB12[7]	PYB12[6]	PYB12[5]	PYB12[4]	PYB12[3]	PYB12[2]	PYB12[1]	PYB12[0]
	0	0	0	0	0	1	1	1
53	PYB13[7]	PYB13[6]	PYB13[5]	PYB13[4]	PYB13[3]	PYB13[2]	PYB13[1]	PYB13[0]
	0	0	1	1	1	0	0	1
54	PYB14[7]	PYB14[6]	PYB14[5]	PYB14[4]	PYB14[3]	PYB14[2]	PYB14[1]	PYB14[0]
	0	0	1	0	0	1	1	0
55	PYB15[7]	PYB15[6]	PYB15[5]	PYB15[4]	PYB15[3]	PYB15[2]	PYB15[1]	PYB15[0]
	0	0	0	1	1	1	1	1

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
56	PYB16[7]	PYB16[6]	PYB16[5]	PYB16[4]	PYB16[3]	PYB16[2]	PYB16[1]	PYB16[0]
	0	1	0	1	0	1	0	0
57	PYB17[7]	PYB17[6]	PYB17[5]	PYB17[4]	PYB17[3]	PYB17[2]	PYB17[1]	PYB17[0]
	0	1	0	0	0	1	1	0
58	PYB18[7]	PYB18[6]	PYB18[5]	PYB18[4]	PYB18[3]	PYB18[2]	PYB18[1]	PYB18[0]
	0	0	1	0	0	0	1	0
59	NYB0[7]	NYB0[6]	NYB0[5]	NYB0[4]	NYB0[3]	NYB0[2]	NYB0[1]	NYB0[0]
	0	1	1	0	1	1	1	1
5A	NYB1[7]	NYB1[6]	NYB1[5]	NYB1[4]	NYB1[3]	NYB1[2]	NYB1[1]	NYB1[0]
	0	0	1	1	1	0	1	1
5B	NYB2[7]	NYB2[6]	NYB2[5]	NYB2[4]	NYB2[3]	NYB2[2]	NYB2[1]	NYB2[0]
	0	0	1	0	0	1	1	0
5C	NYB3[7]	NYB3[6]	NYB3[5]	NYB3[4]	NYB3[3]	NYB3[2]	NYB3[1]	NYB3[0]
	0	1	1	1	1	1	1	1
5D	NYB4[7]	NYB4[6]	NYB4[5]	NYB4[4]	NYB4[3]	NYB4[2]	NYB4[1]	NYB4[0]
	0	1	0	1	1	0	1	0
5E	NYB5[7]	NYB5[6]	NYB5[5]	NYB5[4]	NYB5[3]	NYB5[2]	NYB5[1]	NYB5[0]
	0	0	1	1	1	1	0	1
5F	NYB6[7]	NYB6[6]	NYB6[5]	NYB6[4]	NYB6[3]	NYB6[2]	NYB6[1]	NYB6[0]
	0	0	1	0	1	0	0	1
60	NYB7[7]	NYB7[6]	NYB7[5]	NYB7[4]	NYB7[3]	NYB7[2]	NYB7[1]	NYB7[0]
	0	0	0	0	1	0	1	0
61	NYB8[7]	NYB8[6]	NYB8[5]	NYB8[4]	NYB8[3]	NYB8[2]	NYB8[1]	NYB8[0]
	0	1	1	0	0	0	1	1
62	NYB9[7]	NYB9[6]	NYB9[5]	NYB9[4]	NYB9[3]	NYB9[2]	NYB9[1]	NYB9[0]
	0	1	0	0	1	0	0	1
63	NYB10[7]	NYB10[6]	NYB10[5]	NYB10[4]	NYB10[3]	NYB10[2]	NYB10[1]	NYB10[0]
	0	0	1	0	1	0	1	1
64	NYB11[7]	NYB11[6]	NYB11[5]	NYB11[4]	NYB11[3]	NYB11[2]	NYB11[1]	NYB11[0]
	0	0	0	1	0	1	0	0
65	NYB12[7]	NYB12[6]	NYB12[5]	NYB12[4]	NYB12[3]	NYB12[2]	NYB12[1]	NYB12[0]
	0	0	0	0	0	1	1	1
66	NYB13[7]	NYB13[6]	NYB13[5]	NYB13[4]	NYB13[3]	NYB13[2]	NYB13[1]	NYB13[0]
	0	0	1	1	1	0	0	1
67	NYB14[7]	NYB14[6]	NYB14[5]	NYB14[4]	NYB14[3]	NYB14[2]	NYB14[1]	NYB14[0]
	0	0	1	0	0	1	1	0
68	NYB15[7]	NYB15[6]	NYB15[5]	NYB15[4]	NYB15[3]	NYB15[2]	NYB15[1]	NYB15[0]
	0	0	0	1	1	1	1	1
69	NYB16[7]	NYB16[6]	NYB16[5]	NYB16[4]	NYB16[3]	NYB16[2]	NYB16[1]	NYB16[0]
	0	1	0	1	0	1	0	0
6A	NYB17[7]	NYB17[6]	NYB17[5]	NYB17[4]	NYB17[3]	NYB17[2]	NYB17[1]	NYB17[0]
	0	1	0	0	0	1	1	0
6B	NYB18[7]	NYB18[6]	NYB18[5]	NYB18[4]	NYB18[3]	NYB18[2]	NYB18[1]	NYB18[0]
	0	0	1	0	0	0	1	0

PYA0[7:0]~PYA18[7:0]: Group A positive polarity gamma setting.

NYA0[7:0]~NYA18[7:0]: Group A negative polarity gamma setting.

PYB0[7:0]~PYB18[7:0]: Group B positive polarity gamma setting.

NYB0[7:0]~NYB18[7:0]: Group B negative polarity gamma setting.

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
6C	MTP_CS	MTP_ADR[6]	MTP_ADR[5]	MTP_ADR[4]	MTP_ADR[3]	MTP_ADR[2]	MTP_ADR[1]	MTP_ADR[0]
	0	0	0	0	0	0	0	0
6D	MTP_DIN[7]	MTP_DIN[6]	MTP_DIN[5]	MTP_DIN[4]	MTP_DIN[3]	MTP_DIN[2]	MTP_DIN[1]	MTP_DIN[0]
	0	0	0	0	0	0	0	0
6E	MTP_DOUT[7]	MTP_DOUT[6]	MTP_DOUT[5]	MTP_DOUT[4]	MTP_DOUT[3]	MTP_DOUT[2]	MTP_DOUT[1]	MTP_DOUT[0]
	0	0	0	0	0	0	0	0
6F		MTP_BUSY	MTP_AUTOW	MTPCLK_EN	MTP_SRL	MTP_CLEN	MTP_WRITE	MTP_READ
		0	0	0	0	0	0	0

MTP_CS: MTP chip select enable. 1 : enable, 0 : disable.

MTP_ADR[6:0]: MTP address. 0~127 bytes.

MTP_DIN[7:0]: MTP input data.

MTP_DOUT[7:0]: MTP output data.

MTPCLK_EN: MTP clock enable control. 1: Enable, 0: Disable.

MTP_BUSY: When writing MTP data and an error occurred, this bit will be 1. This bit is read only and it will be reset to 0 when powered off.

MTP_AUTOW: MTP auto write function.
MTP_AUTOW=1: SC5004 will automatically write data from register to MTP and waiting >150ms, this register bit will be reset to 0.
MTP_AUTOW=0: disable

MTP_SRL: Engineer mode, it must be “0”.

MTP_CLEN: Engineer mode, it must be “0”

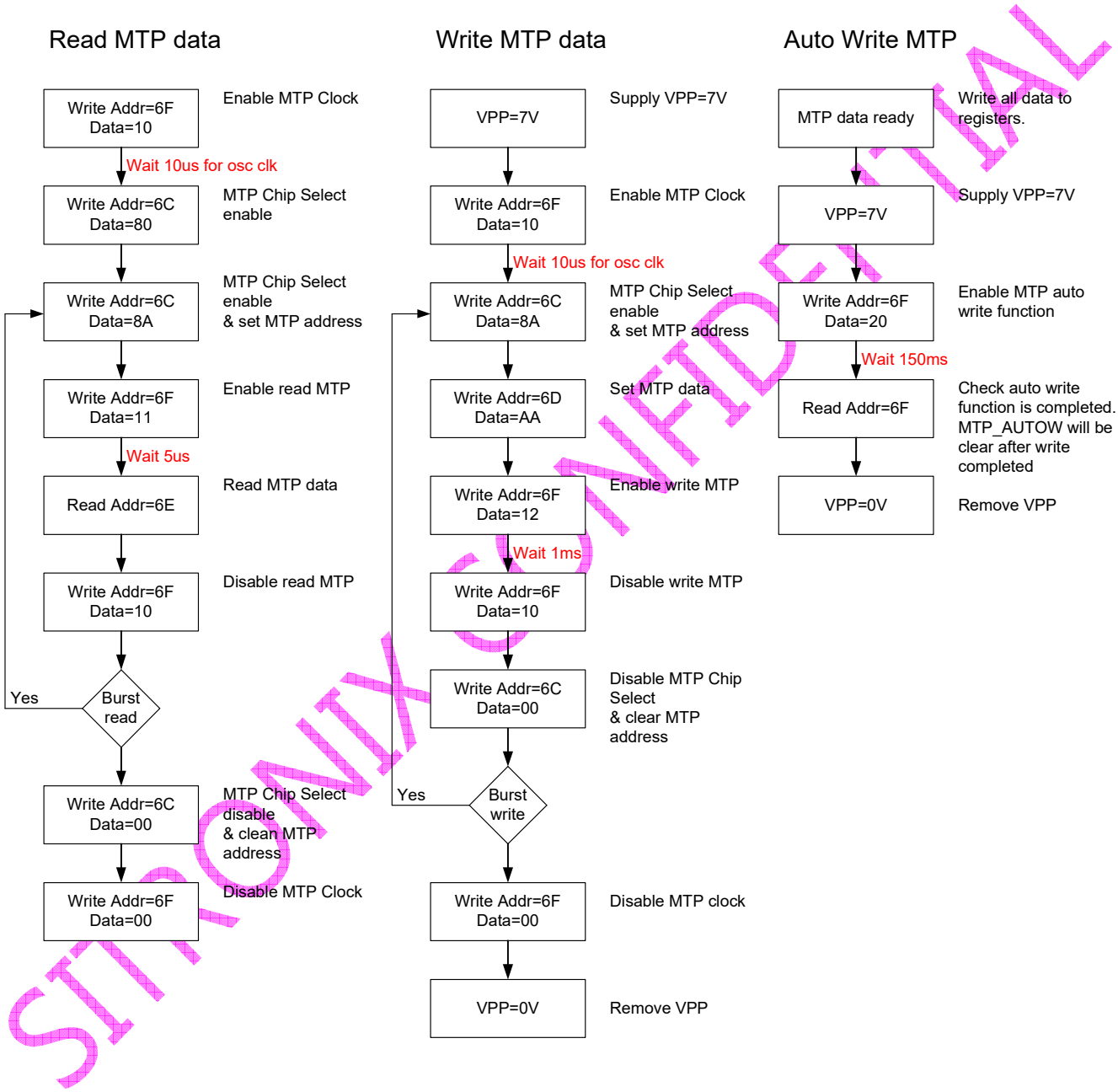
MTP_WRITE: Write MTP.

MTP_READ: Read MTP.

MTP processing flow

Using SPI/I²C interface to control internal register of MTP (address=6Ch~6Fh). SC5004 will generate MTP control signals to R/W internal MTP block.

Read and write MTP flow as below figure.



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Digital supply voltage	VDD	-0.5 to 5.0	V
LVDS supply voltage	VDD_LVDS	-0.5 to 5.0	V
MTP supply voltage	VDD_MTP	-0.5 to 8.0	V
Analog supply voltage,	VDDA	-0.5 to 14.85	V
Digital input voltage	---	-0.3 to VDD+0.3	V
Storage temperature	---	-55 to +125	℃
Operating temperature	---	-20 to +85	℃

CAUTIONS：
Stresses beyond "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operations beyond those indicated under " typical operating conditions" is not implied. Exposure to absolute maximum rating conditions may affect device reliability

Recommended Operating Range

(GND = GND_LVDS = GNDA = 0V, TA = -20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	3.0	3.3	3.6	V
MTP supply voltage	VDD_MTP	6.3	7.0	7.7	V
Analog supply voltage,	VDDA	8.0	10.4	13.5	V
LVDS supply voltage	VDD_LVDS	3.0	3.3	3.6	V

DC Electrical Characteristics

(VDD=3.0~3.6V, VDDA=8.0~13.5V, GND=GNDA=0V, TA=-20~85℃)

Source driver

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Power supply voltage	VDD	3.0	3.3	3.6	V	
Power supply voltage	VDDA	8.0	10.4	13.5	V	
Analog operation Current	I_{VDDA}	-	9	15	mA	No load, F_{CLK}=45Mhz, F_{HS}=48K@VDDA=10.4V GMAH=10V, GMAL=0.4V Data pattern=00/H -> FF/H (loop)
Analog stand-by Current	I_{STBA}	-	10	50	uA	RSTB=0 or STBYB=0 No load. Clock & all functions are stopped (GMAH=GMAL=0V)
Input level of Gamma High	GMAH	VDDA-2.5	RVDDA	VDDA	V	Gamma correction voltage input
Input level of Gamma low	GMAL	GNDA	0	2	V	Gamma correction voltage input
Output voltage deviation	DV_{RMS}	-	+/- 15	+/- 30	mV	Vo=GNDA+0.2V~GNDA + 2.0V Vo=VDDA -2.0V~VDDA-0.2V VDDA=10.4V (Note 1,2)
		-	+/- 3	+/- 10	mV	Vo=GNDA+2.0V~VDDA-2.0V VDDA=10.4V (Note 1,2)
Output voltage offset between chips	V_{OC}	-	-	+/- 5	mV	Data code=7F/H @VDDA=12.0V, GMAH=10.4V, GMAL=0V
Dynamic range of output	V_{DYNA}	0.2	-	VDDA-0.2	V	SO[1]~SO[1284], pure source mode
		0.2	-	VDDA-0.5	V	SO[1]~SO[1284], when LDO_EN=H and RVDDA set as GMAH input
Sinking current of output	I_{OL}	80	-	-	uA	SO[1]~SO[1284]; Vo=0.2V vs. 1.1V, VDDA=13.5V
Driving current of outputs	I_{OH}	80	-	-	uA	SO[1]~SO[1284]; Vo=13.3V vs. 12.4V, VDDA=13.5V
Resistance of Gamma R-string	R_{GAMMA}	0.7*R_{INT}	1.0* R_{INT}	1.3* R_{INT}	ohm	R_{INT}: Internal gamma resistor=100kΩ

Note 1 : $DV_{RMS} = V_{SOD} / 1284 – (V_{SODH}x-V_{SODL}x)$, x=1,2,3…1284

V_{SOD} : Sum of $(V_{SODH}x – V_{SODL}x)$, x=1,2,3…1284

$V_{SODH}x$: Source output x gray level positive polarity voltage deviation, x=1,2,3…1284

$V_{SODL}x$: Source output x gray level negative polarity voltage deviation, x=1,2,3…1284

Note 2 : The value of Typ. is specified by 3 sigma

CMOS interface and circuit

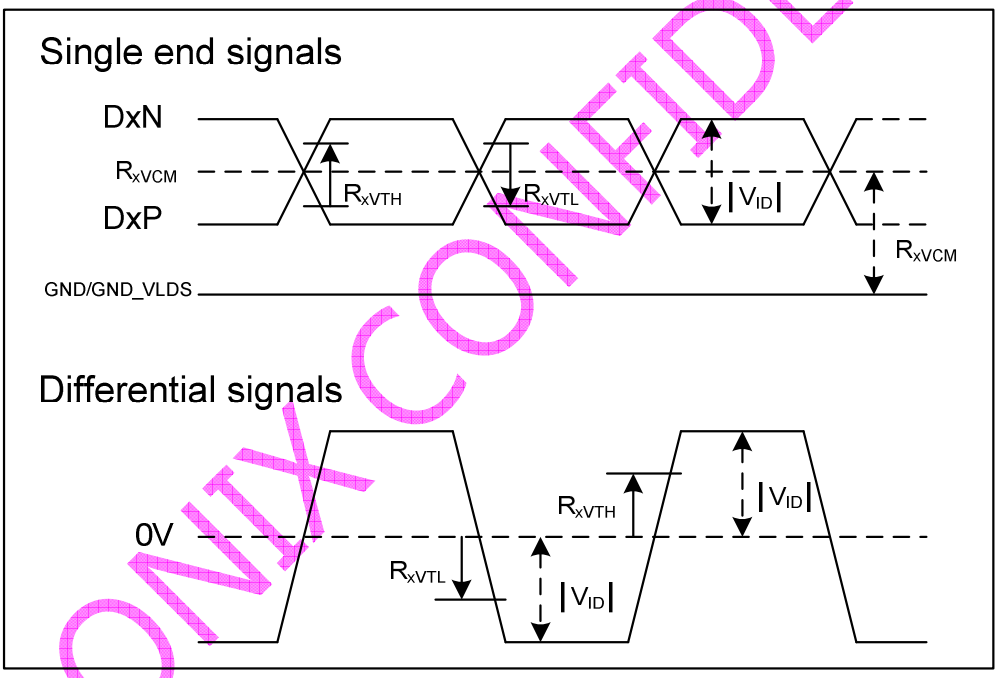
(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Power supply voltage	VDD	3.0	3.3	3.6	V	
Low level input voltage	V_{IL}	0	-	0.3xVDD	V	CMOS I/F digital circuit
High level input voltage	V_{IH}	0.7xVDD	-	VDD	V	CMOS I/F digital circuit
Input leakage current	I_{LEAK}	-	-	+/-1	uA	CMOS I/F digital circuit
High level output voltage	V_{OH1}	VDD-0.4	-	-	V	I_{OH}=-400uA
	V_{OH2}	VDD-0.4	-	-		I_{OH}=-1mA (EIO1, EIO2)
Low level output voltage	V_{OL1}	-	-	GND+0.4	V	I_{OL}=+400uA
	V_{OL2}	-	-	GND+0.4		I_{OL}=+1mA (EIO1, EIO2)
Pull low/high resistor	R_{PULL}	180K	250K	320K	ohm	For the digital input pin @VDD=3.3V
Digital operation Current	I_{VDD}	-	13	20	mA	F_{CLK}=45MHz, F_{LD}=48K @VDD=3.3V Data pattern=55/H -> AA/H (loop)
Digital stand-by current	I_{STBD}	-	10	50	uA	RSTB=0 or STBYB=0 All functions are stopped CLK & Dxx are connect to GND All input setting pin set as default

LVDS receiver characteristic (Receiver Differential Input：D0P~D3P, D0N~D3N, CLKP, CLKN)

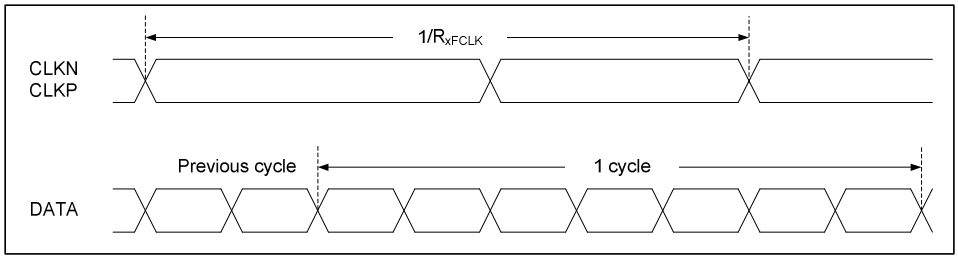
(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

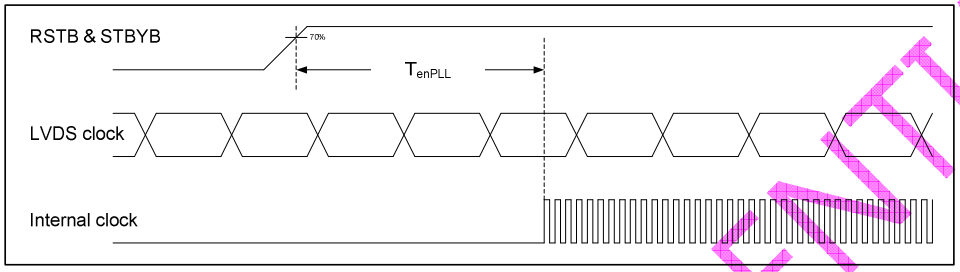
Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Differential input high threshold voltage	R_{xVTH}			0.1	V	R_{xVCM} = 1.2V
Differential input low threshold voltage	R_{xVTL}	-0.1			V	
Input voltage range (singled-end)	R_{xVIN}	0		VDD-1.0	V	
Differential input common mode voltage	R_{xVCM}	$\lvert V_{ID} \rvert$ /2		2.4- $\lvert V_{ID} \rvert$ /2	V	
Differential input voltage	$\lvert V_{ID} \rvert$	0.2		0.6	V	
Differential input leakage current	RV_{xliz}	-10		10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	F_{CLK}=65 MHz , VDD_LVDS=3.3V Data pattern=55/H → AA/H (loop)
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	RSTB=0 or STBYB=0 All functions are stopped CLKx & D0x connect to GND

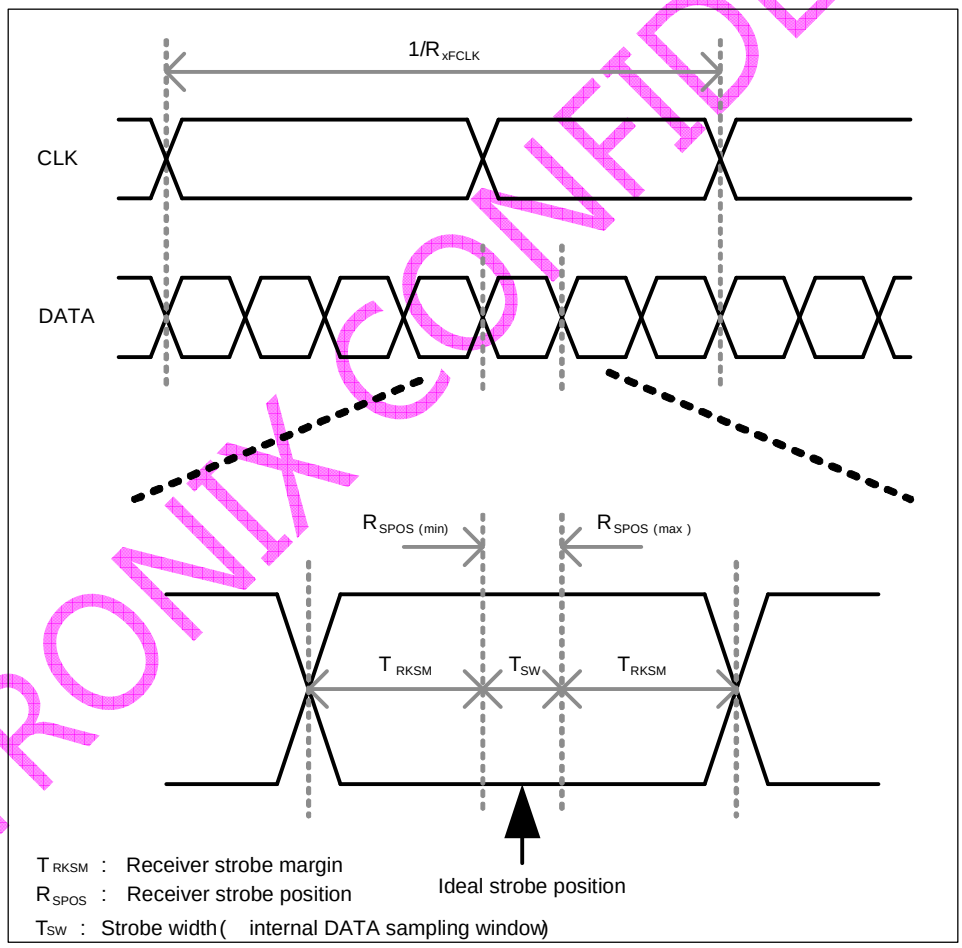


LVDS AC characteristic (VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Clock Frequency	R_{xFCLK}	20		80	MHz	
Input data skew margin	T_{RSKM}	400			ps	$\lvert V_{ID} \rvert$ = 400mV, R_{xVCM}=1.2V R_{xFCLK}=80MHz
Clock high time	T_{LVCH}		4/(7xRxFCLK)		ns	
Clock low time	T_{LVCL}		3/(7xRxFCLK)		ns	
PLL wake-up time	TenPLL			150	us	





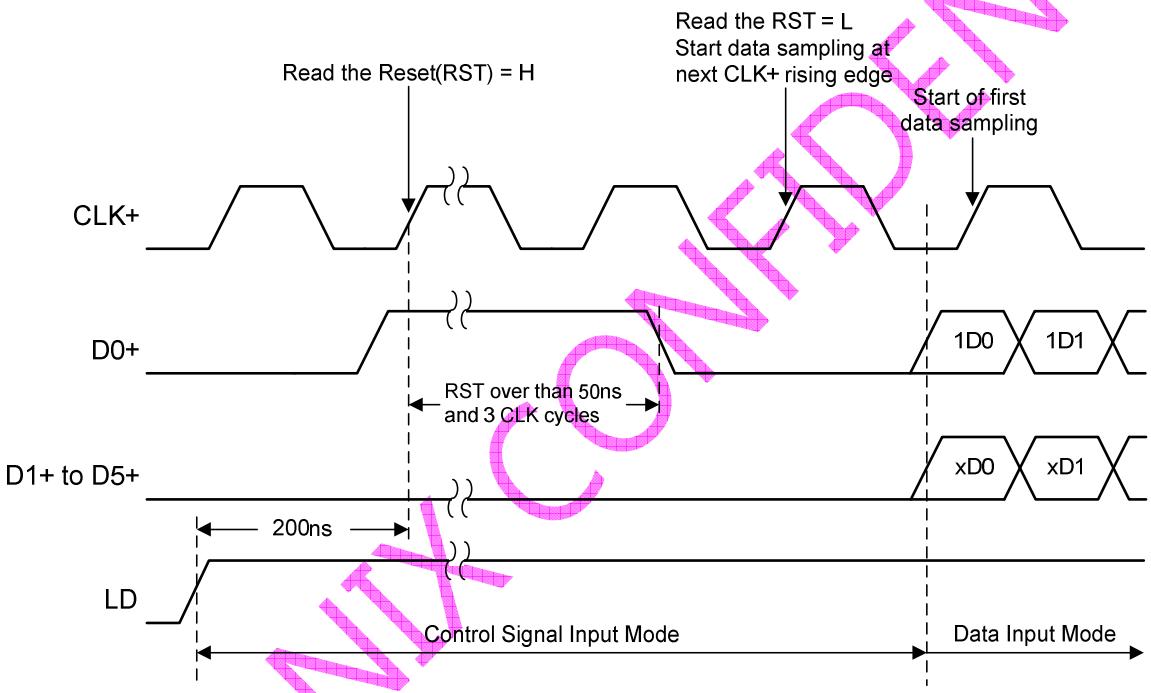


Spread Spectrum Clocking (SSC) tolerance of LVDS receiver

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Modulation frequency	SSC_{MF}			100	kHz	
Modulation rate	SSC_{MR}			+/-3	%	R_{xFCLK}=70MHz

Taking in the mini-LVDS display data

1. Fix EIO1(2) to “H” to set a chip to be a lead chip. Connect each EIO2(1) to EIO1(2) of next chip.
2. The lead chip is set to “control signal input mode” (so called “control mode”), and receivers at D0+/-, and CLK+/- of all chips are activated by rising edge of LS.
3. Input the reset (RST) signal as “L” to D0+/-. This RST should be kept over 200ns after rising of LS.
4. RST as “H” is input to D0+/- and “H” width should be over 50nsec and also over 3CLK cycles.
5. Input the RST as “L” to D0+/- and then changed to the “data input mode” function.
   By the way, input LS again when a second RST is necessary.
6. Data sampling starts at the rising edge of CLK after reading of “RST=L”.
7. At the same time data sampling starts, internal counter starts counting the data cycle for EIO2(1) signal generation.
8. After data sampling is finished, the receivers turn off.
9. After the receivers turn off, keep the timing for more than 5 CLK cycles until LS is applied.
10. Figure below shows the rough timing chart from application of LS to the start of data sampling.



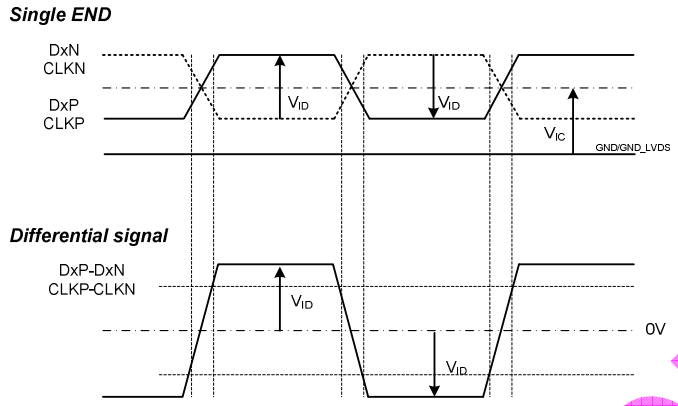
mini-LVDS source driver mode

mini-LVDS receiver characteristics (Receiver Differential Input：D0P~D5P, D0N~D5N, CLKP, CLKN)

(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Mini-LVDS High Input Voltage	V_{ID}	150	200	600	mV	
Input voltage (center)	V_{IC}	0.3+V_{ID}	1.2	VDD-1.1- V_{ID}	V	

mini- LVDS signal definition



mini-LVDS AC Electrical Characteristics

(VDD=VDD_LVDS=3.0~3.6V, VDDA=8.0~13.5V, GND=GNDA=0V, TA=-20~85℃)

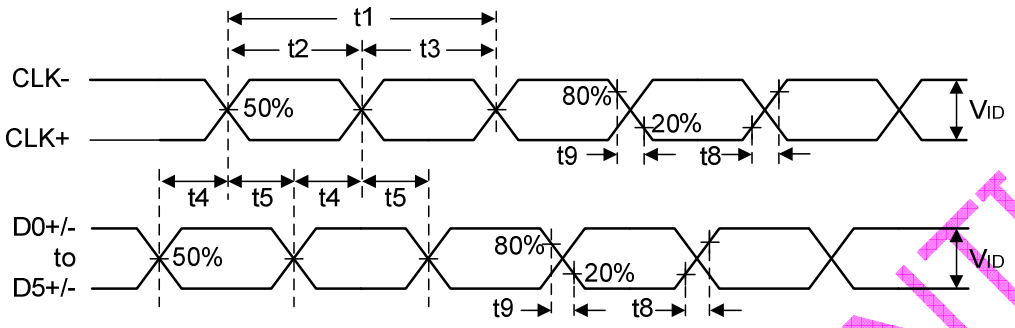
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock pulse cycle	t1	5.88			ns	f_{MINI_LVDS} Max.=170MHz
Clock pulse high period	t2	0.4 CLK		0.6 CLK	ns	
Clock pulse low period	t3	0.4 CLK		0.6 CLK	ns	
Data setup time	t4	1			ns	
Data hold time	t5	1			ns	
Start pulse setup time	t6	0			ns	
Start pulse delay time	t7			3 or 4	CLK	Load = 25 pF, 6bit=3, 8bit=4
CLK, DxA/B rise time	t8			0.4	ns	
CLK, DxA/B fall time	t9			0.4	ns	
Reset(RST) high period	t10	50ns or moreover 3 CLK cycles				
LD high period	t11	2			CLK	
POL setup time	t12	6			ns	
POL hold time	t13	6			ns	
Driver output delay time	t14			4	µs	(1) (3)
	t15			8	µs	(2) (3)
Receiver off to LD timing	t16	6			CLK	
LD to Reset input time	t17	200			ns	
Reset low to LD rise time	t18	0			ns	
LD to source output time	t19	24		t11+ 2	CLK	t11 ≦ 24 CLK, t19=24CLK t11 > 24 CLK, t19=t11+ 2CLK

Notes:

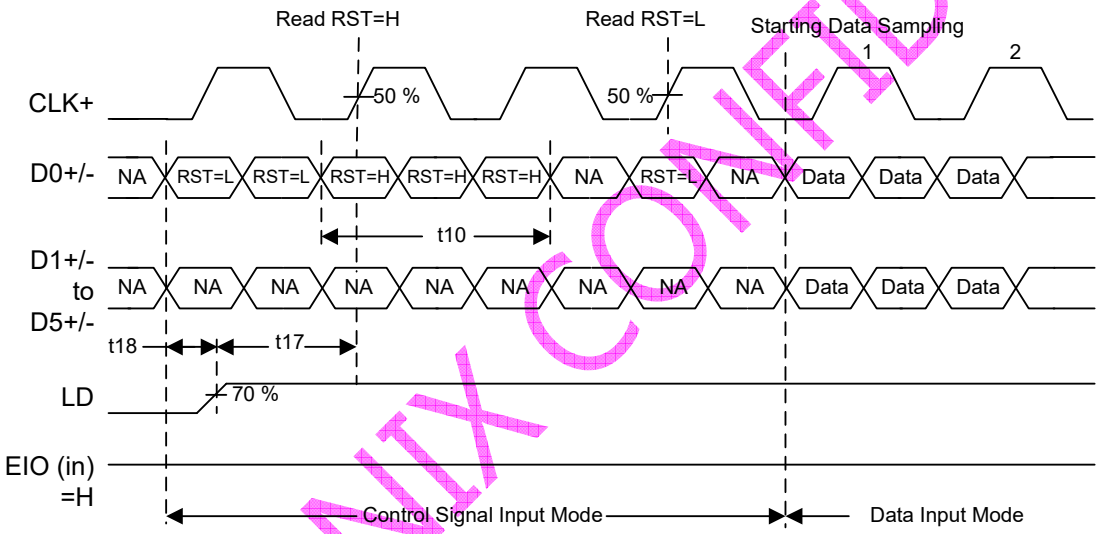
1. The value is specified when the drive voltage value reaches the target output voltage level of 90%
2. The value is specified when the drive voltage value reaches the target output voltage level of 99%
3. The value is referred to source output load condition

mini-LVDS timing diagram

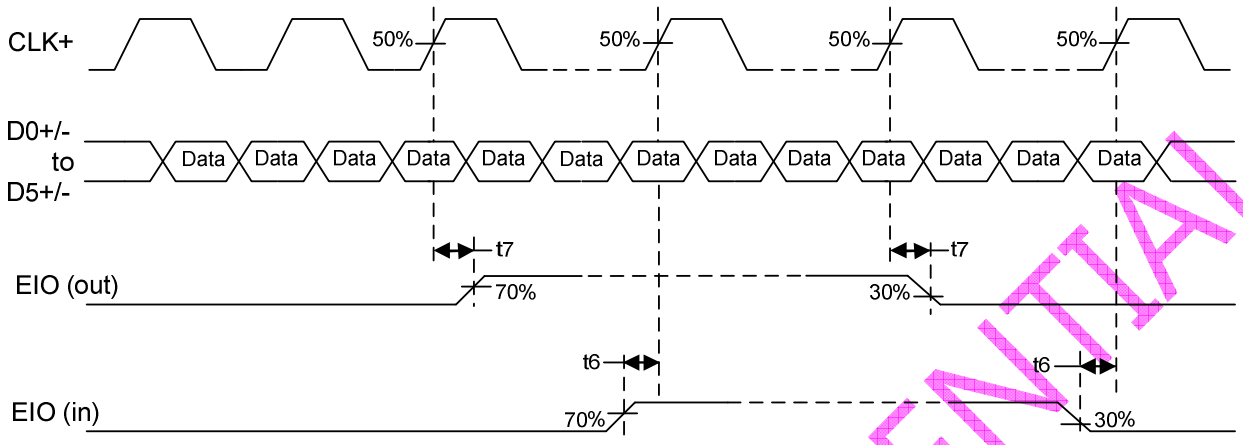
(1) DATA Read Timing



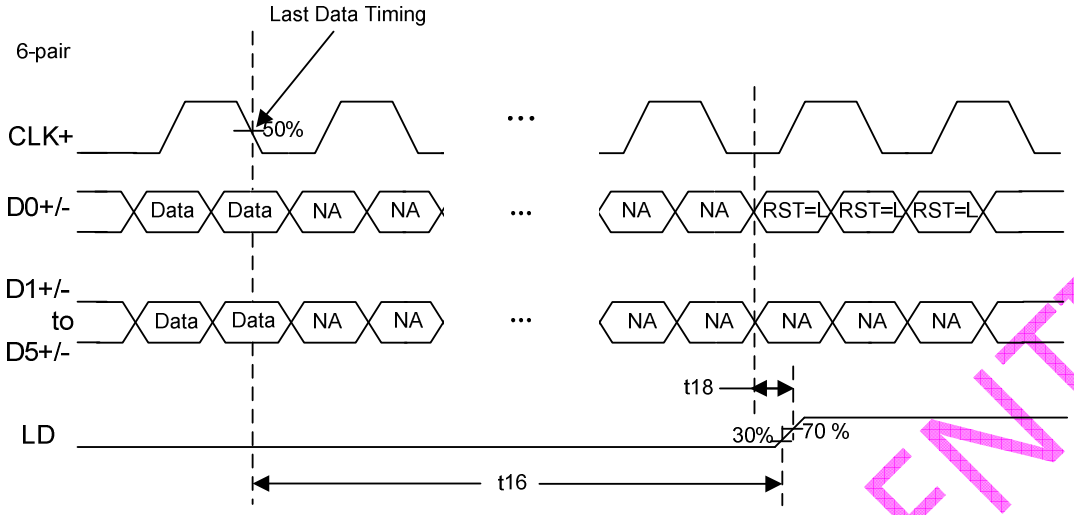
(2) Input DATA timing(Lead Chip)



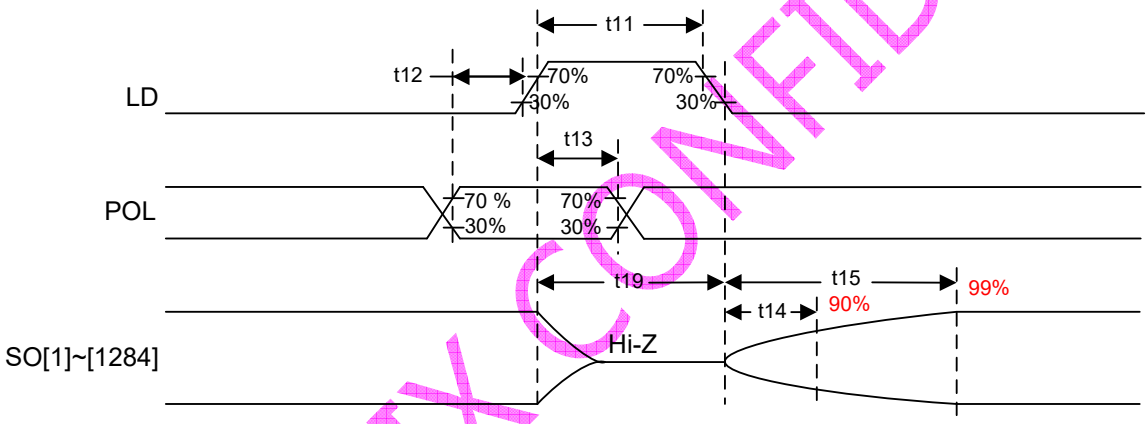
2. Input Data timing (Cascade chips)



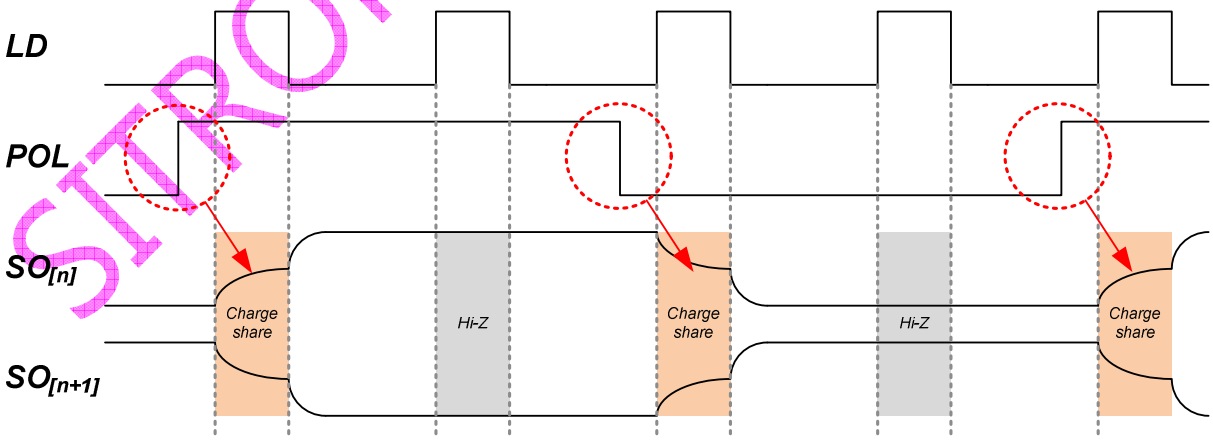
(4) Last Data Sampling to LS Timing



2. mini-LVDS, RSDS and CMOS General Timing



2. mini-LVDS, RSDS and CMOS charge share function



Note: Charge share setting can be change by register CS_ALL (19/h, bit6).

RSDS source driver mode

RSDS receiver characteristics (Receiver Differential Input：DxxP~DxxN, CLKP, CLKN)

(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

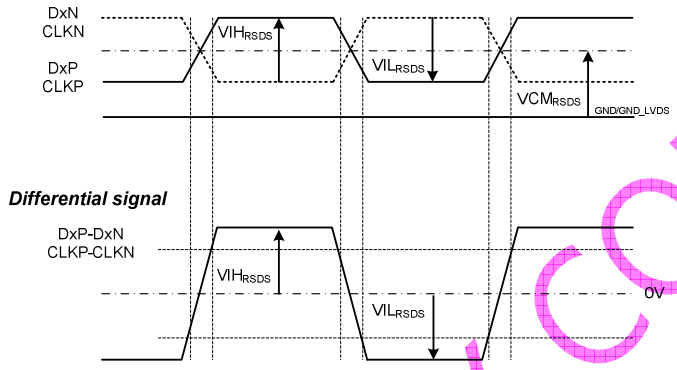
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RSDS high input voltage	VIH_{RSDS}	100	200	-	mV	f_{RSDS} > 70MHz
		70	200	-	mV	
RSDS low input voltage	VIL_{RSDS}	-	-200	-100	mV	f_{RSDS} > 70MHz
		-	-200	-70	mV	
RSDS common mode input voltage range	VCM_{RSDS}(1)	0.4	-	VDD-1.1	V	$VDIFF_{RSDS}$ (2) = 200 mV

Notes:

1. VCM_{RSDS} = (VCLKP + VCLKN) / 2 or VCM_{RSDS} = (VDxxP + VDxxN) / 2
2. $VDIFF_{RSDS}$ = VCLKP – VCLKN or $VDIFF_{RSDS}$ = VDxxP – VDxxN
   The typical RSDS swing level of peak to peak is 400mV, ranging from -200 to +200mV

RSDS signal definition

Single END



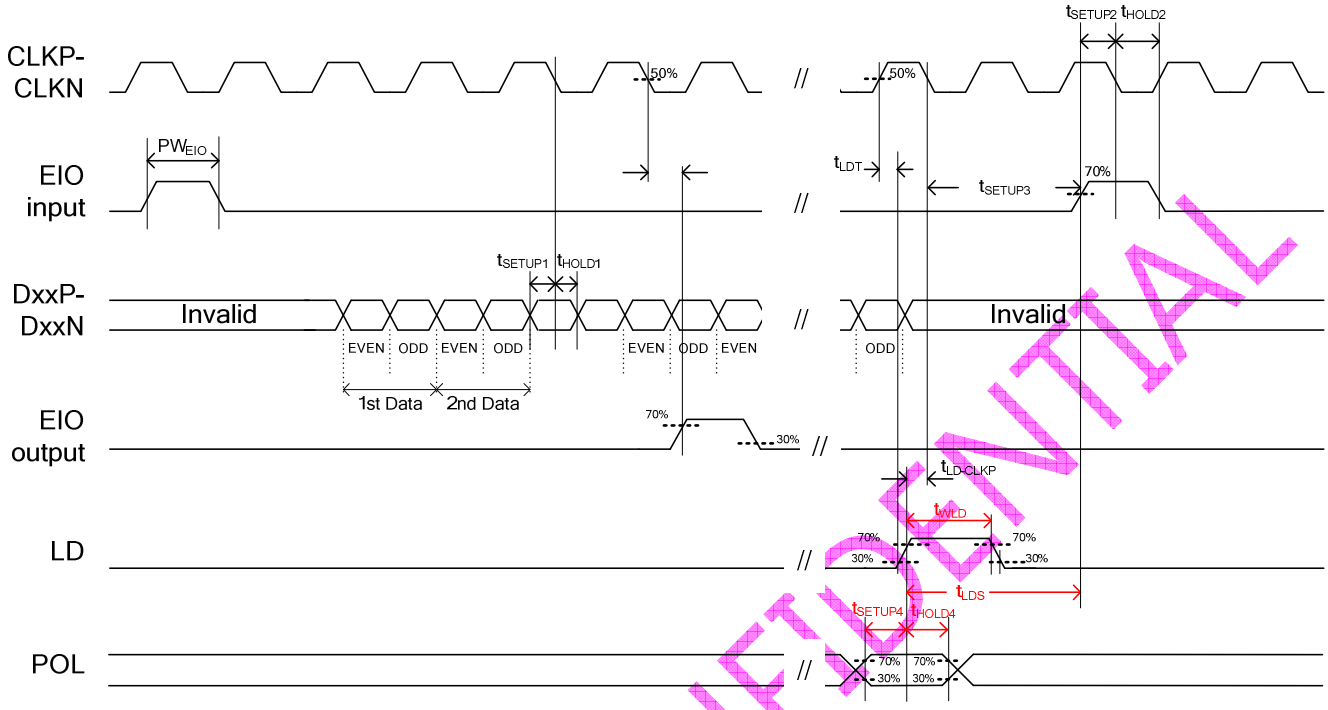
Differential signal

RSDS mode AC Electrical Characteristics

(VDD=VDD_LVDS=3.0~3.6V, VDDA=8.0~13.5V, GND=GND_LVDS=GNDA=0V, TA= -20~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock pulse width	PW_{CLK}	8.33			ns	f_{RSDS} Max.=120Mhz
Clock pulse low period	$PW_{CLK(L)}$	3.7			ns	
Clock pulse high period	$PW_{CLK(H)}$	3.7			ns	
Data setup time	t_{SETUP1}	2			ns	
Data hold time	t_{HOLD1}	0			ns	
Start pulse setup time	t_{SETUP2}	2			ns	
Start pulse hold time	t_{HOLD2}	2			ns	
Start pulse delay time	t_{PLH1}			6.33	ns	LOAD=15pF, f_{RSDS}=120MHz
EIO signal pulse width	PW_{EIO}	1	2	2	CLK	
LD to EIO setup time	t_{SETUP3}	5			CLK	
Last data timing	t_{LDT}	1			CLK	
LD-CLKP time	$t_{LD-CLKP}$	4			ns	LS rising to CLKP falling
POL setup time	t_{SETUP4}	6			ns	
POL hold time	t_{HOLD4}	6			ns	
LD high period	t_{WLD}	2			CLK	
LD – EIO input time	t_{LD-EIO}	6			CLK	LS rising to EIO rising
LD to source output time	t19	24		t_{WLD}+ 2	CLK	$t_{WLD} \leqq$ 24 CLK, t19=24CLK t_{WLD} > 24 CLK, t19=t_{WLD}+ 2CLK

RSDS Timing Diagram



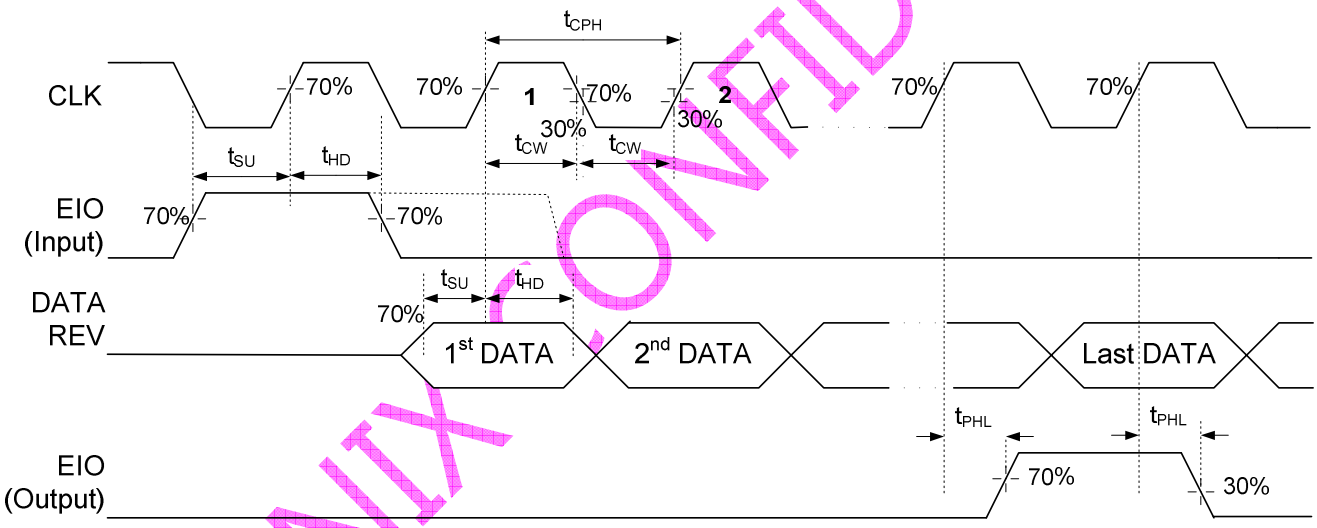
CMOS source driver mode

AC Electrical Characteristics

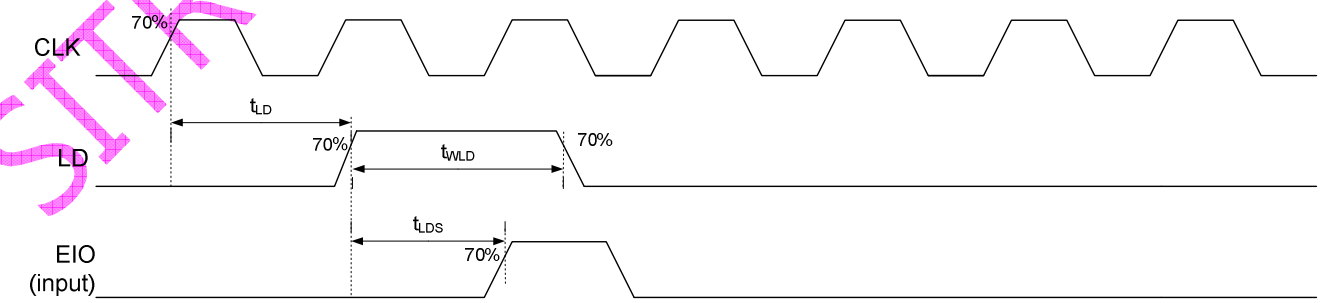
(VDD=VDD_LVDS=3.0~3.6V, VDDA=8.0~13.5V, GND=GND_LVDS=GNDA=0V, TA= -20~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
CLK frequency	f_{CLK}	-	-	60	MHz	
CLK pulse width	t_{CW}	40%	-	60%	t_{CPH}	
Data setup time	t_{SU}	4	-	-	ns	D00~D27,REV and EIO1/2 to CLK
Data hold time	t_{HD}	2	-	-	ns	D00~D27,REV and EIO1/2 to CLK
Propagation delay of EIO1/2	t_{PHL}	-	-	8.33	ns	LOAD=15pF
Time that the last data to LD	t_{LD}	1	-	-	t_{CPH}	
Time that LD to EIO1/2	t_{LDS}	5	-	-	t_{CPH}	
LD high period	t_{WLD}	2			t_{CPH}	
LD to source output time	t19	24		t_{WLD}+ 2	CLK	$t_{WLD} \leqq$ 24 CLK, t19=24CLK t_{WLD} > 24 CLK, t19=t_{WLD}+ 2CLK

CMOS Timing Diagram (1)

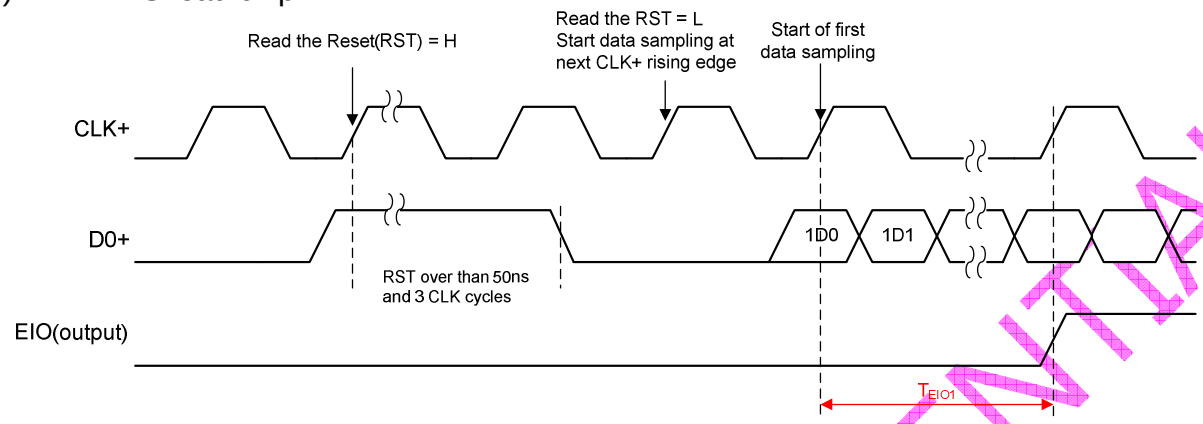


CMOS Timing Diagram (2)

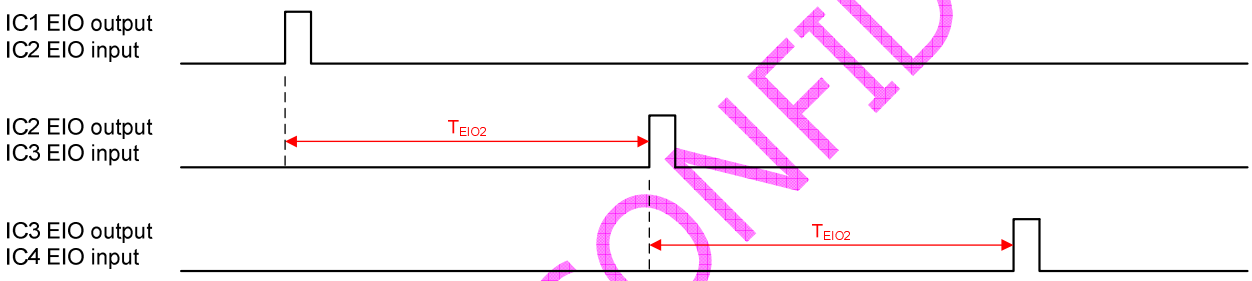


Source driver mode EIO output timing

(1)mini-LVDS lead chip



2. CMOS/RSDS/mini-LVDS cascade chip



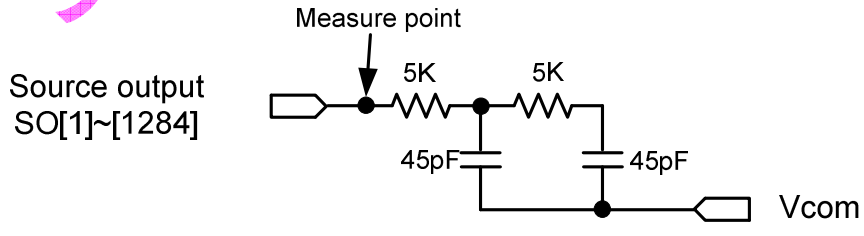
mini-LVDS				
Source total channels	6 bit		8 bit	
	T_{EIO1}	T_{EIO2}	T_{EIO1}	T_{EIO2}
1284	628	642	837	856
1278	625	639	833	852
1200	586	600	781	800
1152	562	576	749	768
1080	526	540	701	720
1026	499	513	665	684
1020	496	510	661	680
960	466	480	621	640

Unit : CLK

CMOS / RSDS		
Source total channels	6 bit	8 bit
	T_{EIO2}	T_{EIO2}
1284	428	428
1278	426	426
1200	400	400
1152	384	384
1080	360	360
1026	342	342
1020	340	340
960	320	320

Unit : CLK

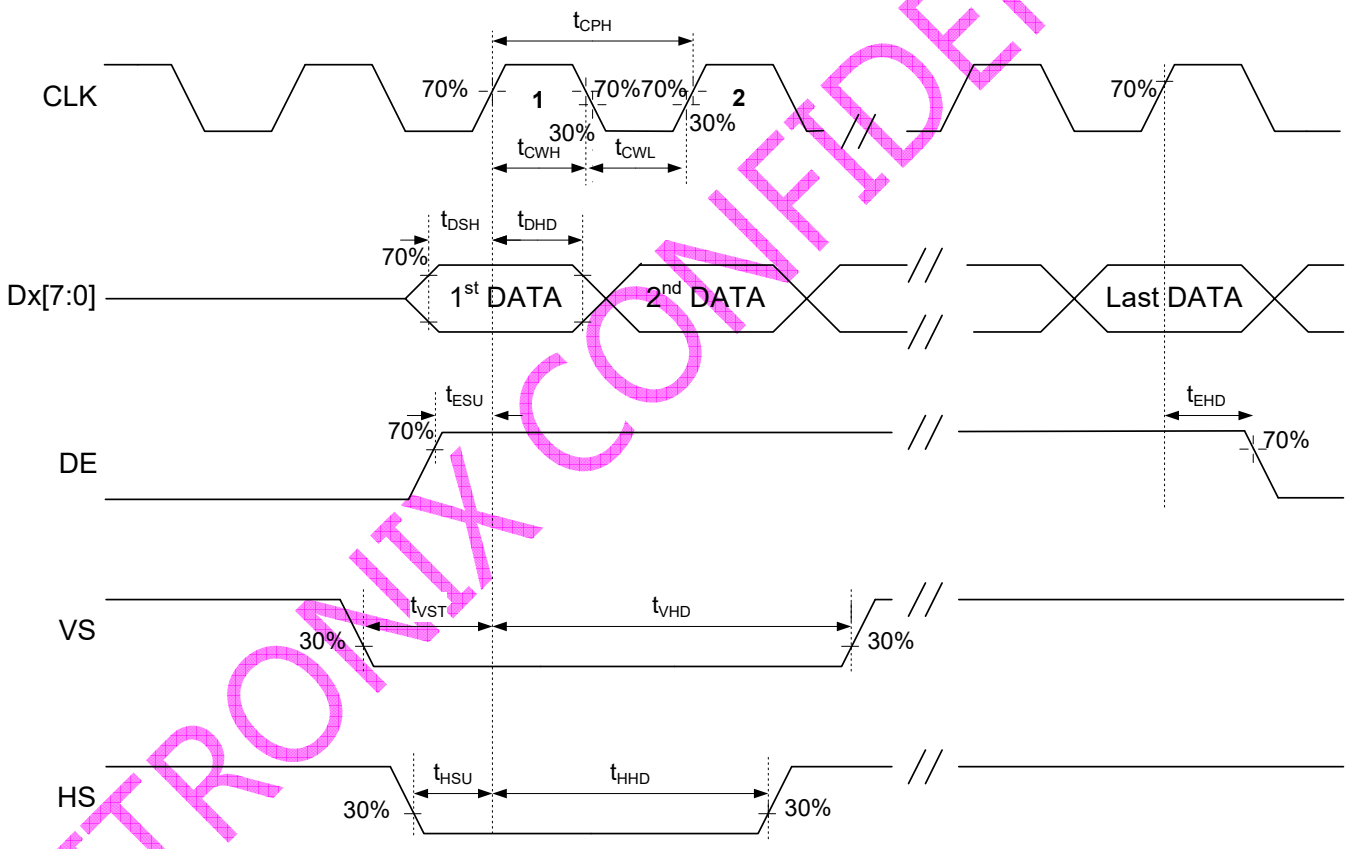
Source output load condition



CMOS TCON mode AC Electrical Characteristics

(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
CLK cycle time	t_{CPH}	16.7			ns	
CLK pulse high duty	t_{CWH}	40	50	60	%	
CLK pulse low duty	t_{CWL}	40	50	60	%	
VS setup time	t_{VST}	4	-	-	ns	
VS hold time	t_{VHD}	2	-	-	ns	
HS setup time	t_{HST}	4	-	-	ns	
HS hold time	t_{HHD}	2	-	-	ns	
Data setup time	t_{DSH}	4	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to CLK
Date hold time	t_{DHD}	2	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to CLK
DE setup time	t_{ESU}	4	-	-	ns	
DE hold time	t_{EHD}	2	-	-	ns	

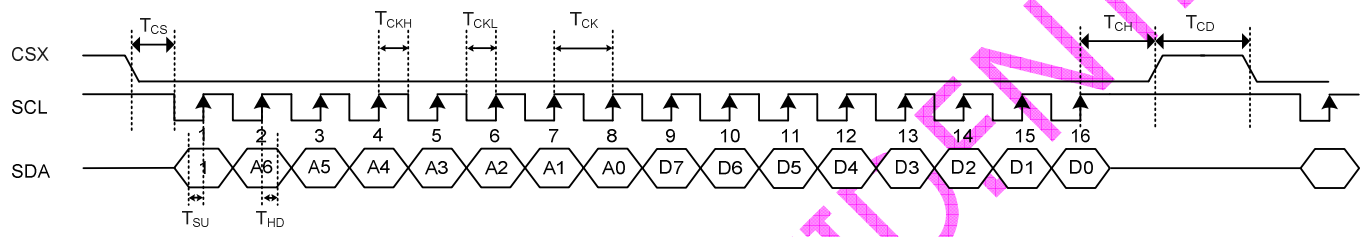


Note: Upper timing diagram CLK_POL=H, DE_POL=L, VS_POL=L, HS_POL=L

SPI interface timing

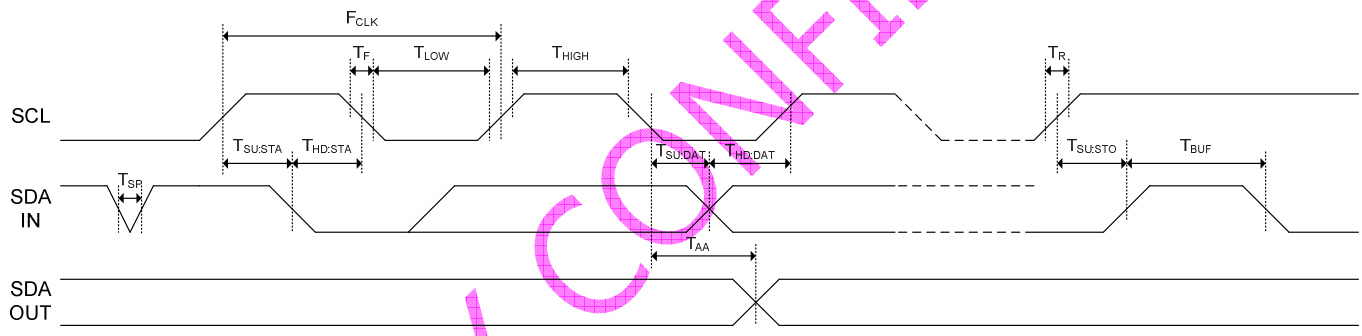
(VDD=VDD_LVDS=3.0~3.6V, GND=GND_LVDS=0V, TA=-20~85℃)

Parameter	Symbol	Min	Typ.	Max.		Condition
SCL period	T_{CK}	60			ns	
SCL high width	T_{CKH}	30			ns	
SCL low width	T_{CKL}	30			ns	
Data setup time	T_{SU}	12			ns	
Data hold time	T_{HD}	12			ns	
CSX to SCL setup time	T_{CS}	20			ns	
CSX to SDA hold time	T_{CH}	20			ns	
CSX high pulse width	T_{CD}	50			ns	



I²C interface timing

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Clock frequency	FCLK			400	kHz	
Clock high time	THIGH	600			ns	
Clock low time	TLOW	1300			ns	
SDA and SCL rise time	TR			300	ns	
SDA and SCL fall time	TF			300	ns	
Start condition hold time	THD:STA	600			ns	
Start condition setup time	TSU:STA	600			ns	
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	100			ns	
Stop condition setup time	TSU:STO	600			ns	
Output valid from clock	TAA			900	ns	
Bus free-time: Time the bus must be free before a new transmission can start	TBUF	1300			ns	
Input filter spike suppression (SDA and SCL pins)	TSP			50	ns	

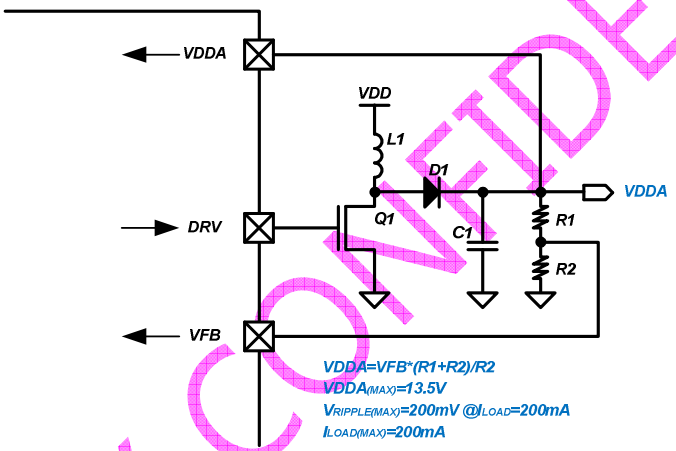


Power circuit

PWM booster for VDDA voltage

(VDD=3.3V, VDDA=10V, TA=-20~85℃, typical values ar e at TA=30℃ unless otherwise noted)

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Booster output voltage	VDDA	8		13.5	V	
Output ripple voltage	V_{RIPPLE}	-	-	100	mV	I_{LOAD}=200mA
PWM output current load	I_{LOAD}	-	-	200	mA	
DRV output voltage for PWM	V_{DRV}	0	-	VDD	V	
Feedback regulation voltage	V_{FB}	1.15	1.2	1.25	V	
Feedback input bias current	I_{FB}	-	-	0.1	uA	V_{FB}=1.2V
Duty cycle maximum	D_{MAX}	-	-	85	%	
PWM DRV frequency	f_{DRV}	720	900	1080	kHz	PWMF[2:0]=100, TA=30℃
PWM DRV period	t_{DRV}	-	$1/f_{DRV}$	-	-	
Soft Start Time	$t_{SOFT-START}$	0.5	-	2	mS	
Line regulation	-	3			%/V	VDD=3.0~3.6V, VDDA=10V, I_{LOAD}=10mA
Load regulation	-	13.05			%/A	VDD=3.3V, I_{LOAD}=1~200mA

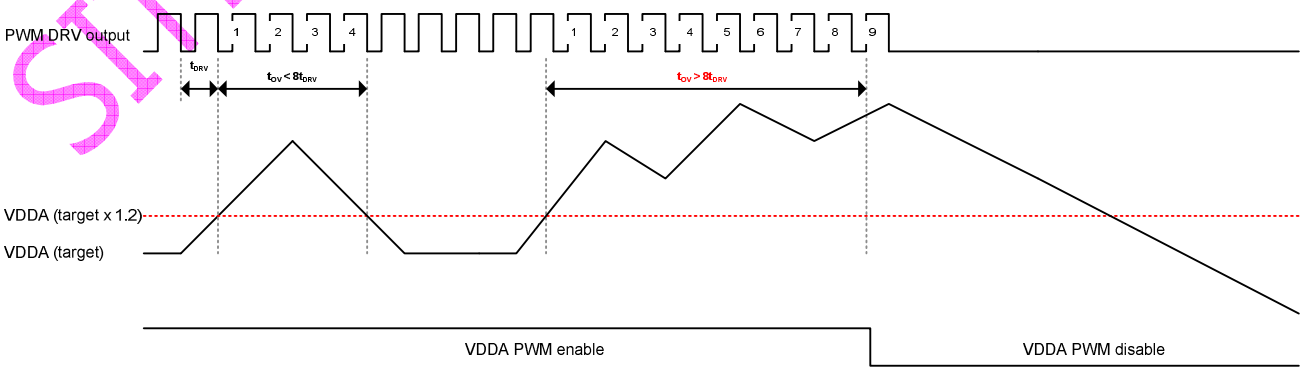


VDDA PWM booster Over Voltage Protection (OVP)

There is a software bit OVP_EN for PWM over voltage protection control.
When OVP_EN=1, VDDA voltage > Target x 1.2 and holding time > 8 t_{DRV} then the PWM booster will be shut down immediately to protect internal circuit. User have to reset again to escape protection mechanism.

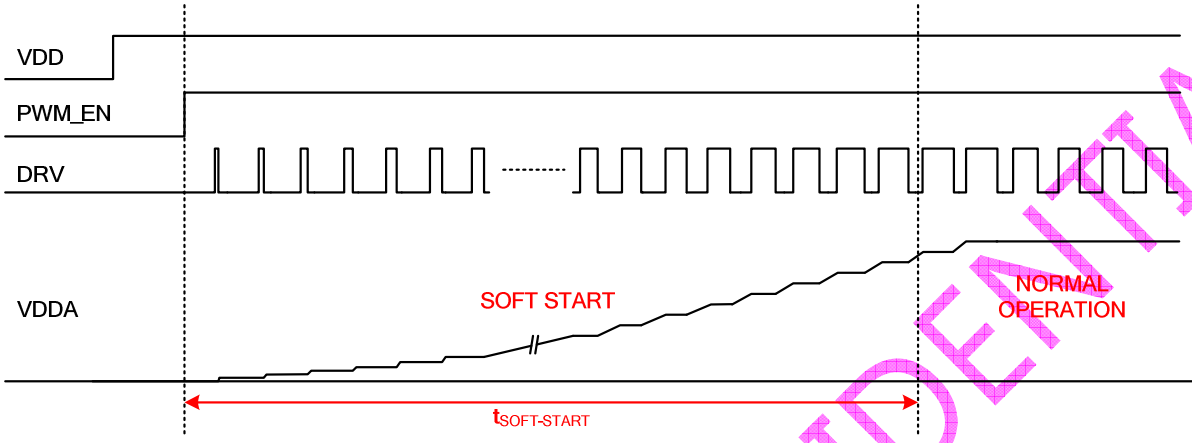
OVP_EN : over voltage protection enable control
H : enable
L : disable

Note : t_{DRV} period is related to PWMF[2:0] setting (0.18 ~ 1.44MHz)



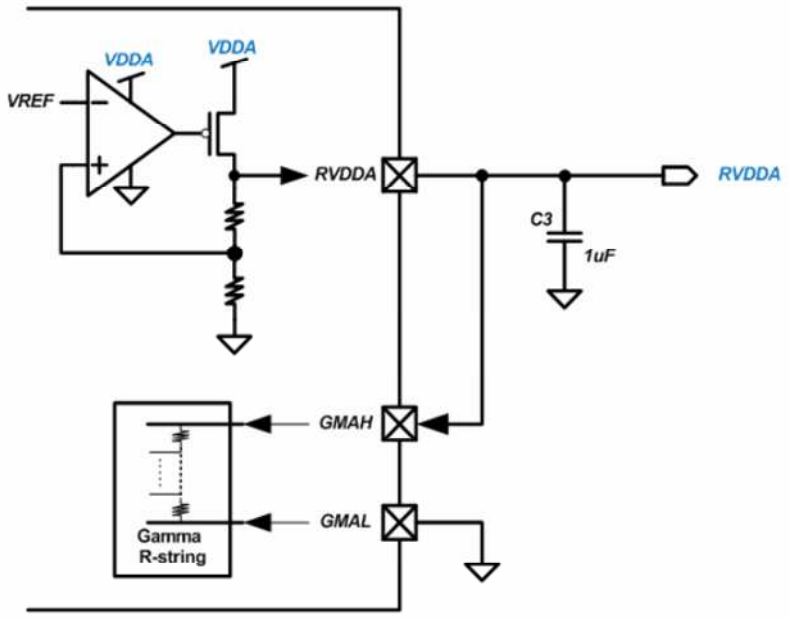
PWM Soft Start

When PWM_EN='1', boost regulator go into soft-start state at first. In this state, DRV pin outputs the soft-start pulse which the duty increases with time (remains $t_{SOFT-START}$) to avoid inrush current.
After the soft-start state, boost regulator will go into normal operation.



RVDDA LDO for Gamma voltage

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Regulator output voltage	RVDDA	VDDA-2.5V	-	VDDA-0.5	V	RV_{LOAD}=5mA
RVDDA output current load	RV_{LOAD}	-	-	5	mA	
RVDDA load regulation	RV_{DROP}	-	-	100	mV	RV_{LOAD}=0 to 5mA



RV[5:0]	RVDDA voltage
000000	7.1V
000001	7.2V
⋮	⋮
011111	10.3V
100000	10.4V
⋮	⋮
111110	13.3V
111111	13.4V

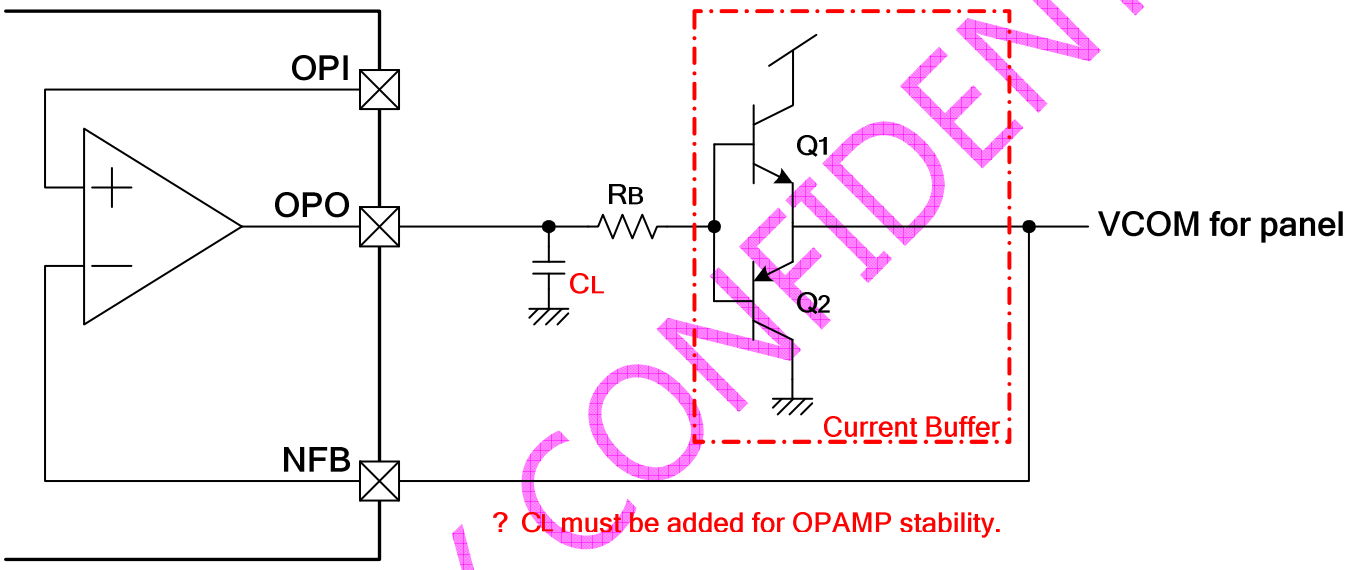
Note : VDDA-2.5V ≦ RVDDA ≦ VDDA-0.5V (Max. = 13.0V)

Voltage buffer for Vcom voltage

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Voltage buffer input voltage	V_{OPI}	0.1	-	VDDA-0.1	V	
Voltage buffer output voltage	V_{OPO}	V_{OPI}-0.05	-	V_{OPI}+0.05	V	
Voltage buffer output current	I_{VBUF}	-	-	30	mA	V_{OPO} = 5V force 4.9 or 5.1V @VDDA=13.5V
Slew rate	SR	-	1	-	V/us	V_{OPO} : 10% to 90%, C_{LOAD}=0.1uF @VDDA=13.5V

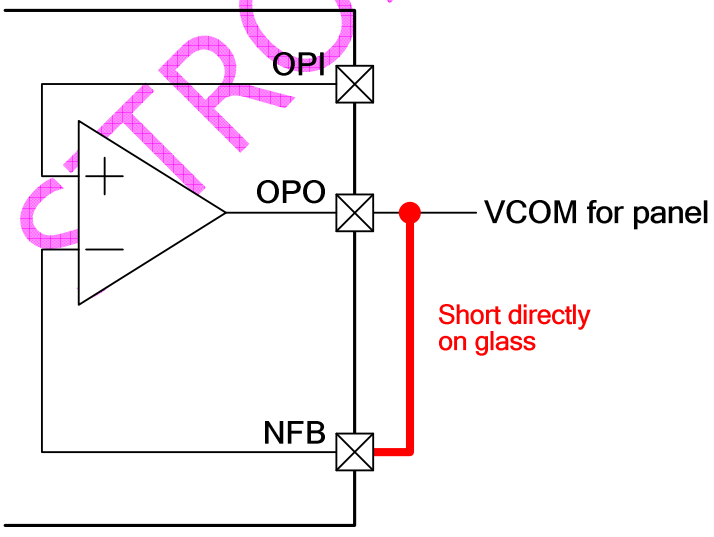
Because of panel loading difference, SC5004 internal Vcom buffer driving ability may not enough, so we proposed 2 kinds of connection for different demands.

For large panel loading(if SC5004 OPAMP driving current is not enough)



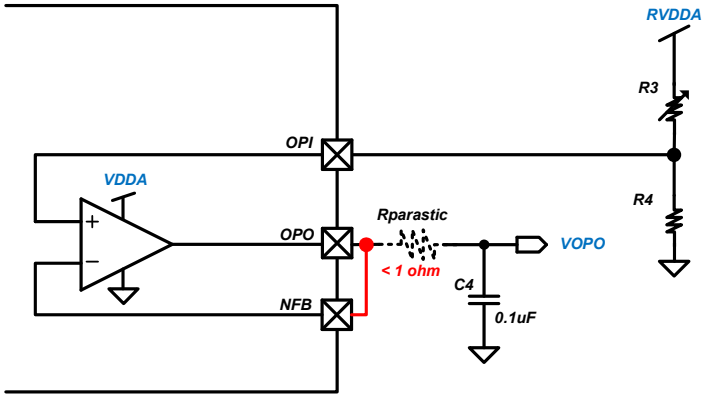
? CL must be added for OPAMP stability.

For normal panel loading



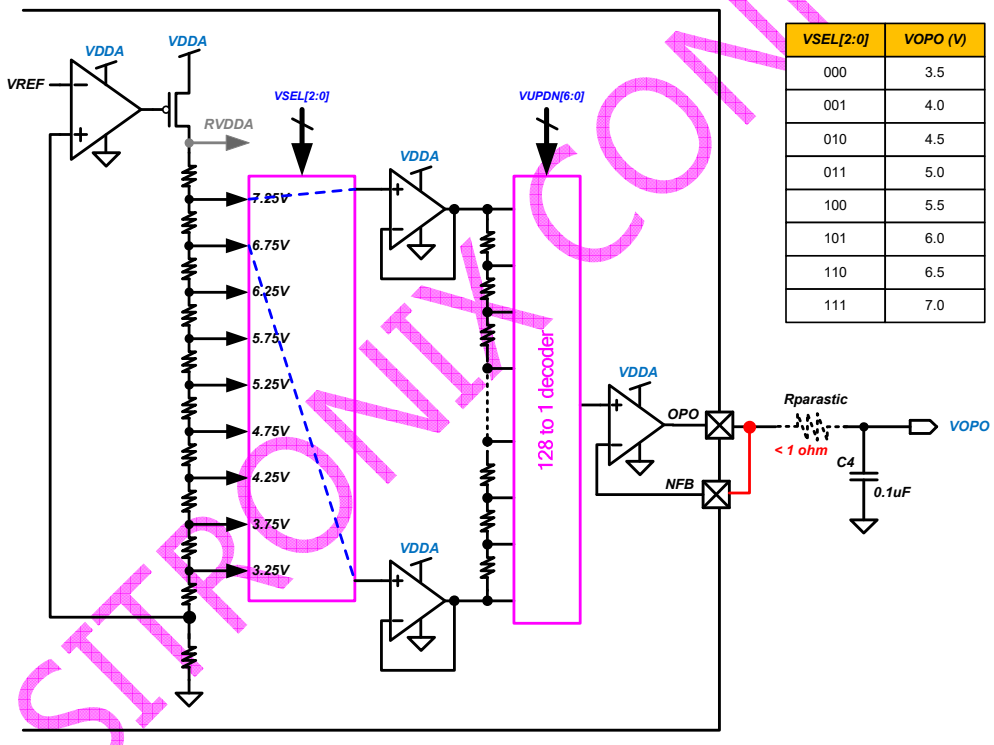
Voltage buffer application type 1 (analog adjustment)

User can select type 1 (Register: VB_TYPE=1) analog adjust method for voltage buffer input voltage control.



Voltage buffer application type 2 (digital adjustment)

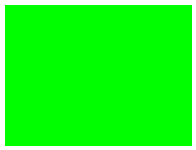
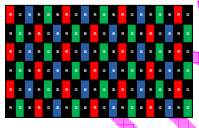
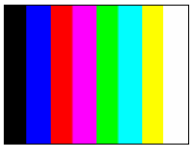
User can select type 2 (Register: VB_TYPE=0) digital adjust method with register VSEL[2:0] and VUPDN[6:0] for input voltage control.



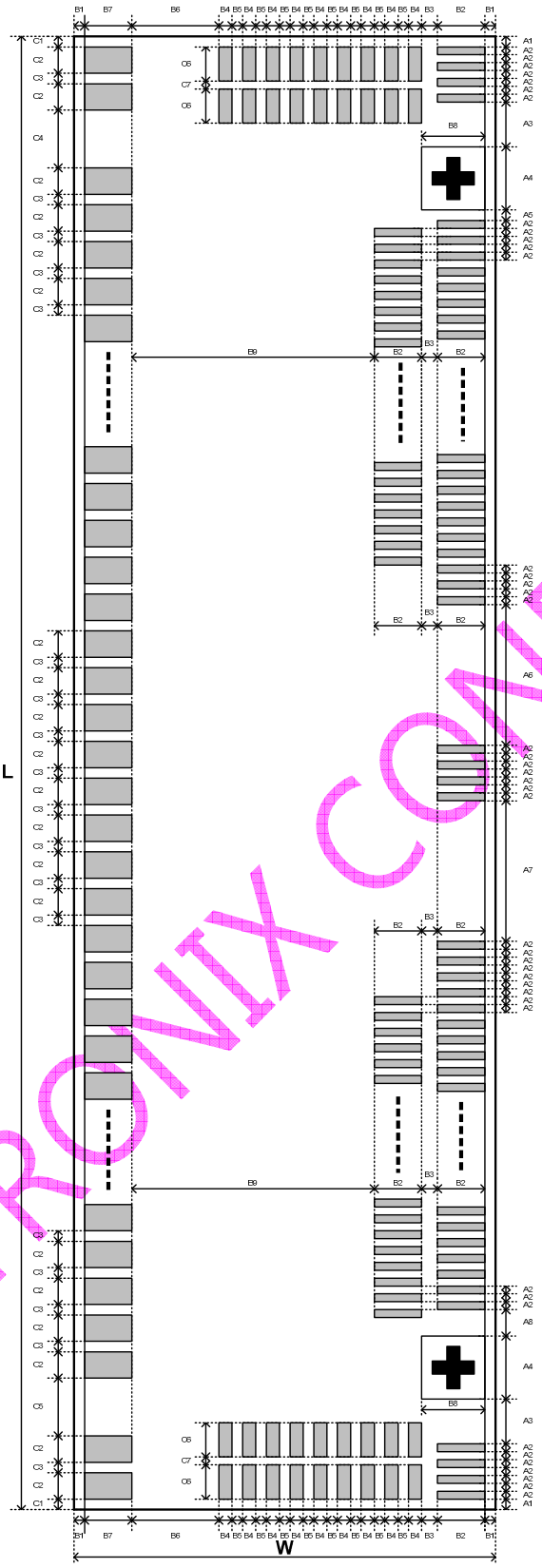
VSEL[2:0]	VOPO (V)
000	3.5
001	4.0
010	4.5
011	5.0
100	5.5
101	6.0
110	6.5
111	7.0

VUPDN[6:0]	VOPO (V)
0000000	-320mV
0000001	-315mV
⋮	⋮
0111110	-10mV
0111111	- 5 mV
1000000	Default
1000001	+ 5 mV
1000010	+10mV
⋮	⋮
1111110	+310mV
1111111	+315mV

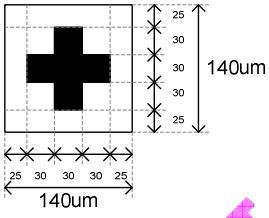
BIST Pattern

BIST_PAT[3:0]	Pattern	Test Function Description	Notice
0000		Black pattern	
0001		Color R alignment with color filter.	
0010		Color G alignment with color filter.	
0011		Color B alignment with color filter.	
0100		White Pattern.	
0101		Flicker Pattern	Depend on INV[1:0] setting
0110		Border pattern.	
0111		256 gray color	
1000		Vertical 8 color bar	
others	0000 → 1000	Auto run	

Chip Outline Dimensions



Alignment mark dimension



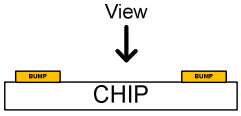
BUMP PAD dimension

Type	Size (um)
	115x18
	30x80
	100x60

Chip outline dimension

Type	Dimension (um)
A1	17
A2	18
A3	99
A4	140
A5	34
A6	335
A7	317
A8	52
B1	17
B2	115
B3	30
B4	30
B5	24
B6	179
B7	100
B8	140
B9	526
C1	19.5
C2	60
C3	25
C4	143
C5	163
C6	80
C7	20

	Min	Typical	Max
W	-30	950	+40
L	-30	24950	+40



Pad Coordination

No.	PAD name	X	Y	Width	Height
1	SHIELDING	-12434	385.5	18	115
2	GSDR	-12403	283	80	30
3	GSDR	-12303	283	80	30
4	CUTR	-12403	229	80	30
5	CUTR	-12303	229	80	30
6	XONR	-12403	175	80	30
7	XONR	-12303	175	80	30
8	OEVR	-12403	121	80	30
9	OEVR	-12303	121	80	30
10	UDR	-12403	67	80	30
11	UDR	-12303	67	80	30
12	CKVR	-12403	13	80	30
13	CKVR	-12303	13	80	30
14	STV2R	-12403	-41	80	30
15	STV2R	-12303	-41	80	30
16	STV1R	-12403	-95	80	30
17	STV1R	-12303	-95	80	30
18	SHIELDING	-12403	-149	80	30
19	SHIELDING	-12303	-149	80	30
20	SHIELDING	-12410.5	-393	60	100
21	SHIELDING	-12325.5	-393	60	100
22	COMR_B	-12122.5	-393	60	100
23	COMR_B	-12037.5	-393	60	100
24	MEAS1R	-11952.5	-393	60	100
25	MEAS2R	-11867.5	-393	60	100
26	VDD_MTP	-11782.5	-393	60	100
27	VDD_MTP	-11697.5	-393	60	100
28	VDD_MTP	-11612.5	-393	60	100
29	VDD_MTP	-11527.5	-393	60	100
30	VDDA	-11442.5	-393	60	100
31	VDDA	-11357.5	-393	60	100
32	VDDA	-11272.5	-393	60	100
33	VDDA	-11187.5	-393	60	100
34	GNDA	-11102.5	-393	60	100
35	GNDA	-11017.5	-393	60	100
36	GNDA	-10932.5	-393	60	100
37	GNDA	-10847.5	-393	60	100
38	GMAH	-10762.5	-393	60	100
39	GMAH	-10677.5	-393	60	100
40	GMAH	-10592.5	-393	60	100
41	GMAH	-10507.5	-393	60	100
42	GMAL	-10422.5	-393	60	100
43	GMAL	-10337.5	-393	60	100
44	GMAL	-10252.5	-393	60	100
45	GMAL	-10167.5	-393	60	100
46	GND	-10082.5	-393	60	100
47	GND	-9997.5	-393	60	100
48	GND	-9912.5	-393	60	100
49	GND	-9827.5	-393	60	100
50	VDD	-9742.5	-393	60	100
51	VDD	-9657.5	-393	60	100
52	VDD	-9572.5	-393	60	100
53	VDD	-9487.5	-393	60	100
54	SHIELDING	-9402.5	-393	60	100
55	SHIELDING	-9317.5	-393	60	100
56	SHIELDING	-9232.5	-393	60	100
57	GND_DMY	-9147.5	-393	60	100
58	SW_CTRL	-9062.5	-393	60	100
59	VDD_DMY	-8977.5	-393	60	100
60	CID[0]	-8892.5	-393	60	100
61	GND_DMY	-8807.5	-393	60	100
62	CID[1]	-8722.5	-393	60	100
63	VDD_DMY	-8637.5	-393	60	100
64	MASTER	-8552.5	-393	60	100
65	GND_DMY	-8467.5	-393	60	100
66	MASLOC	-8382.5	-393	60	100
67	VDD_DMY	-8297.5	-393	60	100
68	IF_SEL[0]	-8212.5	-393	60	100
69	GND_DMY	-8127.5	-393	60	100
70	IF_SEL[1]	-8042.5	-393	60	100

No.	PAD name	X	Y	Width	Height
71	VDD_DMY	-7957.5	-393	60	100
72	IPOR_ENB	-7872.5	-393	60	100
73	GND_DMY	-7787.5	-393	60	100
74	EEP_EN	-7702.5	-393	60	100
75	VDD_DMY	-7617.5	-393	60	100
76	MTP_EN	-7532.5	-393	60	100
77	GND_DMY	-7447.5	-393	60	100
78	ROM_RLB	-7362.5	-393	60	100
79	VDD_DMY	-7277.5	-393	60	100
80	SHIELDING	-7192.5	-393	60	100
81	CSB	-7107.5	-393	60	100
82	SDA	-7022.5	-393	60	100
83	SCL	-6937.5	-393	60	100
84	SHIELDING	-6852.5	-393	60	100
85	GND_DMY	-6767.5	-393	60	100
86	SPI_I2C	-6682.5	-393	60	100
87	VDD_DMY	-6597.5	-393	60	100
88	TCON	-6512.5	-393	60	100
89	GND_DMY	-6427.5	-393	60	100
90	BIT6	-6342.5	-393	60	100
91	VDD_DMY	-6257.5	-393	60	100
92	DISP_ON	-6172.5	-393	60	100
93	GND_DMY	-6087.5	-393	60	100
94	VDD	-6002.5	-393	60	100
95	VDD	-5917.5	-393	60	100
96	VDD	-5832.5	-393	60	100
97	VDD	-5747.5	-393	60	100
98	GND	-5662.5	-393	60	100
99	GND	-5577.5	-393	60	100
100	GND	-5492.5	-393	60	100
101	GND	-5407.5	-393	60	100
102	SHIELDING	-5322.5	-393	60	100
103	SHIELDING	-5237.5	-393	60	100
104	GNDA	-5152.5	-393	60	100
105	GNDA	-5067.5	-393	60	100
106	GNDA	-4982.5	-393	60	100
107	GNDA	-4897.5	-393	60	100
108	VDDA	-4812.5	-393	60	100
109	VDDA	-4727.5	-393	60	100
110	VDDA	-4642.5	-393	60	100
111	VDDA	-4557.5	-393	60	100
112	VDD_DMY	-4472.5	-393	60	100
113	LR	-4387.5	-393	60	100
114	GND_DMY	-4302.5	-393	60	100
115	UD	-4217.5	-393	60	100
116	VDD_DMY	-4132.5	-393	60	100
117	LVDS_SWAP	-4047.5	-393	60	100
118	GND_DMY	-3962.5	-393	60	100
119	MODE	-3877.5	-393	60	100
120	VDD_DMY	-3792.5	-393	60	100
121	NBW	-3707.5	-393	60	100
122	GND_DMY	-3622.5	-393	60	100
123	RSDS_HF	-3537.5	-393	60	100
124	VDD_DMY	-3452.5	-393	60	100
125	CLK_POL	-3367.5	-393	60	100
126	GND_DMY	-3282.5	-393	60	100
127	VS_POL	-3197.5	-393	60	100
128	VDD_DMY	-3112.5	-393	60	100
129	EIO2	-3027.5	-393	60	100
130	EIO2	-2942.5	-393	60	100
131	EIO2	-2857.5	-393	60	100
132	GND_DMY	-2772.5	-393	60	100
133	DE_LD	-2687.5	-393	60	100
134	VDD_DMY	-2602.5	-393	60	100
135	OHP_EN	-2517.5	-393	60	100
136	GND_DMY	-2432.5	-393	60	100
137	BIST	-2347.5	-393	60	100
138	VDD_DMY	-2262.5	-393	60	100
139	RES[0]	-2177.5	-393	60	100
140	GND_DMY	-2092.5	-393	60	100

No.	PAD name	X	Y	Width	Height
141	RES[1]	-2007.5	-393	60	100
142	VDD_DMY	-1922.5	-393	60	100
143	RES[2]	-1837.5	-393	60	100
144	GND_DMY	-1752.5	-393	60	100
145	RES[3]	-1667.5	-393	60	100
146	VDD_DMY	-1582.5	-393	60	100
147	HS_REV	-1497.5	-393	60	100
148	GND_DMY	-1412.5	-393	60	100
149	GND_LVDS	-1327.5	-393	60	100
150	GND_LVDS	-1242.5	-393	60	100
151	GND_LVDS	-1157.5	-393	60	100
152	GND_LVDS	-1072.5	-393	60	100
153	GND_LVDS	-987.5	-393	60	100
154	D27	-902.5	-393	60	100
155	D26	-817.5	-393	60	100
156	DASHD	-732.5	-393	60	100
157	D25	-647.5	-393	60	100
158	D24	-562.5	-393	60	100
159	DASHD	-477.5	-393	60	100
160	D23	-392.5	-393	60	100
161	D22	-307.5	-393	60	100
162	DASHD	-222.5	-393	60	100
163	D21	-137.5	-393	60	100
164	D20	-52.5	-393	60	100
165	DASHD	32.5	-393	60	100
166	CLKP	117.5	-393	60	100
167	CLKN	202.5	-393	60	100
168	DASHD	287.5	-393	60	100
169	D17	372.5	-393	60	100
170	D16	457.5	-393	60	100
171	DASHD	542.5	-393	60	100
172	D15	627.5	-393	60	100
173	D14	712.5	-393	60	100
174	DASHD	797.5	-393	60	100
175	D13	882.5	-393	60	100
176	D12	967.5	-393	60	100
177	DASHD	1052.5	-393	60	100
178	D11	1137.5	-393	60	100
179	D10	1222.5	-393	60	100
180	DASHD	1307.5	-393	60	100
181	D07	1392.5	-393	60	100
182	D06	1477.5	-393	60	100
183	DASHD	1562.5	-393	60	100
184	D05	1647.5	-393	60	100
185	D04	1732.5	-393	60	100
186	DASHD	1817.5	-393	60	100
187	D03	1902.5	-393	60	100
188	D02	1987.5	-393	60	100
189	DASHD	2072.5	-393	60	100
190	D01	2157.5	-393	60	100
191	D00	2242.5	-393	60	100
192	DASHD	2327.5	-393	60	100
193	VDD_LVDS	2412.5	-393	60	100
194	VDD_LVDS	2497.5	-393	60	100
195	VDD_LVDS	2582.5	-393	60	100
196	VDD_LVDS	2667.5	-393	60	100
197	VDD_LVDS	2752.5	-393	60	100
198	VDD_DMY	2837.5	-393	60	100
199	EIO1	2922.5	-393	60	100
200	EIO1	3007.5	-393	60	100
201	EIO1	3092.5	-393	60	100
202	GND_DMY	3177.5	-393	60	100
203	OVER_HEAT	3262.5	-393	60	100
204	HEATER	3347.5	-393	60	100
205	DFB	3432.5	-393	60	100
206	GND_DMY	3517.5	-393	60	100
207	VDD	3602.5	-393	60	100
208	VDD	3687.5	-393	60	100
209	VDD	3772.5	-393	60	100
210	VDD	3857.5	-393	60	100

No.	PAD name	X	Y	Width	Height
211	GND	3942.5	-393	60	100
212	GND	4027.5	-393	60	100
213	GND	4112.5	-393	60	100
214	GND	4197.5	-393	60	100
215	GNDA	4282.5	-393	60	100
216	GNDA	4367.5	-393	60	100
217	GNDA	4452.5	-393	60	100
218	GNDA	4537.5	-393	60	100
219	VDDA	4622.5	-393	60	100
220	VDDA	4707.5	-393	60	100
221	VDDA	4792.5	-393	60	100
222	VDDA	4877.5	-393	60	100
223	RSTB	4962.5	-393	60	100
224	VDD_DMY	5047.5	-393	60	100
225	STBYB	5132.5	-393	60	100
226	GND_DMY	5217.5	-393	60	100
227	PON_STV	5302.5	-393	60	100
228	VDD_DMY	5387.5	-393	60	100
229	POFF_CKV	5472.5	-393	60	100
230	GND_DMY	5557.5	-393	60	100
231	DIMI	5642.5	-393	60	100
232	VDD_DMY	5727.5	-393	60	100
233	DIMO	5812.5	-393	60	100
234	GND_DMY	5897.5	-393	60	100
235	MLSB	5982.5	-393	60	100
236	VDD_DMY	6067.5	-393	60	100
237	BGR	6152.5	-393	60	100
238	GND_DMY	6237.5	-393	60	100
239	TS_EN	6322.5	-393	60	100
240	VDD_DMY	6407.5	-393	60	100
241	TP[1]	6492.5	-393	60	100
242	TP[2]	6577.5	-393	60	100
243	TP[3]	6662.5	-393	60	100
244	TP[4]	6747.5	-393	60	100
245	GND_DMY	6832.5	-393	60	100
246	TP[5]	6917.5	-393	60	100
247	TP[6]	7002.5	-393	60	100
248	TP[7]	7087.5	-393	60	100
249	TP[8]	7172.5	-393	60	100
250	TP[9]	7257.5	-393	60	100
251	TP[10]	7342.5	-393	60	100
252	TP[11]	7427.5	-393	60	100
253	TP[12]	7512.5	-393	60	100
254	TP[13]	7597.5	-393	60	100
255	TP[14]	7682.5	-393	60	100
256	TP[15]	7767.5	-393	60	100
257	TP[16]	7852.5	-393	60	100
258	TP[17]	7937.5	-393	60	100
259	GND_DMY	8022.5	-393	60	100
260	PWM_EN	8107.5	-393	60	100
261	VDD_DMY	8192.5	-393	60	100
262	GSD_EN	8277.5	-393	60	100
263	GND_DMY	8362.5	-393	60	100
264	LDO_EN	8447.5	-393	60	100
265	VDD_DMY	8532.5	-393	60	100
266	VBUF_EN	8617.5	-393	60	100
267	GND_DMY	8702.5	-393	60	100
268	SHIELDING	8787.5	-393	60	100
269	SHIELDING	8872.5	-393	60	100
270	SHIELDING	8957.5	-393	60	100
271	VDDA	9042.5	-393	60	100
272	VDDA	9127.5	-393	60	100
273	VDDA	9212.5	-393	60	100
274	VDDA	9297.5	-393	60	100
275	GNDA	9382.5	-393	60	100
276	GNDA	9467.5	-393	60	100
277	GNDA	9552.5	-393	60	100
278	GNDA	9637.5	-393	60	100
279	SHIELDING	9722.5	-393	60	100
280	SHIELDING	9807.5	-393	60	100

No.	PAD name	X	Y	Width	Height
281	GND	9892.5	-393	60	100
282	GND	9977.5	-393	60	100
283	GND	10062.5	-393	60	100
284	GND	10147.5	-393	60	100
285	VDD	10232.5	-393	60	100
286	VDD	10317.5	-393	60	100
287	VDD	10402.5	-393	60	100
288	VDD	10487.5	-393	60	100
289	DASHD	10572.5	-393	60	100
290	TP[18]	10657.5	-393	60	100
291	RVDDA	10742.5	-393	60	100
292	RVDDA	10827.5	-393	60	100
293	DASHD	10912.5	-393	60	100
294	DRV	10997.5	-393	60	100
295	DRV	11082.5	-393	60	100
296	DASHD	11167.5	-393	60	100
297	VFB	11252.5	-393	60	100
298	DASHD	11337.5	-393	60	100
299	OPI	11422.5	-393	60	100
300	DASHD	11507.5	-393	60	100
301	NFB	11592.5	-393	60	100
302	OPO	11677.5	-393	60	100
303	OPO	11762.5	-393	60	100
304	MEAS1L	11847.5	-393	60	100
305	MEAS2L	11932.5	-393	60	100
306	COML_B	12017.5	-393	60	100
307	COML_B	12102.5	-393	60	100
308	SHIELDING	12325.5	-393	60	100
309	SHIELDING	12410.5	-393	60	100
310	SHIELDING	12303	-149	80	30
311	SHIELDING	12403	-149	80	30
312	STV2L	12303	-95	80	30
313	STV2L	12403	-95	80	30
314	STV1L	12303	-41	80	30
315	STV1L	12403	-41	80	30
316	CKVL	12303	13	80	30
317	CKVL	12403	13	80	30
318	UDL	12303	67	80	30
319	UDL	12403	67	80	30
320	OEVL	12303	121	80	30
321	OEVL	12403	121	80	30
322	XONL	12303	175	80	30
323	XONL	12403	175	80	30
324	CUTL	12303	229	80	30
325	CUTL	12403	229	80	30
326	GSDL	12303	283	80	30
327	GSDL	12403	283	80	30
328	SHIELDING	12434	385.5	18	115
329	COML_T	12398	385.5	18	115
330	COML_T	12362	385.5	18	115
331	SHIELDING	12326	385.5	18	115
332	ALIGNMENT_MARK_L	12148	377	90	90
333	SO[1]	12035	240.5	18	115
334	SO[2]	12017	385.5	18	115
335	SO[3]	11999	240.5	18	115
336	SO[4]	11981	385.5	18	115
337	SO[5]	11963	240.5	18	115
338	SO[6]	11945	385.5	18	115
339	SO[7]	11927	240.5	18	115
340	SO[8]	11909	385.5	18	115
341	SO[9]	11891	240.5	18	115
342	SO[10]	11873	385.5	18	115
343	SO[11]	11855	240.5	18	115
344	SO[12]	11837	385.5	18	115
345	SO[13]	11819	240.5	18	115
346	SO[14]	11801	385.5	18	115
347	SO[15]	11783	240.5	18	115
348	SO[16]	11765	385.5	18	115
349	SO[17]	11747	240.5	18	115
350	SO[18]	11729	385.5	18	115

No.	PAD name	X	Y	Width	Height
351	SO[19]	11711	240.5	18	115
352	SO[20]	11693	385.5	18	115
353	SO[21]	11675	240.5	18	115
354	SO[22]	11657	385.5	18	115
355	SO[23]	11639	240.5	18	115
356	SO[24]	11621	385.5	18	115
357	SO[25]	11603	240.5	18	115
358	SO[26]	11585	385.5	18	115
359	SO[27]	11567	240.5	18	115
360	SO[28]	11549	385.5	18	115
361	SO[29]	11531	240.5	18	115
362	SO[30]	11513	385.5	18	115
363	SO[31]	11495	240.5	18	115
364	SO[32]	11477	385.5	18	115
365	SO[33]	11459	240.5	18	115
366	SO[34]	11441	385.5	18	115
367	SO[35]	11423	240.5	18	115
368	SO[36]	11405	385.5	18	115
369	SO[37]	11387	240.5	18	115
370	SO[38]	11369	385.5	18	115
371	SO[39]	11351	240.5	18	115
372	SO[40]	11333	385.5	18	115
373	SO[41]	11315	240.5	18	115
374	SO[42]	11297	385.5	18	115
375	SO[43]	11279	240.5	18	115
376	SO[44]	11261	385.5	18	115
377	SO[45]	11243	240.5	18	115
378	SO[46]	11225	385.5	18	115
379	SO[47]	11207	240.5	18	115
380	SO[48]	11189	385.5	18	115
381	SO[49]	11171	240.5	18	115
382	SO[50]	11153	385.5	18	115
383	SO[51]	11135	240.5	18	115
384	SO[52]	11117	385.5	18	115
385	SO[53]	11099	240.5	18	115
386	SO[54]	11081	385.5	18	115
387	SO[55]	11063	240.5	18	115
388	SO[56]	11045	385.5	18	115
389	SO[57]	11027	240.5	18	115
390	SO[58]	11009	385.5	18	115
391	SO[59]	10991	240.5	18	115
392	SO[60]	10973	385.5	18	115
393	SO[61]	10955	240.5	18	115
394	SO[62]	10937	385.5	18	115
395	SO[63]	10919	240.5	18	115
396	SO[64]	10901	385.5	18	115
397	SO[65]	10883	240.5	18	115
398	SO[66]	10865	385.5	18	115
399	SO[67]	10847	240.5	18	115
400	SO[68]	10829	385.5	18	115
401	SO[69]	10811	240.5	18	115
402	SO[70]	10793	385.5	18	115
403	SO[71]	10775	240.5	18	115
404	SO[72]	10757	385.5	18	115
405	SO[73]	10739	240.5	18	115
406	SO[74]	10721	385.5	18	115
407	SO[75]	10703	240.5	18	115
408	SO[76]	10685	385.5	18	115
409	SO[77]	10667	240.5	18	115
410	SO[78]	10649	385.5	18	115
411	SO[79]	10631	240.5	18	115
412	SO[80]	10613	385.5	18	115
413	SO[81]	10595	240.5	18	115
414	SO[82]	10577	385.5	18	115
415	SO[83]	10559	240.5	18	115
416	SO[84]	10541	385.5	18	115
417	SO[85]	10523	240.5	18	115
418	SO[86]	10505	385.5	18	115
419	SO[87]	10487	240.5	18	115
420	SO[88]	10469	385.5	18	115

No.	PAD name	X	Y	Width	Height
421	SO[89]	10451	240.5	18	115
422	SO[90]	10433	385.5	18	115
423	SO[91]	10415	240.5	18	115
424	SO[92]	10397	385.5	18	115
425	SO[93]	10379	240.5	18	115
426	SO[94]	10361	385.5	18	115
427	SO[95]	10343	240.5	18	115
428	SO[96]	10325	385.5	18	115
429	SO[97]	10307	240.5	18	115
430	SO[98]	10289	385.5	18	115
431	SO[99]	10271	240.5	18	115
432	SO[100]	10253	385.5	18	115
433	SO[101]	10235	240.5	18	115
434	SO[102]	10217	385.5	18	115
435	SO[103]	10199	240.5	18	115
436	SO[104]	10181	385.5	18	115
437	SO[105]	10163	240.5	18	115
438	SO[106]	10145	385.5	18	115
439	SO[107]	10127	240.5	18	115
440	SO[108]	10109	385.5	18	115
441	SO[109]	10091	240.5	18	115
442	SO[110]	10073	385.5	18	115
443	SO[111]	10055	240.5	18	115
444	SO[112]	10037	385.5	18	115
445	SO[113]	10019	240.5	18	115
446	SO[114]	10001	385.5	18	115
447	SO[115]	9983	240.5	18	115
448	SO[116]	9965	385.5	18	115
449	SO[117]	9947	240.5	18	115
450	SO[118]	9929	385.5	18	115
451	SO[119]	9911	240.5	18	115
452	SO[120]	9893	385.5	18	115
453	SO[121]	9875	240.5	18	115
454	SO[122]	9857	385.5	18	115
455	SO[123]	9839	240.5	18	115
456	SO[124]	9821	385.5	18	115
457	SO[125]	9803	240.5	18	115
458	SO[126]	9785	385.5	18	115
459	SO[127]	9767	240.5	18	115
460	SO[128]	9749	385.5	18	115
461	SO[129]	9731	240.5	18	115
462	SO[130]	9713	385.5	18	115
463	SO[131]	9695	240.5	18	115
464	SO[132]	9677	385.5	18	115
465	SO[133]	9659	240.5	18	115
466	SO[134]	9641	385.5	18	115
467	SO[135]	9623	240.5	18	115
468	SO[136]	9605	385.5	18	115
469	SO[137]	9587	240.5	18	115
470	SO[138]	9569	385.5	18	115
471	SO[139]	9551	240.5	18	115
472	SO[140]	9533	385.5	18	115
473	SO[141]	9515	240.5	18	115
474	SO[142]	9497	385.5	18	115
475	SO[143]	9479	240.5	18	115
476	SO[144]	9461	385.5	18	115
477	SO[145]	9443	240.5	18	115
478	SO[146]	9425	385.5	18	115
479	SO[147]	9407	240.5	18	115
480	SO[148]	9389	385.5	18	115
481	SO[149]	9371	240.5	18	115
482	SO[150]	9353	385.5	18	115
483	SO[151]	9335	240.5	18	115
484	SO[152]	9317	385.5	18	115
485	SO[153]	9299	240.5	18	115
486	SO[154]	9281	385.5	18	115
487	SO[155]	9263	240.5	18	115
488	SO[156]	9245	385.5	18	115
489	SO[157]	9227	240.5	18	115
490	SO[158]	9209	385.5	18	115

No.	PAD name	X	Y	Width	Height
491	SO[159]	9191	240.5	18	115
492	SO[160]	9173	385.5	18	115
493	SO[161]	9155	240.5	18	115
494	SO[162]	9137	385.5	18	115
495	SO[163]	9119	240.5	18	115
496	SO[164]	9101	385.5	18	115
497	SO[165]	9083	240.5	18	115
498	SO[166]	9065	385.5	18	115
499	SO[167]	9047	240.5	18	115
500	SO[168]	9029	385.5	18	115
501	SO[169]	9011	240.5	18	115
502	SO[170]	8993	385.5	18	115
503	SO[171]	8975	240.5	18	115
504	SO[172]	8957	385.5	18	115
505	SO[173]	8939	240.5	18	115
506	SO[174]	8921	385.5	18	115
507	SO[175]	8903	240.5	18	115
508	SO[176]	8885	385.5	18	115
509	SO[177]	8867	240.5	18	115
510	SO[178]	8849	385.5	18	115
511	SO[179]	8831	240.5	18	115
512	SO[180]	8813	385.5	18	115
513	SO[181]	8795	240.5	18	115
514	SO[182]	8777	385.5	18	115
515	SO[183]	8759	240.5	18	115
516	SO[184]	8741	385.5	18	115
517	SO[185]	8723	240.5	18	115
518	SO[186]	8705	385.5	18	115
519	SO[187]	8687	240.5	18	115
520	SO[188]	8669	385.5	18	115
521	SO[189]	8651	240.5	18	115
522	SO[190]	8633	385.5	18	115
523	SO[191]	8615	240.5	18	115
524	SO[192]	8597	385.5	18	115
525	SO[193]	8579	240.5	18	115
526	SO[194]	8561	385.5	18	115
527	SO[195]	8543	240.5	18	115
528	SO[196]	8525	385.5	18	115
529	SO[197]	8507	240.5	18	115
530	SO[198]	8489	385.5	18	115
531	SO[199]	8471	240.5	18	115
532	SO[200]	8453	385.5	18	115
533	SO[201]	8435	240.5	18	115
534	SO[202]	8417	385.5	18	115
535	SO[203]	8399	240.5	18	115
536	SO[204]	8381	385.5	18	115
537	SO[205]	8363	240.5	18	115
538	SO[206]	8345	385.5	18	115
539	SO[207]	8327	240.5	18	115
540	SO[208]	8309	385.5	18	115
541	SO[209]	8291	240.5	18	115
542	SO[210]	8273	385.5	18	115
543	SO[211]	8255	240.5	18	115
544	SO[212]	8237	385.5	18	115
545	SO[213]	8219	240.5	18	115
546	SO[214]	8201	385.5	18	115
547	SO[215]	8183	240.5	18	115
548	SO[216]	8165	385.5	18	115
549	SO[217]	8147	240.5	18	115
550	SO[218]	8129	385.5	18	115
551	SO[219]	8111	240.5	18	115
552	SO[220]	8093	385.5	18	115
553	SO[221]	8075	240.5	18	115
554	SO[222]	8057	385.5	18	115
555	SO[223]	8039	240.5	18	115
556	SO[224]	8021	385.5	18	115
557	SO[225]	8003	240.5	18	115
558	SO[226]	7985	385.5	18	115
559	SO[227]	7967	240.5	18	115
560	SO[228]	7949	385.5	18	115

No.	PAD name	X	Y	Width	Height
561	SO[229]	7931	240.5	18	115
562	SO[230]	7913	385.5	18	115
563	SO[231]	7895	240.5	18	115
564	SO[232]	7877	385.5	18	115
565	SO[233]	7859	240.5	18	115
566	SO[234]	7841	385.5	18	115
567	SO[235]	7823	240.5	18	115
568	SO[236]	7805	385.5	18	115
569	SO[237]	7787	240.5	18	115
570	SO[238]	7769	385.5	18	115
571	SO[239]	7751	240.5	18	115
572	SO[240]	7733	385.5	18	115
573	SO[241]	7715	240.5	18	115
574	SO[242]	7697	385.5	18	115
575	SO[243]	7679	240.5	18	115
576	SO[244]	7661	385.5	18	115
577	SO[245]	7643	240.5	18	115
578	SO[246]	7625	385.5	18	115
579	SO[247]	7607	240.5	18	115
580	SO[248]	7589	385.5	18	115
581	SO[249]	7571	240.5	18	115
582	SO[250]	7553	385.5	18	115
583	SO[251]	7535	240.5	18	115
584	SO[252]	7517	385.5	18	115
585	SO[253]	7499	240.5	18	115
586	SO[254]	7481	385.5	18	115
587	SO[255]	7463	240.5	18	115
588	SO[256]	7445	385.5	18	115
589	SO[257]	7427	240.5	18	115
590	SO[258]	7409	385.5	18	115
591	SO[259]	7391	240.5	18	115
592	SO[260]	7373	385.5	18	115
593	SO[261]	7355	240.5	18	115
594	SO[262]	7337	385.5	18	115
595	SO[263]	7319	240.5	18	115
596	SO[264]	7301	385.5	18	115
597	SO[265]	7283	240.5	18	115
598	SO[266]	7265	385.5	18	115
599	SO[267]	7247	240.5	18	115
600	SO[268]	7229	385.5	18	115
601	SO[269]	7211	240.5	18	115
602	SO[270]	7193	385.5	18	115
603	SO[271]	7175	240.5	18	115
604	SO[272]	7157	385.5	18	115
605	SO[273]	7139	240.5	18	115
606	SO[274]	7121	385.5	18	115
607	SO[275]	7103	240.5	18	115
608	SO[276]	7085	385.5	18	115
609	SO[277]	7067	240.5	18	115
610	SO[278]	7049	385.5	18	115
611	SO[279]	7031	240.5	18	115
612	SO[280]	7013	385.5	18	115
613	SO[281]	6995	240.5	18	115
614	SO[282]	6977	385.5	18	115
615	SO[283]	6959	240.5	18	115
616	SO[284]	6941	385.5	18	115
617	SO[285]	6923	240.5	18	115
618	SO[286]	6905	385.5	18	115
619	SO[287]	6887	240.5	18	115
620	SO[288]	6869	385.5	18	115
621	SO[289]	6851	240.5	18	115
622	SO[290]	6833	385.5	18	115
623	SO[291]	6815	240.5	18	115
624	SO[292]	6797	385.5	18	115
625	SO[293]	6779	240.5	18	115
626	SO[294]	6761	385.5	18	115
627	SO[295]	6743	240.5	18	115
628	SO[296]	6725	385.5	18	115
629	SO[297]	6707	240.5	18	115
630	SO[298]	6689	385.5	18	115

No.	PAD name	X	Y	Width	Height
631	SO[299]	6671	240.5	18	115
632	SO[300]	6653	385.5	18	115
633	SO[301]	6635	240.5	18	115
634	SO[302]	6617	385.5	18	115
635	SO[303]	6599	240.5	18	115
636	SO[304]	6581	385.5	18	115
637	SO[305]	6563	240.5	18	115
638	SO[306]	6545	385.5	18	115
639	SO[307]	6527	240.5	18	115
640	SO[308]	6509	385.5	18	115
641	SO[309]	6491	240.5	18	115
642	SO[310]	6473	385.5	18	115
643	SO[311]	6455	240.5	18	115
644	SO[312]	6437	385.5	18	115
645	SO[313]	6419	240.5	18	115
646	SO[314]	6401	385.5	18	115
647	SO[315]	6383	240.5	18	115
648	SO[316]	6365	385.5	18	115
649	SO[317]	6347	240.5	18	115
650	SO[318]	6329	385.5	18	115
651	SO[319]	6311	240.5	18	115
652	SO[320]	6293	385.5	18	115
653	SO[321]	6275	240.5	18	115
654	SO[322]	6257	385.5	18	115
655	SO[323]	6239	240.5	18	115
656	SO[324]	6221	385.5	18	115
657	SO[325]	6203	240.5	18	115
658	SO[326]	6185	385.5	18	115
659	SO[327]	6167	240.5	18	115
660	SO[328]	6149	385.5	18	115
661	SO[329]	6131	240.5	18	115
662	SO[330]	6113	385.5	18	115
663	SO[331]	6095	240.5	18	115
664	SO[332]	6077	385.5	18	115
665	SO[333]	6059	240.5	18	115
666	SO[334]	6041	385.5	18	115
667	SO[335]	6023	240.5	18	115
668	SO[336]	6005	385.5	18	115
669	SO[337]	5987	240.5	18	115
670	SO[338]	5969	385.5	18	115
671	SO[339]	5951	240.5	18	115
672	SO[340]	5933	385.5	18	115
673	SO[341]	5915	240.5	18	115
674	SO[342]	5897	385.5	18	115
675	SO[343]	5879	240.5	18	115
676	SO[344]	5861	385.5	18	115
677	SO[345]	5843	240.5	18	115
678	SO[346]	5825	385.5	18	115
679	SO[347]	5807	240.5	18	115
680	SO[348]	5789	385.5	18	115
681	SO[349]	5771	240.5	18	115
682	SO[350]	5753	385.5	18	115
683	SO[351]	5735	240.5	18	115
684	SO[352]	5717	385.5	18	115
685	SO[353]	5699	240.5	18	115
686	SO[354]	5681	385.5	18	115
687	SO[355]	5663	240.5	18	115
688	SO[356]	5645	385.5	18	115
689	SO[357]	5627	240.5	18	115
690	SO[358]	5609	385.5	18	115
691	SO[359]	5591	240.5	18	115
692	SO[360]	5573	385.5	18	115
693	SO[361]	5555	240.5	18	115
694	SO[362]	5537	385.5	18	115
695	SO[363]	5519	240.5	18	115
696	SO[364]	5501	385.5	18	115
697	SO[365]	5483	240.5	18	115
698	SO[366]	5465	385.5	18	115
699	SO[367]	5447	240.5	18	115
700	SO[368]	5429	385.5	18	115

No.	PAD name	X	Y	Width	Height
701	SO[369]	5411	240.5	18	115
702	SO[370]	5393	385.5	18	115
703	SO[371]	5375	240.5	18	115
704	SO[372]	5357	385.5	18	115
705	SO[373]	5339	240.5	18	115
706	SO[374]	5321	385.5	18	115
707	SO[375]	5303	240.5	18	115
708	SO[376]	5285	385.5	18	115
709	SO[377]	5267	240.5	18	115
710	SO[378]	5249	385.5	18	115
711	SO[379]	5231	240.5	18	115
712	SO[380]	5213	385.5	18	115
713	SO[381]	5195	240.5	18	115
714	SO[382]	5177	385.5	18	115
715	SO[383]	5159	240.5	18	115
716	SO[384]	5141	385.5	18	115
717	SO[385]	5123	240.5	18	115
718	SO[386]	5105	385.5	18	115
719	SO[387]	5087	240.5	18	115
720	SO[388]	5069	385.5	18	115
721	SO[389]	5051	240.5	18	115
722	SO[390]	5033	385.5	18	115
723	SO[391]	5015	240.5	18	115
724	SO[392]	4997	385.5	18	115
725	SO[393]	4979	240.5	18	115
726	SO[394]	4961	385.5	18	115
727	SO[395]	4943	240.5	18	115
728	SO[396]	4925	385.5	18	115
729	SO[397]	4907	240.5	18	115
730	SO[398]	4889	385.5	18	115
731	SO[399]	4871	240.5	18	115
732	SO[400]	4853	385.5	18	115
733	SO[401]	4835	240.5	18	115
734	SO[402]	4817	385.5	18	115
735	SO[403]	4799	240.5	18	115
736	SO[404]	4781	385.5	18	115
737	SO[405]	4763	240.5	18	115
738	SO[406]	4745	385.5	18	115
739	SO[407]	4727	240.5	18	115
740	SO[408]	4709	385.5	18	115
741	SO[409]	4691	240.5	18	115
742	SO[410]	4673	385.5	18	115
743	SO[411]	4655	240.5	18	115
744	SO[412]	4637	385.5	18	115
745	SO[413]	4619	240.5	18	115
746	SO[414]	4601	385.5	18	115
747	SO[415]	4583	240.5	18	115
748	SO[416]	4565	385.5	18	115
749	SO[417]	4547	240.5	18	115
750	SO[418]	4529	385.5	18	115
751	SO[419]	4511	240.5	18	115
752	SO[420]	4493	385.5	18	115
753	SO[421]	4475	240.5	18	115
754	SO[422]	4457	385.5	18	115
755	SO[423]	4439	240.5	18	115
756	SO[424]	4421	385.5	18	115
757	SO[425]	4403	240.5	18	115
758	SO[426]	4385	385.5	18	115
759	SO[427]	4367	240.5	18	115
760	SO[428]	4349	385.5	18	115
761	SO[429]	4331	240.5	18	115
762	SO[430]	4313	385.5	18	115
763	SO[431]	4295	240.5	18	115
764	SO[432]	4277	385.5	18	115
765	SO[433]	4259	240.5	18	115
766	SO[434]	4241	385.5	18	115
767	SO[435]	4223	240.5	18	115
768	SO[436]	4205	385.5	18	115
769	SO[437]	4187	240.5	18	115
770	SO[438]	4169	385.5	18	115

No.	PAD name	X	Y	Width	Height
771	SO[439]	4151	240.5	18	115
772	SO[440]	4133	385.5	18	115
773	SO[441]	4115	240.5	18	115
774	SO[442]	4097	385.5	18	115
775	SO[443]	4079	240.5	18	115
776	SO[444]	4061	385.5	18	115
777	SO[445]	4043	240.5	18	115
778	SO[446]	4025	385.5	18	115
779	SO[447]	4007	240.5	18	115
780	SO[448]	3989	385.5	18	115
781	SO[449]	3971	240.5	18	115
782	SO[450]	3953	385.5	18	115
783	SO[451]	3935	240.5	18	115
784	SO[452]	3917	385.5	18	115
785	SO[453]	3899	240.5	18	115
786	SO[454]	3881	385.5	18	115
787	SO[455]	3863	240.5	18	115
788	SO[456]	3845	385.5	18	115
789	SO[457]	3827	240.5	18	115
790	SO[458]	3809	385.5	18	115
791	SO[459]	3791	240.5	18	115
792	SO[460]	3773	385.5	18	115
793	SO[461]	3755	240.5	18	115
794	SO[462]	3737	385.5	18	115
795	SO[463]	3719	240.5	18	115
796	SO[464]	3701	385.5	18	115
797	SO[465]	3683	240.5	18	115
798	SO[466]	3665	385.5	18	115
799	SO[467]	3647	240.5	18	115
800	SO[468]	3629	385.5	18	115
801	SO[469]	3611	240.5	18	115
802	SO[470]	3593	385.5	18	115
803	SO[471]	3575	240.5	18	115
804	SO[472]	3557	385.5	18	115
805	SO[473]	3539	240.5	18	115
806	SO[474]	3521	385.5	18	115
807	SO[475]	3503	240.5	18	115
808	SO[476]	3485	385.5	18	115
809	SO[477]	3467	240.5	18	115
810	SO[478]	3449	385.5	18	115
811	SO[479]	3431	240.5	18	115
812	SO[480]	3413	385.5	18	115
813	SO[481]	3395	240.5	18	115
814	SO[482]	3377	385.5	18	115
815	SO[483]	3359	240.5	18	115
816	SO[484]	3341	385.5	18	115
817	SO[485]	3323	240.5	18	115
818	SO[486]	3305	385.5	18	115
819	SO[487]	3287	240.5	18	115
820	SO[488]	3269	385.5	18	115
821	SO[489]	3251	240.5	18	115
822	SO[490]	3233	385.5	18	115
823	SO[491]	3215	240.5	18	115
824	SO[492]	3197	385.5	18	115
825	SO[493]	3179	240.5	18	115
826	SO[494]	3161	385.5	18	115
827	SO[495]	3143	240.5	18	115
828	SO[496]	3125	385.5	18	115
829	SO[497]	3107	240.5	18	115
830	SO[498]	3089	385.5	18	115
831	SO[499]	3071	240.5	18	115
832	SO[500]	3053	385.5	18	115
833	SO[501]	3035	240.5	18	115
834	SO[502]	3017	385.5	18	115
835	SO[503]	2999	240.5	18	115
836	SO[504]	2981	385.5	18	115
837	SO[505]	2963	240.5	18	115
838	SO[506]	2945	385.5	18	115
839	SO[507]	2927	240.5	18	115
840	SO[508]	2909	385.5	18	115

No.	PAD name	X	Y	Width	Height
841	SO[509]	2891	240.5	18	115
842	SO[510]	2873	385.5	18	115
843	SO[511]	2855	240.5	18	115
844	SO[512]	2837	385.5	18	115
845	SO[513]	2819	240.5	18	115
846	SO[514]	2801	385.5	18	115
847	SO[515]	2783	240.5	18	115
848	SO[516]	2765	385.5	18	115
849	SO[517]	2747	240.5	18	115
850	SO[518]	2729	385.5	18	115
851	SO[519]	2711	240.5	18	115
852	SO[520]	2693	385.5	18	115
853	SO[521]	2675	240.5	18	115
854	SO[522]	2657	385.5	18	115
855	SO[523]	2639	240.5	18	115
856	SO[524]	2621	385.5	18	115
857	SO[525]	2603	240.5	18	115
858	SO[526]	2585	385.5	18	115
859	SO[527]	2567	240.5	18	115
860	SO[528]	2549	385.5	18	115
861	SO[529]	2531	240.5	18	115
862	SO[530]	2513	385.5	18	115
863	SO[531]	2495	240.5	18	115
864	SO[532]	2477	385.5	18	115
865	SO[533]	2459	240.5	18	115
866	SO[534]	2441	385.5	18	115
867	SO[535]	2423	240.5	18	115
868	SO[536]	2405	385.5	18	115
869	SO[537]	2387	240.5	18	115
870	SO[538]	2369	385.5	18	115
871	SO[539]	2351	240.5	18	115
872	SO[540]	2333	385.5	18	115
873	SO[541]	2315	240.5	18	115
874	SO[542]	2297	385.5	18	115
875	SO[543]	2279	240.5	18	115
876	SO[544]	2261	385.5	18	115
877	SO[545]	2243	240.5	18	115
878	SO[546]	2225	385.5	18	115
879	SO[547]	2207	240.5	18	115
880	SO[548]	2189	385.5	18	115
881	SO[549]	2171	240.5	18	115
882	SO[550]	2153	385.5	18	115
883	SO[551]	2135	240.5	18	115
884	SO[552]	2117	385.5	18	115
885	SO[553]	2099	240.5	18	115
886	SO[554]	2081	385.5	18	115
887	SO[555]	2063	240.5	18	115
888	SO[556]	2045	385.5	18	115
889	SO[557]	2027	240.5	18	115
890	SO[558]	2009	385.5	18	115
891	SO[559]	1991	240.5	18	115
892	SO[560]	1973	385.5	18	115
893	SO[561]	1955	240.5	18	115
894	SO[562]	1937	385.5	18	115
895	SO[563]	1919	240.5	18	115
896	SO[564]	1901	385.5	18	115
897	SO[565]	1883	240.5	18	115
898	SO[566]	1865	385.5	18	115
899	SO[567]	1847	240.5	18	115
900	SO[568]	1829	385.5	18	115
901	SO[569]	1811	240.5	18	115
902	SO[570]	1793	385.5	18	115
903	SO[571]	1775	240.5	18	115
904	SO[572]	1757	385.5	18	115
905	SO[573]	1739	240.5	18	115
906	SO[574]	1721	385.5	18	115
907	SO[575]	1703	240.5	18	115
908	SO[576]	1685	385.5	18	115
909	SO[577]	1667	240.5	18	115
910	SO[578]	1649	385.5	18	115
911	SO[579]	1631	240.5	18	115
912	SO[580]	1613	385.5	18	115
913	SO[581]	1595	240.5	18	115
914	SO[582]	1577	385.5	18	115
915	SO[583]	1559	240.5	18	115
916	SO[584]	1541	385.5	18	115
917	SO[585]	1523	240.5	18	115
918	SO[586]	1505	385.5	18	115
919	SO[587]	1487	240.5	18	115
920	SO[588]	1469	385.5	18	115
921	SO[589]	1451	240.5	18	115
922	SO[590]	1433	385.5	18	115
923	SO[591]	1415	240.5	18	115
924	SO[592]	1397	385.5	18	115
925	SO[593]	1379	240.5	18	115
926	SO[594]	1361	385.5	18	115
927	SO[595]	1343	240.5	18	115
928	SO[596]	1325	385.5	18	115
929	SO[597]	1307	240.5	18	115
930	SO[598]	1289	385.5	18	115
931	SO[599]	1271	240.5	18	115
932	SO[600]	1253	385.5	18	115
933	SO[601]	1235	240.5	18	115
934	SO[602]	1217	385.5	18	115
935	SO[603]	1199	240.5	18	115
936	SO[604]	1181	385.5	18	115
937	SO[605]	1163	240.5	18	115
938	SO[606]	1145	385.5	18	115
939	SO[607]	1127	240.5	18	115
940	SO[608]	1109	385.5	18	115
941	SO[609]	1091	240.5	18	115
942	SO[610]	1073	385.5	18	115
943	SO[611]	1055	240.5	18	115
944	SO[612]	1037	385.5	18	115
945	SO[613]	1019	240.5	18	115
946	SO[614]	1001	385.5	18	115
947	SO[615]	983	240.5	18	115
948	SO[616]	965	385.5	18	115
949	SO[617]	947	240.5	18	115
950	SO[618]	929	385.5	18	115
951	SO[619]	911	240.5	18	115
952	SO[620]	893	385.5	18	115
953	SO[621]	875	240.5	18	115
954	SO[622]	857	385.5	18	115
955	SO[623]	839	240.5	18	115
956	SO[624]	821	385.5	18	115
957	SO[625]	803	240.5	18	115
958	SO[626]	785	385.5	18	115
959	SO[627]	767	240.5	18	115
960	SO[628]	749	385.5	18	115
961	SO[629]	731	240.5	18	115
962	SO[630]	713	385.5	18	115
963	SO[631]	695	240.5	18	115
964	SO[632]	677	385.5	18	115
965	SO[633]	659	240.5	18	115
966	SO[634]	641	385.5	18	115
967	SO[635]	623	240.5	18	115
968	SO[636]	605	385.5	18	115
969	SO[637]	587	240.5	18	115
970	SO[638]	569	385.5	18	115
971	SO[639]	551	240.5	18	115
972	SO[640]	533	385.5	18	115
973	SO[641]	515	240.5	18	115
974	SO[642]	497	385.5	18	115
975	SHIELDING	461	385.5	18	115
976	SHIELDING	425	385.5	18	115
977	SHIELDING	389	385.5	18	115
978	SHIELDING	54	385.5	18	115
979	SHIELDING	18	385.5	18	115
980	SHIELDING	-18	385.5	18	115

No.	PAD name	X	Y	Width	Height
981	SHIELDING	-54	385.5	18	115
982	SHIELDING	-407	385.5	18	115
983	SHIELDING	-443	385.5	18	115
984	SHIELDING	-479	385.5	18	115
985	SO[643]	-497	240.5	18	115
986	SO[644]	-515	385.5	18	115
987	SO[645]	-533	240.5	18	115
988	SO[646]	-551	385.5	18	115
989	SO[647]	-569	240.5	18	115
990	SO[648]	-587	385.5	18	115
991	SO[649]	-605	240.5	18	115
992	SO[650]	-623	385.5	18	115
993	SO[651]	-641	240.5	18	115
994	SO[652]	-659	385.5	18	115
995	SO[653]	-677	240.5	18	115
996	SO[654]	-695	385.5	18	115
997	SO[655]	-713	240.5	18	115
998	SO[656]	-731	385.5	18	115
999	SO[657]	-749	240.5	18	115
1000	SO[658]	-767	385.5	18	115
1001	SO[659]	-785	240.5	18	115
1002	SO[660]	-803	385.5	18	115
1003	SO[661]	-821	240.5	18	115
1004	SO[662]	-839	385.5	18	115
1005	SO[663]	-857	240.5	18	115
1006	SO[664]	-875	385.5	18	115
1007	SO[665]	-893	240.5	18	115
1008	SO[666]	-911	385.5	18	115
1009	SO[667]	-929	240.5	18	115
1010	SO[668]	-947	385.5	18	115
1011	SO[669]	-965	240.5	18	115
1012	SO[670]	-983	385.5	18	115
1013	SO[671]	-1001	240.5	18	115
1014	SO[672]	-1019	385.5	18	115
1015	SO[673]	-1037	240.5	18	115
1016	SO[674]	-1055	385.5	18	115
1017	SO[675]	-1073	240.5	18	115
1018	SO[676]	-1091	385.5	18	115
1019	SO[677]	-1109	240.5	18	115
1020	SO[678]	-1127	385.5	18	115
1021	SO[679]	-1145	240.5	18	115
1022	SO[680]	-1163	385.5	18	115
1023	SO[681]	-1181	240.5	18	115
1024	SO[682]	-1199	385.5	18	115
1025	SO[683]	-1217	240.5	18	115
1026	SO[684]	-1235	385.5	18	115
1027	SO[685]	-1253	240.5	18	115
1028	SO[686]	-1271	385.5	18	115
1029	SO[687]	-1289	240.5	18	115
1030	SO[688]	-1307	385.5	18	115
1031	SO[689]	-1325	240.5	18	115
1032	SO[690]	-1343	385.5	18	115
1033	SO[691]	-1361	240.5	18	115
1034	SO[692]	-1379	385.5	18	115
1035	SO[693]	-1397	240.5	18	115
1036	SO[694]	-1415	385.5	18	115
1037	SO[695]	-1433	240.5	18	115
1038	SO[696]	-1451	385.5	18	115
1039	SO[697]	-1469	240.5	18	115
1040	SO[698]	-1487	385.5	18	115
1041	SO[699]	-1505	240.5	18	115
1042	SO[700]	-1523	385.5	18	115
1043	SO[701]	-1541	240.5	18	115
1044	SO[702]	-1559	385.5	18	115
1045	SO[703]	-1577	240.5	18	115
1046	SO[704]	-1595	385.5	18	115
1047	SO[705]	-1613	240.5	18	115
1048	SO[706]	-1631	385.5	18	115
1049	SO[707]	-1649	240.5	18	115
1050	SO[708]	-1667	385.5	18	115

No.	PAD name	X	Y	Width	Height
1051	SO[709]	-1685	240.5	18	115
1052	SO[710]	-1703	385.5	18	115
1053	SO[711]	-1721	240.5	18	115
1054	SO[712]	-1739	385.5	18	115
1055	SO[713]	-1757	240.5	18	115
1056	SO[714]	-1775	385.5	18	115
1057	SO[715]	-1793	240.5	18	115
1058	SO[716]	-1811	385.5	18	115
1059	SO[717]	-1829	240.5	18	115
1060	SO[718]	-1847	385.5	18	115
1061	SO[719]	-1865	240.5	18	115
1062	SO[720]	-1883	385.5	18	115
1063	SO[721]	-1901	240.5	18	115
1064	SO[722]	-1919	385.5	18	115
1065	SO[723]	-1937	240.5	18	115
1066	SO[724]	-1955	385.5	18	115
1067	SO[725]	-1973	240.5	18	115
1068	SO[726]	-1991	385.5	18	115
1069	SO[727]	-2009	240.5	18	115
1070	SO[728]	-2027	385.5	18	115
1071	SO[729]	-2045	240.5	18	115
1072	SO[730]	-2063	385.5	18	115
1073	SO[731]	-2081	240.5	18	115
1074	SO[732]	-2099	385.5	18	115
1075	SO[733]	-2117	240.5	18	115
1076	SO[734]	-2135	385.5	18	115
1077	SO[735]	-2153	240.5	18	115
1078	SO[736]	-2171	385.5	18	115
1079	SO[737]	-2189	240.5	18	115
1080	SO[738]	-2207	385.5	18	115
1081	SO[739]	-2225	240.5	18	115
1082	SO[740]	-2243	385.5	18	115
1083	SO[741]	-2261	240.5	18	115
1084	SO[742]	-2279	385.5	18	115
1085	SO[743]	-2297	240.5	18	115
1086	SO[744]	-2315	385.5	18	115
1087	SO[745]	-2333	240.5	18	115
1088	SO[746]	-2351	385.5	18	115
1089	SO[747]	-2369	240.5	18	115
1090	SO[748]	-2387	385.5	18	115
1091	SO[749]	-2405	240.5	18	115
1092	SO[750]	-2423	385.5	18	115
1093	SO[751]	-2441	240.5	18	115
1094	SO[752]	-2459	385.5	18	115
1095	SO[753]	-2477	240.5	18	115
1096	SO[754]	-2495	385.5	18	115
1097	SO[755]	-2513	240.5	18	115
1098	SO[756]	-2531	385.5	18	115
1099	SO[757]	-2549	240.5	18	115
1100	SO[758]	-2567	385.5	18	115
1101	SO[759]	-2585	240.5	18	115
1102	SO[760]	-2603	385.5	18	115
1103	SO[761]	-2621	240.5	18	115
1104	SO[762]	-2639	385.5	18	115
1105	SO[763]	-2657	240.5	18	115
1106	SO[764]	-2675	385.5	18	115
1107	SO[765]	-2693	240.5	18	115
1108	SO[766]	-2711	385.5	18	115
1109	SO[767]	-2729	240.5	18	115
1110	SO[768]	-2747	385.5	18	115
1111	SO[769]	-2765	240.5	18	115
1112	SO[770]	-2783	385.5	18	115
1113	SO[771]	-2801	240.5	18	115
1114	SO[772]	-2819	385.5	18	115
1115	SO[773]	-2837	240.5	18	115
1116	SO[774]	-2855	385.5	18	115
1117	SO[775]	-2873	240.5	18	115
1118	SO[776]	-2891	385.5	18	115
1119	SO[777]	-2909	240.5	18	115
1120	SO[778]	-2927	385.5	18	115

No.	PAD name	X	Y	Width	Height
1121	SO[779]	-2945	240.5	18	115
1122	SO[780]	-2963	385.5	18	115
1123	SO[781]	-2981	240.5	18	115
1124	SO[782]	-2999	385.5	18	115
1125	SO[783]	-3017	240.5	18	115
1126	SO[784]	-3035	385.5	18	115
1127	SO[785]	-3053	240.5	18	115
1128	SO[786]	-3071	385.5	18	115
1129	SO[787]	-3089	240.5	18	115
1130	SO[788]	-3107	385.5	18	115
1131	SO[789]	-3125	240.5	18	115
1132	SO[790]	-3143	385.5	18	115
1133	SO[791]	-3161	240.5	18	115
1134	SO[792]	-3179	385.5	18	115
1135	SO[793]	-3197	240.5	18	115
1136	SO[794]	-3215	385.5	18	115
1137	SO[795]	-3233	240.5	18	115
1138	SO[796]	-3251	385.5	18	115
1139	SO[797]	-3269	240.5	18	115
1140	SO[798]	-3287	385.5	18	115
1141	SO[799]	-3305	240.5	18	115
1142	SO[800]	-3323	385.5	18	115
1143	SO[801]	-3341	240.5	18	115
1144	SO[802]	-3359	385.5	18	115
1145	SO[803]	-3377	240.5	18	115
1146	SO[804]	-3395	385.5	18	115
1147	SO[805]	-3413	240.5	18	115
1148	SO[806]	-3431	385.5	18	115
1149	SO[807]	-3449	240.5	18	115
1150	SO[808]	-3467	385.5	18	115
1151	SO[809]	-3485	240.5	18	115
1152	SO[810]	-3503	385.5	18	115
1153	SO[811]	-3521	240.5	18	115
1154	SO[812]	-3539	385.5	18	115
1155	SO[813]	-3557	240.5	18	115
1156	SO[814]	-3575	385.5	18	115
1157	SO[815]	-3593	240.5	18	115
1158	SO[816]	-3611	385.5	18	115
1159	SO[817]	-3629	240.5	18	115
1160	SO[818]	-3647	385.5	18	115
1161	SO[819]	-3665	240.5	18	115
1162	SO[820]	-3683	385.5	18	115
1163	SO[821]	-3701	240.5	18	115
1164	SO[822]	-3719	385.5	18	115
1165	SO[823]	-3737	240.5	18	115
1166	SO[824]	-3755	385.5	18	115
1167	SO[825]	-3773	240.5	18	115
1168	SO[826]	-3791	385.5	18	115
1169	SO[827]	-3809	240.5	18	115
1170	SO[828]	-3827	385.5	18	115
1171	SO[829]	-3845	240.5	18	115
1172	SO[830]	-3863	385.5	18	115
1173	SO[831]	-3881	240.5	18	115
1174	SO[832]	-3899	385.5	18	115
1175	SO[833]	-3917	240.5	18	115
1176	SO[834]	-3935	385.5	18	115
1177	SO[835]	-3953	240.5	18	115
1178	SO[836]	-3971	385.5	18	115
1179	SO[837]	-3989	240.5	18	115
1180	SO[838]	-4007	385.5	18	115
1181	SO[839]	-4025	240.5	18	115
1182	SO[840]	-4043	385.5	18	115
1183	SO[841]	-4061	240.5	18	115
1184	SO[842]	-4079	385.5	18	115
1185	SO[843]	-4097	240.5	18	115
1186	SO[844]	-4115	385.5	18	115
1187	SO[845]	-4133	240.5	18	115
1188	SO[846]	-4151	385.5	18	115
1189	SO[847]	-4169	240.5	18	115
1190	SO[848]	-4187	385.5	18	115

No.	PAD name	X	Y	Width	Height
1191	SO[849]	-4205	240.5	18	115
1192	SO[850]	-4223	385.5	18	115
1193	SO[851]	-4241	240.5	18	115
1194	SO[852]	-4259	385.5	18	115
1195	SO[853]	-4277	240.5	18	115
1196	SO[854]	-4295	385.5	18	115
1197	SO[855]	-4313	240.5	18	115
1198	SO[856]	-4331	385.5	18	115
1199	SO[857]	-4349	240.5	18	115
1200	SO[858]	-4367	385.5	18	115
1201	SO[859]	-4385	240.5	18	115
1202	SO[860]	-4403	385.5	18	115
1203	SO[861]	-4421	240.5	18	115
1204	SO[862]	-4439	385.5	18	115
1205	SO[863]	-4457	240.5	18	115
1206	SO[864]	-4475	385.5	18	115
1207	SO[865]	-4493	240.5	18	115
1208	SO[866]	-4511	385.5	18	115
1209	SO[867]	-4529	240.5	18	115
1210	SO[868]	-4547	385.5	18	115
1211	SO[869]	-4565	240.5	18	115
1212	SO[870]	-4583	385.5	18	115
1213	SO[871]	-4601	240.5	18	115
1214	SO[872]	-4619	385.5	18	115
1215	SO[873]	-4637	240.5	18	115
1216	SO[874]	-4655	385.5	18	115
1217	SO[875]	-4673	240.5	18	115
1218	SO[876]	-4691	385.5	18	115
1219	SO[877]	-4709	240.5	18	115
1220	SO[878]	-4727	385.5	18	115
1221	SO[879]	-4745	240.5	18	115
1222	SO[880]	-4763	385.5	18	115
1223	SO[881]	-4781	240.5	18	115
1224	SO[882]	-4799	385.5	18	115
1225	SO[883]	-4817	240.5	18	115
1226	SO[884]	-4835	385.5	18	115
1227	SO[885]	-4853	240.5	18	115
1228	SO[886]	-4871	385.5	18	115
1229	SO[887]	-4889	240.5	18	115
1230	SO[888]	-4907	385.5	18	115
1231	SO[889]	-4925	240.5	18	115
1232	SO[890]	-4943	385.5	18	115
1233	SO[891]	-4961	240.5	18	115
1234	SO[892]	-4979	385.5	18	115
1235	SO[893]	-4997	240.5	18	115
1236	SO[894]	-5015	385.5	18	115
1237	SO[895]	-5033	240.5	18	115
1238	SO[896]	-5051	385.5	18	115
1239	SO[897]	-5069	240.5	18	115
1240	SO[898]	-5087	385.5	18	115
1241	SO[899]	-5105	240.5	18	115
1242	SO[900]	-5123	385.5	18	115
1243	SO[901]	-5141	240.5	18	115
1244	SO[902]	-5159	385.5	18	115
1245	SO[903]	-5177	240.5	18	115
1246	SO[904]	-5195	385.5	18	115
1247	SO[905]	-5213	240.5	18	115
1248	SO[906]	-5231	385.5	18	115
1249	SO[907]	-5249	240.5	18	115
1250	SO[908]	-5267	385.5	18	115
1251	SO[909]	-5285	240.5	18	115
1252	SO[910]	-5303	385.5	18	115
1253	SO[911]	-5321	240.5	18	115
1254	SO[912]	-5339	385.5	18	115
1255	SO[913]	-5357	240.5	18	115
1256	SO[914]	-5375	385.5	18	115
1257	SO[915]	-5393	240.5	18	115
1258	SO[916]	-5411	385.5	18	115
1259	SO[917]	-5429	240.5	18	115
1260	SO[918]	-5447	385.5	18	115

No.	PAD name	X	Y	Width	Height
1261	SO[919]	-5465	240.5	18	115
1262	SO[920]	-5483	385.5	18	115
1263	SO[921]	-5501	240.5	18	115
1264	SO[922]	-5519	385.5	18	115
1265	SO[923]	-5537	240.5	18	115
1266	SO[924]	-5555	385.5	18	115
1267	SO[925]	-5573	240.5	18	115
1268	SO[926]	-5591	385.5	18	115
1269	SO[927]	-5609	240.5	18	115
1270	SO[928]	-5627	385.5	18	115
1271	SO[929]	-5645	240.5	18	115
1272	SO[930]	-5663	385.5	18	115
1273	SO[931]	-5681	240.5	18	115
1274	SO[932]	-5699	385.5	18	115
1275	SO[933]	-5717	240.5	18	115
1276	SO[934]	-5735	385.5	18	115
1277	SO[935]	-5753	240.5	18	115
1278	SO[936]	-5771	385.5	18	115
1279	SO[937]	-5789	240.5	18	115
1280	SO[938]	-5807	385.5	18	115
1281	SO[939]	-5825	240.5	18	115
1282	SO[940]	-5843	385.5	18	115
1283	SO[941]	-5861	240.5	18	115
1284	SO[942]	-5879	385.5	18	115
1285	SO[943]	-5897	240.5	18	115
1286	SO[944]	-5915	385.5	18	115
1287	SO[945]	-5933	240.5	18	115
1288	SO[946]	-5951	385.5	18	115
1289	SO[947]	-5969	240.5	18	115
1290	SO[948]	-5987	385.5	18	115
1291	SO[949]	-6005	240.5	18	115
1292	SO[950]	-6023	385.5	18	115
1293	SO[951]	-6041	240.5	18	115
1294	SO[952]	-6059	385.5	18	115
1295	SO[953]	-6077	240.5	18	115
1296	SO[954]	-6095	385.5	18	115
1297	SO[955]	-6113	240.5	18	115
1298	SO[956]	-6131	385.5	18	115
1299	SO[957]	-6149	240.5	18	115
1300	SO[958]	-6167	385.5	18	115
1301	SO[959]	-6185	240.5	18	115
1302	SO[960]	-6203	385.5	18	115
1303	SO[961]	-6221	240.5	18	115
1304	SO[962]	-6239	385.5	18	115
1305	SO[963]	-6257	240.5	18	115
1306	SO[964]	-6275	385.5	18	115
1307	SO[965]	-6293	240.5	18	115
1308	SO[966]	-6311	385.5	18	115
1309	SO[967]	-6329	240.5	18	115
1310	SO[968]	-6347	385.5	18	115
1311	SO[969]	-6365	240.5	18	115
1312	SO[970]	-6383	385.5	18	115
1313	SO[971]	-6401	240.5	18	115
1314	SO[972]	-6419	385.5	18	115
1315	SO[973]	-6437	240.5	18	115
1316	SO[974]	-6455	385.5	18	115
1317	SO[975]	-6473	240.5	18	115
1318	SO[976]	-6491	385.5	18	115
1319	SO[977]	-6509	240.5	18	115
1320	SO[978]	-6527	385.5	18	115
1321	SO[979]	-6545	240.5	18	115
1322	SO[980]	-6563	385.5	18	115
1323	SO[981]	-6581	240.5	18	115
1324	SO[982]	-6599	385.5	18	115
1325	SO[983]	-6617	240.5	18	115
1326	SO[984]	-6635	385.5	18	115
1327	SO[985]	-6653	240.5	18	115
1328	SO[986]	-6671	385.5	18	115
1329	SO[987]	-6689	240.5	18	115
1330	SO[988]	-6707	385.5	18	115

No.	PAD name	X	Y	Width	Height
1331	SO[989]	-6725	240.5	18	115
1332	SO[990]	-6743	385.5	18	115
1333	SO[991]	-6761	240.5	18	115
1334	SO[992]	-6779	385.5	18	115
1335	SO[993]	-6797	240.5	18	115
1336	SO[994]	-6815	385.5	18	115
1337	SO[995]	-6833	240.5	18	115
1338	SO[996]	-6851	385.5	18	115
1339	SO[997]	-6869	240.5	18	115
1340	SO[998]	-6887	385.5	18	115
1341	SO[999]	-6905	240.5	18	115
1342	SO[1000]	-6923	385.5	18	115
1343	SO[1001]	-6941	240.5	18	115
1344	SO[1002]	-6959	385.5	18	115
1345	SO[1003]	-6977	240.5	18	115
1346	SO[1004]	-6995	385.5	18	115
1347	SO[1005]	-7013	240.5	18	115
1348	SO[1006]	-7031	385.5	18	115
1349	SO[1007]	-7049	240.5	18	115
1350	SO[1008]	-7067	385.5	18	115
1351	SO[1009]	-7085	240.5	18	115
1352	SO[1010]	-7103	385.5	18	115
1353	SO[1011]	-7121	240.5	18	115
1354	SO[1012]	-7139	385.5	18	115
1355	SO[1013]	-7157	240.5	18	115
1356	SO[1014]	-7175	385.5	18	115
1357	SO[1015]	-7193	240.5	18	115
1358	SO[1016]	-7211	385.5	18	115
1359	SO[1017]	-7229	240.5	18	115
1360	SO[1018]	-7247	385.5	18	115
1361	SO[1019]	-7265	240.5	18	115
1362	SO[1020]	-7283	385.5	18	115
1363	SO[1021]	-7301	240.5	18	115
1364	SO[1022]	-7319	385.5	18	115
1365	SO[1023]	-7337	240.5	18	115
1366	SO[1024]	-7355	385.5	18	115
1367	SO[1025]	-7373	240.5	18	115
1368	SO[1026]	-7391	385.5	18	115
1369	SO[1027]	-7409	240.5	18	115
1370	SO[1028]	-7427	385.5	18	115
1371	SO[1029]	-7445	240.5	18	115
1372	SO[1030]	-7463	385.5	18	115
1373	SO[1031]	-7481	240.5	18	115
1374	SO[1032]	-7499	385.5	18	115
1375	SO[1033]	-7517	240.5	18	115
1376	SO[1034]	-7535	385.5	18	115
1377	SO[1035]	-7553	240.5	18	115
1378	SO[1036]	-7571	385.5	18	115
1379	SO[1037]	-7589	240.5	18	115
1380	SO[1038]	-7607	385.5	18	115
1381	SO[1039]	-7625	240.5	18	115
1382	SO[1040]	-7643	385.5	18	115
1383	SO[1041]	-7661	240.5	18	115
1384	SO[1042]	-7679	385.5	18	115
1385	SO[1043]	-7697	240.5	18	115
1386	SO[1044]	-7715	385.5	18	115
1387	SO[1045]	-7733	240.5	18	115
1388	SO[1046]	-7751	385.5	18	115
1389	SO[1047]	-7769	240.5	18	115
1390	SO[1048]	-7787	385.5	18	115
1391	SO[1049]	-7805	240.5	18	115
1392	SO[1050]	-7823	385.5	18	115
1393	SO[1051]	-7841	240.5	18	115
1394	SO[1052]	-7859	385.5	18	115
1395	SO[1053]	-7877	240.5	18	115
1396	SO[1054]	-7895	385.5	18	115
1397	SO[1055]	-7913	240.5	18	115
1398	SO[1056]	-7931	385.5	18	115
1399	SO[1057]	-7949	240.5	18	115
1400	SO[1058]	-7967	385.5	18	115

No.	PAD name	X	Y	Width	Height
1401	SO[1059]	-7985	240.5	18	115
1402	SO[1060]	-8003	385.5	18	115
1403	SO[1061]	-8021	240.5	18	115
1404	SO[1062]	-8039	385.5	18	115
1405	SO[1063]	-8057	240.5	18	115
1406	SO[1064]	-8075	385.5	18	115
1407	SO[1065]	-8093	240.5	18	115
1408	SO[1066]	-8111	385.5	18	115
1409	SO[1067]	-8129	240.5	18	115
1410	SO[1068]	-8147	385.5	18	115
1411	SO[1069]	-8165	240.5	18	115
1412	SO[1070]	-8183	385.5	18	115
1413	SO[1071]	-8201	240.5	18	115
1414	SO[1072]	-8219	385.5	18	115
1415	SO[1073]	-8237	240.5	18	115
1416	SO[1074]	-8255	385.5	18	115
1417	SO[1075]	-8273	240.5	18	115
1418	SO[1076]	-8291	385.5	18	115
1419	SO[1077]	-8309	240.5	18	115
1420	SO[1078]	-8327	385.5	18	115
1421	SO[1079]	-8345	240.5	18	115
1422	SO[1080]	-8363	385.5	18	115
1423	SO[1081]	-8381	240.5	18	115
1424	SO[1082]	-8399	385.5	18	115
1425	SO[1083]	-8417	240.5	18	115
1426	SO[1084]	-8435	385.5	18	115
1427	SO[1085]	-8453	240.5	18	115
1428	SO[1086]	-8471	385.5	18	115
1429	SO[1087]	-8489	240.5	18	115
1430	SO[1088]	-8507	385.5	18	115
1431	SO[1089]	-8525	240.5	18	115
1432	SO[1090]	-8543	385.5	18	115
1433	SO[1091]	-8561	240.5	18	115
1434	SO[1092]	-8579	385.5	18	115
1435	SO[1093]	-8597	240.5	18	115
1436	SO[1094]	-8615	385.5	18	115
1437	SO[1095]	-8633	240.5	18	115
1438	SO[1096]	-8651	385.5	18	115
1439	SO[1097]	-8669	240.5	18	115
1440	SO[1098]	-8687	385.5	18	115
1441	SO[1099]	-8705	240.5	18	115
1442	SO[1100]	-8723	385.5	18	115
1443	SO[1101]	-8741	240.5	18	115
1444	SO[1102]	-8759	385.5	18	115
1445	SO[1103]	-8777	240.5	18	115
1446	SO[1104]	-8795	385.5	18	115
1447	SO[1105]	-8813	240.5	18	115
1448	SO[1106]	-8831	385.5	18	115
1449	SO[1107]	-8849	240.5	18	115
1450	SO[1108]	-8867	385.5	18	115
1451	SO[1109]	-8885	240.5	18	115
1452	SO[1110]	-8903	385.5	18	115
1453	SO[1111]	-8921	240.5	18	115
1454	SO[1112]	-8939	385.5	18	115
1455	SO[1113]	-8957	240.5	18	115
1456	SO[1114]	-8975	385.5	18	115
1457	SO[1115]	-8993	240.5	18	115
1458	SO[1116]	-9011	385.5	18	115
1459	SO[1117]	-9029	240.5	18	115
1460	SO[1118]	-9047	385.5	18	115
1461	SO[1119]	-9065	240.5	18	115
1462	SO[1120]	-9083	385.5	18	115
1463	SO[1121]	-9101	240.5	18	115
1464	SO[1122]	-9119	385.5	18	115
1465	SO[1123]	-9137	240.5	18	115
1466	SO[1124]	-9155	385.5	18	115
1467	SO[1125]	-9173	240.5	18	115
1468	SO[1126]	-9191	385.5	18	115
1469	SO[1127]	-9209	240.5	18	115
1470	SO[1128]	-9227	385.5	18	115

No.	PAD name	X	Y	Width	Height
1471	SO[1129]	-9245	240.5	18	115
1472	SO[1130]	-9263	385.5	18	115
1473	SO[1131]	-9281	240.5	18	115
1474	SO[1132]	-9299	385.5	18	115
1475	SO[1133]	-9317	240.5	18	115
1476	SO[1134]	-9335	385.5	18	115
1477	SO[1135]	-9353	240.5	18	115
1478	SO[1136]	-9371	385.5	18	115
1479	SO[1137]	-9389	240.5	18	115
1480	SO[1138]	-9407	385.5	18	115
1481	SO[1139]	-9425	240.5	18	115
1482	SO[1140]	-9443	385.5	18	115
1483	SO[1141]	-9461	240.5	18	115
1484	SO[1142]	-9479	385.5	18	115
1485	SO[1143]	-9497	240.5	18	115
1486	SO[1144]	-9515	385.5	18	115
1487	SO[1145]	-9533	240.5	18	115
1488	SO[1146]	-9551	385.5	18	115
1489	SO[1147]	-9569	240.5	18	115
1490	SO[1148]	-9587	385.5	18	115
1491	SO[1149]	-9605	240.5	18	115
1492	SO[1150]	-9623	385.5	18	115
1493	SO[1151]	-9641	240.5	18	115
1494	SO[1152]	-9659	385.5	18	115
1495	SO[1153]	-9677	240.5	18	115
1496	SO[1154]	-9695	385.5	18	115
1497	SO[1155]	-9713	240.5	18	115
1498	SO[1156]	-9731	385.5	18	115
1499	SO[1157]	-9749	240.5	18	115
1500	SO[1158]	-9767	385.5	18	115
1501	SO[1159]	-9785	240.5	18	115
1502	SO[1160]	-9803	385.5	18	115
1503	SO[1161]	-9821	240.5	18	115
1504	SO[1162]	-9839	385.5	18	115
1505	SO[1163]	-9857	240.5	18	115
1506	SO[1164]	-9875	385.5	18	115
1507	SO[1165]	-9893	240.5	18	115
1508	SO[1166]	-9911	385.5	18	115
1509	SO[1167]	-9929	240.5	18	115
1510	SO[1168]	-9947	385.5	18	115
1511	SO[1169]	-9965	240.5	18	115
1512	SO[1170]	-9983	385.5	18	115
1513	SO[1171]	-10001	240.5	18	115
1514	SO[1172]	-10019	385.5	18	115
1515	SO[1173]	-10037	240.5	18	115
1516	SO[1174]	-10055	385.5	18	115
1517	SO[1175]	-10073	240.5	18	115
1518	SO[1176]	-10091	385.5	18	115
1519	SO[1177]	-10109	240.5	18	115
1520	SO[1178]	-10127	385.5	18	115
1521	SO[1179]	-10145	240.5	18	115
1522	SO[1180]	-10163	385.5	18	115
1523	SO[1181]	-10181	240.5	18	115
1524	SO[1182]	-10199	385.5	18	115
1525	SO[1183]	-10217	240.5	18	115
1526	SO[1184]	-10235	385.5	18	115
1527	SO[1185]	-10253	240.5	18	115
1528	SO[1186]	-10271	385.5	18	115
1529	SO[1187]	-10289	240.5	18	115
1530	SO[1188]	-10307	385.5	18	115
1531	SO[1189]	-10325	240.5	18	115
1532	SO[1190]	-10343	385.5	18	115
1533	SO[1191]	-10361	240.5	18	115
1534	SO[1192]	-10379	385.5	18	115
1535	SO[1193]	-10397	240.5	18	115
1536	SO[1194]	-10415	385.5	18	115
1537	SO[1195]	-10433	240.5	18	115
1538	SO[1196]	-10451	385.5	18	115
1539	SO[1197]	-10469	240.5	18	115
1540	SO[1198]	-10487	385.5	18	115

No.	PAD name	X	Y	Width	Height
1541	SO[1199]	-10505	240.5	18	115
1542	SO[1200]	-10523	385.5	18	115
1543	SO[1201]	-10541	240.5	18	115
1544	SO[1202]	-10559	385.5	18	115
1545	SO[1203]	-10577	240.5	18	115
1546	SO[1204]	-10595	385.5	18	115
1547	SO[1205]	-10613	240.5	18	115
1548	SO[1206]	-10631	385.5	18	115
1549	SO[1207]	-10649	240.5	18	115
1550	SO[1208]	-10667	385.5	18	115
1551	SO[1209]	-10685	240.5	18	115
1552	SO[1210]	-10703	385.5	18	115
1553	SO[1211]	-10721	240.5	18	115
1554	SO[1212]	-10739	385.5	18	115
1555	SO[1213]	-10757	240.5	18	115
1556	SO[1214]	-10775	385.5	18	115
1557	SO[1215]	-10793	240.5	18	115
1558	SO[1216]	-10811	385.5	18	115
1559	SO[1217]	-10829	240.5	18	115
1560	SO[1218]	-10847	385.5	18	115
1561	SO[1219]	-10865	240.5	18	115
1562	SO[1220]	-10883	385.5	18	115
1563	SO[1221]	-10901	240.5	18	115
1564	SO[1222]	-10919	385.5	18	115
1565	SO[1223]	-10937	240.5	18	115
1566	SO[1224]	-10955	385.5	18	115
1567	SO[1225]	-10973	240.5	18	115
1568	SO[1226]	-10991	385.5	18	115
1569	SO[1227]	-11009	240.5	18	115
1570	SO[1228]	-11027	385.5	18	115
1571	SO[1229]	-11045	240.5	18	115
1572	SO[1230]	-11063	385.5	18	115
1573	SO[1231]	-11081	240.5	18	115
1574	SO[1232]	-11099	385.5	18	115
1575	SO[1233]	-11117	240.5	18	115
1576	SO[1234]	-11135	385.5	18	115
1577	SO[1235]	-11153	240.5	18	115
1578	SO[1236]	-11171	385.5	18	115
1579	SO[1237]	-11189	240.5	18	115
1580	SO[1238]	-11207	385.5	18	115
1581	SO[1239]	-11225	240.5	18	115
1582	SO[1240]	-11243	385.5	18	115
1583	SO[1241]	-11261	240.5	18	115
1584	SO[1242]	-11279	385.5	18	115
1585	SO[1243]	-11297	240.5	18	115
1586	SO[1244]	-11315	385.5	18	115
1587	SO[1245]	-11333	240.5	18	115
1588	SO[1246]	-11351	385.5	18	115
1589	SO[1247]	-11369	240.5	18	115
1590	SO[1248]	-11387	385.5	18	115
1591	SO[1249]	-11405	240.5	18	115
1592	SO[1250]	-11423	385.5	18	115
1593	SO[1251]	-11441	240.5	18	115
1594	SO[1252]	-11459	385.5	18	115
1595	SO[1253]	-11477	240.5	18	115
1596	SO[1254]	-11495	385.5	18	115
1597	SO[1255]	-11513	240.5	18	115
1598	SO[1256]	-11531	385.5	18	115
1599	SO[1257]	-11549	240.5	18	115
1600	SO[1258]	-11567	385.5	18	115
1601	SO[1259]	-11585	240.5	18	115
1602	SO[1260]	-11603	385.5	18	115
1603	SO[1261]	-11621	240.5	18	115
1604	SO[1262]	-11639	385.5	18	115
1605	SO[1263]	-11657	240.5	18	115
1606	SO[1264]	-11675	385.5	18	115
1607	SO[1265]	-11693	240.5	18	115
1608	SO[1266]	-11711	385.5	18	115
1609	SO[1267]	-11729	240.5	18	115
1610	SO[1268]	-11747	385.5	18	115

No.	PAD name	X	Y	Width	Height
1611	SO[1269]	-11765	240.5	18	115
1612	SO[1270]	-11783	385.5	18	115
1613	SO[1271]	-11801	240.5	18	115
1614	SO[1272]	-11819	385.5	18	115
1615	SO[1273]	-11837	240.5	18	115
1616	SO[1274]	-11855	385.5	18	115
1617	SO[1275]	-11873	240.5	18	115
1618	SO[1276]	-11891	385.5	18	115
1619	SO[1277]	-11909	240.5	18	115
1620	SO[1278]	-11927	385.5	18	115
1621	SO[1279]	-11945	240.5	18	115
1622	SO[1280]	-11963	385.5	18	115
1623	SO[1281]	-11981	240.5	18	115
1624	SO[1282]	-11999	385.5	18	115
1625	SO[1283]	-12017	240.5	18	115
1626	SO[1284]	-12035	385.5	18	115
1627	ALIGNMENT_MARK_R	-12148	377	90	90
1628	SHIELDING	-12326	385.5	18	115
1629	COMR_T	-12362	385.5	18	115
1630	COMR_T	-12398	385.5	18	115

Ordering information

Part.No	Package
SC5004 – GxSy – Gz	G : means COG x : means chip thick ness 3 = 400um 4 = 300um 5 = 250um 6 = 200um S : means pad shrink y : means pad shrink size 03 = 3um 04 = 4um 05 = 5um 06 = 6um G : means MTP code z : means MTP code version

Revision History

Version	Description of Changes	Page	Date
V1.0	New release		2016/07/11
V1.1	1. Modify Timing Characteristic 2. Modify Power on/off sequence 3. Revise operating temperature	66-70 58,59,60,62,65 All	2017/01/04