SC72568P-G6-E43

1200CH System-On-Chip Driver for 800RGBx480 Dual Gate TFT LCD

Datasheet

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1. GENERAL DESCRIPTION

IC offers an all-in-one chip solution of 800RGBx480 for color dual gate TFT-LCD panel. The driver IC output ports consist of 1200 source channels and 24 gate control channels for panel application. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded 3-wire SPI interfaces and I^2C interface for function setting. The display data bits sent from MCU via LVDS and RGB interface directly related to the pixels of LCD panel. The source output supports 256 gray scale with real 8-bit DAC to get a small output deviation for high color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

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2. FEATURES

- Display Resolution
  - Support dual gate panel resolution: 800RGB (H) * 480(V)
  - 256 gray scale with true 8-bit DAC
  - Full color mode: 16.7M colors (24-bit 8(R):8(G):8(B))
- LCD Driver Output Circuits
  - Source outputs: 1200channels
  - Gate outputs: 24 GIP control signals
  - Common electrode output
- Display Data Interface
  - 1 lane and 2 lane MIPI interface
  - 3 lane and 4 lane LVDS interface
  - 24-bit RGB interface support: SYNC, SYNC-DE and DE mode
- Register Setting Interface
  - 3-wire SPI interface
  - I^2C interface
- On Chip Build-In Circuits
  - DC/DC converter
  - Multi-OTP circuit
  - Timing controller
- Wide Supply Voltage Range
  - I/O voltage (VDDI to DGND): 3.2V ~3.6V
  - Analog voltage (VDD to AGND): 3.2V ~3.6V
  - Charge pump voltage (PVDD to PGND): 3.2V ~3.6V
- On-Chip Power System
  - VGHS: 8V ~ 16V
  - VGL: -6.6V ~ -12V
  - GVDD: 4.176V ~ 5.952V
  - GVCL: -2.976V ~ -4.496V
  - VCOM: GND (Including built-in circuit for compensating feed-through voltage)
  - Maximum Vop: Vop(Max.) ≤ GVDD-VCOM” = VCOM”-GVCL
- Display inversion type support: 2-dot inversion
- Optimized Layout for COG Assembly
- Support 1 Power Mode, 3 Power Mode and 5 Power Mode
- Built-in Multi-OTP Programming Circuit
  - Internal VPP power supply
- Multi-OTP Adjustable Parameters
  - 7-bit for VCOM offset adjustment

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- 7-bit ID1/ID2/ID3 OTP for end user use

- Temperature Range: −30°C ~ 85°C
- Only for BOE 4.3 800RGBx480 Panel (GV043WVQ-N80)
- GAS function for preventing image sticking when abnormal power off
- Design for industrial applications; this product is not designed for use in cars, aircraft equipment, military equipment and other applications in extreme environment

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3. PAD ARRANGEMENT

3.1 Output Bump Dimension

(T.B.D)

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4. PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DP1	-11712	-347.5	34	DGND	-9765	-347.5
2	DP1	-11653	-347.5	35	DGND	-9706	-347.5
3	DP1	-11594	-347.5	36	DGND	-9647	-347.5
4	DP1	-11535	-347.5	37	DGND	-9588	-347.5
5	DN1	-11476	-347.5	38	DGND	-9529	-347.5
6	DN1	-11417	-347.5	39	VCCM	-9470	-347.5
7	DN1	-11358	-347.5	40	VPP	-9411	-347.5
8	DN1	-11299	-347.5	41	DGND	-9352	-347.5
9	DGND	-11240	-347.5	42	DGND	-9293	-347.5
10	DGND	-11181	-347.5	43	DGND	-9234	-347.5
11	CP	-11122	-347.5	44	DGND	-9175	-347.5
12	CP	-11063	-347.5	45	DGND	-9116	-347.5
13	CP	-11004	-347.5	46	DGND	-9057	-347.5
14	CP	-10945	-347.5	47	DGND	-8998	-347.5
15	CN	-10886	-347.5	48	DGND	-8939	-347.5
16	CN	-10827	-347.5	49	VDD	-8880	-347.5
17	CN	-10768	-347.5	50	VDD	-8821	-347.5
18	CN	-10709	-347.5	51	VDD	-8762	-347.5
19	DGND	-10650	-347.5	52	VDD	-8703	-347.5
20	DGND	-10591	-347.5	53	VDD	-8644	-347.5
21	DP0	-10532	-347.5	54	VDD	-8585	-347.5
22	DP0	-10473	-347.5	55	VDD	-8526	-347.5
23	DP0	-10414	-347.5	56	VDD	-8467	-347.5
24	DP0	-10355	-347.5	57	DISP	-8408	-347.5
25	DN0	-10296	-347.5	58	DISP	-8349	-347.5
26	DN0	-10237	-347.5	59	GRB	-8290	-347.5
27	DN0	-10178	-347.5	60	GRB	-8231	-347.5
28	DN0	-10119	-347.5	61	SDA	-8172	-347.5
29	DGND	-10060	-347.5	62	SDA	-8113	-347.5
30	DGND	-10001	-347.5	63	SCL	-8054	-347.5
31	DGND	-9942	-347.5	64	SCL	-7995	-347.5
32	DGND	-9883	-347.5	65	CS	-7936	-347.5
33	DGND	-9824	-347.5	66	CS	-7877	-347.5

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	BIST_EN	-7818	-347.5	100	HSYNC	-5871	-347.5
68	BIST_EN	-7759	-347.5	101	VSYNC	-5812	-347.5
69	DB[0]	-7700	-347.5	102	VSYNC	-5753	-347.5
70	DB[0]	-7641	-347.5	103	DE	-5694	-347.5
71	DB[1]	-7582	-347.5	104	DE	-5635	-347.5
72	DB[1]	-7523	-347.5	105	DGND	-5576	-347.5
73	TEST_IN[0]	-7464	-347.5	106	DGND	-5517	-347.5
74	TEST_IN[0]	-7405	-347.5	107	DGND	-5458	-347.5
75	DB[2]	-7346	-347.5	108	DGND	-5399	-347.5
76	DB[2]	-7287	-347.5	109	DGND	-5340	-347.5
77	DB[3]	-7228	-347.5	110	DGND	-5281	-347.5
78	DB[3]	-7169	-347.5	111	DGND	-5222	-347.5
79	TEST_IN[1]	-7110	-347.5	112	DGND	-5163	-347.5
80	TEST_IN[1]	-7051	-347.5	113	VDDI	-5104	-347.5
81	DCLKP	-6992	-347.5	114	VDDI	-5045	-347.5
82	DCLKP	-6933	-347.5	115	VDDI	-4986	-347.5
83	DCLKN	-6874	-347.5	116	VDDI	-4927	-347.5
84	DCLKN	-6815	-347.5	117	VDDI	-4868	-347.5
85	TEST_IN[2]	-6756	-347.5	118	VDDI	-4809	-347.5
86	TEST_IN[2]	-6697	-347.5	119	VDDI	-4750	-347.5
87	DB[4]	-6638	-347.5	120	VDDI	-4691	-347.5
88	DB[4]	-6579	-347.5	121	DG[0]	-4632	-347.5
89	DB[5]	-6520	-347.5	122	DG[0]	-4573	-347.5
90	DB[5]	-6461	-347.5	123	DG[1]	-4514	-347.5
91	TEST_IN[3]	-6402	-347.5	124	DG[1]	-4455	-347.5
92	TEST_IN[3]	-6343	-347.5	125	DG[2]	-4396	-347.5
93	DB[6]	-6284	-347.5	126	DG[2]	-4337	-347.5
94	DB[6]	-6225	-347.5	127	DG[3]	-4278	-347.5
95	DB[7]	-6166	-347.5	128	DG[3]	-4219	-347.5
96	DB[7]	-6107	-347.5	129	DG[4]	-4160	-347.5
97	EXT_G	-6048	-347.5	130	DG[4]	-4101	-347.5
98	EXT_G	-5989	-347.5	131	DG[5]	-4042	-347.5
99	HSYNC	-5930	-347.5	132	DG[5]	-3983	-347.5

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
133	DG[6]	-3924	-347.5	166	VDPOL_LVDS_SEL	-1977	-347.5
134	DG[6]	-3865	-347.5	167	HDPOL_LVDS_SWAP	-1918	-347.5
135	DG[7]	-3806	-347.5	168	HDPOL_LVDS_SWAP	-1859	-347.5
136	DG[7]	-3747	-347.5	169	DCLKPOL	-1800	-347.5
137	EXT_S	-3688	-347.5	170	DCLKPOL	-1741	-347.5
138	EXT_S	-3629	-347.5	171	LVDS_FMT	-1682	-347.5
139	DR[0]	-3570	-347.5	172	LVDS_FMT	-1623	-347.5
140	DR[0]	-3511	-347.5	173	VDIR	-1564	-347.5
141	DR[1]	-3452	-347.5	174	VDIR	-1505	-347.5
142	DR[1]	-3393	-347.5	175	HDIR	-1446	-347.5
143	DR[2]	-3334	-347.5	176	HDIR	-1387	-347.5
144	DR[2]	-3275	-347.5	177	SPI_I2C_SEL	-1328	-347.5
145	DR[3]	-3216	-347.5	178	SPI_I2C_SEL	-1269	-347.5
146	DR[3]	-3157	-347.5	179	VCC	-1210	-347.5
147	DR[4]	-3098	-347.5	180	VCC	-1151	-347.5
148	DR[4]	-3039	-347.5	181	VCC	-1092	-347.5
149	DR[5]	-2980	-347.5	182	VCC	-1033	-347.5
150	DR[5]	-2921	-347.5	183	PVDD	-974	-347.5
151	DR[6]	-2862	-347.5	184	PVDD	-915	-347.5
152	DR[6]	-2803	-347.5	185	PVDD	-856	-347.5
153	DR[7]	-2744	-347.5	186	PVDD	-797	-347.5
154	DR[7]	-2685	-347.5	187	PVDD	-738	-347.5
155	INTF[0]	-2626	-347.5	188	PVDD	-679	-347.5
156	INTF[0]	-2567	-347.5	189	PVDD	-620	-347.5
157	INTF[1]	-2508	-347.5	190	PVDD	-561	-347.5
158	INTF[1]	-2449	-347.5	191	PVDD	-502	-347.5
159	AUTO_DL_EN	-2390	-347.5	192	PVDD	-443	-347.5
160	AUTO_DL_EN	-2331	-347.5	193	PVDD	-384	-347.5
161	ERR1	-2272	-347.5	194	PVDD	-325	-347.5
162	ERR1	-2213	-347.5	195	DUMMY	-266	-347.5
163	ERR2	-2154	-347.5	196	AGND	-207	-347.5
164	ERR2	-2095	-347.5	197	AGND	-148	-347.5
165	VDPOL_LANE_SEL	-2036	-347.5	198	DUMMY	-89	-347.5

PAD No.	PIN Name	X	Y
199	AGND	-30	-347.5
200	AGND	30	-347.5
201	AGND	89	-347.5
202	AGND	148	-347.5
203	AGND	207	-347.5
204	AGND	266	-347.5
205	AGND	325	-347.5
206	AGND	384	-347.5
207	AGND	443	-347.5
208	AGND	502	-347.5
209	AGND	561	-347.5
210	AGND	620	-347.5
211	SGND	679	-347.5
212	SGND	738	-347.5
213	SGND	797	-347.5
214	SGND	856	-347.5
215	SGND	915	-347.5
216	SGND	974	-347.5
217	SGND	1033	-347.5
218	SGND	1092	-347.5
219	SGND	1151	-347.5
220	SGND	1210	-347.5
221	SGND	1269	-347.5
222	SGND	1328	-347.5
223	SGND	1387	-347.5
224	SGND	1446	-347.5
225	SGND	1505	-347.5
226	SGND	1564	-347.5
227	VCCA	1623	-347.5
228	VCCA	1682	-347.5
229	DUMMY	1741	-347.5
230	GVCL	1800	-347.5
231	GVCL	1859	-347.5

PAD No.	PIN Name	X	Y
232	DUMMY	1918	-347.5
233	VGSP	1977	-347.5
234	VGSP	2036	-347.5
235	DUMMY	2095	-347.5
236	GVDD	2154	-347.5
237	GVDD	2213	-347.5
238	DUMMY	2272	-347.5
239	SGND	2331	-347.5
240	SGND	2390	-347.5
241	SGND	2449	-347.5
242	SGND	2508	-347.5
243	SGND	2567	-347.5
244	SGND	2626	-347.5
245	SGND	2685	-347.5
246	SGND	2744	-347.5
247	SGND	2803	-347.5
248	SGND	2862	-347.5
249	SGND	2921	-347.5
250	SGND	2980	-347.5
251	SGND	3039	-347.5
252	SGND	3098	-347.5
253	SGND	3157	-347.5
254	SGND	3216	-347.5
255	SGND	3275	-347.5
256	SGND	3334	-347.5
257	SGND	3393	-347.5
258	SGND	3452	-347.5
259	SGND	3511	-347.5
260	SVCL	3570	-347.5
261	SVCL	3629	-347.5
262	SVCL	3688	-347.5
263	SVCL	3747	-347.5
264	SVCL	3806	-347.5

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PAD No.	PIN Name	X	Y
265	SVCL	3865	-347.5
266	SVCL	3924	-347.5
267	SVDD	3983	-347.5
268	SVDD	4042	-347.5
269	SVDD	4101	-347.5
270	SVDD	4160	-347.5
271	SVDD	4219	-347.5
272	SVDD	4278	-347.5
273	SVDD	4337	-347.5
274	SVDD	4396	-347.5
275	PGND	4455	-347.5
276	PGND	4514	-347.5
277	PGND	4573	-347.5
278	PGND	4632	-347.5
279	PGND	4691	-347.5
280	PGND	4750	-347.5
281	PGND	4809	-347.5
282	PGND	4868	-347.5
283	PGND	4927	-347.5
284	PGND	4986	-347.5
285	PGND	5045	-347.5
286	PGND	5104	-347.5
287	PGND	5163	-347.5
288	PGND	5222	-347.5
289	PGND	5281	-347.5
290	PGND	5340	-347.5
291	PGND	5399	-347.5
292	PGND	5458	-347.5
293	PGND	5517	-347.5
294	PGND	5576	-347.5
295	PGND	5635	-347.5
296	PGND	5694	-347.5
297	PGND	5753	-347.5

PAD No.	PIN Name	X	Y
298	PGND	5812	-347.5
299	PGND	5871	-347.5
300	PGND	5930	-347.5
301	PGND	5989	-347.5
302	C11P	6048	-347.5
303	C11P	6107	-347.5
304	C11P	6166	-347.5
305	C11P	6225	-347.5
306	DUMMY	6284	-347.5
307	C11P	6343	-347.5
308	C11P	6402	-347.5
309	C11P	6461	-347.5
310	C11P	6520	-347.5
311	C11N	6579	-347.5
312	C11N	6638	-347.5
313	C11N	6697	-347.5
314	C11N	6756	-347.5
315	C11N	6815	-347.5
316	DUMMY	6874	-347.5
317	C12N	6933	-347.5
318	C12N	6992	-347.5
319	C12N	7051	-347.5
320	C12N	7110	-347.5
321	C12P	7169	-347.5
322	C12P	7228	-347.5
323	C12P	7287	-347.5
324	C12P	7346	-347.5
325	C12P	7405	-347.5
326	DUMMY	7464	-347.5
327	PVDD	7523	-347.5
328	PVDD	7582	-347.5
329	PVDD	7641	-347.5
330	PVDD	7700	-347.5

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PAD No.	PIN Name	X	Y
331	PVDD	7759	-347.5
332	PVDD	7818	-347.5
333	PVDD	7877	-347.5
334	PVDD	7936	-347.5
335	PVDD	7995	-347.5
336	PVDD	8054	-347.5
337	PVDD	8113	-347.5
338	PVDD	8172	-347.5
339	PVDD	8231	-347.5
340	PVDD	8290	-347.5
341	PVDD	8349	-347.5
342	PVDD	8408	-347.5
343	PVDD	8467	-347.5
344	PVDD	8526	-347.5
345	PVDD	8585	-347.5
346	PVDD	8644	-347.5
347	PVDD	8703	-347.5
348	PVDD	8762	-347.5
349	PVDD	8821	-347.5
350	PVDD	8880	-347.5
351	PVDD	8939	-347.5
352	PVDD	8998	-347.5
353	DUMMY	9057	-347.5
354	VGH	9116	-347.5
355	VGH	9175	-347.5
356	VGH	9234	-347.5
357	VGH	9293	-347.5
358	VGH	9352	-347.5
359	VGH	9411	-347.5
360	DUMMY	9470	-347.5
361	PGND	9529	-347.5
362	PGND	9588	-347.5
363	PGND	9647	-347.5

PAD No.	PIN Name	X	Y
364	PGND	9706	-347.5
365	PGND	9765	-347.5
366	PGND	9824	-347.5
367	PGND	9883	-347.5
368	VGL	9942	-347.5
369	VGL	10001	-347.5
370	VGL	10060	-347.5
371	VGL	10119	-347.5
372	VGL	10178	-347.5
373	VGL	10237	-347.5
374	DUMMY	10296	-347.5
375	PGND	10355	-347.5
376	PGND	10414	-347.5
377	PGND	10473	-347.5
378	PGND	10532	-347.5
379	PGND	10591	-347.5
380	PGND	10650	-347.5
381	PGND	10709	-347.5
382	PGND	10768	-347.5
383	PGND	10827	-347.5
384	PGND	10886	-347.5
385	PVDD	10945	-347.5
386	PVDD	11004	-347.5
387	PVDD	11063	-347.5
388	PVDD	11122	-347.5
389	PVDD	11181	-347.5
390	PVDD	11240	-347.5
391	VCOM	11299	-347.5
392	VCOM	11358	-347.5
393	VCOM	11417	-347.5
394	VCOM	11476	-347.5
395	VCOM	11535	-347.5
396	VCOM	11594	-347.5

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PAD No.	PIN Name	X	Y
397	VCOM	11653	-347.5
398	VCOM	11712	-347.5
399	VGH	11606	337.5
400	VGH	11592	222.5
401	VGH	11578	337.5
402	VGH	11564	222.5
403	VGH	11550	337.5
404	VGH	11536	222.5
405	GOR[11]	11522	337.5
406	GOR[11]	11508	222.5
407	GOR[11]	11494	337.5
408	GOR[12]	11480	222.5
409	GOR[12]	11466	337.5
410	GOR[12]	11452	222.5
411	GOR[1]	11382	337.5
412	GOR[1]	11368	222.5
413	GOR[1]	11354	337.5
414	GOR[2]	11340	222.5
415	GOR[2]	11326	337.5
416	GOR[2]	11312	222.5
417	GOR[3]	11298	337.5
418	GOR[3]	11284	222.5
419	GOR[3]	11270	337.5
420	GOR[4]	11256	222.5
421	GOR[4]	11242	337.5
422	GOR[4]	11228	222.5
423	GOR[5]	11214	337.5
424	GOR[5]	11200	222.5
425	GOR[5]	11186	337.5
426	GOR[6]	11172	222.5
427	GOR[6]	11158	337.5
428	GOR[6]	11144	222.5
429	GOR[7]	11130	337.5

PAD No.	PIN Name	X	Y
430	GOR[7]	11116	222.5
431	GOR[7]	11102	337.5
432	GOR[8]	11088	222.5
433	GOR[8]	11074	337.5
434	GOR[8]	11060	222.5
435	GOR[9]	11046	337.5
436	GOR[9]	11032	222.5
437	GOR[9]	11018	337.5
438	GOR[10]	11004	222.5
439	GOR[10]	10990	337.5
440	GOR[10]	10976	222.5
441	VGH	10906	337.5
442	VGH	10892	222.5
443	VGH	10878	337.5
444	VGH	10864	222.5
445	VGH	10850	337.5
446	VGH	10836	222.5
447	VGL	10822	337.5
448	VGL	10808	222.5
449	VGL	10794	337.5
450	VGL	10780	222.5
451	VGL	10766	337.5
452	VGL	10752	222.5
453	DUMMY	10682	337.5
454	DUMMY	10668	222.5
455	DUMMY	10654	337.5
456	DUMMY	10640	222.5
457	DUMMY	10626	337.5
458	DUMMY	10612	222.5
459	DUMMY	10598	337.5
460	DUMMY	10584	222.5
461	DUMMY	10570	337.5
462	DUMMY	10556	222.5

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PAD No.	PIN Name	X	Y
463	DUMMY	10542	337.5
464	DUMMY	10528	222.5
465	DUMMY	10514	337.5
466	DUMMY	10500	222.5
467	DUMMY	10486	337.5
468	DUMMY	10472	222.5
469	DUMMY	10458	337.5
470	DUMMY	10444	222.5
471	DUMMY	10430	337.5
472	DUMMY	10416	222.5
473	DUMMY	10402	337.5
474	DUMMY	10388	222.5
475	DUMMY	10374	337.5
476	DUMMY	10360	222.5
477	DUMMY	10346	337.5
478	DUMMY	10332	222.5
479	DUMMY	10318	337.5
480	DUMMY	10304	222.5
481	DUMMY	10290	337.5
482	DUMMY	10276	222.5
483	DUMMY	10262	337.5
484	DUMMY	10248	222.5
485	DUMMY	10234	337.5
486	DUMMY	10220	222.5
487	DUMMY	10206	337.5
488	DUMMY	10192	222.5
489	DUMMY	10178	337.5
490	DUMMY	10164	222.5
491	DUMMY	10150	337.5
492	DUMMY	10136	222.5
493	DUMMY	10122	337.5
494	DUMMY	10108	222.5
495	DUMMY	10094	337.5

PAD No.	PIN Name	X	Y
496	DUMMY	10080	222.5
497	DUMMY	10066	337.5
498	DUMMY	10052	222.5
499	DUMMY	10038	337.5
500	DUMMY	10024	222.5
501	DUMMY	10010	337.5
502	DUMMY	9996	222.5
503	DUMMY	9982	337.5
504	DUMMY	9968	222.5
505	DUMMY	9954	337.5
506	DUMMY	9940	222.5
507	DUMMY	9926	337.5
508	DUMMY	9912	222.5
509	DUMMY	9898	337.5
510	DUMMY	9884	222.5
511	DUMMY	9870	337.5
512	DUMMY	9856	222.5
513	DUMMY	9842	337.5
514	DUMMY	9828	222.5
515	DUMMY	9814	337.5
516	DUMMY	9800	222.5
517	DUMMY	9786	337.5
518	DUMMY	9772	222.5
519	DUMMY	9758	337.5
520	DUMMY	9744	222.5
521	DUMMY	9730	337.5
522	DUMMY	9716	222.5
523	DUMMY	9702	337.5
524	DUMMY	9688	222.5
525	DUMMY	9674	337.5
526	DUMMY	9660	222.5
527	DUMMY	9646	337.5
528	DUMMY	9632	222.5

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PAD No.	PIN Name	X	Y
529	DUMMY	9618	337.5
530	DUMMY	9604	222.5
531	DUMMY	9590	337.5
532	DUMMY	9576	222.5
533	DUMMY	9562	337.5
534	DUMMY	9548	222.5
535	DUMMY	9534	337.5
536	DUMMY	9520	222.5
537	DUMMY	9506	337.5
538	DUMMY	9492	222.5
539	DUMMY	9478	337.5
540	DUMMY	9464	222.5
541	DUMMY	9450	337.5
542	DUMMY	9436	222.5
543	DUMMY	9422	337.5
544	DUMMY	9408	222.5
545	DUMMY	9394	337.5
546	DUMMY	9380	222.5
547	DUMMY	9366	337.5
548	DUMMY	9352	222.5
549	DUMMY	9338	337.5
550	DUMMY	9324	222.5
551	SGND	9254	337.5
552	SGND	9240	222.5
553	SGND	9226	337.5
554	SGND	9212	222.5
555	SGND	9198	337.5
556	SGND	9184	222.5
557	SGND	9170	337.5
558	SGND	9156	222.5
559	SGND	9142	337.5
560	SGND	9128	222.5
561	SGND	9114	337.5

PAD No.	PIN Name	X	Y
562	SGND	9100	222.5
563	SGND	9086	337.5
564	SGND	9072	222.5
565	SGND	9058	337.5
566	SGND	9044	222.5
567	S0	8988	222.5
568	S1	8974	337.5
569	S2	8960	222.5
570	S3	8946	337.5
571	S4	8932	222.5
572	S5	8918	337.5
573	S6	8904	222.5
574	S7	8890	337.5
575	S8	8876	222.5
576	S9	8862	337.5
577	S10	8848	222.5
578	S11	8834	337.5
579	S12	8820	222.5
580	S13	8806	337.5
581	S14	8792	222.5
582	S15	8778	337.5
583	S16	8764	222.5
584	S17	8750	337.5
585	S18	8736	222.5
586	S19	8722	337.5
587	S20	8708	222.5
588	S21	8694	337.5
589	S22	8680	222.5
590	S23	8666	337.5
591	S24	8652	222.5
592	S25	8638	337.5
593	S26	8624	222.5
594	S27	8610	337.5

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PAD No.	PIN Name	X	Y
595	S28	8596	222.5
596	S29	8582	337.5
597	S30	8568	222.5
598	S31	8554	337.5
599	S32	8540	222.5
600	S33	8526	337.5
601	S34	8512	222.5
602	S35	8498	337.5
603	S36	8484	222.5
604	S37	8470	337.5
605	S38	8456	222.5
606	S39	8442	337.5
607	S40	8428	222.5
608	S41	8414	337.5
609	S42	8400	222.5
610	S43	8386	337.5
611	S44	8372	222.5
612	S45	8358	337.5
613	S46	8344	222.5
614	S47	8330	337.5
615	S48	8316	222.5
616	S49	8302	337.5
617	S50	8288	222.5
618	S51	8274	337.5
619	S52	8260	222.5
620	S53	8246	337.5
621	S54	8232	222.5
622	S55	8218	337.5
623	S56	8204	222.5
624	S57	8190	337.5
625	S58	8176	222.5
626	S59	8162	337.5
627	S60	8148	222.5

PAD No.	PIN Name	X	Y
628	S61	8134	337.5
629	S62	8120	222.5
630	S63	8106	337.5
631	S64	8092	222.5
632	S65	8078	337.5
633	S66	8064	222.5
634	S67	8050	337.5
635	S68	8036	222.5
636	S69	8022	337.5
637	S70	8008	222.5
638	S71	7994	337.5
639	S72	7980	222.5
640	S73	7966	337.5
641	S74	7952	222.5
642	S75	7938	337.5
643	S76	7924	222.5
644	S77	7910	337.5
645	S78	7896	222.5
646	S79	7882	337.5
647	S80	7868	222.5
648	S81	7854	337.5
649	S82	7840	222.5
650	S83	7826	337.5
651	S84	7812	222.5
652	S85	7798	337.5
653	S86	7784	222.5
654	S87	7770	337.5
655	S88	7756	222.5
656	S89	7742	337.5
657	S90	7728	222.5
658	S91	7714	337.5
659	S92	7700	222.5
660	S93	7686	337.5

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PAD No.	PIN Name	X	Y
661	S94	7672	222.5
662	S95	7658	337.5
663	S96	7644	222.5
664	S97	7630	337.5
665	S98	7616	222.5
666	S99	7602	337.5
667	S100	7588	222.5
668	S101	7574	337.5
669	S102	7560	222.5
670	S103	7546	337.5
671	S104	7532	222.5
672	S105	7518	337.5
673	S106	7504	222.5
674	S107	7490	337.5
675	S108	7476	222.5
676	S109	7462	337.5
677	S110	7448	222.5
678	S111	7434	337.5
679	S112	7420	222.5
680	S113	7406	337.5
681	S114	7392	222.5
682	S115	7378	337.5
683	S116	7364	222.5
684	S117	7350	337.5
685	S118	7336	222.5
686	S119	7322	337.5
687	S120	7308	222.5
688	S121	7294	337.5
689	S122	7280	222.5
690	S123	7266	337.5
691	S124	7252	222.5
692	S125	7238	337.5
693	S126	7224	222.5

PAD No.	PIN Name	X	Y
694	S127	7210	337.5
695	S128	7196	222.5
696	S129	7182	337.5
697	S130	7168	222.5
698	S131	7154	337.5
699	S132	7140	222.5
700	S133	7126	337.5
701	S134	7112	222.5
702	S135	7098	337.5
703	S136	7084	222.5
704	S137	7070	337.5
705	S138	7056	222.5
706	S139	7042	337.5
707	S140	7028	222.5
708	S141	7014	337.5
709	S142	7000	222.5
710	S143	6986	337.5
711	S144	6972	222.5
712	S145	6958	337.5
713	S146	6944	222.5
714	S147	6930	337.5
715	S148	6916	222.5
716	S149	6902	337.5
717	S150	6888	222.5
718	S151	6874	337.5
719	S152	6860	222.5
720	S153	6846	337.5
721	S154	6832	222.5
722	S155	6818	337.5
723	S156	6804	222.5
724	S157	6790	337.5
725	S158	6776	222.5
726	S159	6762	337.5

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PAD No.	PIN Name	X	Y
727	S160	6748	222.5
728	S161	6734	337.5
729	S162	6720	222.5
730	S163	6706	337.5
731	S164	6692	222.5
732	S165	6678	337.5
733	S166	6664	222.5
734	S167	6650	337.5
735	S168	6636	222.5
736	S169	6622	337.5
737	S170	6608	222.5
738	S171	6594	337.5
739	S172	6580	222.5
740	S173	6566	337.5
741	S174	6552	222.5
742	S175	6538	337.5
743	S176	6524	222.5
744	S177	6510	337.5
745	S178	6496	222.5
746	S179	6482	337.5
747	S180	6468	222.5
748	S181	6454	337.5
749	S182	6440	222.5
750	S183	6426	337.5
751	S184	6412	222.5
752	S185	6398	337.5
753	S186	6384	222.5
754	S187	6370	337.5
755	S188	6356	222.5
756	S189	6342	337.5
757	S190	6328	222.5
758	S191	6314	337.5
759	S192	6300	222.5

PAD No.	PIN Name	X	Y
760	S193	6286	337.5
761	S194	6272	222.5
762	S195	6258	337.5
763	S196	6244	222.5
764	S197	6230	337.5
765	S198	6216	222.5
766	S199	6202	337.5
767	S200	6188	222.5
768	S201	6174	337.5
769	S202	6160	222.5
770	S203	6146	337.5
771	S204	6132	222.5
772	S205	6118	337.5
773	S206	6104	222.5
774	S207	6090	337.5
775	S208	6076	222.5
776	S209	6062	337.5
777	S210	6048	222.5
778	S211	6034	337.5
779	S212	6020	222.5
780	S213	6006	337.5
781	S214	5992	222.5
782	S215	5978	337.5
783	S216	5964	222.5
784	S217	5950	337.5
785	S218	5936	222.5
786	S219	5922	337.5
787	S220	5908	222.5
788	S221	5894	337.5
789	S222	5880	222.5
790	S223	5866	337.5
791	S224	5852	222.5
792	S225	5838	337.5

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PAD No.	PIN Name	X	Y
793	S226	5824	222.5
794	S227	5810	337.5
795	S228	5796	222.5
796	S229	5782	337.5
797	S230	5768	222.5
798	S231	5754	337.5
799	S232	5740	222.5
800	S233	5726	337.5
801	S234	5712	222.5
802	S235	5698	337.5
803	S236	5684	222.5
804	S237	5670	337.5
805	S238	5656	222.5
806	S239	5642	337.5
807	S240	5628	222.5
808	S241	5614	337.5
809	S242	5600	222.5
810	S243	5586	337.5
811	S244	5572	222.5
812	S245	5558	337.5
813	S246	5544	222.5
814	S247	5530	337.5
815	S248	5516	222.5
816	S249	5502	337.5
817	S250	5488	222.5
818	S251	5474	337.5
819	S252	5460	222.5
820	S253	5446	337.5
821	S254	5432	222.5
822	S255	5418	337.5
823	S256	5404	222.5
824	S257	5390	337.5
825	S258	5376	222.5

PAD No.	PIN Name	X	Y
826	S259	5362	337.5
827	S260	5348	222.5
828	S261	5334	337.5
829	S262	5320	222.5
830	S263	5306	337.5
831	S264	5292	222.5
832	S265	5278	337.5
833	S266	5264	222.5
834	S267	5250	337.5
835	S268	5236	222.5
836	S269	5222	337.5
837	S270	5208	222.5
838	S271	5194	337.5
839	S272	5180	222.5
840	S273	5166	337.5
841	S274	5152	222.5
842	S275	5138	337.5
843	S276	5124	222.5
844	S277	5110	337.5
845	S278	5096	222.5
846	S279	5082	337.5
847	S280	5068	222.5
848	S281	5054	337.5
849	S282	5040	222.5
850	S283	5026	337.5
851	S284	5012	222.5
852	S285	4998	337.5
853	S286	4984	222.5
854	S287	4970	337.5
855	S288	4956	222.5
856	S289	4942	337.5
857	S290	4928	222.5
858	S291	4914	337.5

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PAD No.	PIN Name	X	Y
859	S292	4900	222.5
860	S293	4886	337.5
861	S294	4872	222.5
862	S295	4858	337.5
863	S296	4844	222.5
864	S297	4830	337.5
865	S298	4816	222.5
866	S299	4802	337.5
867	S300	4788	222.5
868	SGND	4718	337.5
869	SGND	4704	222.5
870	SGND	4690	337.5
871	SGND	4676	222.5
872	SGND	4662	337.5
873	SGND	4648	222.5
874	SGND	4634	337.5
875	SGND	4620	222.5
876	SGND	4606	337.5
877	SGND	4592	222.5
878	SGND	4578	337.5
879	SGND	4564	222.5
880	SGND	4550	337.5
881	SGND	4536	222.5
882	SGND	4522	337.5
883	SGND	4508	222.5
884	S301	4438	337.5
885	S302	4424	222.5
886	S303	4410	337.5
887	S304	4396	222.5
888	S305	4382	337.5
889	S306	4368	222.5
890	S307	4354	337.5
891	S308	4340	222.5

PAD No.	PIN Name	X	Y
892	S309	4326	337.5
893	S310	4312	222.5
894	S311	4298	337.5
895	S312	4284	222.5
896	S313	4270	337.5
897	S314	4256	222.5
898	S315	4242	337.5
899	S316	4228	222.5
900	S317	4214	337.5
901	S318	4200	222.5
902	S319	4186	337.5
903	S320	4172	222.5
904	S321	4158	337.5
905	S322	4144	222.5
906	S323	4130	337.5
907	S324	4116	222.5
908	S325	4102	337.5
909	S326	4088	222.5
910	S327	4074	337.5
911	S328	4060	222.5
912	S329	4046	337.5
913	S330	4032	222.5
914	S331	4018	337.5
915	S332	4004	222.5
916	S333	3990	337.5
917	S334	3976	222.5
918	S335	3962	337.5
919	S336	3948	222.5
920	S337	3934	337.5
921	S338	3920	222.5
922	S339	3906	337.5
923	S340	3892	222.5
924	S341	3878	337.5

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PAD No.	PIN Name	X	Y
925	S342	3864	222.5
926	S343	3850	337.5
927	S344	3836	222.5
928	S345	3822	337.5
929	S346	3808	222.5
930	S347	3794	337.5
931	S348	3780	222.5
932	S349	3766	337.5
933	S350	3752	222.5
934	S351	3738	337.5
935	S352	3724	222.5
936	S353	3710	337.5
937	S354	3696	222.5
938	S355	3682	337.5
939	S356	3668	222.5
940	S357	3654	337.5
941	S358	3640	222.5
942	S359	3626	337.5
943	S360	3612	222.5
944	S361	3598	337.5
945	S362	3584	222.5
946	S363	3570	337.5
947	S364	3556	222.5
948	S365	3542	337.5
949	S366	3528	222.5
950	S367	3514	337.5
951	S368	3500	222.5
952	S369	3486	337.5
953	S370	3472	222.5
954	S371	3458	337.5
955	S372	3444	222.5
956	S373	3430	337.5
957	S374	3416	222.5

PAD No.	PIN Name	X	Y
958	S375	3402	337.5
959	S376	3388	222.5
960	S377	3374	337.5
961	S378	3360	222.5
962	S379	3346	337.5
963	S380	3332	222.5
964	S381	3318	337.5
965	S382	3304	222.5
966	S383	3290	337.5
967	S384	3276	222.5
968	S385	3262	337.5
969	S386	3248	222.5
970	S387	3234	337.5
971	S388	3220	222.5
972	S389	3206	337.5
973	S390	3192	222.5
974	S391	3178	337.5
975	S392	3164	222.5
976	S393	3150	337.5
977	S394	3136	222.5
978	S395	3122	337.5
979	S396	3108	222.5
980	S397	3094	337.5
981	S398	3080	222.5
982	S399	3066	337.5
983	S400	3052	222.5
984	S401	3038	337.5
985	S402	3024	222.5
986	S403	3010	337.5
987	S404	2996	222.5
988	S405	2982	337.5
989	S406	2968	222.5
990	S407	2954	337.5

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PAD No.	PIN Name	X	Y
991	S408	2940	222.5
992	S409	2926	337.5
993	S410	2912	222.5
994	S411	2898	337.5
995	S412	2884	222.5
996	S413	2870	337.5
997	S414	2856	222.5
998	S415	2842	337.5
999	S416	2828	222.5
1000	S417	2814	337.5
1001	S418	2800	222.5
1002	S419	2786	337.5
1003	S420	2772	222.5
1004	S421	2758	337.5
1005	S422	2744	222.5
1006	S423	2730	337.5
1007	S424	2716	222.5
1008	S425	2702	337.5
1009	S426	2688	222.5
1010	S427	2674	337.5
1011	S428	2660	222.5
1012	S429	2646	337.5
1013	S430	2632	222.5
1014	S431	2618	337.5
1015	S432	2604	222.5
1016	S433	2590	337.5
1017	S434	2576	222.5
1018	S435	2562	337.5
1019	S436	2548	222.5
1020	S437	2534	337.5
1021	S438	2520	222.5
1022	S439	2506	337.5
1023	S440	2492	222.5

PAD No.	PIN Name	X	Y
1024	S441	2478	337.5
1025	S442	2464	222.5
1026	S443	2450	337.5
1027	S444	2436	222.5
1028	S445	2422	337.5
1029	S446	2408	222.5
1030	S447	2394	337.5
1031	S448	2380	222.5
1032	S449	2366	337.5
1033	S450	2352	222.5
1034	S451	2338	337.5
1035	S452	2324	222.5
1036	S453	2310	337.5
1037	S454	2296	222.5
1038	S455	2282	337.5
1039	S456	2268	222.5
1040	S457	2254	337.5
1041	S458	2240	222.5
1042	S459	2226	337.5
1043	S460	2212	222.5
1044	S461	2198	337.5
1045	S462	2184	222.5
1046	S463	2170	337.5
1047	S464	2156	222.5
1048	S465	2142	337.5
1049	S466	2128	222.5
1050	S467	2114	337.5
1051	S468	2100	222.5
1052	S469	2086	337.5
1053	S470	2072	222.5
1054	S471	2058	337.5
1055	S472	2044	222.5
1056	S473	2030	337.5

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PAD No.	PIN Name	X	Y
1057	S474	2016	222.5
1058	S475	2002	337.5
1059	S476	1988	222.5
1060	S477	1974	337.5
1061	S478	1960	222.5
1062	S479	1946	337.5
1063	S480	1932	222.5
1064	S481	1918	337.5
1065	S482	1904	222.5
1066	S483	1890	337.5
1067	S484	1876	222.5
1068	S485	1862	337.5
1069	S486	1848	222.5
1070	S487	1834	337.5
1071	S488	1820	222.5
1072	S489	1806	337.5
1073	S490	1792	222.5
1074	S491	1778	337.5
1075	S492	1764	222.5
1076	S493	1750	337.5
1077	S494	1736	222.5
1078	S495	1722	337.5
1079	S496	1708	222.5
1080	S497	1694	337.5
1081	S498	1680	222.5
1082	S499	1666	337.5
1083	S500	1652	222.5
1084	S501	1638	337.5
1085	S502	1624	222.5
1086	S503	1610	337.5
1087	S504	1596	222.5
1088	S505	1582	337.5
1089	S506	1568	222.5

PAD No.	PIN Name	X	Y
1090	S507	1554	337.5
1091	S508	1540	222.5
1092	S509	1526	337.5
1093	S510	1512	222.5
1094	S511	1498	337.5
1095	S512	1484	222.5
1096	S513	1470	337.5
1097	S514	1456	222.5
1098	S515	1442	337.5
1099	S516	1428	222.5
1100	S517	1414	337.5
1101	S518	1400	222.5
1102	S519	1386	337.5
1103	S520	1372	222.5
1104	S521	1358	337.5
1105	S522	1344	222.5
1106	S523	1330	337.5
1107	S524	1316	222.5
1108	S525	1302	337.5
1109	S526	1288	222.5
1110	S527	1274	337.5
1111	S528	1260	222.5
1112	S529	1246	337.5
1113	S530	1232	222.5
1114	S531	1218	337.5
1115	S532	1204	222.5
1116	S533	1190	337.5
1117	S534	1176	222.5
1118	S535	1162	337.5
1119	S536	1148	222.5
1120	S537	1134	337.5
1121	S538	1120	222.5
1122	S539	1106	337.5

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PAD No.	PIN Name	X	Y
1123	S540	1092	222.5
1124	S541	1078	337.5
1125	S542	1064	222.5
1126	S543	1050	337.5
1127	S544	1036	222.5
1128	S545	1022	337.5
1129	S546	1008	222.5
1130	S547	994	337.5
1131	S548	980	222.5
1132	S549	966	337.5
1133	S550	952	222.5
1134	S551	938	337.5
1135	S552	924	222.5
1136	S553	910	337.5
1137	S554	896	222.5
1138	S555	882	337.5
1139	S556	868	222.5
1140	S557	854	337.5
1141	S558	840	222.5
1142	S559	826	337.5
1143	S560	812	222.5
1144	S561	798	337.5
1145	S562	784	222.5
1146	S563	770	337.5
1147	S564	756	222.5
1148	S565	742	337.5
1149	S566	728	222.5
1150	S567	714	337.5
1151	S568	700	222.5
1152	S569	686	337.5
1153	S570	672	222.5
1154	S571	658	337.5
1155	S572	644	222.5

PAD No.	PIN Name	X	Y
1156	S573	630	337.5
1157	S574	616	222.5
1158	S575	602	337.5
1159	S576	588	222.5
1160	S577	574	337.5
1161	S578	560	222.5
1162	S579	546	337.5
1163	S580	532	222.5
1164	S581	518	337.5
1165	S582	504	222.5
1166	S583	490	337.5
1167	S584	476	222.5
1168	S585	462	337.5
1169	S586	448	222.5
1170	S587	434	337.5
1171	S588	420	222.5
1172	S589	406	337.5
1173	S590	392	222.5
1174	S591	378	337.5
1175	S592	364	222.5
1176	S593	350	337.5
1177	S594	336	222.5
1178	S595	322	337.5
1179	S596	308	222.5
1180	S597	294	337.5
1181	S598	280	222.5
1182	S599	266	337.5
1183	S600	252	222.5
1184	SGND	182	337.5
1185	SGND	168	222.5
1186	SGND	154	337.5
1187	SGND	140	222.5
1188	SGND	126	337.5

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PAD No.	PIN Name	X	Y
1189	SGND	112	222.5
1190	SGND	98	337.5
1191	SGND	84	222.5
1192	SGND	70	337.5
1193	SGND	56	222.5
1194	SGND	42	337.5
1195	SGND	28	222.5
1196	SGND	-28	222.5
1197	SGND	-42	337.5
1198	SGND	-56	222.5
1199	SGND	-70	337.5
1200	SGND	-84	222.5
1201	SGND	-98	337.5
1202	SGND	-112	222.5
1203	SGND	-126	337.5
1204	SGND	-140	222.5
1205	SGND	-154	337.5
1206	SGND	-168	222.5
1207	SGND	-182	337.5
1208	S601	-252	222.5
1209	S602	-266	337.5
1210	S603	-280	222.5
1211	S604	-294	337.5
1212	S605	-308	222.5
1213	S606	-322	337.5
1214	S607	-336	222.5
1215	S608	-350	337.5
1216	S609	-364	222.5
1217	S610	-378	337.5
1218	S611	-392	222.5
1219	S612	-406	337.5
1220	S613	-420	222.5
1221	S614	-434	337.5

PAD No.	PIN Name	X	Y
1222	S615	-448	222.5
1223	S616	-462	337.5
1224	S617	-476	222.5
1225	S618	-490	337.5
1226	S619	-504	222.5
1227	S620	-518	337.5
1228	S621	-532	222.5
1229	S622	-546	337.5
1230	S623	-560	222.5
1231	S624	-574	337.5
1232	S625	-588	222.5
1233	S626	-602	337.5
1234	S627	-616	222.5
1235	S628	-630	337.5
1236	S629	-644	222.5
1237	S630	-658	337.5
1238	S631	-672	222.5
1239	S632	-686	337.5
1240	S633	-700	222.5
1241	S634	-714	337.5
1242	S635	-728	222.5
1243	S636	-742	337.5
1244	S637	-756	222.5
1245	S638	-770	337.5
1246	S639	-784	222.5
1247	S640	-798	337.5
1248	S641	-812	222.5
1249	S642	-826	337.5
1250	S643	-840	222.5
1251	S644	-854	337.5
1252	S645	-868	222.5
1253	S646	-882	337.5
1254	S647	-896	222.5

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PAD No.	PIN Name	X	Y
1255	S648	-910	337.5
1256	S649	-924	222.5
1257	S650	-938	337.5
1258	S651	-952	222.5
1259	S652	-966	337.5
1260	S653	-980	222.5
1261	S654	-994	337.5
1262	S655	-1008	222.5
1263	S656	-1022	337.5
1264	S657	-1036	222.5
1265	S658	-1050	337.5
1266	S659	-1064	222.5
1267	S660	-1078	337.5
1268	S661	-1092	222.5
1269	S662	-1106	337.5
1270	S663	-1120	222.5
1271	S664	-1134	337.5
1272	S665	-1148	222.5
1273	S666	-1162	337.5
1274	S667	-1176	222.5
1275	S668	-1190	337.5
1276	S669	-1204	222.5
1277	S670	-1218	337.5
1278	S671	-1232	222.5
1279	S672	-1246	337.5
1280	S673	-1260	222.5
1281	S674	-1274	337.5
1282	S675	-1288	222.5
1283	S676	-1302	337.5
1284	S677	-1316	222.5
1285	S678	-1330	337.5
1286	S679	-1344	222.5
1287	S680	-1358	337.5

PAD No.	PIN Name	X	Y
1288	S681	-1372	222.5
1289	S682	-1386	337.5
1290	S683	-1400	222.5
1291	S684	-1414	337.5
1292	S685	-1428	222.5
1293	S686	-1442	337.5
1294	S687	-1456	222.5
1295	S688	-1470	337.5
1296	S689	-1484	222.5
1297	S690	-1498	337.5
1298	S691	-1512	222.5
1299	S692	-1526	337.5
1300	S693	-1540	222.5
1301	S694	-1554	337.5
1302	S695	-1568	222.5
1303	S696	-1582	337.5
1304	S697	-1596	222.5
1305	S698	-1610	337.5
1306	S699	-1624	222.5
1307	S700	-1638	337.5
1308	S701	-1652	222.5
1309	S702	-1666	337.5
1310	S703	-1680	222.5
1311	S704	-1694	337.5
1312	S705	-1708	222.5
1313	S706	-1722	337.5
1314	S707	-1736	222.5
1315	S708	-1750	337.5
1316	S709	-1764	222.5
1317	S710	-1778	337.5
1318	S711	-1792	222.5
1319	S712	-1806	337.5
1320	S713	-1820	222.5

PAD No.	PIN Name	X	Y
1321	S714	-1834	337.5
1322	S715	-1848	222.5
1323	S716	-1862	337.5
1324	S717	-1876	222.5
1325	S718	-1890	337.5
1326	S719	-1904	222.5
1327	S720	-1918	337.5
1328	S721	-1932	222.5
1329	S722	-1946	337.5
1330	S723	-1960	222.5
1331	S724	-1974	337.5
1332	S725	-1988	222.5
1333	S726	-2002	337.5
1334	S727	-2016	222.5
1335	S728	-2030	337.5
1336	S729	-2044	222.5
1337	S730	-2058	337.5
1338	S731	-2072	222.5
1339	S732	-2086	337.5
1340	S733	-2100	222.5
1341	S734	-2114	337.5
1342	S735	-2128	222.5
1343	S736	-2142	337.5
1344	S737	-2156	222.5
1345	S738	-2170	337.5
1346	S739	-2184	222.5
1347	S740	-2198	337.5
1348	S741	-2212	222.5
1349	S742	-2226	337.5
1350	S743	-2240	222.5
1351	S744	-2254	337.5
1352	S745	-2268	222.5
1353	S746	-2282	337.5

PAD No.	PIN Name	X	Y
1354	S747	-2296	222.5
1355	S748	-2310	337.5
1356	S749	-2324	222.5
1357	S750	-2338	337.5
1358	S751	-2352	222.5
1359	S752	-2366	337.5
1360	S753	-2380	222.5
1361	S754	-2394	337.5
1362	S755	-2408	222.5
1363	S756	-2422	337.5
1364	S757	-2436	222.5
1365	S758	-2450	337.5
1366	S759	-2464	222.5
1367	S760	-2478	337.5
1368	S761	-2492	222.5
1369	S762	-2506	337.5
1370	S763	-2520	222.5
1371	S764	-2534	337.5
1372	S765	-2548	222.5
1373	S766	-2562	337.5
1374	S767	-2576	222.5
1375	S768	-2590	337.5
1376	S769	-2604	222.5
1377	S770	-2618	337.5
1378	S771	-2632	222.5
1379	S772	-2646	337.5
1380	S773	-2660	222.5
1381	S774	-2674	337.5
1382	S775	-2688	222.5
1383	S776	-2702	337.5
1384	S777	-2716	222.5
1385	S778	-2730	337.5
1386	S779	-2744	222.5

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PAD No.	PIN Name	X	Y
1387	S780	-2758	337.5
1388	S781	-2772	222.5
1389	S782	-2786	337.5
1390	S783	-2800	222.5
1391	S784	-2814	337.5
1392	S785	-2828	222.5
1393	S786	-2842	337.5
1394	S787	-2856	222.5
1395	S788	-2870	337.5
1396	S789	-2884	222.5
1397	S790	-2898	337.5
1398	S791	-2912	222.5
1399	S792	-2926	337.5
1400	S793	-2940	222.5
1401	S794	-2954	337.5
1402	S795	-2968	222.5
1403	S796	-2982	337.5
1404	S797	-2996	222.5
1405	S798	-3010	337.5
1406	S799	-3024	222.5
1407	S800	-3038	337.5
1408	S801	-3052	222.5
1409	S802	-3066	337.5
1410	S803	-3080	222.5
1411	S804	-3094	337.5
1412	S805	-3108	222.5
1413	S806	-3122	337.5
1414	S807	-3136	222.5
1415	S808	-3150	337.5
1416	S809	-3164	222.5
1417	S810	-3178	337.5
1418	S811	-3192	222.5
1419	S812	-3206	337.5

PAD No.	PIN Name	X	Y
1420	S813	-3220	222.5
1421	S814	-3234	337.5
1422	S815	-3248	222.5
1423	S816	-3262	337.5
1424	S817	-3276	222.5
1425	S818	-3290	337.5
1426	S819	-3304	222.5
1427	S820	-3318	337.5
1428	S821	-3332	222.5
1429	S822	-3346	337.5
1430	S823	-3360	222.5
1431	S824	-3374	337.5
1432	S825	-3388	222.5
1433	S826	-3402	337.5
1434	S827	-3416	222.5
1435	S828	-3430	337.5
1436	S829	-3444	222.5
1437	S830	-3458	337.5
1438	S831	-3472	222.5
1439	S832	-3486	337.5
1440	S833	-3500	222.5
1441	S834	-3514	337.5
1442	S835	-3528	222.5
1443	S836	-3542	337.5
1444	S837	-3556	222.5
1445	S838	-3570	337.5
1446	S839	-3584	222.5
1447	S840	-3598	337.5
1448	S841	-3612	222.5
1449	S842	-3626	337.5
1450	S843	-3640	222.5
1451	S844	-3654	337.5
1452	S845	-3668	222.5

PAD No.	PIN Name	X	Y
1453	S846	-3682	337.5
1454	S847	-3696	222.5
1455	S848	-3710	337.5
1456	S849	-3724	222.5
1457	S850	-3738	337.5
1458	S851	-3752	222.5
1459	S852	-3766	337.5
1460	S853	-3780	222.5
1461	S854	-3794	337.5
1462	S855	-3808	222.5
1463	S856	-3822	337.5
1464	S857	-3836	222.5
1465	S858	-3850	337.5
1466	S859	-3864	222.5
1467	S860	-3878	337.5
1468	S861	-3892	222.5
1469	S862	-3906	337.5
1470	S863	-3920	222.5
1471	S864	-3934	337.5
1472	S865	-3948	222.5
1473	S866	-3962	337.5
1474	S867	-3976	222.5
1475	S868	-3990	337.5
1476	S869	-4004	222.5
1477	S870	-4018	337.5
1478	S871	-4032	222.5
1479	S872	-4046	337.5
1480	S873	-4060	222.5
1481	S874	-4074	337.5
1482	S875	-4088	222.5
1483	S876	-4102	337.5
1484	S877	-4116	222.5
1485	S878	-4130	337.5

PAD No.	PIN Name	X	Y
1486	S879	-4144	222.5
1487	S880	-4158	337.5
1488	S881	-4172	222.5
1489	S882	-4186	337.5
1490	S883	-4200	222.5
1491	S884	-4214	337.5
1492	S885	-4228	222.5
1493	S886	-4242	337.5
1494	S887	-4256	222.5
1495	S888	-4270	337.5
1496	S889	-4284	222.5
1497	S890	-4298	337.5
1498	S891	-4312	222.5
1499	S892	-4326	337.5
1500	S893	-4340	222.5
1501	S894	-4354	337.5
1502	S895	-4368	222.5
1503	S896	-4382	337.5
1504	S897	-4396	222.5
1505	S898	-4410	337.5
1506	S899	-4424	222.5
1507	S900	-4438	337.5
1508	SGND	-4508	222.5
1509	SGND	-4522	337.5
1510	SGND	-4536	222.5
1511	SGND	-4550	337.5
1512	SGND	-4564	222.5
1513	SGND	-4578	337.5
1514	SGND	-4592	222.5
1515	SGND	-4606	337.5
1516	SGND	-4620	222.5
1517	SGND	-4634	337.5
1518	SGND	-4648	222.5

PAD No.	PIN Name	X	Y
1519	SGND	-4662	337.5
1520	SGND	-4676	222.5
1521	SGND	-4690	337.5
1522	SGND	-4704	222.5
1523	SGND	-4718	337.5
1524	S901	-4788	222.5
1525	S902	-4802	337.5
1526	S903	-4816	222.5
1527	S904	-4830	337.5
1528	S905	-4844	222.5
1529	S906	-4858	337.5
1530	S907	-4872	222.5
1531	S908	-4886	337.5
1532	S909	-4900	222.5
1533	S910	-4914	337.5
1534	S911	-4928	222.5
1535	S912	-4942	337.5
1536	S913	-4956	222.5
1537	S914	-4970	337.5
1538	S915	-4984	222.5
1539	S916	-4998	337.5
1540	S917	-5012	222.5
1541	S918	-5026	337.5
1542	S919	-5040	222.5
1543	S920	-5054	337.5
1544	S921	-5068	222.5
1545	S922	-5082	337.5
1546	S923	-5096	222.5
1547	S924	-5110	337.5
1548	S925	-5124	222.5
1549	S926	-5138	337.5
1550	S927	-5152	222.5
1551	S928	-5166	337.5

PAD No.	PIN Name	X	Y
1552	S929	-5180	222.5
1553	S930	-5194	337.5
1554	S931	-5208	222.5
1555	S932	-5222	337.5
1556	S933	-5236	222.5
1557	S934	-5250	337.5
1558	S935	-5264	222.5
1559	S936	-5278	337.5
1560	S937	-5292	222.5
1561	S938	-5306	337.5
1562	S939	-5320	222.5
1563	S940	-5334	337.5
1564	S941	-5348	222.5
1565	S942	-5362	337.5
1566	S943	-5376	222.5
1567	S944	-5390	337.5
1568	S945	-5404	222.5
1569	S946	-5418	337.5
1570	S947	-5432	222.5
1571	S948	-5446	337.5
1572	S949	-5460	222.5
1573	S950	-5474	337.5
1574	S951	-5488	222.5
1575	S952	-5502	337.5
1576	S953	-5516	222.5
1577	S954	-5530	337.5
1578	S955	-5544	222.5
1579	S956	-5558	337.5
1580	S957	-5572	222.5
1581	S958	-5586	337.5
1582	S959	-5600	222.5
1583	S960	-5614	337.5
1584	S961	-5628	222.5

PAD No.	PIN Name	X	Y
1585	S962	-5642	337.5
1586	S963	-5656	222.5
1587	S964	-5670	337.5
1588	S965	-5684	222.5
1589	S966	-5698	337.5
1590	S967	-5712	222.5
1591	S968	-5726	337.5
1592	S969	-5740	222.5
1593	S970	-5754	337.5
1594	S971	-5768	222.5
1595	S972	-5782	337.5
1596	S973	-5796	222.5
1597	S974	-5810	337.5
1598	S975	-5824	222.5
1599	S976	-5838	337.5
1600	S977	-5852	222.5
1601	S978	-5866	337.5
1602	S979	-5880	222.5
1603	S980	-5894	337.5
1604	S981	-5908	222.5
1605	S982	-5922	337.5
1606	S983	-5936	222.5
1607	S984	-5950	337.5
1608	S985	-5964	222.5
1609	S986	-5978	337.5
1610	S987	-5992	222.5
1611	S988	-6006	337.5
1612	S989	-6020	222.5
1613	S990	-6034	337.5
1614	S991	-6048	222.5
1615	S992	-6062	337.5
1616	S993	-6076	222.5
1617	S994	-6090	337.5
1618	S995	-6104	222.5
1619	S996	-6118	337.5
1620	S997	-6132	222.5
1621	S998	-6146	337.5
1622	S999	-6160	222.5
1623	S1000	-6174	337.5
1624	S1001	-6188	222.5
1625	S1002	-6202	337.5
1626	S1003	-6216	222.5
1627	S1004	-6230	337.5
1628	S1005	-6244	222.5
1629	S1006	-6258	337.5
1630	S1007	-6272	222.5
1631	S1008	-6286	337.5
1632	S1009	-6300	222.5
1633	S1010	-6314	337.5
1634	S1011	-6328	222.5
1635	S1012	-6342	337.5
1636	S1013	-6356	222.5
1637	S1014	-6370	337.5
1638	S1015	-6384	222.5
1639	S1016	-6398	337.5
1640	S1017	-6412	222.5
1641	S1018	-6426	337.5
1642	S1019	-6440	222.5
1643	S1020	-6454	337.5
1644	S1021	-6468	222.5
1645	S1022	-6482	337.5
1646	S1023	-6496	222.5
1647	S1024	-6510	337.5
1648	S1025	-6524	222.5
1649	S1026	-6538	337.5
1650	S1027	-6552	222.5

PAD No.	PIN Name	X	Y
1651	S1028	-6566	337.5
1652	S1029	-6580	222.5
1653	S1030	-6594	337.5
1654	S1031	-6608	222.5
1655	S1032	-6622	337.5
1656	S1033	-6636	222.5
1657	S1034	-6650	337.5
1658	S1035	-6664	222.5
1659	S1036	-6678	337.5
1660	S1037	-6692	222.5
1661	S1038	-6706	337.5
1662	S1039	-6720	222.5
1663	S1040	-6734	337.5
1664	S1041	-6748	222.5
1665	S1042	-6762	337.5
1666	S1043	-6776	222.5
1667	S1044	-6790	337.5
1668	S1045	-6804	222.5
1669	S1046	-6818	337.5
1670	S1047	-6832	222.5
1671	S1048	-6846	337.5
1672	S1049	-6860	222.5
1673	S1050	-6874	337.5
1674	S1051	-6888	222.5
1675	S1052	-6902	337.5
1676	S1053	-6916	222.5
1677	S1054	-6930	337.5
1678	S1055	-6944	222.5
1679	S1056	-6958	337.5
1680	S1057	-6972	222.5
1681	S1058	-6986	337.5
1682	S1059	-7000	222.5
1683	S1060	-7014	337.5

PAD No.	PIN Name	X	Y
1684	S1061	-7028	222.5
1685	S1062	-7042	337.5
1686	S1063	-7056	222.5
1687	S1064	-7070	337.5
1688	S1065	-7084	222.5
1689	S1066	-7098	337.5
1690	S1067	-7112	222.5
1691	S1068	-7126	337.5
1692	S1069	-7140	222.5
1693	S1070	-7154	337.5
1694	S1071	-7168	222.5
1695	S1072	-7182	337.5
1696	S1073	-7196	222.5
1697	S1074	-7210	337.5
1698	S1075	-7224	222.5
1699	S1076	-7238	337.5
1700	S1077	-7252	222.5
1701	S1078	-7266	337.5
1702	S1079	-7280	222.5
1703	S1080	-7294	337.5
1704	S1081	-7308	222.5
1705	S1082	-7322	337.5
1706	S1083	-7336	222.5
1707	S1084	-7350	337.5
1708	S1085	-7364	222.5
1709	S1086	-7378	337.5
1710	S1087	-7392	222.5
1711	S1088	-7406	337.5
1712	S1089	-7420	222.5
1713	S1090	-7434	337.5
1714	S1091	-7448	222.5
1715	S1092	-7462	337.5
1716	S1093	-7476	222.5

PAD No.	PIN Name	X	Y
1717	S1094	-7490	337.5
1718	S1095	-7504	222.5
1719	S1096	-7518	337.5
1720	S1097	-7532	222.5
1721	S1098	-7546	337.5
1722	S1099	-7560	222.5
1723	S1100	-7574	337.5
1724	S1101	-7588	222.5
1725	S1102	-7602	337.5
1726	S1103	-7616	222.5
1727	S1104	-7630	337.5
1728	S1105	-7644	222.5
1729	S1106	-7658	337.5
1730	S1107	-7672	222.5
1731	S1108	-7686	337.5
1732	S1109	-7700	222.5
1733	S1110	-7714	337.5
1734	S1111	-7728	222.5
1735	S1112	-7742	337.5
1736	S1113	-7756	222.5
1737	S1114	-7770	337.5
1738	S1115	-7784	222.5
1739	S1116	-7798	337.5
1740	S1117	-7812	222.5
1741	S1118	-7826	337.5
1742	S1119	-7840	222.5
1743	S1120	-7854	337.5
1744	S1121	-7868	222.5
1745	S1122	-7882	337.5
1746	S1123	-7896	222.5
1747	S1124	-7910	337.5
1748	S1125	-7924	222.5
1749	S1126	-7938	337.5

PAD No.	PIN Name	X	Y
1750	S1127	-7952	222.5
1751	S1128	-7966	337.5
1752	S1129	-7980	222.5
1753	S1130	-7994	337.5
1754	S1131	-8008	222.5
1755	S1132	-8022	337.5
1756	S1133	-8036	222.5
1757	S1134	-8050	337.5
1758	S1135	-8064	222.5
1759	S1136	-8078	337.5
1760	S1137	-8092	222.5
1761	S1138	-8106	337.5
1762	S1139	-8120	222.5
1763	S1140	-8134	337.5
1764	S1141	-8148	222.5
1765	S1142	-8162	337.5
1766	S1143	-8176	222.5
1767	S1144	-8190	337.5
1768	S1145	-8204	222.5
1769	S1146	-8218	337.5
1770	S1147	-8232	222.5
1771	S1148	-8246	337.5
1772	S1149	-8260	222.5
1773	S1150	-8274	337.5
1774	S1151	-8288	222.5
1775	S1152	-8302	337.5
1776	S1153	-8316	222.5
1777	S1154	-8330	337.5
1778	S1155	-8344	222.5
1779	S1156	-8358	337.5
1780	S1157	-8372	222.5
1781	S1158	-8386	337.5
1782	S1159	-8400	222.5

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PAD No.	PIN Name	X	Y
1783	S1160	-8414	337.5
1784	S1161	-8428	222.5
1785	S1162	-8442	337.5
1786	S1163	-8456	222.5
1787	S1164	-8470	337.5
1788	S1165	-8484	222.5
1789	S1166	-8498	337.5
1790	S1167	-8512	222.5
1791	S1168	-8526	337.5
1792	S1169	-8540	222.5
1793	S1170	-8554	337.5
1794	S1171	-8568	222.5
1795	S1172	-8582	337.5
1796	S1173	-8596	222.5
1797	S1174	-8610	337.5
1798	S1175	-8624	222.5
1799	S1176	-8638	337.5
1800	S1177	-8652	222.5
1801	S1178	-8666	337.5
1802	S1179	-8680	222.5
1803	S1180	-8694	337.5
1804	S1181	-8708	222.5
1805	S1182	-8722	337.5
1806	S1183	-8736	222.5
1807	S1184	-8750	337.5
1808	S1185	-8764	222.5
1809	S1186	-8778	337.5
1810	S1187	-8792	222.5
1811	S1188	-8806	337.5
1812	S1189	-8820	222.5
1813	S1190	-8834	337.5
1814	S1191	-8848	222.5
1815	S1192	-8862	337.5

PAD No.	PIN Name	X	Y
1816	S1193	-8876	222.5
1817	S1194	-8890	337.5
1818	S1195	-8904	222.5
1819	S1196	-8918	337.5
1820	S1197	-8932	222.5
1821	S1198	-8946	337.5
1822	S1199	-8960	222.5
1823	S1200	-8974	337.5
1824	S1201	-8988	222.5
1825	SGND	-9044	222.5
1826	SGND	-9058	337.5
1827	SGND	-9072	222.5
1828	SGND	-9086	337.5
1829	SGND	-9100	222.5
1830	SGND	-9114	337.5
1831	SGND	-9128	222.5
1832	SGND	-9142	337.5
1833	SGND	-9156	222.5
1834	SGND	-9170	337.5
1835	SGND	-9184	222.5
1836	SGND	-9198	337.5
1837	SGND	-9212	222.5
1838	SGND	-9226	337.5
1839	SGND	-9240	222.5
1840	SGND	-9254	337.5
1841	DUMMY	-9324	222.5
1842	DUMMY	-9338	337.5
1843	DUMMY	-9352	222.5
1844	DUMMY	-9366	337.5
1845	DUMMY	-9380	222.5
1846	DUMMY	-9394	337.5
1847	DUMMY	-9408	222.5
1848	DUMMY	-9422	337.5

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PAD No.	PIN Name	X	Y
1849	DUMMY	-9436	222.5
1850	DUMMY	-9450	337.5
1851	DUMMY	-9464	222.5
1852	DUMMY	-9478	337.5
1853	DUMMY	-9492	222.5
1854	DUMMY	-9506	337.5
1855	DUMMY	-9520	222.5
1856	DUMMY	-9534	337.5
1857	DUMMY	-9548	222.5
1858	DUMMY	-9562	337.5
1859	DUMMY	-9576	222.5
1860	DUMMY	-9590	337.5
1861	DUMMY	-9604	222.5
1862	DUMMY	-9618	337.5
1863	DUMMY	-9632	222.5
1864	DUMMY	-9646	337.5
1865	DUMMY	-9660	222.5
1866	DUMMY	-9674	337.5
1867	DUMMY	-9688	222.5
1868	DUMMY	-9702	337.5
1869	DUMMY	-9716	222.5
1870	DUMMY	-9730	337.5
1871	DUMMY	-9744	222.5
1872	DUMMY	-9758	337.5
1873	DUMMY	-9772	222.5
1874	DUMMY	-9786	337.5
1875	DUMMY	-9800	222.5
1876	DUMMY	-9814	337.5
1877	DUMMY	-9828	222.5
1878	DUMMY	-9842	337.5
1879	DUMMY	-9856	222.5
1880	DUMMY	-9870	337.5
1881	DUMMY	-9884	222.5

PAD No.	PIN Name	X	Y
1882	DUMMY	-9898	337.5
1883	DUMMY	-9912	222.5
1884	DUMMY	-9926	337.5
1885	DUMMY	-9940	222.5
1886	DUMMY	-9954	337.5
1887	DUMMY	-9968	222.5
1888	DUMMY	-9982	337.5
1889	DUMMY	-9996	222.5
1890	DUMMY	-10010	337.5
1891	DUMMY	-10024	222.5
1892	DUMMY	-10038	337.5
1893	DUMMY	-10052	222.5
1894	DUMMY	-10066	337.5
1895	DUMMY	-10080	222.5
1896	DUMMY	-10094	337.5
1897	DUMMY	-10108	222.5
1898	DUMMY	-10122	337.5
1899	DUMMY	-10136	222.5
1900	DUMMY	-10150	337.5
1901	DUMMY	-10164	222.5
1902	DUMMY	-10178	337.5
1903	DUMMY	-10192	222.5
1904	DUMMY	-10206	337.5
1905	DUMMY	-10220	222.5
1906	DUMMY	-10234	337.5
1907	DUMMY	-10248	222.5
1908	DUMMY	-10262	337.5
1909	DUMMY	-10276	222.5
1910	DUMMY	-10290	337.5
1911	DUMMY	-10304	222.5
1912	DUMMY	-10318	337.5
1913	DUMMY	-10332	222.5
1914	DUMMY	-10346	337.5

PAD No.	PIN Name	X	Y
1915	DUMMY	-10360	222.5
1916	DUMMY	-10374	337.5
1917	DUMMY	-10388	222.5
1918	DUMMY	-10402	337.5
1919	DUMMY	-10416	222.5
1920	DUMMY	-10430	337.5
1921	DUMMY	-10444	222.5
1922	DUMMY	-10458	337.5
1923	DUMMY	-10472	222.5
1924	DUMMY	-10486	337.5
1925	DUMMY	-10500	222.5
1926	DUMMY	-10514	337.5
1927	DUMMY	-10528	222.5
1928	DUMMY	-10542	337.5
1929	DUMMY	-10556	222.5
1930	DUMMY	-10570	337.5
1931	DUMMY	-10584	222.5
1932	DUMMY	-10598	337.5
1933	DUMMY	-10612	222.5
1934	DUMMY	-10626	337.5
1935	DUMMY	-10640	222.5
1936	DUMMY	-10654	337.5
1937	DUMMY	-10668	222.5
1938	DUMMY	-10682	337.5
1939	DUMMY	-10752	222.5
1940	VGL	-10766	337.5
1941	DUMMY	-10780	222.5
1942	VGL	-10794	337.5
1943	DUMMY	-10808	222.5
1944	VGL	-10822	337.5
1945	DUMMY	-10836	222.5
1946	VGH	-10850	337.5
1947	DUMMY	-10864	222.5

PAD No.	PIN Name	X	Y
1948	VGH	-10878	337.5
1949	DUMMY	-10892	222.5
1950	VGH	-10906	337.5
1951	GOL[10]	-10976	222.5
1952	GOL[10]	-10990	337.5
1953	GOL[10]	-11004	222.5
1954	GOL[9]	-11018	337.5
1955	GOL[9]	-11032	222.5
1956	GOL[9]	-11046	337.5
1957	GOL[8]	-11060	222.5
1958	GOL[8]	-11074	337.5
1959	GOL[8]	-11088	222.5
1960	GOL[7]	-11102	337.5
1961	GOL[7]	-11116	222.5
1962	GOL[7]	-11130	337.5
1963	GOL[6]	-11144	222.5
1964	GOL[6]	-11158	337.5
1965	GOL[6]	-11172	222.5
1966	GOL[5]	-11186	337.5
1967	GOL[5]	-11200	222.5
1968	GOL[5]	-11214	337.5
1969	GOL[4]	-11228	222.5
1970	GOL[4]	-11242	337.5
1971	GOL[4]	-11256	222.5
1972	GOL[3]	-11270	337.5
1973	GOL[3]	-11284	222.5
1974	GOL[3]	-11298	337.5
1975	GOL[2]	-11312	222.5
1976	GOL[2]	-11326	337.5
1977	GOL[2]	-11340	222.5
1978	GOL[1]	-11354	337.5
1979	GOL[1]	-11368	222.5
1980	GOL[1]	-11382	337.5

PAD No.	PIN Name	X	Y
1981	GOL[12]	-11452	222.5
1982	GOL[12]	-11466	337.5
1983	GOL[12]	-11480	222.5
1984	GOL[11]	-11494	337.5
1985	GOL[11]	-11508	222.5
1986	GOL[11]	-11522	337.5
1987	VGH	-11536	222.5
1988	VGH	-11550	337.5
1989	VGH	-11564	222.5
1990	VGH	-11578	337.5
1991	VGH	-11592	222.5
1992	VGH	-11606	337.5
1993	L_MARK	-11812	-337
1994	R_MARK	11812	-337

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5. BLOCK DIAGRAM

T.B.D

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6. PIN DESCRIPTION

6.1 Pin Function

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">3-Wire SPI Interface Pins</td></tr>
<tr><td>SPI_ I²C _SEL</td><td>I</td><td>3-wire SPI and I²C interface control.
<table>
<tr><th>SPI_ I²C _SEL</th><th>Function Description</th></tr>
<tr><td>L</td><td>I²C interface</td></tr>
<tr><td>H</td><td>3-wire SPI interface (Default)</td></tr>
</table></td></tr>
<tr><td>CS</td><td>I</td><td>Serial communication chip selection.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input and output.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input.</td></tr>
<tr><td colspan="3">Control Pins</td></tr>
<tr><td>EXT_S
EXT_G</td><td>I</td><td>Power mode setting
<table>
<tr><th>EXT_S</th><th>EXT_G</th><th>Function Description</th></tr>
<tr><td>L</td><td>L</td><td>1 power mode (Internal pump)</td></tr>
<tr><td>L</td><td>H</td><td>Reserved (Do not use)</td></tr>
<tr><td>H</td><td>L</td><td>3 power mode (External power supply)
3 Power mode (Charge pump controller)</td></tr>
<tr><td>H</td><td>H</td><td>5 power mode (External power supply)</td></tr>
</table></td></tr>
<tr><td>VCSW[2:1]</td><td>O</td><td>Charge pump controller (power IC) control pin.</td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. When GRB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>DISP</td><td>I</td><td>DISP sets the display mode.
<table>
<tr><th>DISP</th><th>Function Description</th></tr>
<tr><td>L</td><td>Standby mode(Default)</td></tr>
<tr><td>H</td><td>Normal display mode</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>I</td><td>Horizontal scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>HDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From right to left</td></tr>
<tr><td>H</td><td>From left to right(Default)</td></tr>
</table></td></tr>
<tr><td>VDIR</td><td>I</td><td>Vertical scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>VDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From down to up</td></tr>
<tr><td>H</td><td>From up to down(Default)</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>AUTODL</td><td>I</td><td>OTP trim function control pin. When normal display, AUTODL should be set to “H” and the value in the OTP will be downloaded automatically.
<table>
<tr><th>AUTODL</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable auto-refresh function</td></tr>
<tr><td>H</td><td>Enable auto-refresh function(Default)</td></tr>
</table></td></tr>
<tr><td>BIST_EN</td><td>I</td><td>BIST function control pin.
<table>
<tr><th>BIST_EN</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable BIST function(Default)</td></tr>
<tr><td>H</td><td>Enable BIST function</td></tr>
</table></td></tr>
<tr><td>INTF1 / INTF0</td><td>I</td><td>Set interface.
<table>
<tr><th>INTF 1</th><th>INTF 0</th><th>Function Description</th></tr>
<tr><td>L</td><td>L</td><td>RGB Interface</td></tr>
<tr><td>L</td><td>H</td><td>Reserved</td></tr>
<tr><td>H</td><td>L</td><td>LVDS Interface</td></tr>
<tr><td>H</td><td>H</td><td>MIPI Interface</td></tr>
</table></td></tr>
<tr><td colspan="3">Interface Control Pins</td></tr>
<tr><td>VDPOL_LVDS_SEL</td><td>I</td><td>VDPOL_LVDS_SEL sets VSYNC polarity in RGB interface and data format 3, 4 lane in LVDS interface.
<table>
<tr><th>MCU Type</th><th>VDPOL_LVDS_SEL</th><th>Function Description</th></tr>
<tr><td rowspan="2">RGB interface</td><td>L</td><td>VSYNC polarity: positive</td></tr>
<tr><td>H</td><td>VSYNC polarity: negative(Default)</td></tr>
<tr><td rowspan="2">LVDS interface</td><td>L</td><td>LVDS 3 lane</td></tr>
<tr><td>H</td><td>LVDS 4 lane(Default)</td></tr>
</table>
VDPOL_LVDS_SEL pin should be connected to “L” when it is used in MIPI interface.</td></tr>
<tr><td>HDPOL_LVDS_SWAP</td><td>I</td><td>HDPOL sets HSYNC polarity in RGB interface.
<table>
<tr><th>MCU Type</th><th>HDPOL_LVDS_SWAP</th><th>Function Description</th></tr>
<tr><td rowspan="2">RGB interface</td><td>L</td><td>HSYNC polarity: positive</td></tr>
<tr><td>H</td><td>HSYNC polarity: negative(Default)</td></tr>
<tr><td rowspan="2">LVDS interface</td><td>L</td><td>RESERVED</td></tr>
<tr><td>H</td><td>RESERVED</td></tr>
</table>
HDPOL_LVDS_SWAP pin should be connected to “L” when it is used in MIPI interface.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DCLKPOL</td><td>I</td><td>DCLKPOL sets DCLK polarity in RGB interface.
<table>
<tr><th>DCLKPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>DCLK polarity: positive</td></tr>
<tr><td>H</td><td>DCLK polarity: negative(Default)</td></tr>
</table>
DCLKPOL pin should be connected to “L” when it is used in LVDS and MIPI interface.</td></tr>
<tr><td>LVDS_FMT</td><td>I</td><td>LVDS_FMT sets LVDS data format.
<table>
<tr><th>LVDS_FMT</th><th>Function Description</th></tr>
<tr><td>L</td><td>VESA Mode</td></tr>
<tr><td>H</td><td>JEIDA Mode(Default)</td></tr>
</table>
LVDS_FMT pin should be connected to “L” when it is used in RGB and MIPI interface.</td></tr>
<tr><td colspan="3">Input Interface Pins</td></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]</td><td>I</td><td>RGB interface and LVDS interface data input pins.
LVDS pin definition. Please refer to LVDS Input Pin Mapping Table.
<table>
<tr><th>MCU Type</th><th colspan="2">Function Description</th></tr>
<tr><td rowspan="3">RGB interface</td><td>DR[7:0]</td><td>8 bit data bus display red data</td></tr>
<tr><td>DG[7:0]</td><td>8 bit data bus display green data</td></tr>
<tr><td>DB[7:0]</td><td>8 bit data bus display blue data</td></tr>
<tr><td rowspan="6">LVDS interface</td><td>DR[7:0]</td><td>DR[7:0] are not used in LVDS mode and should be connected to “L”</td></tr>
<tr><td>DG[7:0]</td><td>DG[7:0] are not used in LVDS mode and should be connected to “L”</td></tr>
<tr><td>DB[1:0]</td><td>LVDS input lane: RX0N/ RX0P</td></tr>
<tr><td>DB[3:2]</td><td>LVDS input lane: RX1N/ RX1P</td></tr>
<tr><td>DB[5:4]</td><td>LVDS input lane: RX2N/ RX2P</td></tr>
<tr><td>DB[7:6]</td><td>LVDS input lane: RX3N/ RX3P</td></tr>
<tr><td rowspan="3">MIPI Interface</td><td>DR[7:0]</td><td>DR[7:0] are not used in MIPI mode and should be connected to “L”</td></tr>
<tr><td>DG[7:0]</td><td>DG[7:0] are not used in MIPI mode and should be connected to “L”</td></tr>
<tr><td>DB[7:0]</td><td>DB[7:0] are not used in MIPI mode and should be connected to “L”</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DCLKP</td><td>I</td><td>Pixel clock/ RXCLKP control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>Pixel clock input pin</td></tr>
<tr><td>LVDS interface</td><td>RXCLKP control pin. This is LVDS clock input pin, detail pin define please refer to LVDS Input Pin Mapping Table</td></tr>
<tr><td>MIPI interface</td><td>MIPI interface: DCLKP is not used in MIPI interface and should be connected to “L”</td></tr>
</table></td></tr>
<tr><td>DCLKN</td><td>I</td><td>RXCLKN control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>RGB interface: DCLKN is not used in RGB interface and should be connected to “L”</td></tr>
<tr><td>LVDS interface</td><td>LVDS clock input pin, detail pin define please refer to LVDS Input Pin Mapping Table</td></tr>
<tr><td>MIPI interface</td><td>MIPI interface: DCLKN is not used in MIPI interface and should be connected to “L”</td></tr>
</table></td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync signal applied to the RGB interface.
HSYNC pin should be connected to “L” when it is used in LVDS and MIPI interface.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync signal applied to the RGB interface.
VSYNC pin should be connected to “L” when it is used in LVDS and MIPI interface.</td></tr>
<tr><td>DE</td><td>I</td><td>Data input enable applied to the RGB interface.
DE pin should be connected to “L” when it is used in LVDS and MIPI interface.</td></tr>
<tr><td>CP</td><td>I</td><td>MIPI-DSI clock lane positive-end input pin
CLKP pin should be connected to “L” when it is used in RGB and LVDS interface.</td></tr>
<tr><td>C</td><td>I</td><td>MIPI-DSI clock lane negative-end input pin
CLKN pin should be connected to “L” when it is used in RGB and LVDS interface</td></tr>
<tr><td>DP0</td><td>I/O</td><td>MIPI-DSI data lane 0 positive-end input/output pin
DATA0P pin should be connected to “L” when it is used in RGB and LVDS interface</td></tr>
<tr><td>DN0</td><td>I/O</td><td>MIPI-DSI data lane 0 negative-end input/output pin
DATA0N pin should be connected to “L” when it is used in RGB and LVDS interface</td></tr>
<tr><td>DP1</td><td>I</td><td>MIPI-DSI data lane 1 positive-end input/output pin
DATA1P pin should be connected to “L” when it is used in RGB and LVDS interface</td></tr>
</table>

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Name	Type	Description
DN1	I	MIPI-DSI data lane 1 negative-end input/output pin DATA1N pin should be connected to “L” when it is used in RGB and LVDS interface
Source / Gate Driver Pins		
S[1200:1]	O	Source driver output signals.
S[1201], S[0]	O	Souce driver output for Zigzag panel type used. If not use, please let it open.
GOR[12:1] GOL[12:1]	O	GIP control signals.
VCOM Generator Pin		
VCOM	C	Power supply for the TFT-LCD common electrode.
Power Supply Pins		
VDD	P	Power supply for analog circuit.
VDD1	P	Power supply for analog circuit.
VDDI	P	Power supply for digital I/O pins.
PVDD	P	Power supply for charge pump circuit.
DGND	P	Ground pin for digital circuit.
AGND	P	Ground pin for analog circuit.
SGND	P	Ground pin for source circuit.
PGND	P	Ground pin for charge pump circuit.
Power Circuit Pins		
SVDD	C	DC/DC converter for positive source OP-AMP driver.
AVDD	C	DC/DC converter for positive gamma voltage.
SVCL	C	DC/DC converter for negative source OP-AMP driver.
AVCL	C	DC/DC converter for negative gamma voltage.
VCC	C	Internal digital power.
VGH	C	Positive power supply for gate driver.
VCCM	C	Internal digital power1.
VGL	C	Negative power supply for gate driver.
C11P	C	The positive terminal of the charge-pump transfer capacitor.
C11N	C	The negative terminal of the charge-pump transfer capacitor.
C12P	C	The positive terminal of the charge-pump transfer capacitor.
C12N	C	The negative terminal of the charge-pump transfer capacitor.
Test Pins		
GVDD	T	Monitor pin of internal positive grayscale power.
GVCL	T	Monitor pin of internal negative grayscale power.
VGSP	T	Monitor pin of internal VCOM offset.

Name	Type	Description
VPP	T	Reserved for test only, please leave it open.
TESTI[4:0]	T	Reserved for test only, please leave those pins open.
DUMMY	D	Dummy pin, please leave those pins open.

Note: 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin.

2. If hardware pin is not used, please fix to "H" by VDDI or "L" by DGND.

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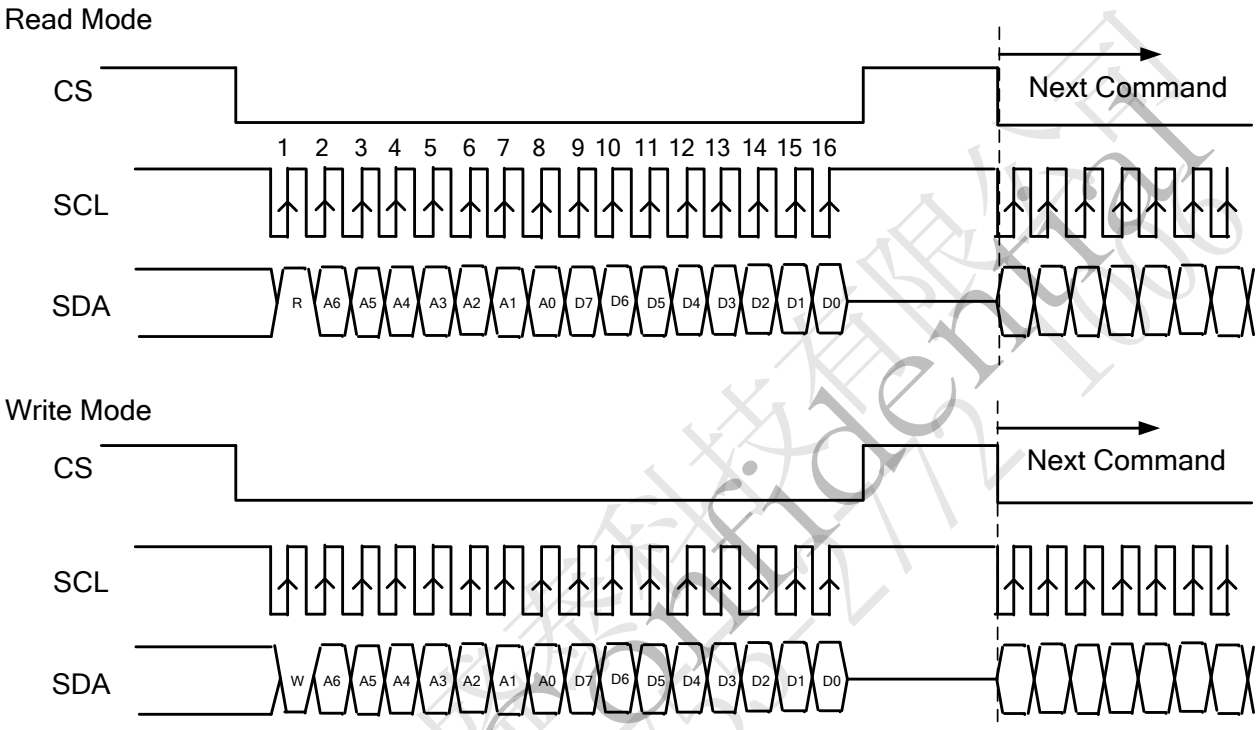
7. COMMUNICATION INTERFACE

7.1 3-wire Serial Interface

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

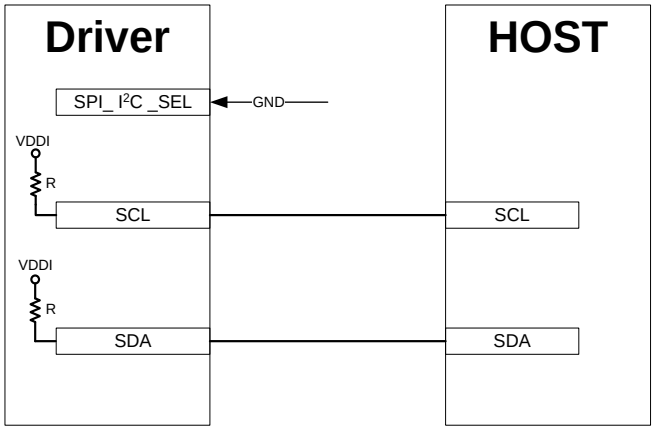
f. Serial block operates with the SCL clock.

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

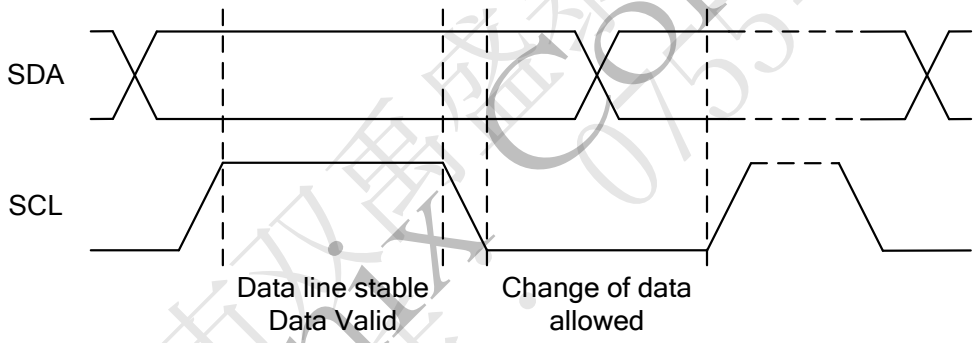
7.2 I²C Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.



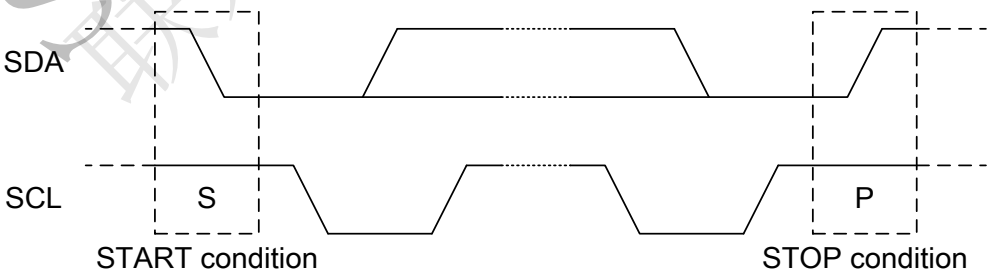
7.2.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

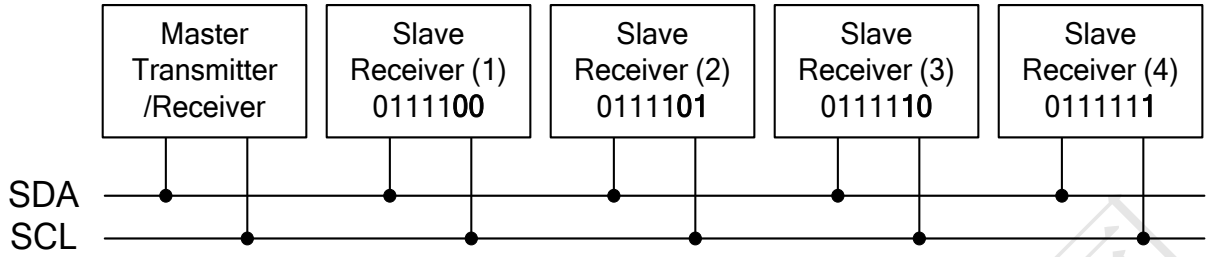


7.2.2 START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.



7.2.3 System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

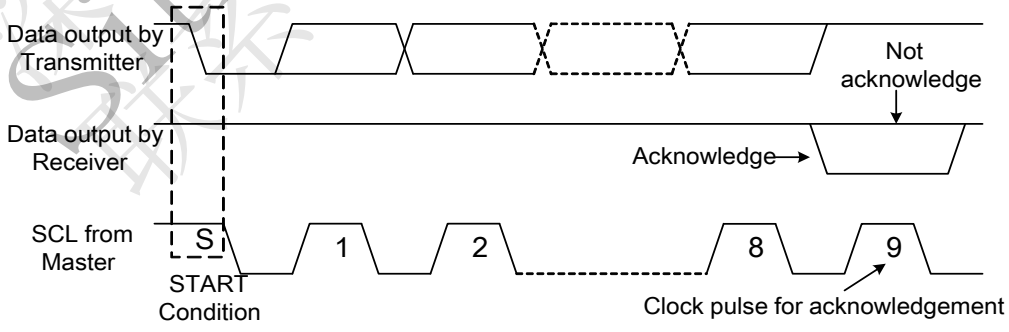
e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

7.2.4 Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated as follows.



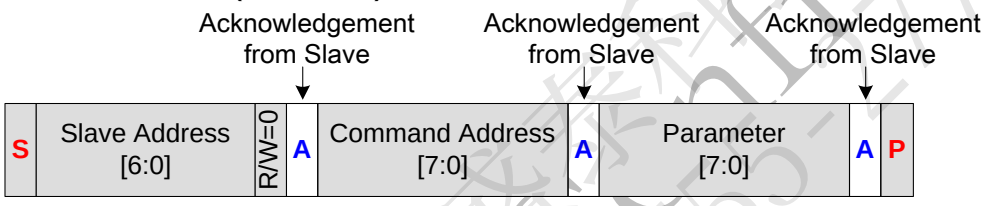
7.2.5 I²C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I²C address could be OTP programing.

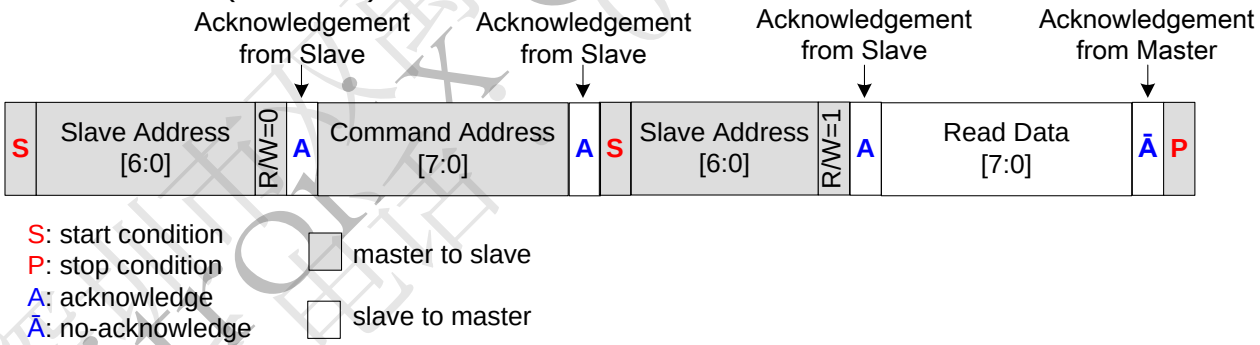
The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.

Write Mode (R/W="0")



Read Mode (R/W="1")



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7.3 RGB Interface

RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side.

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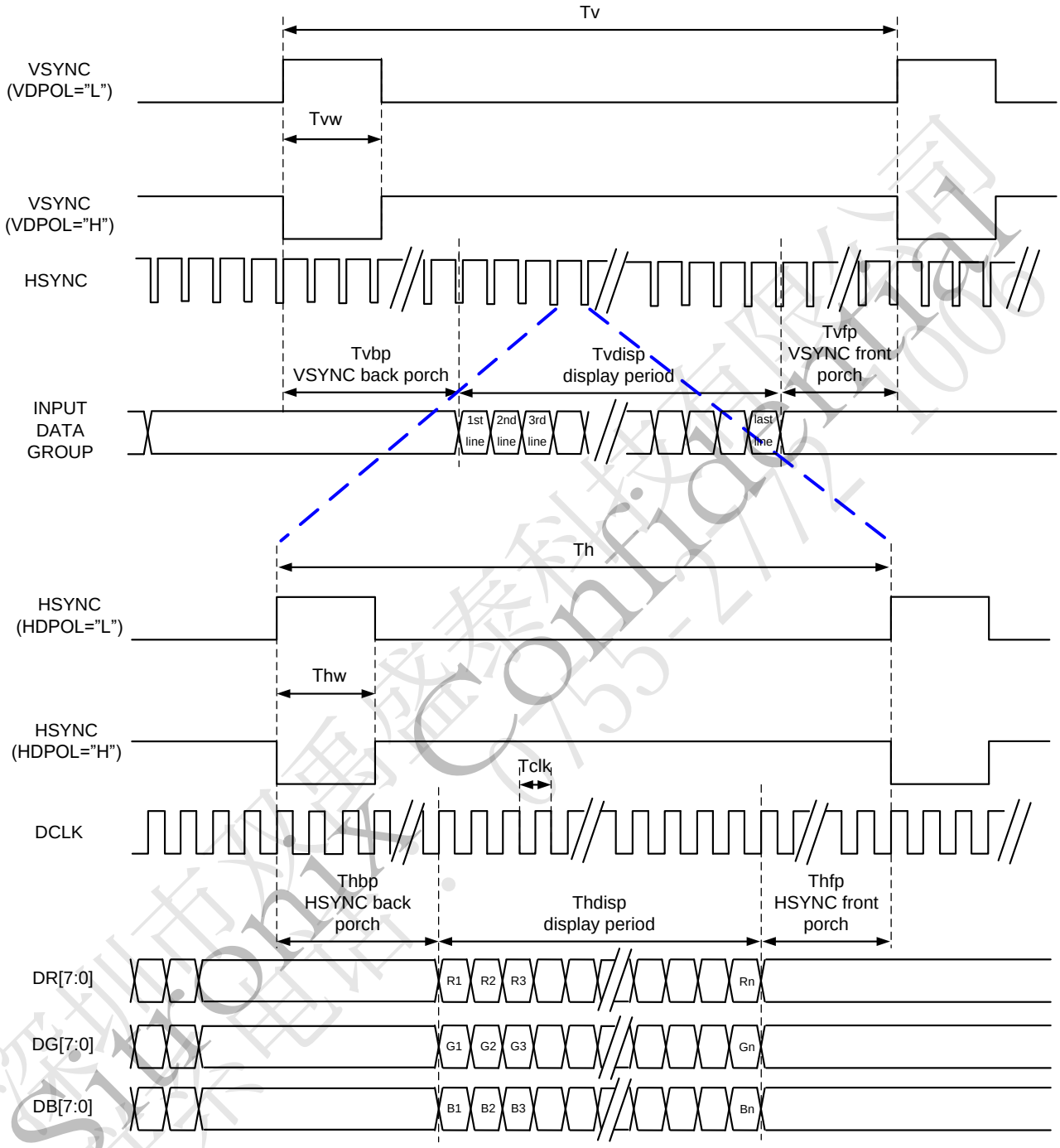
7.3.1 SYNC Mode



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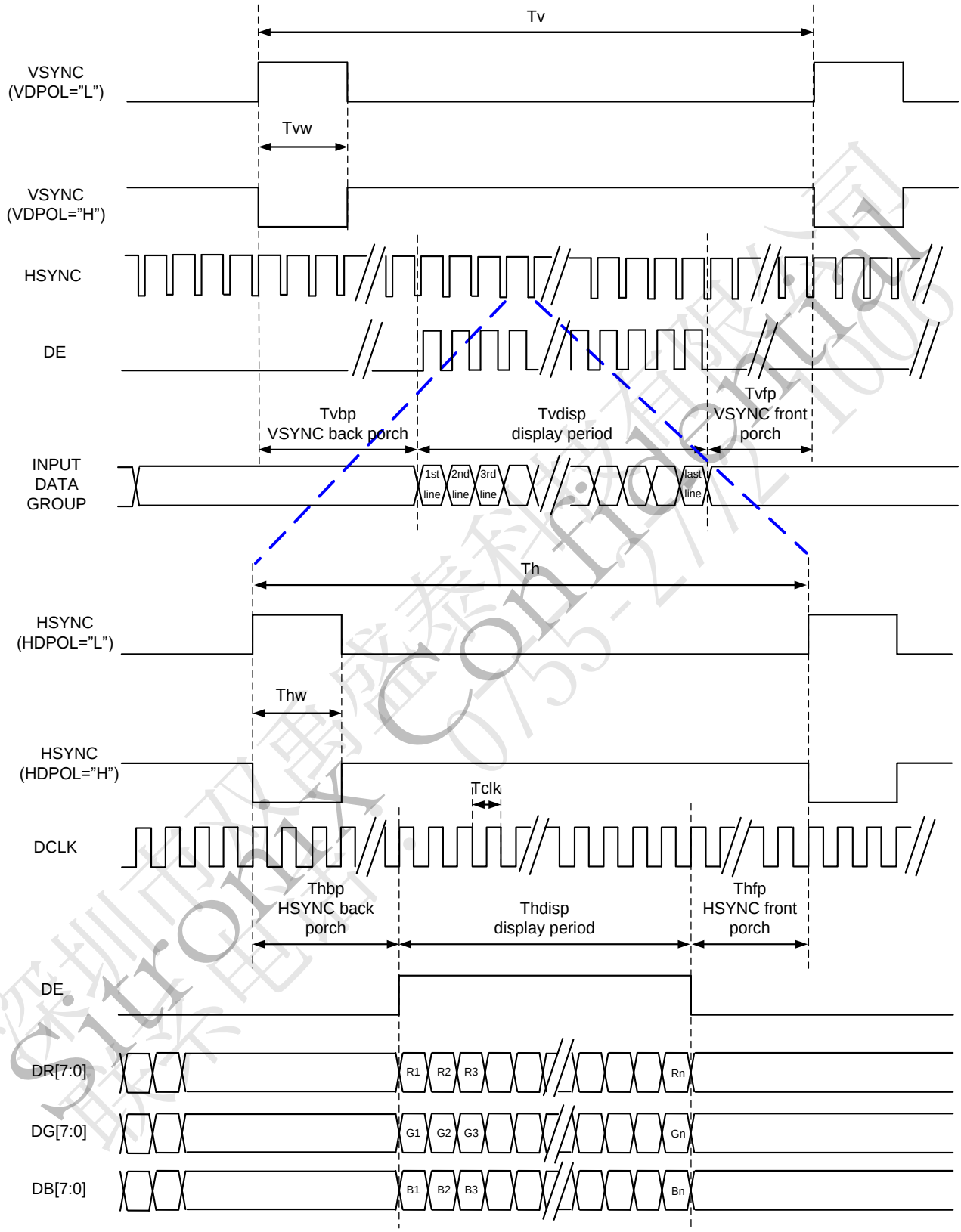
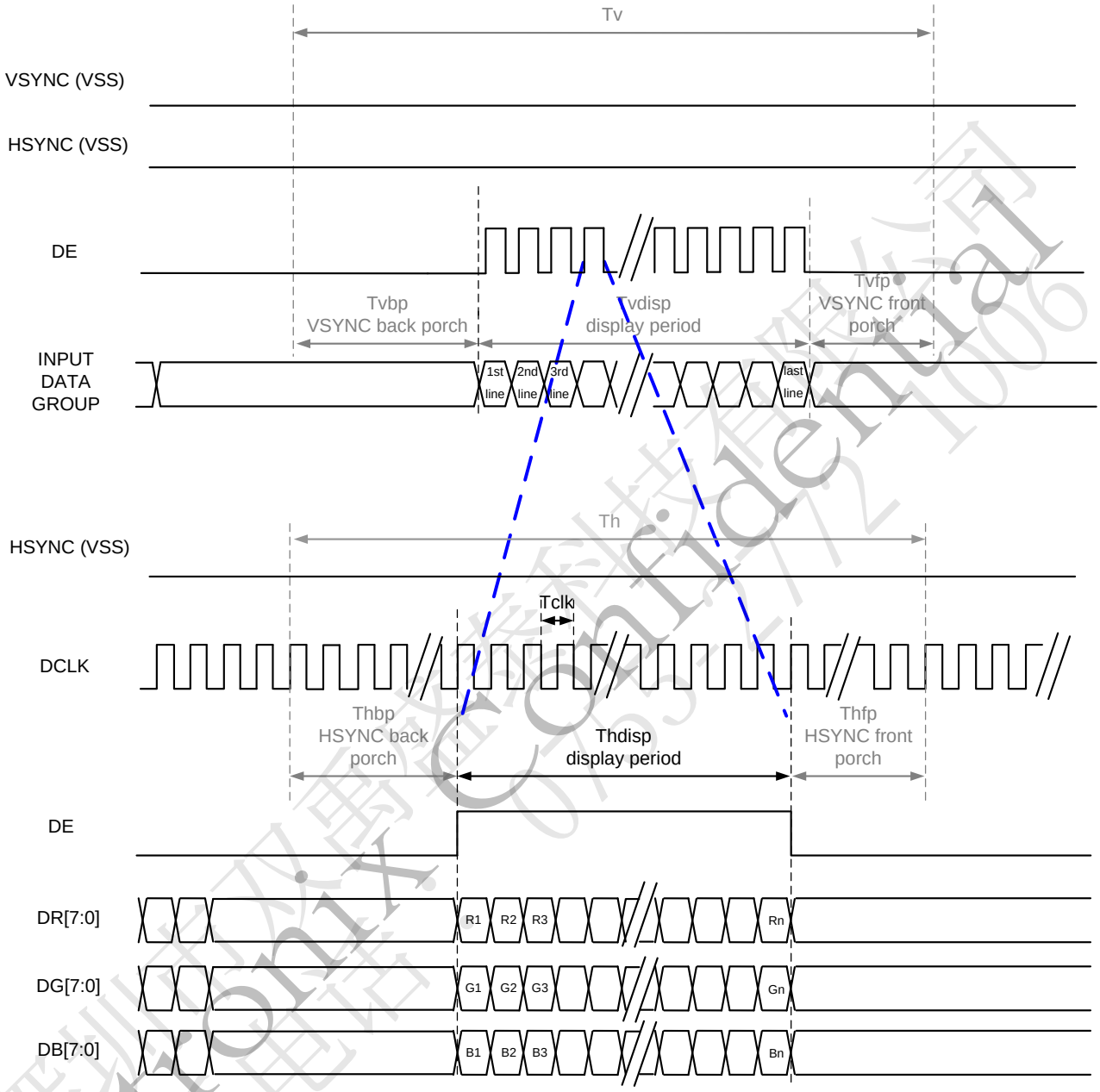
7.3.2 SYNC-DE Mode



7.3.3 DE Mode



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7.3.4 Parallel 24-bit RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C).

Parallel 24-bit RGB Interface Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	23	25	27	MHz	.
HSYNC	Period Time	Th	808	816	848	DCLK	
	Display Period	Thdisp		800		DCLK	
	Back Porch	Thbp	4	8	24	DCLK	
	Front Porch	Thfp	4	8	24	DCLK	
	Pulse Width	Thw	2	4	8	DCLK	
VSYNC	Period Time	Tv	496	512	528	HSYNC	
	Display Period	Tvdisp		480		HSYNC	
	Back Porch	Tvbp	8	16	24	HSYNC	
	Front Porch	Tvfp	8	16	24	HSYNC	
	Pulse Width	Tvw	2	4	8	HSYNC	

Note: 1. The minimum blanking time depends on the GIP timing of the panel specification.

2. To ensure the compatibility of different panels, it is recommended to use the typical setting.

3. It is necessary to keep Tvbp =16 and Thbp =8 in sync mode. DE mode is unnecessary to keep it.

4. The maximum DCLK Frequency is 27MHz. If the case needs faster DCLK, please contact Sitronix.

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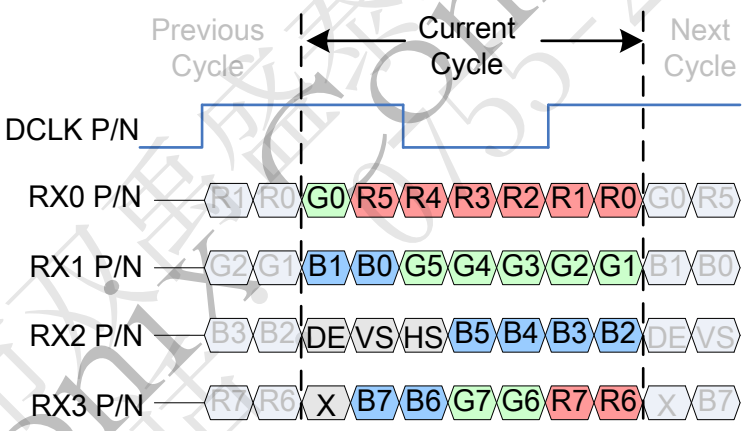
7.4 LVDS Interface

7.4.1 LVDS Input Pin Mapping Table

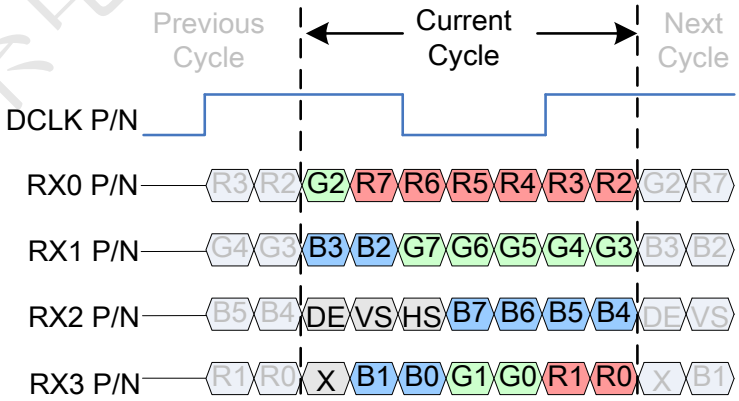
Pin Name RGB (LVDS)	LVDS 3 lane	LVDS 4 Lane
DCLKN	RXCLKN	RXCLKN
DCLKP	RXCLKP	RXCLKP
DB0	RX0P	RX0P
DB1	RX0N	RX0N
DB2	RX1P	RX1P
DB3	RX1N	RX1N
DB4	RX2P	RX2P
DB5	RX2N	RX2N
DB6	-	RX3P
DB7	-	RX3N

Note: Symbol "-" means reserve pin and should fix to "L" by DGND.

7.4.2 4 Lane VESA Data Format Color Bit Map



7.4.3 4 Lane JEIDA Data Format Color Bit Map



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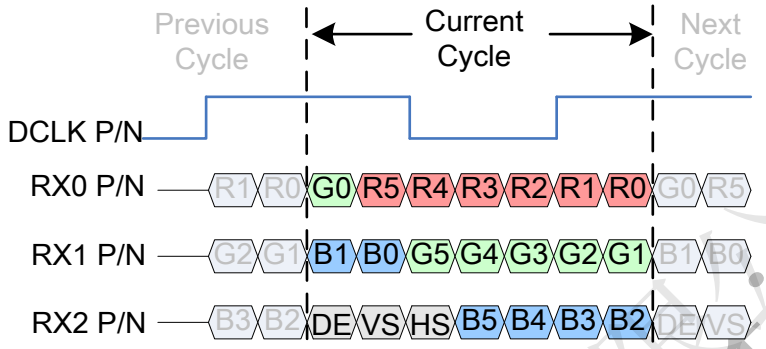
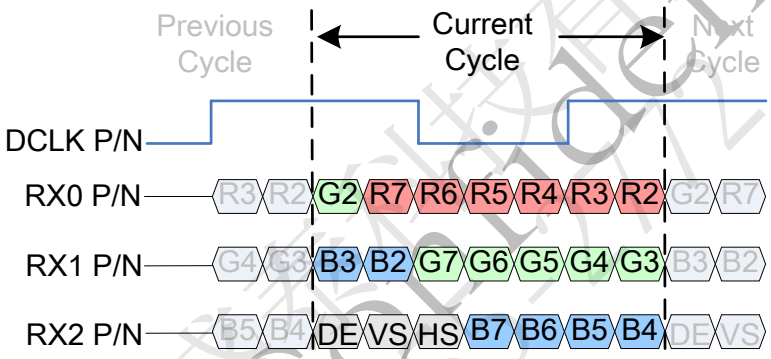
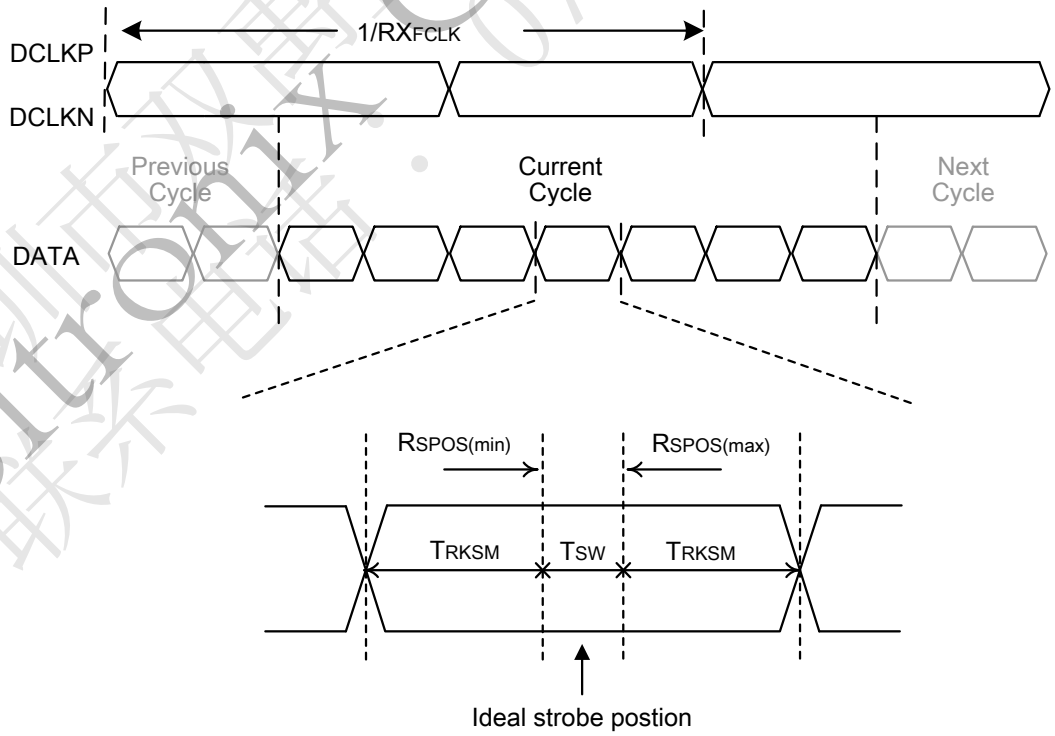
7.4.4 3 Lane VESA Mode Color Bit Map



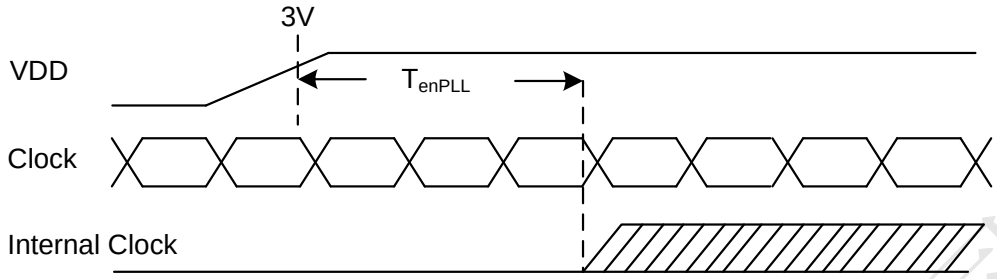
7.4.5 3 Lane JEIDA Mode Color Bit Map



7.4.6 LVDS Input Timing Table



RRKSM : Receiver strobe margin
RSPOS : Receiver strobe position
TSW : Strobe width (internal DATA sampling window)



LVDS Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	RX_{FCLK}	23	25	27	MHz	
Input Data Skew Margin	T_{RSKM}	400	-	-	ps	
Clock High Time	T_{LVCH}	4/(7 x RX_{FCLK})			ns	
Clock Low Time	T_{LVCL}	3/(7 x RX_{FCLK})			ns	
PLL Wake-up Time	T_{enPLL}	-	-	150	us	
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver						
Modulation Frequency	SSC_{MF}	-	-	100	KHz	
Modulation Rate	SSC_{MR}	-	-	+/-3	%	

Note. The maximum RXFCLK Frequency is 27MHz. If the case needs faster RXFCLK, please contact Sitronix.

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7.5 MIPI-DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High-Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low-Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

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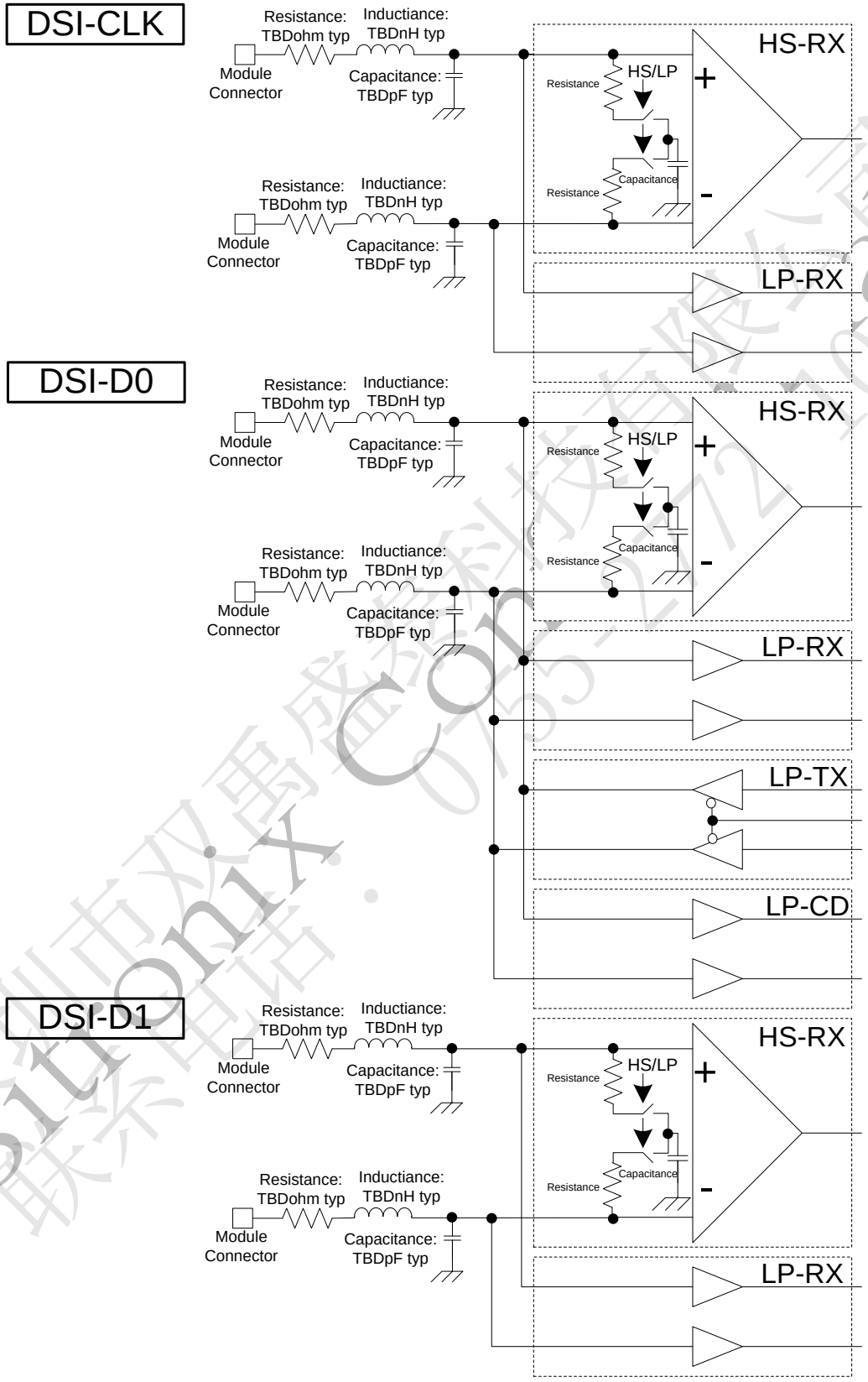
7.5.1 Display Module Pin Configuration for DSI



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7.5.2 Display Serial Interface (DSI)

The communication can be separated 2 different levels between the MCU and the display module:

- Interface level : Low level communication
- Packet level : High level communication

7.5.3 Interface level communication

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low-Power (LP) or High-Speed (HS) mode. Data lane1, data lane2 and data lane3 can be driven High-Speed mode only.

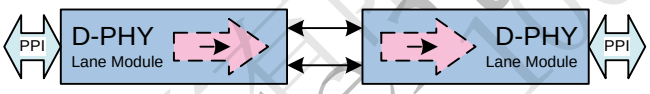
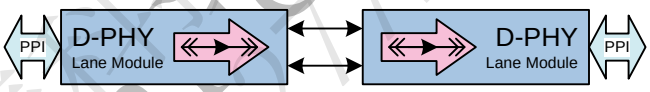
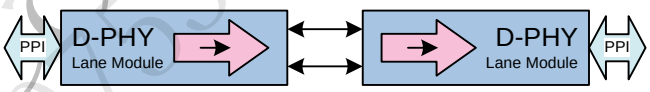
	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	
Data Lane1	Unidirectional lane Forward high-speed only Simplified Escape Mode(ULPS Only)	

Figure 1 The Interface Color Lane Types and Support Mode

Low-Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a Low-Power mode.

High-Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High-Speed (HS) and Low-Power (LP) lane pair are defined below.

Lane Pair State Code	Line Voltage Levels		High-Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Request	Mark-0
LP-10	LP High	LP Low	N/A	LP-Request	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

High-Speed and Low-Power Lane Pair State Descriptions

Notes:

1. During High-Speed transmission the Low-Power observe LP-00 on the Lines.

2. If LP-11 occurs during Escape mode the Lane returns to Stop state.

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7.5.4 DSI-CLOCK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low-Power Mode (LPM LP-11), Ultra-Low Power Mode (ULPM) or High-Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low-Power) when there is entering or leaving Low-Power Mode (LPM) or Ultra-Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low-Power) when there is entering in or leaving out High-Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

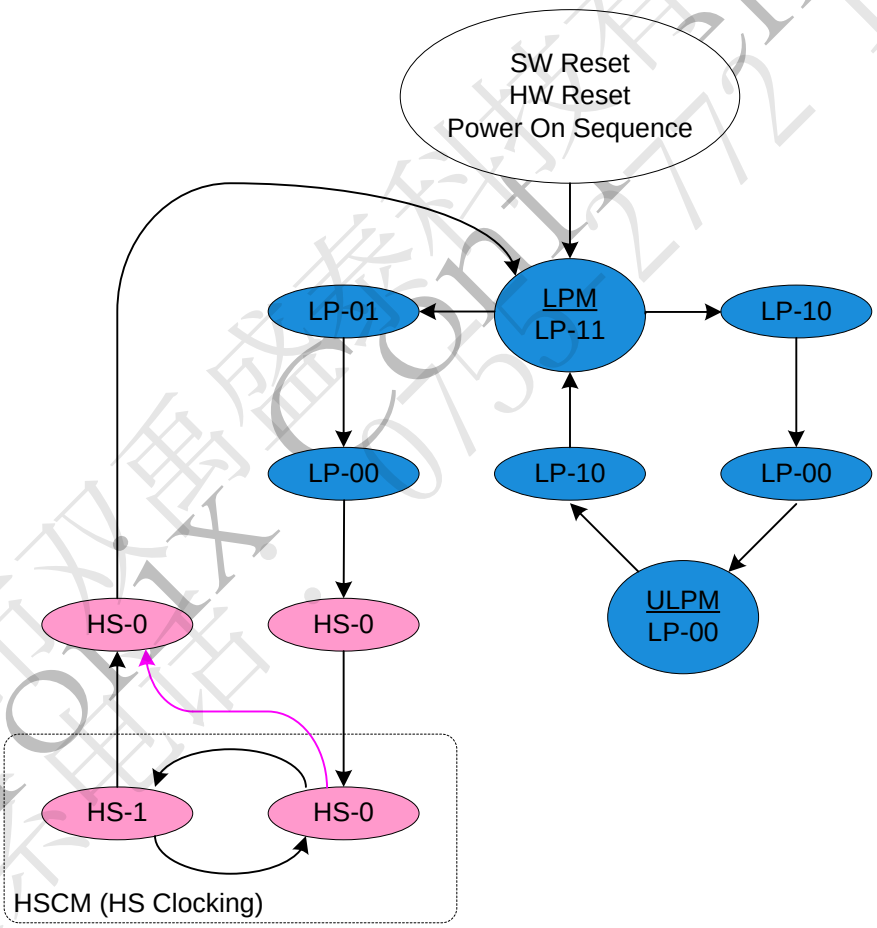

Figure 2 Clock Lanes Power Modes

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7.5.4.1 Low-Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low-Power Mode (LPM),when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP10=>LP-11(LPM).

This sequence is illustrated below.

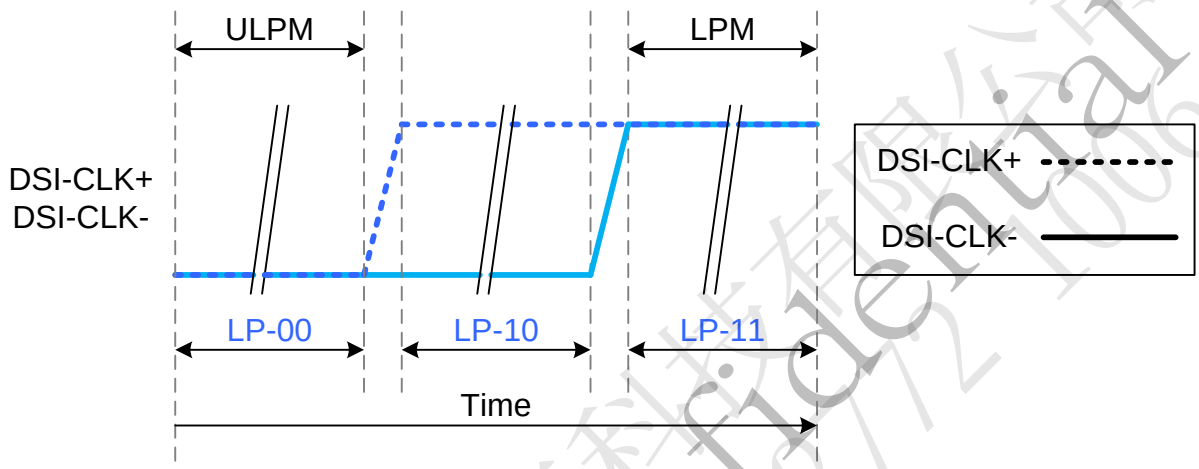

Figure 3 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High-Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

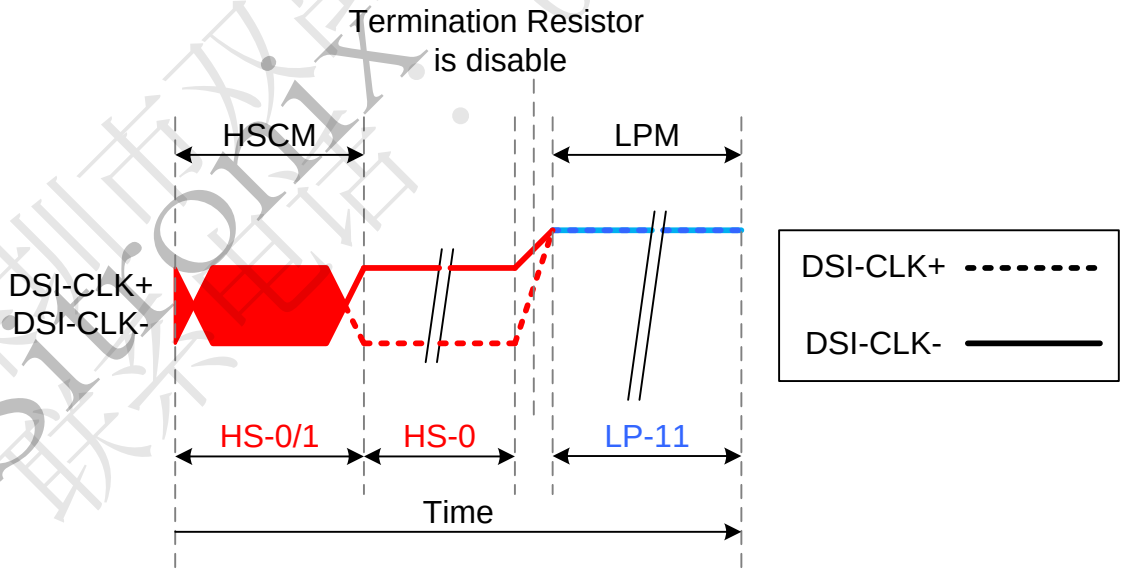

Figure 4 From HSCM to LPM

All three mode changes are illustrated a flow chart below.

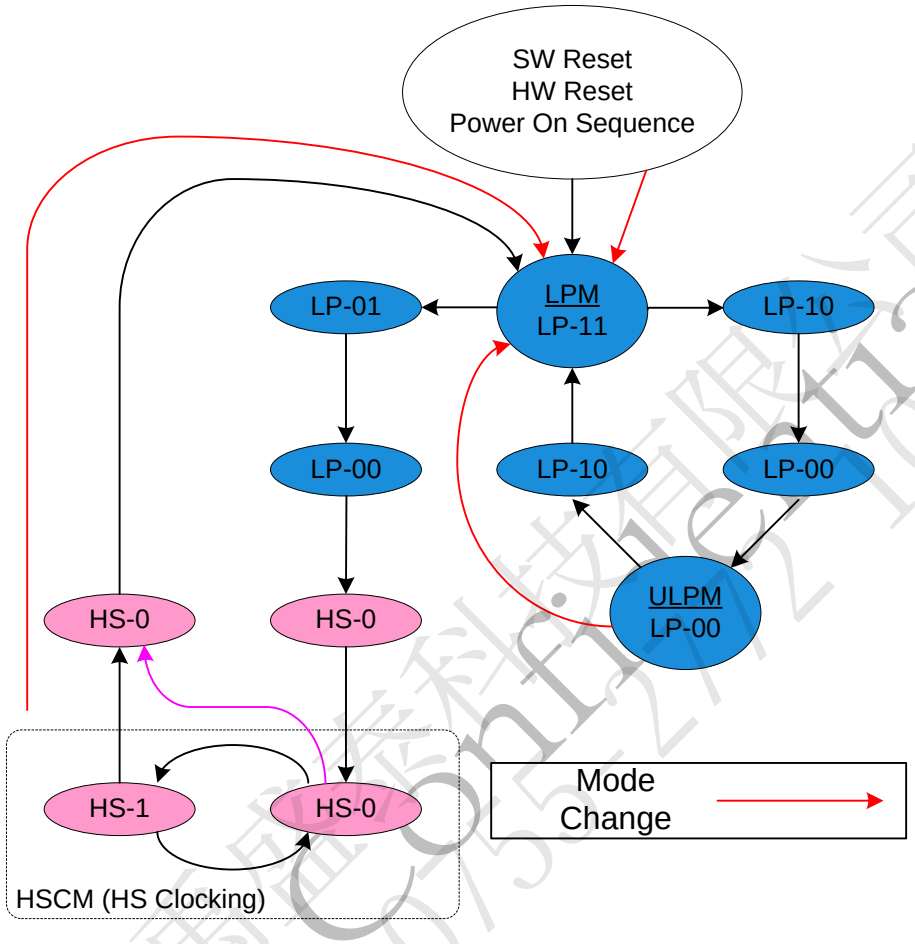

Figure 5 All three mode changes to LPM

7.5.4.2 Ultra-Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra-Low Power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility if from the Low-Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below:

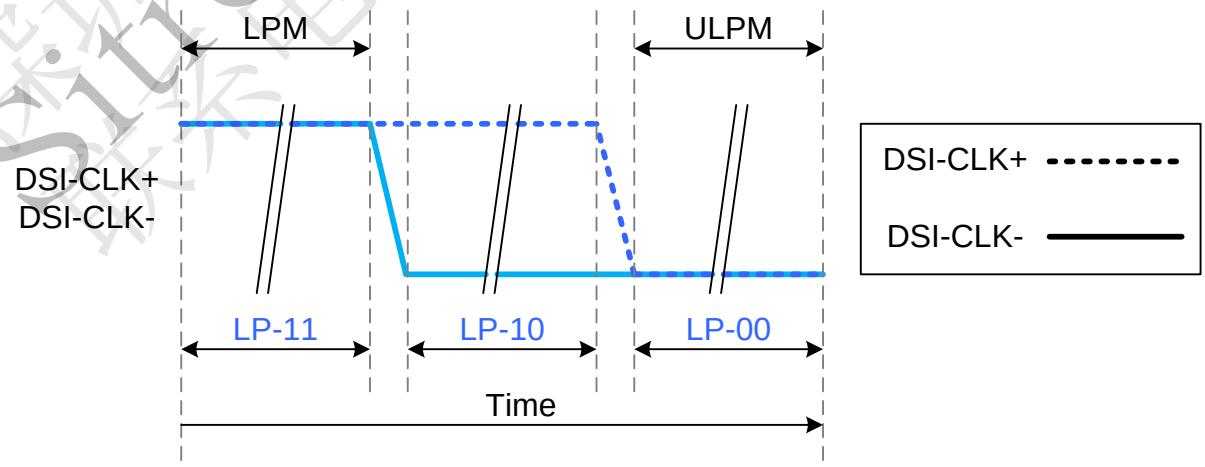

Figure 6 From LPM to UPLM

The mode change is also illustrated below:

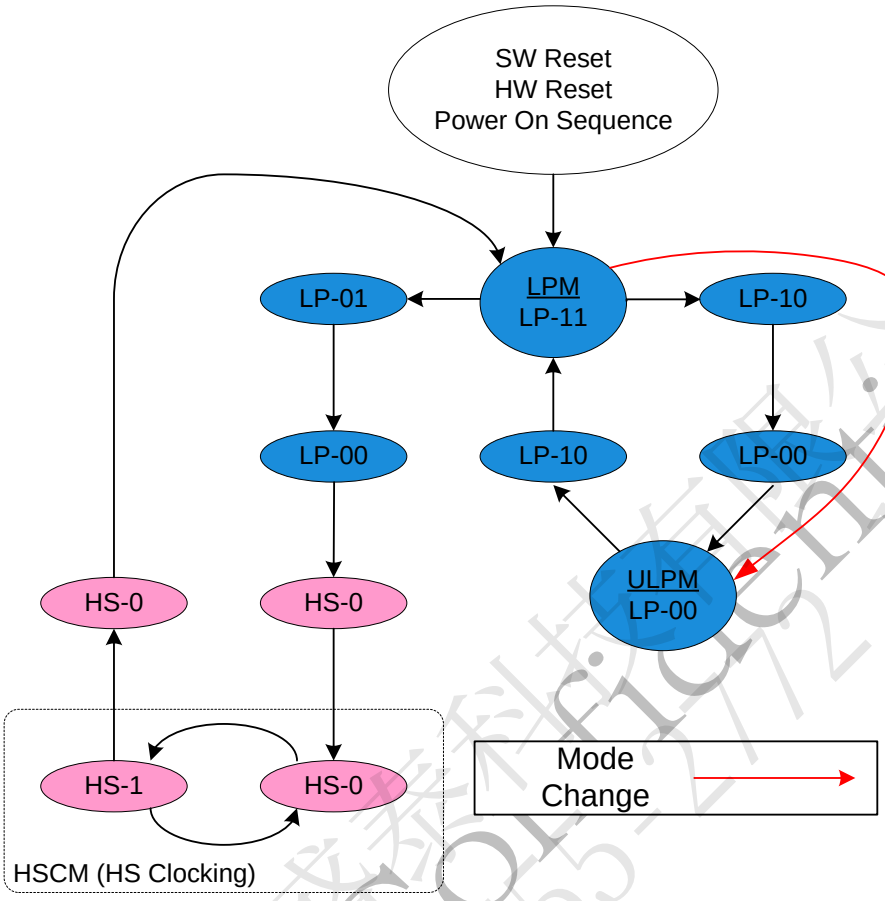

Figure 7 The mode change from LPM to UPLM

7.5.4.3 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High-Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low-Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

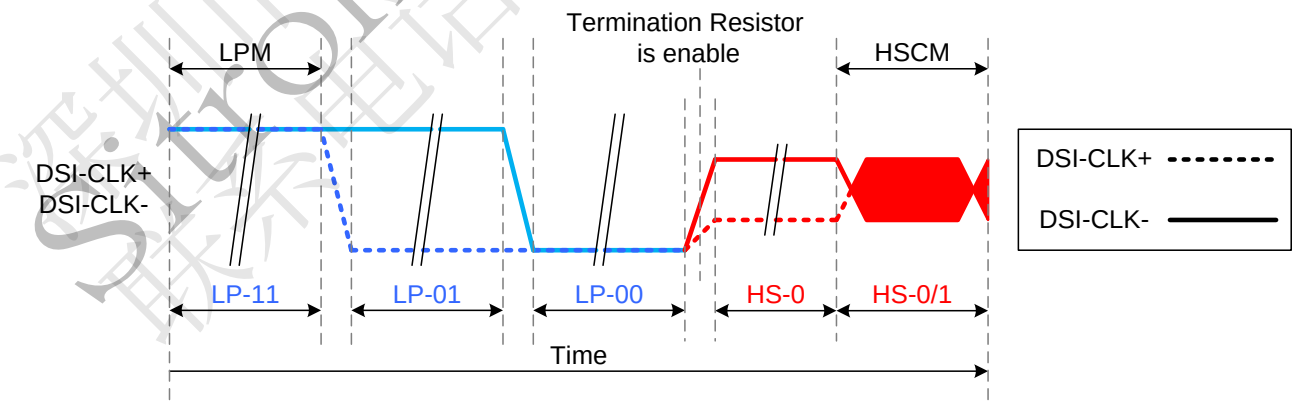

Figure 8 From LPM to HSCM

The mode change is also illustrated below:

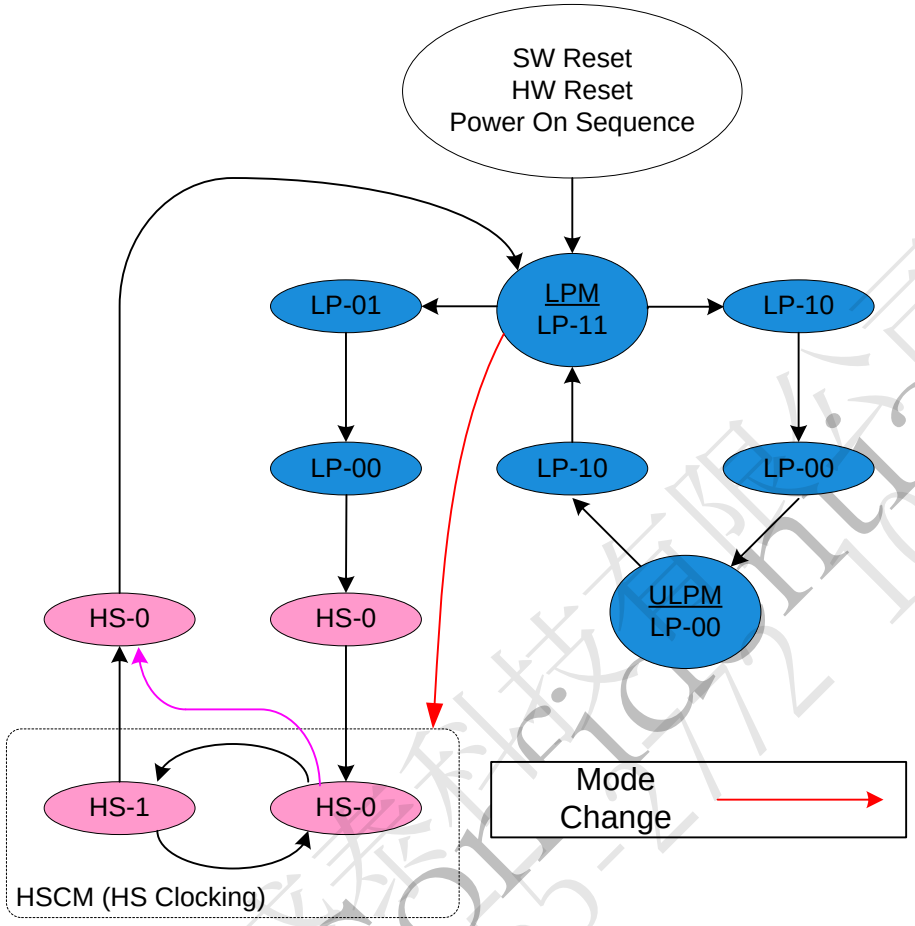

Figure 9 Mode Change from LPM to HSCM on the Flow Chart

The High-Speed clock (DSI-CLK+/-) is started before High-Speed data is sent via DSI-Dn+/- lanes. The High-Speed clock continues clocking after the High-Speed data sending has been stopped.

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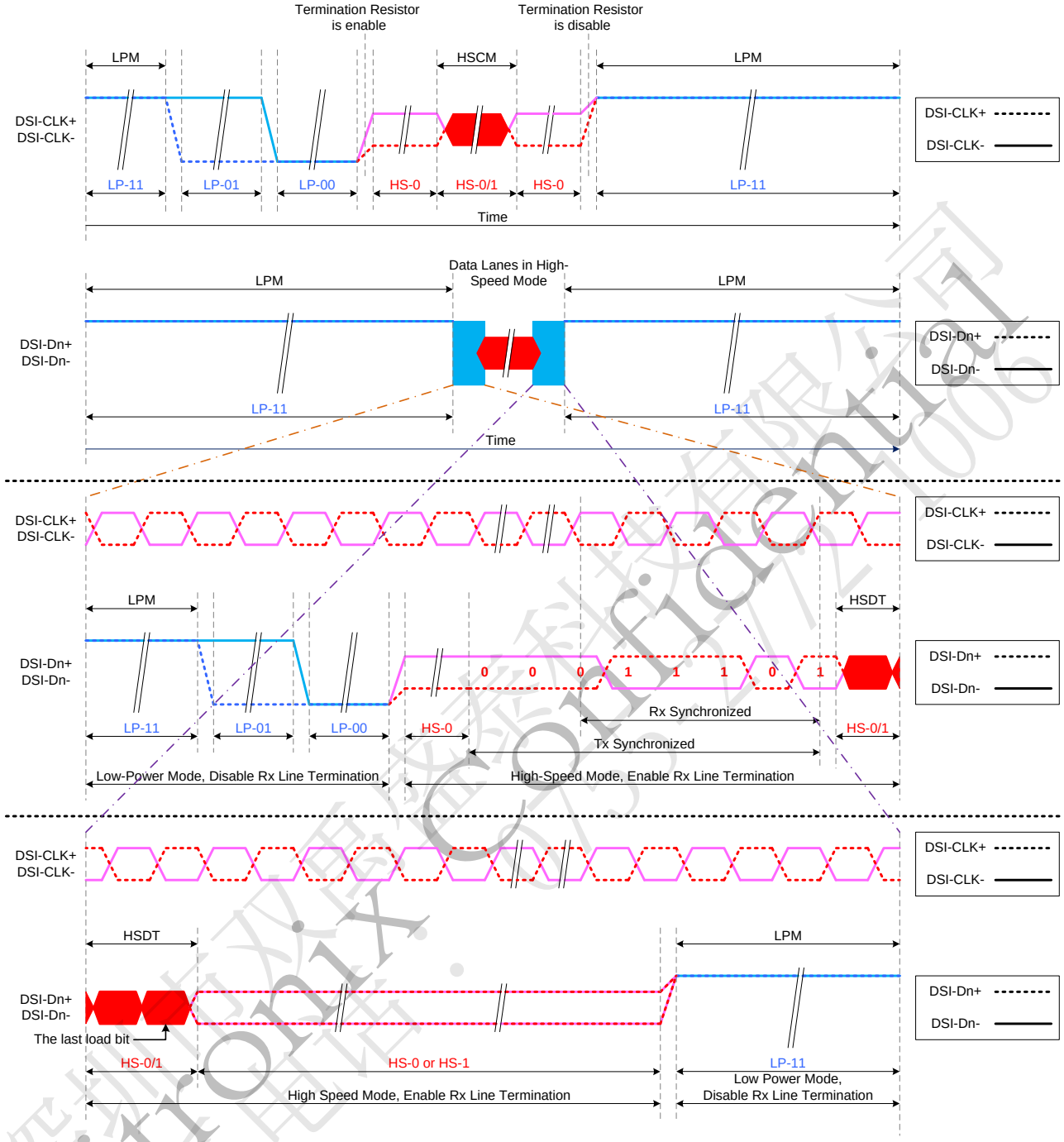

Figure 10 High-Speed Clock Burst

Note:

If the last load bits is HS-0, the transmitter changes form HS-0 to HS-1.

If the last load bits is HS-1, the transmitter changes form HS-1 to HS-0.

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7.5.5 DSI-DATA Lanes

DSI-D0+/- data lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lane is used)

• High-Speed Data Transmission (DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lane is used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Entering and leaving sequence

7.5.5.1 ESCAPE MODE

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low-Power (LP) mode.

These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:

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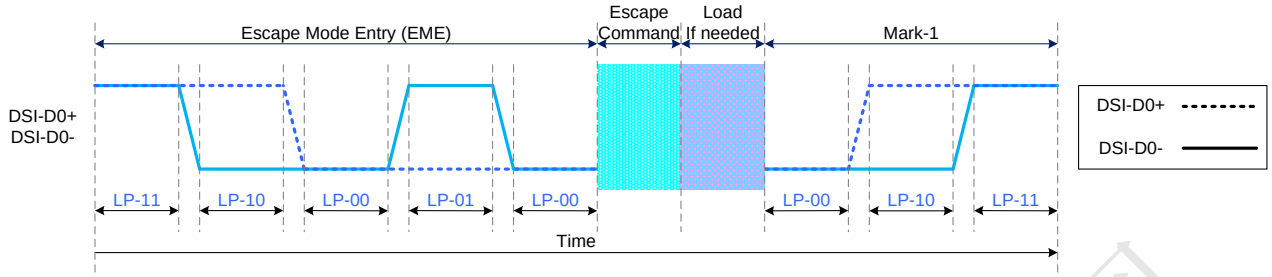

Figure 11 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the Low-Power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➔Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	○
Ultra-Low Power Mode	Mode	0001 1110 bin	○	○
Underfined-1, Note 1	Mode	1001 1111 bin	-	-
Underfined-2, Note 1	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	○
Tearing Effect	Trigger	0101 1101 bin	-	-
Acknowledge	Trigger	0010 0001 bin	-	○
Unknow-5, Note 1	Trigger	1010 0000 bin	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low-Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):

  One or more bytes (8 bits)

  Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

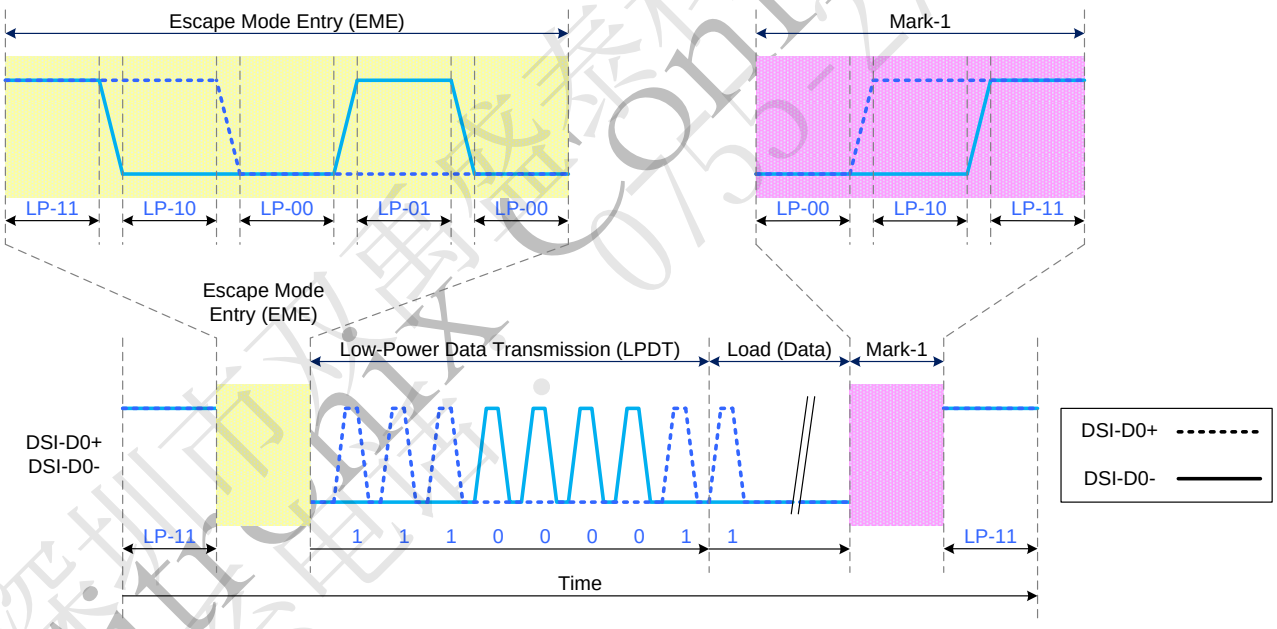

Figure 12 Low-Power Data Transmission (LPDT)

Note:

Load(Data) is presenting that the first bit is logical '1' in this example

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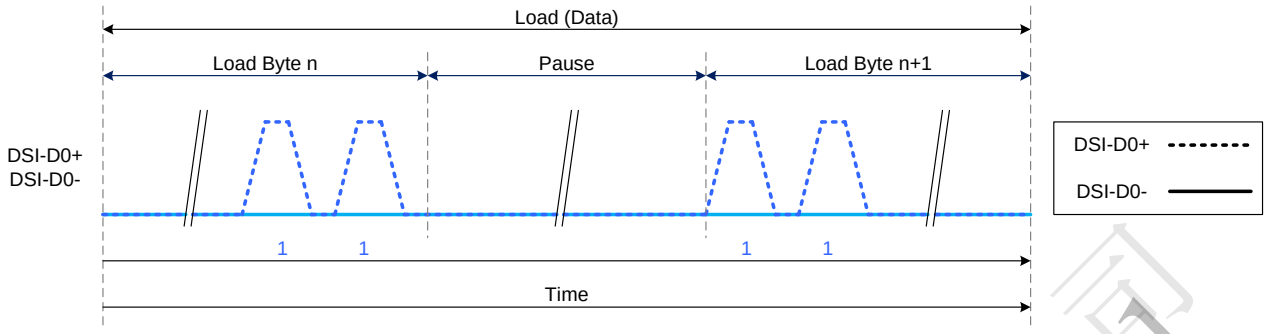

Figure 13 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

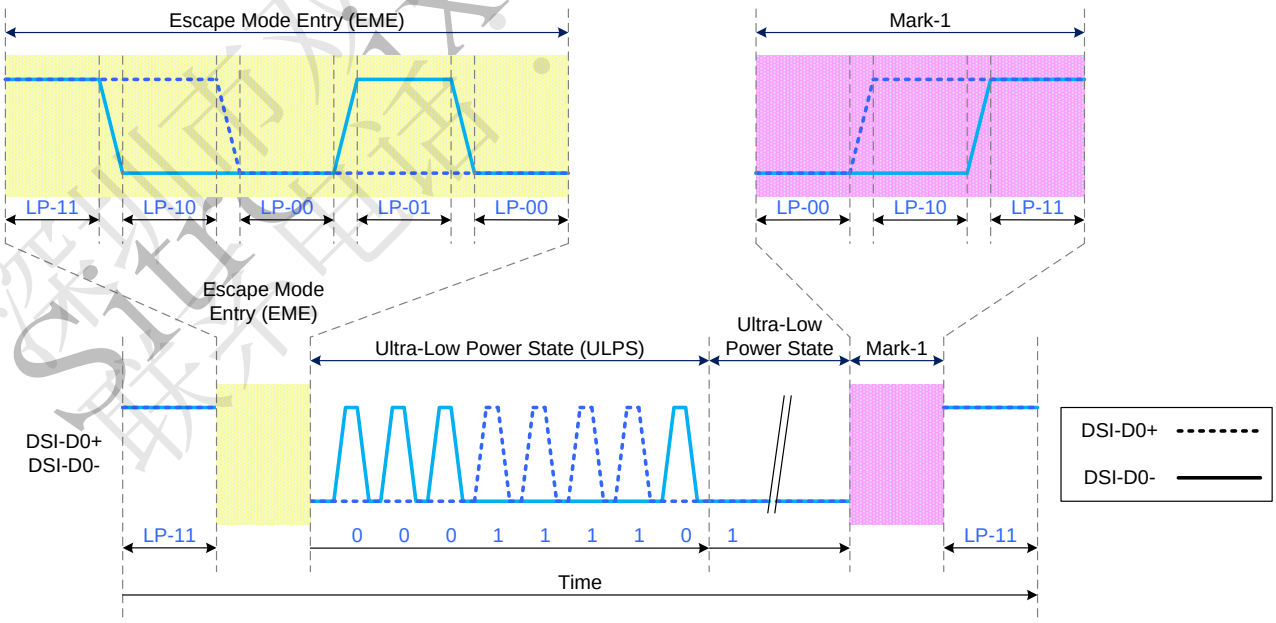

Figure 14 Ultra-Low Power State (ULPS)

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Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

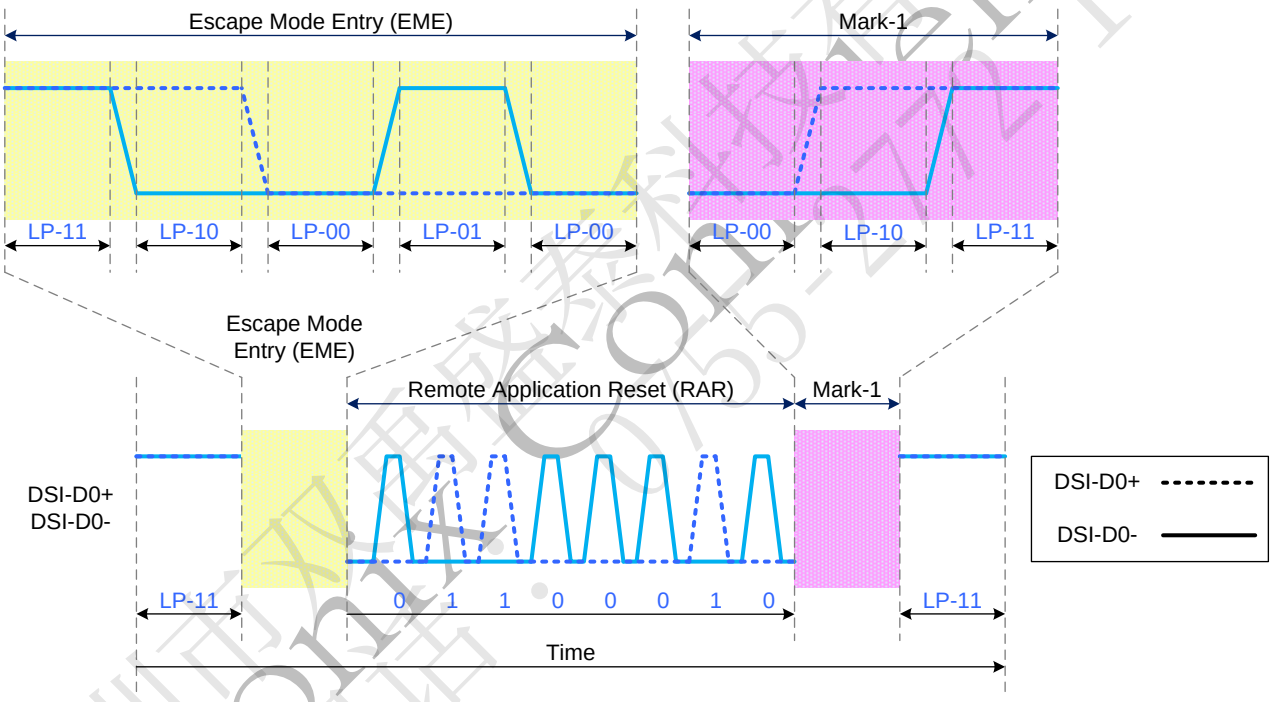

Figure 15 Remote Application Reset (RAR)

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Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

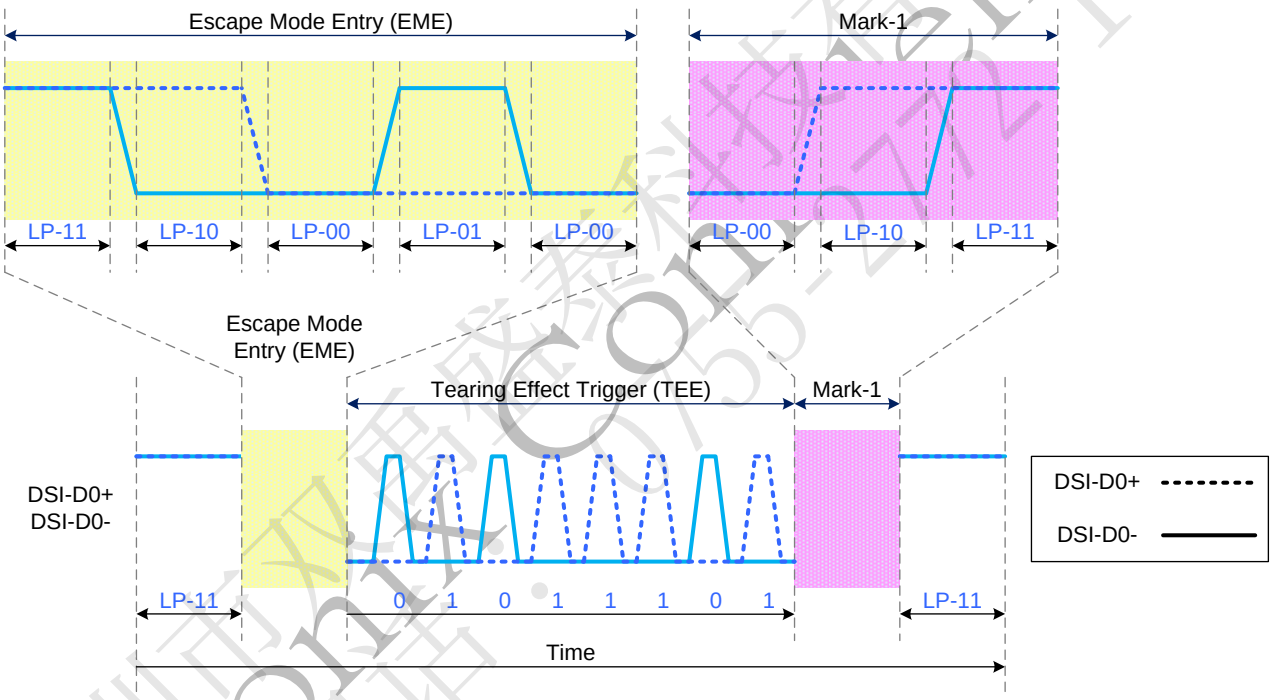

Figure 16 Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

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Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

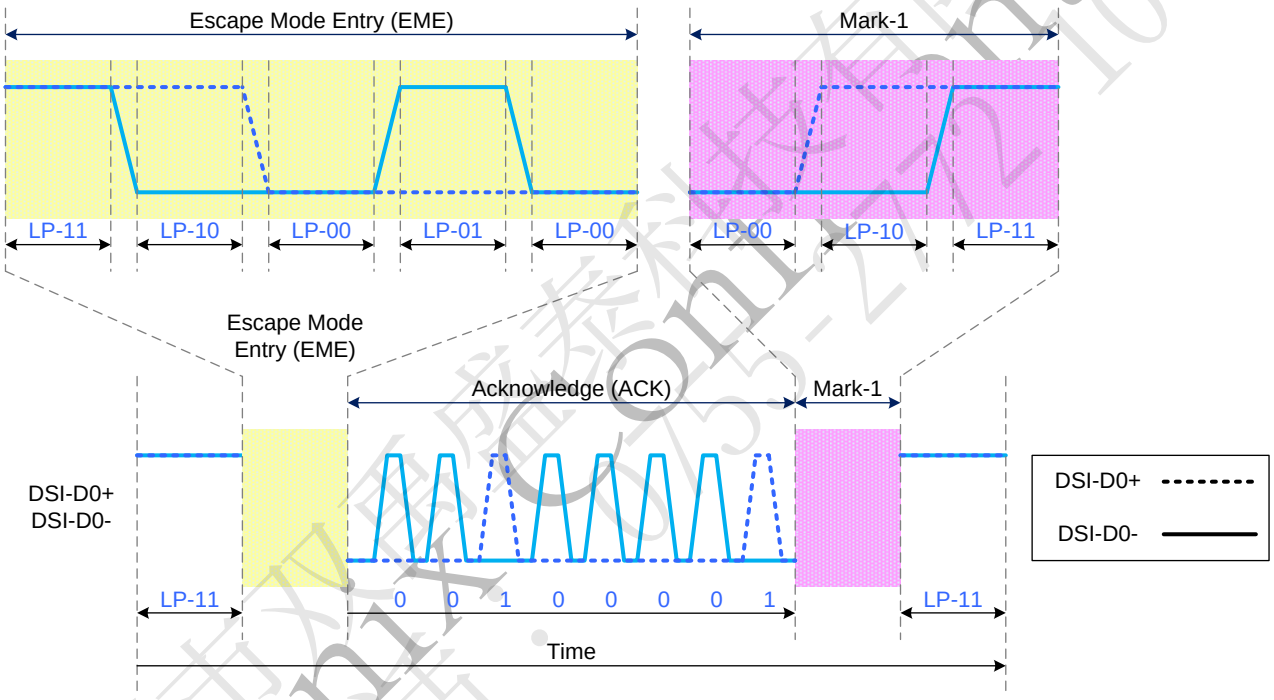

Figure 17 Acknowledge (ACK)

7.5.5.2 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

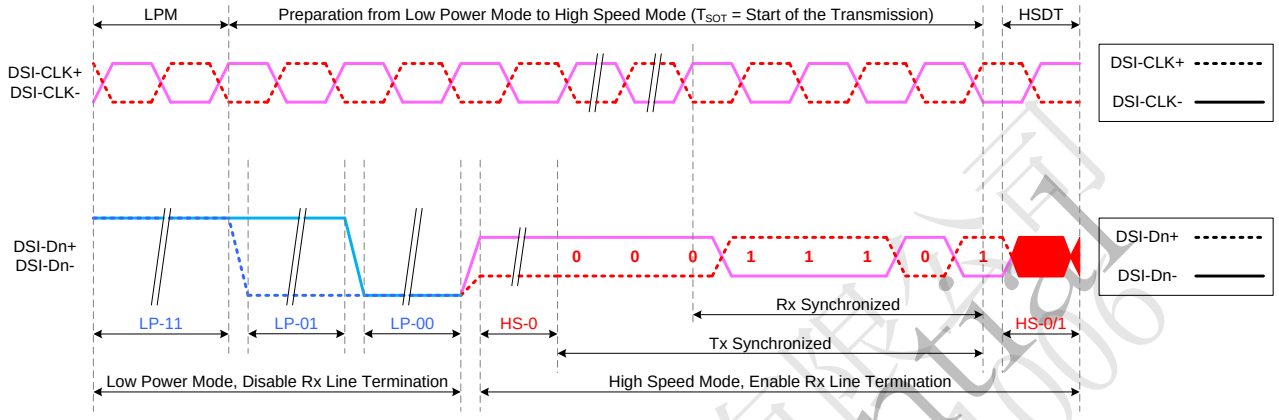

Figure 18 Entering High-Speed Data transmission (T_{SOT} of HSDT)

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Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

• Stops High-Speed Data Transmission

MCU changes to HS-1, if the last load bit is HS-0

MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

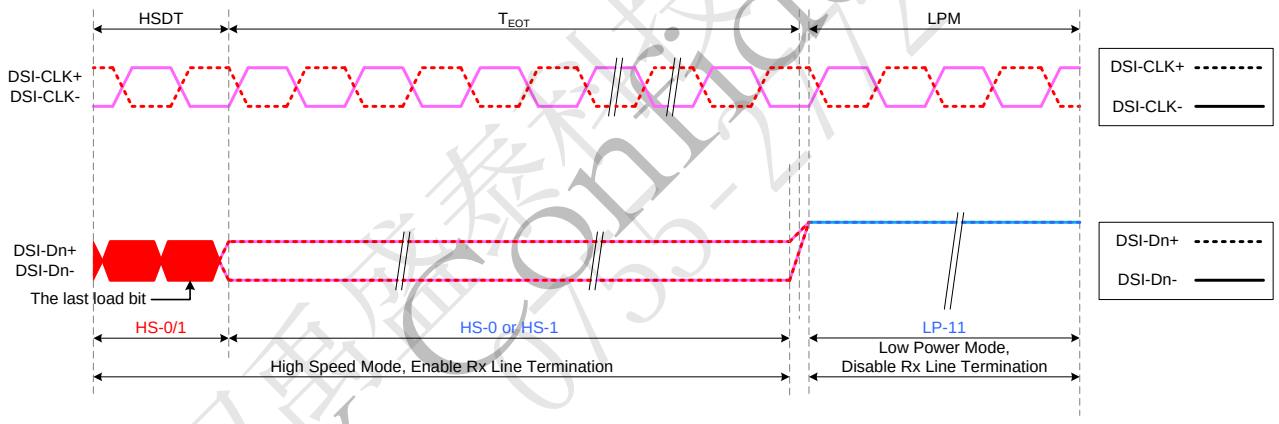

Figure 19 Leaving High-Speed data Transmission (T_{EOT} of HSDT)

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Burst of the High-Speed Data Transmission (HSDT)

The burst of the High-Speed Data Transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

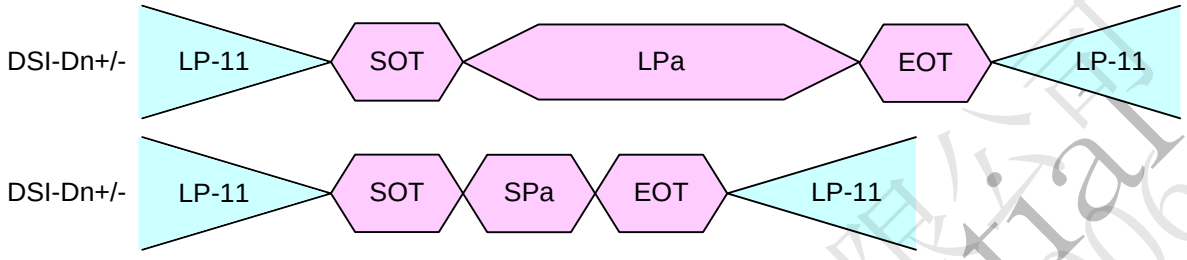

Figure 20 Single Packet in High-Speed Data Transmission with EoT packet disabled

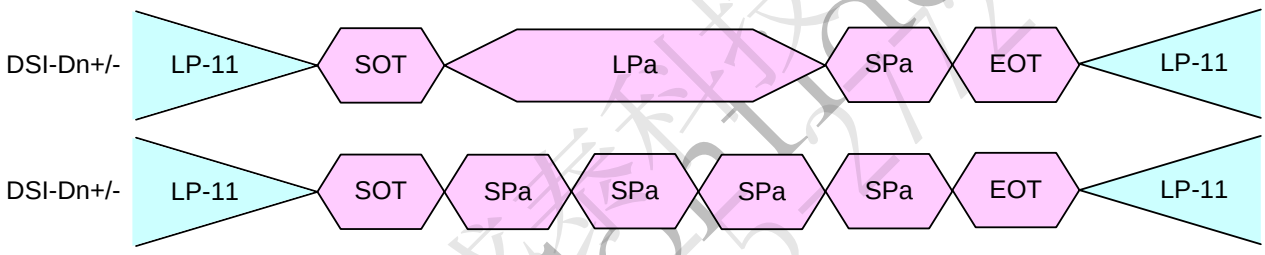

Figure 21 Multiple Packets in High-Speed Data Transmission with EoT packet disabled

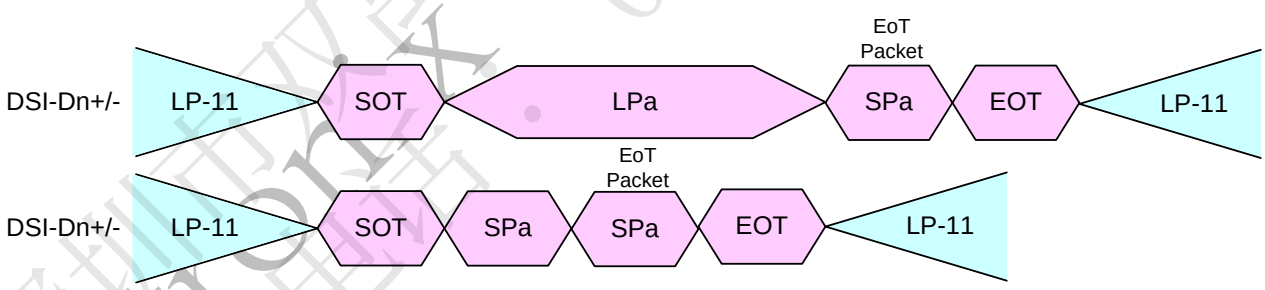

Figure 22 Single Packet in High-Speed Data Transmission with EoT packet enable

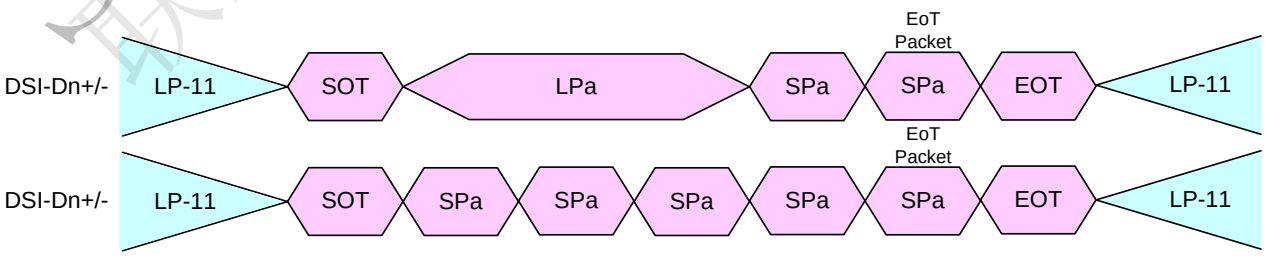

Figure 23 Multiple Packets in High-Speed Data Transmission with EoT packet enable

Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low-Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

7.5.5.3 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module is using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.

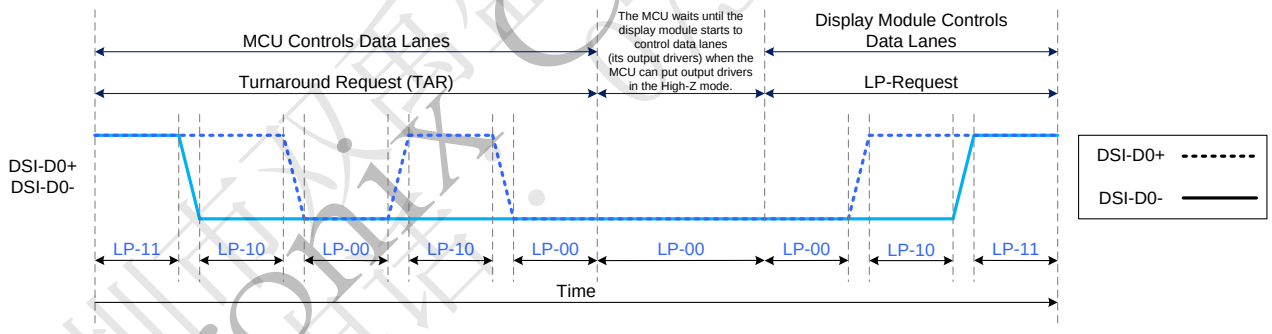

Figure 24 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

7.5.6 Packer Level Communication

7.5.6.1 Short Packet (SPa) and Long Packet (LPa) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low-Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

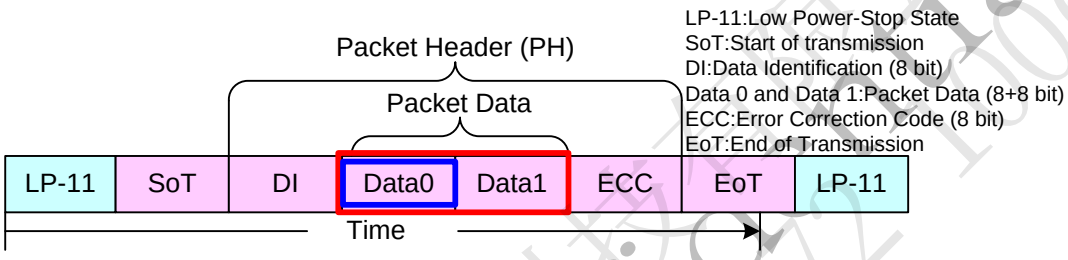

Figure 25 Short Packet (SPa) Structure

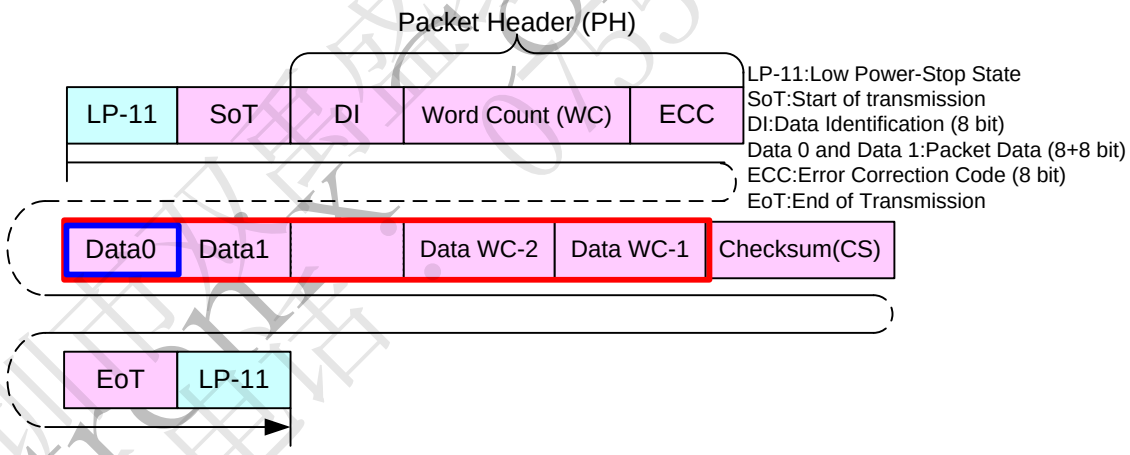

Figure 26 Long Packet (LPa) Structure

Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

7.5.6.2 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

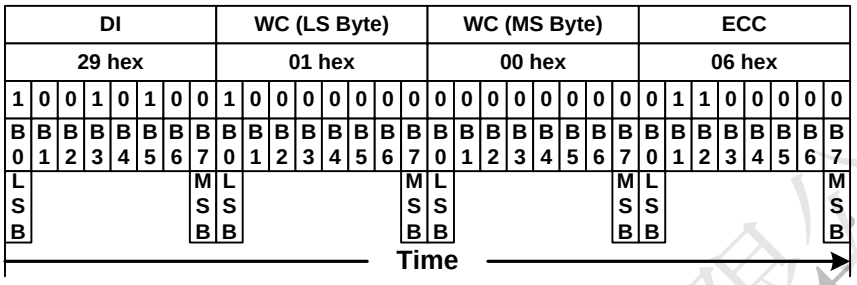

Figure 27 Bit Order of Byte on Packets

7.5.6.3 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

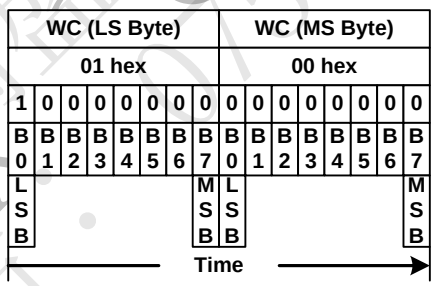

Figure 28 Byte Order of the Multiple Byte on Packets

7.5.6.4 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short

Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and Data 1

• 4th byte: Error Correction Code (ECC)

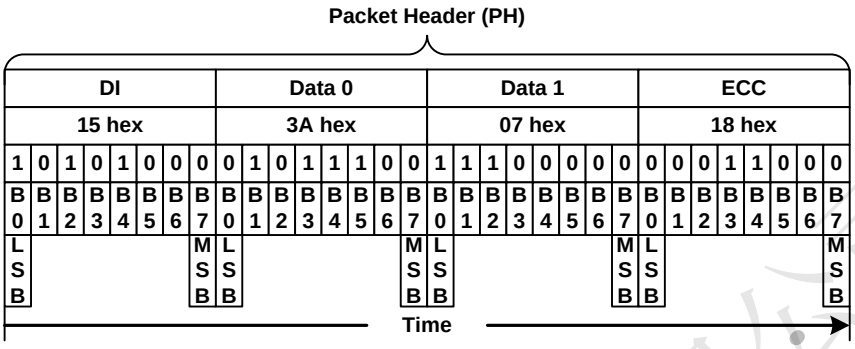

Figure 29 Packet Header (PH) on the Short Packet(SPa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

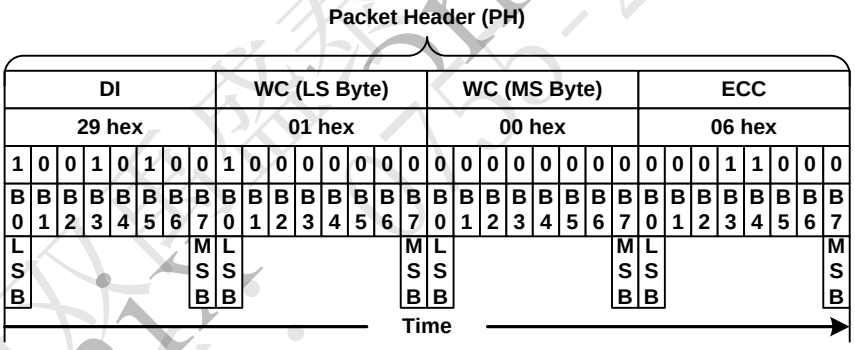

Figure 30 Packet Header (PH) on the Long Packet (LPa)

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- **Data Identification (DI)**

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 31 Data Identification (DI) Structure

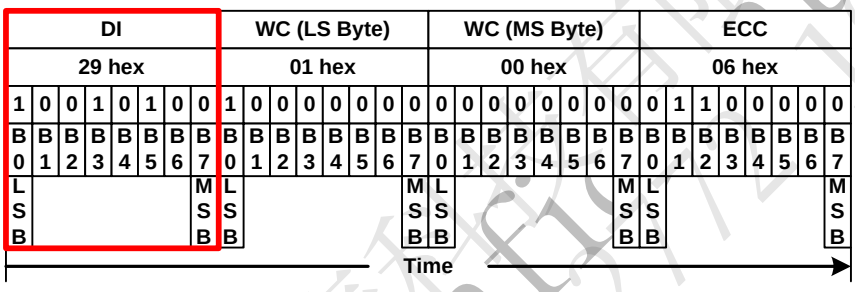

Figure 32 Data Identification (DI) on the Packet Header (PH)

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- **Virtual Channel (VC)**

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

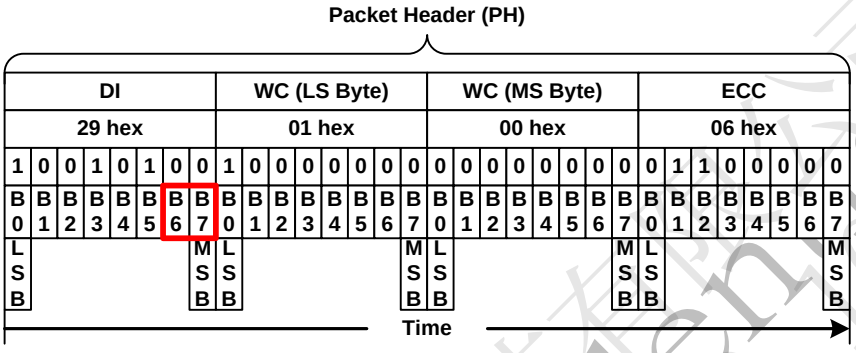

Figure 33 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

• The MCU is using the virtual channel 0 when it sends packets to this display module

• This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

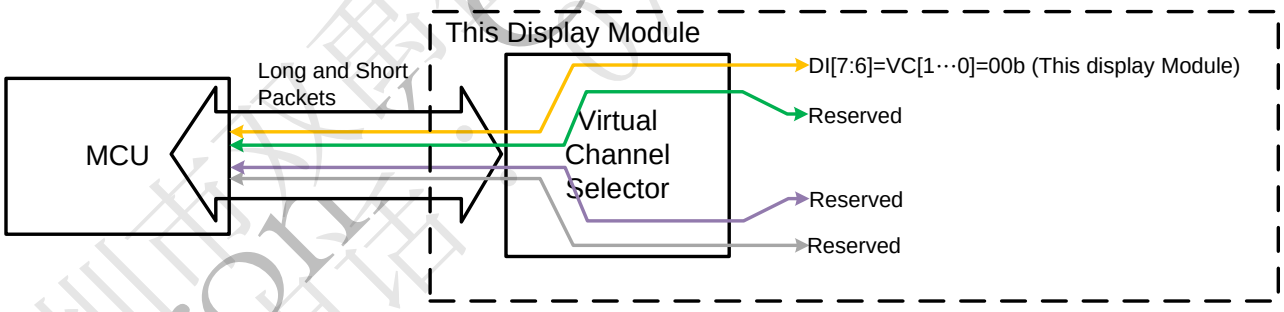

Figure 34 Virtual Channel (VC) Configuration

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- **Data Type (DT)**

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

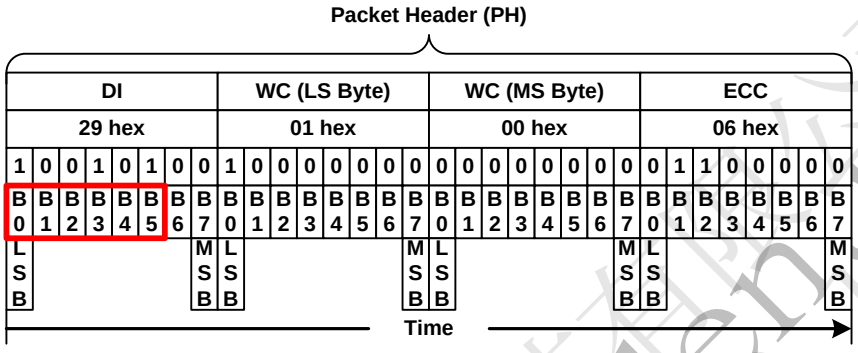

Figure 35 Data Type (DT) on the Packet Header (PH)

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This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to ‘0’ if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS’s parameter)

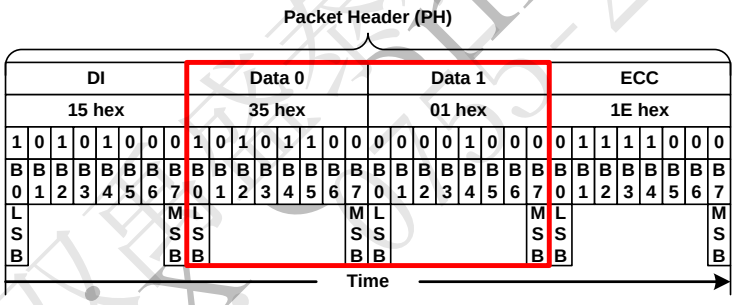
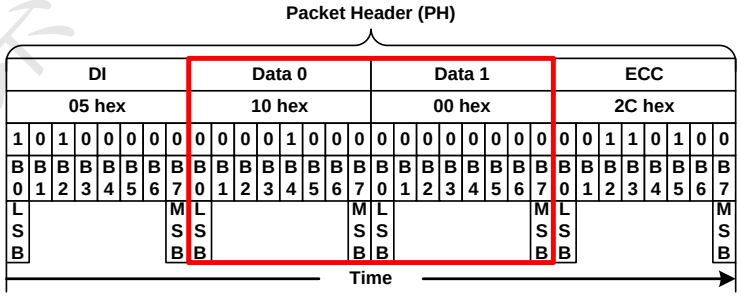


Figure 36 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)



• Data 1: 00hex (Null)

Figure 37 Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

- **Word Count (WC) on the Long Packet (LPa)**

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has Indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

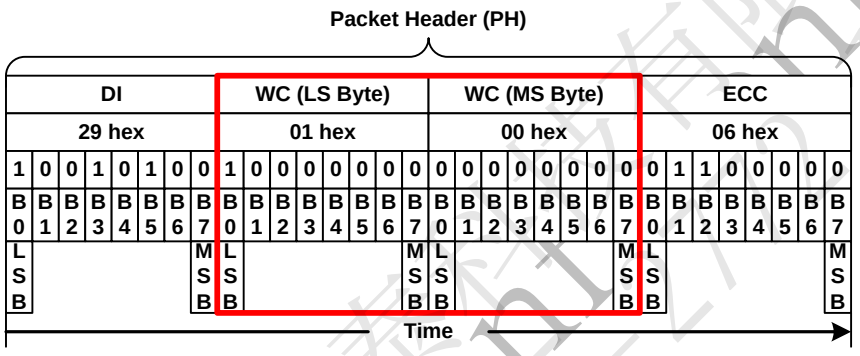


Figure 38 Word Count (WC) on the Long Packet (LPa)

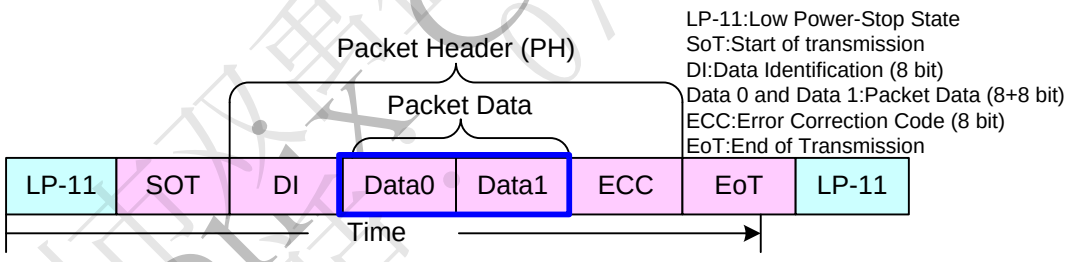


Figure 39 Packet Data (PD) on the Short Packet (SPa)

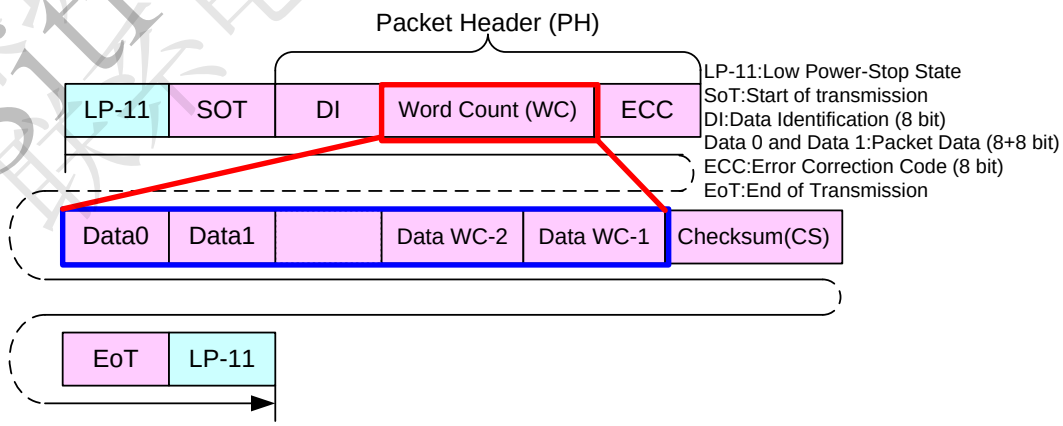


Figure 40 Packet Data (PD) on the Long Packet (LPa)

- **Error Correction Code (ECC)**

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field”

• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

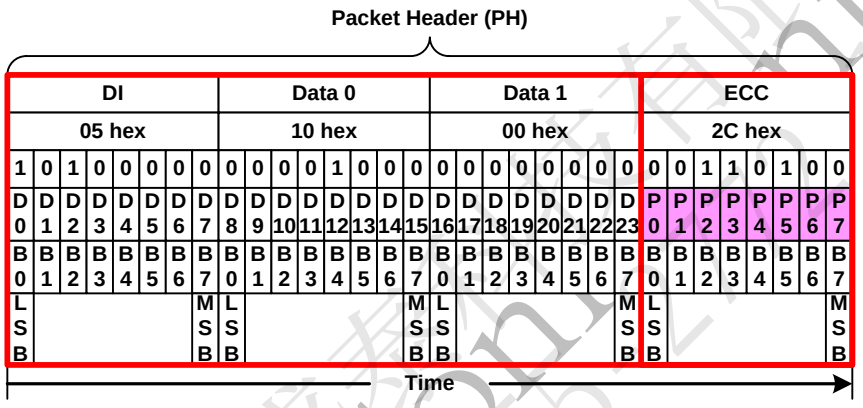


Figure 41 D[23..0] and P[7…0] on the Short Packet (SPa)

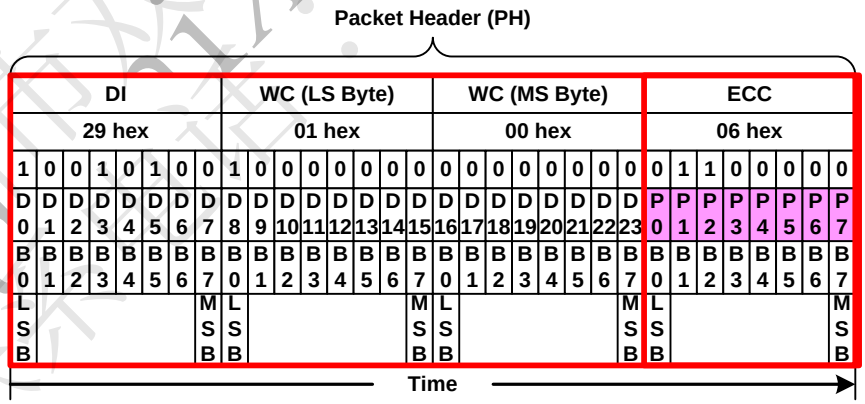


Figure 42 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

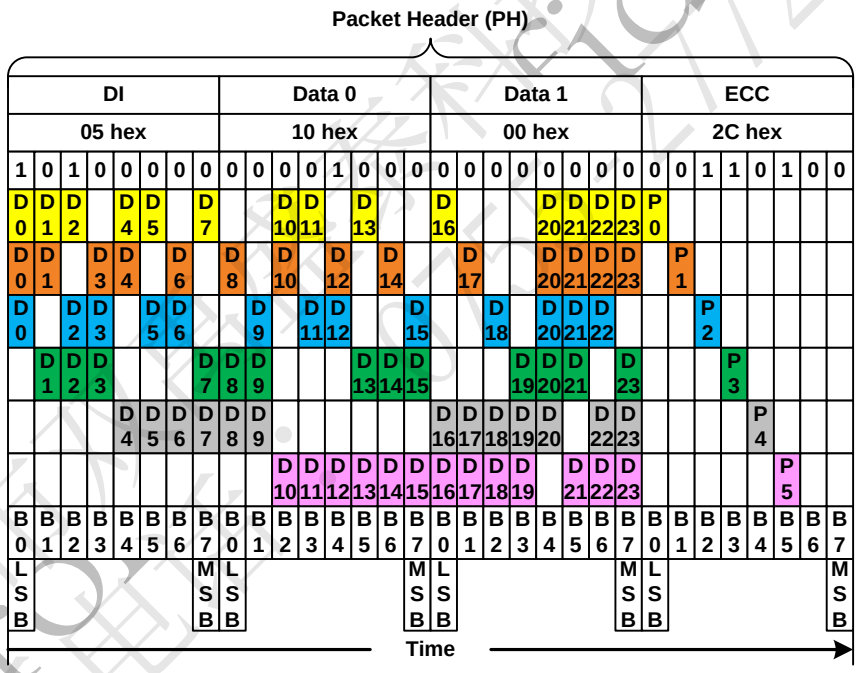


Figure 43 XOR Functionality on the Short Packet (SPa)

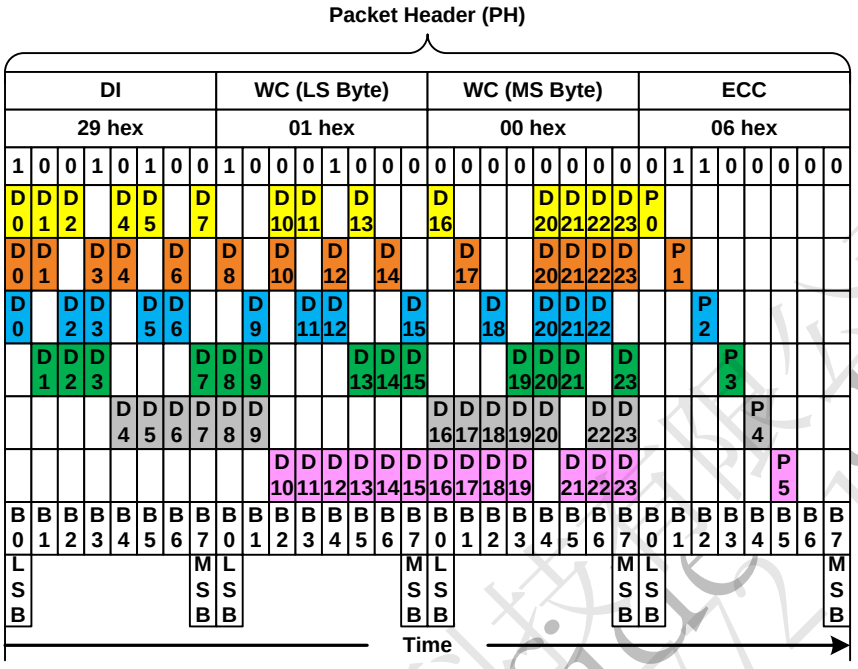


Figure 44 XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

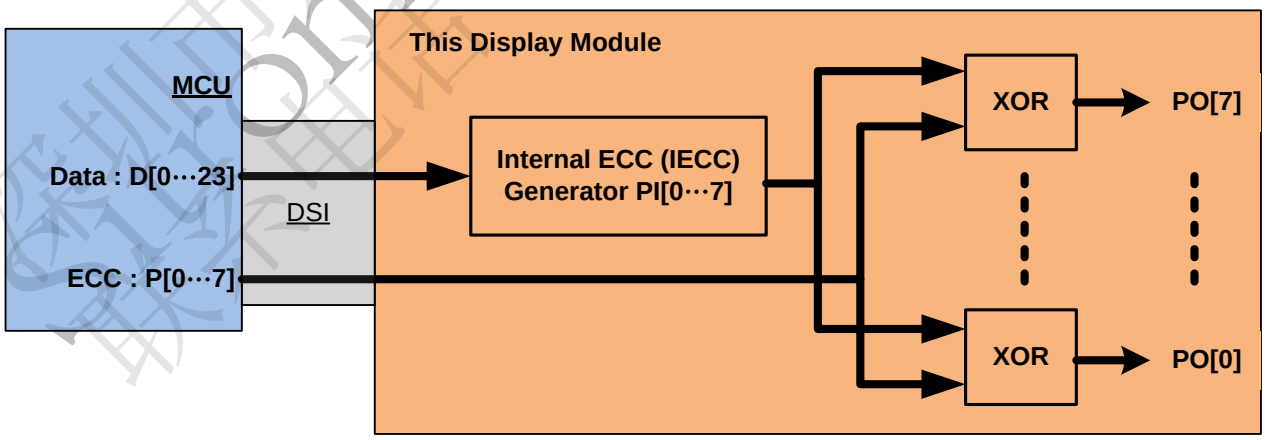


Figure 45 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 0 0h.

The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h

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D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

7.5.6.5 Packet Date (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

7.5.6.6 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

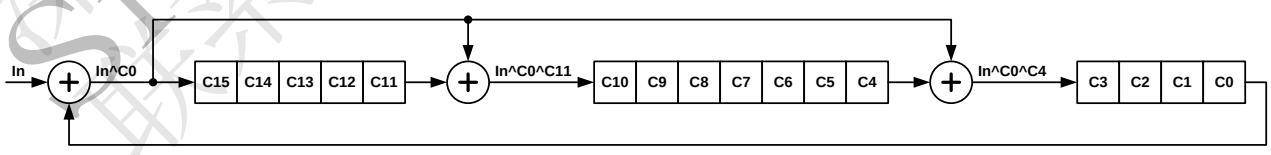

Figure 46 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

Step	In	In^C0	C15	C14	C13	C12	C11	In^C0^C11	C10	C9	C8	C7	C6	C5	C4	In^C0^C4	C3	C2	C1	C0
0	1(LSB)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1
5	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
6	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
7	0(MSB)	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
8	X	X	0	0	0	1	1	X	1	1	0	0	0	0	0	X	1	1	1	0
CRC Result:			0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0
			MSB																	LSB

Figure 47 CRC Calculation – Packet Data (PD) is 01h

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A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is Illustrated below.

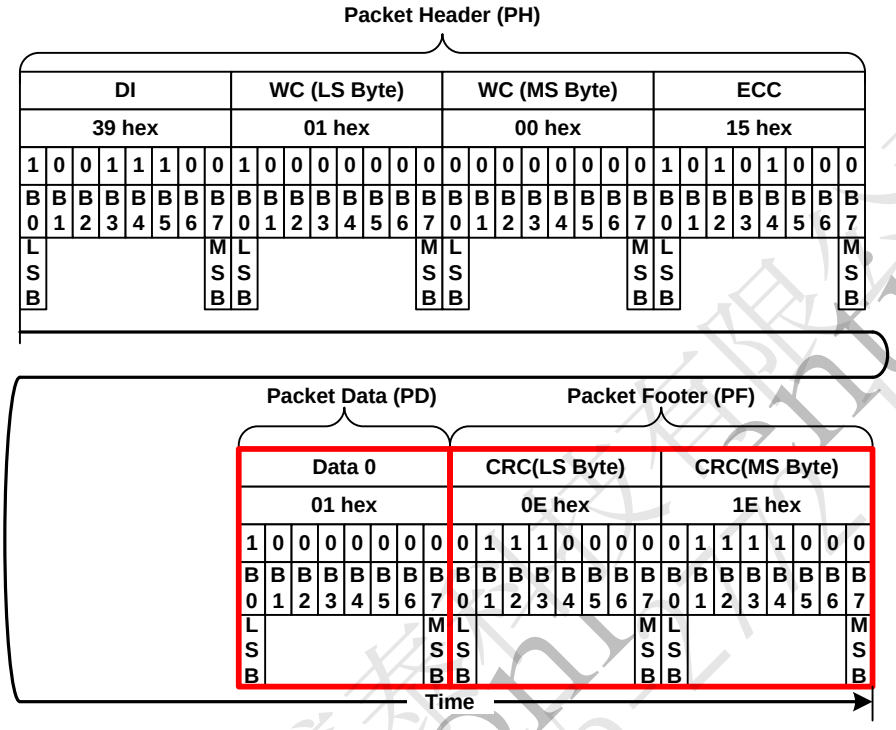

Figure 48 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

7.5.7 Packet Transmissions

7.5.7.1 Packet from the MCU to the Display Module

- **Display Command Set (DCS)**

Display Command Set (DCS), which is defined on chapter “Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in Short Packet (SPa) and Long Packet (LPa) as these are illustrated below.

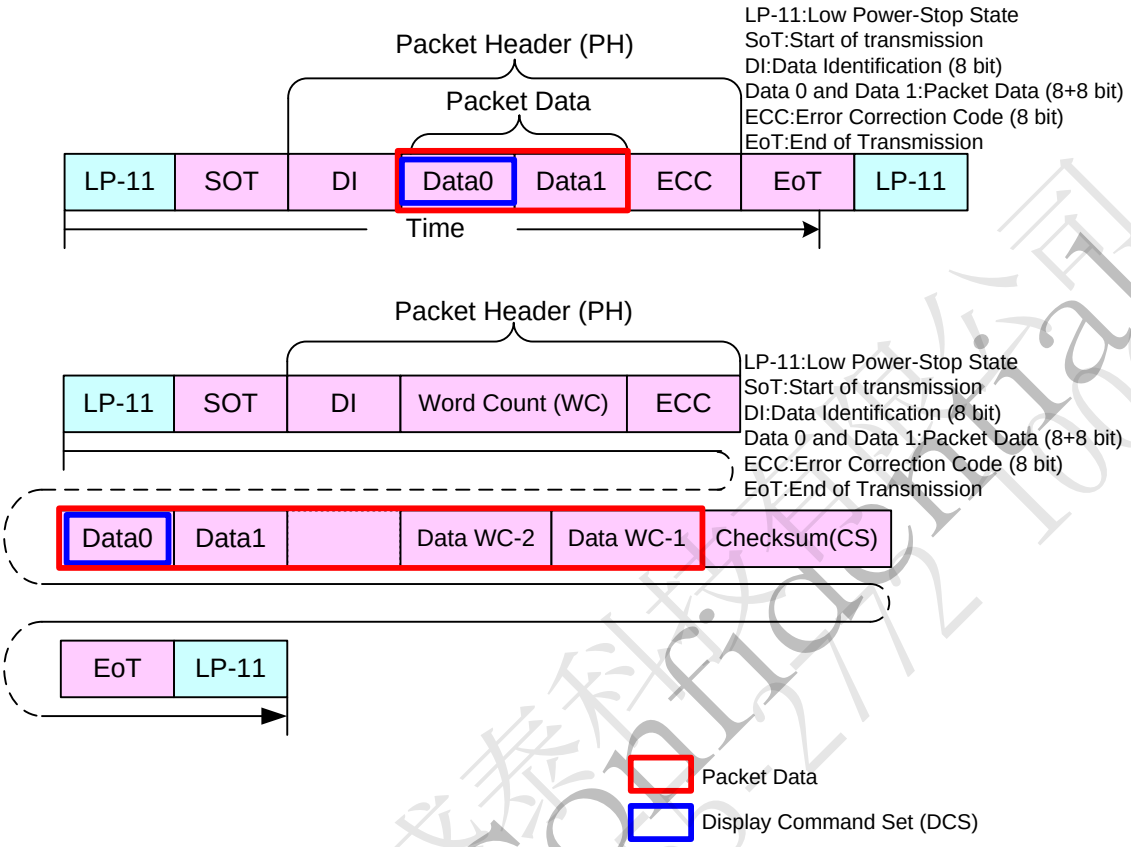

Figure 49 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

7.5.7.2 Packet from the Display Module to the MCU

- **Used Packet Types**

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report.

The used packet type is defined on Data Type (DT).

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

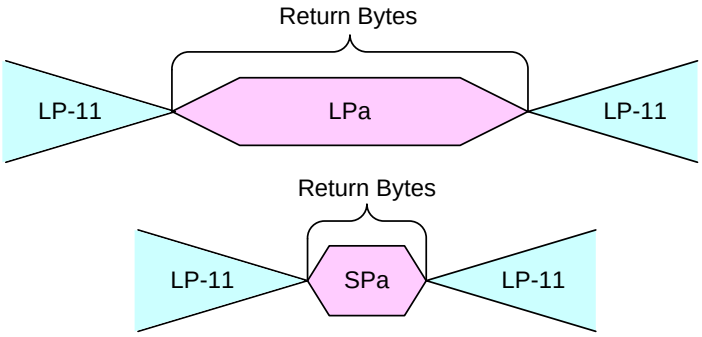

Figure 50 Return Bytes on Signal Packet

From the Display Module (or Other Devices) to the MCU									
Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet: Acknowledge with Error Report) to the MCU when the display module has received a read command. These return packets are illustrated for reference purpose below.

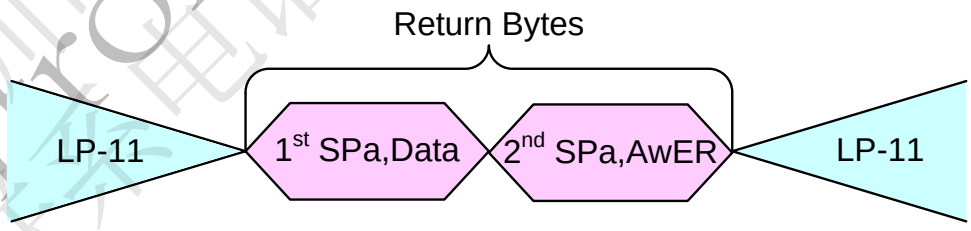

Figure 51 Exception When Return Bytes on Several Packet

Note:

1. AwER=Acknowledge with Error Report

- **Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)**

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description	Sitronix LCD Driver Implementation
0	SoT Error	NO
1	SoT Sync Error	NO
2	EoT Sync Error	NO
3	Escape Mode Entry Command Error	YES
4	Low-Power Transmit Sync Error	YES
5	Any Protocol Timer Time-Out	NO
6	False Control Error	YES
7	Contention is Detected on the Display Module	NO
8	ECC Error, single-bit (detected and corrected)	YES
9	ECC Error, multi-bit (detected, not corrected)	YES
10	Set to "0" internally (Only for Long Packet (LP))	YES
11	DSI Data Type (DT) Not Recognized	YES
12	DSI Virtual Channel (VC) ID Invalid	YES
13	Invalid Transmission Length	NO
14	Reserved, Set to '0' internally	NO
15	DSI Protocol Violation	NO

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Note

AwER will return1-bit zero if the item is no implementation.

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These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD):

Bit 8: ECC Error, single-bit (detected and corrected)

AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

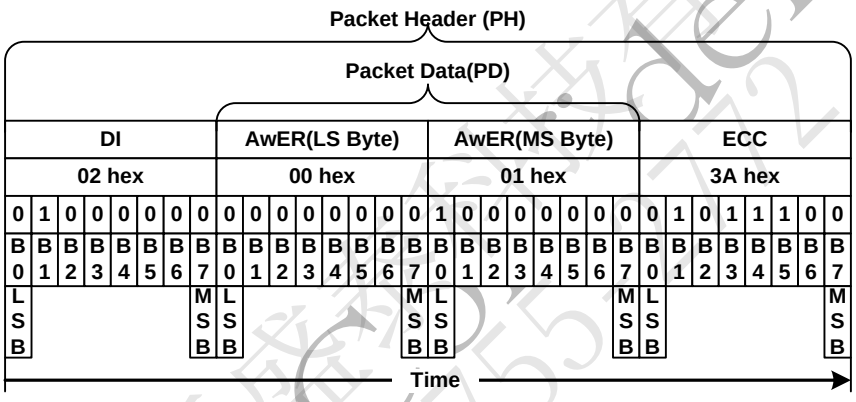

Figure 52 Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.

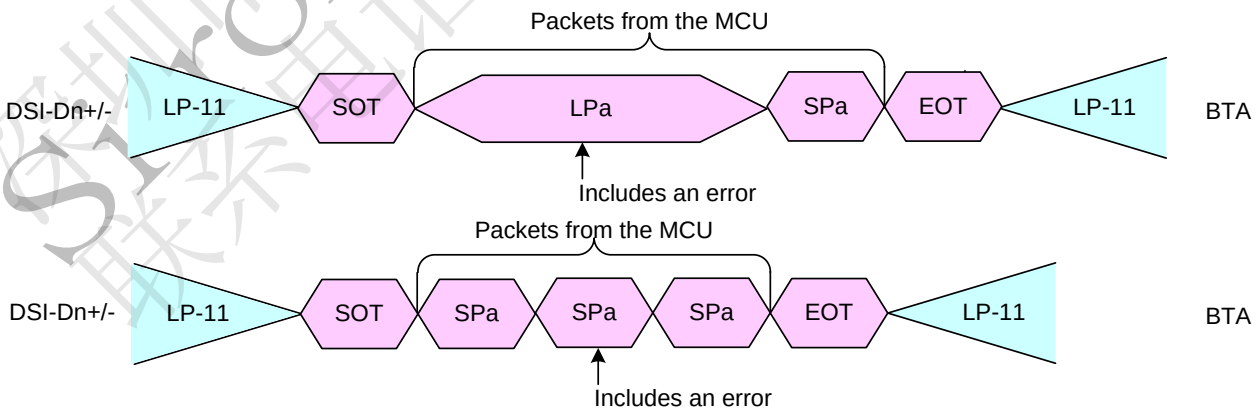

Figure 53 Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Number of the Errors on DSI (05h)" command.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h after the MCU has read the RDNUMED register from the display mo

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8. REGISTER LIST

8.1 Register Summary

COMMAND TABLE1										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
FFh	W	REGISTER PAGE1	EXTC_EN	---	REGISTER PAGE2	---	REGISTER PAGE3	SPI3_RWX	REGISTER PAGE4	00h
10h	W	0	0	0	0	GRB	0	0	DISP	08h
11h	W	CONTRAST[7:0]								40h
14h	W	BRIGHTNESS[7:0]								40h
17h	W		H_BLANKING[6:0]							08h
18h	W		V_BLANKING[6:0]							10h
1Ch	W	0	0	0	0	0	AUTODL	0	0	--
COMMAND TABLE2										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	VRHP[6:0]							--
41h	R/W	0	VRHN[6:0]							--
42h	R/W	VGL[3:0]				VGHS[3:0]				--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

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GAMMA COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	HRATIO[1:0]		VRF[5:0]						--
21h	PFP1[2:0]			PKP0[4:0]					--
22h	PFP2[2:0]			PKP1[4:0]					--
23h	PFP3[2:0]			PKP2[4:0]					--
24h	PFP4[2:0]			PKP3[4:0]					--
25h	PFP5[2:0]			PKP4[4:0]					--
26h	PFP6[2:0]			PKP5[4:0]					--
27h	PFP7[2:0]			PKP6[4:0]					--
28h	0	0	0	PKP7[4:0]					--
29h	0	0	0	PFP0[4:0]					--
2Ah	0	0	0	PFP8[4:0]					--
2Bh	0	0	0	PFP9[4:0]					--
30h	LRATIO[1:0]		VOS[5:0]						--
31h	PFN1[2:0]			PKN0[4:0]					--
32h	PFN2[2:0]			PKN0[4:0]					--
33h	PFN3[2:0]			PKN1[4:0]					--
34h	PFN4[2:0]			PKN2[4:0]					--
35h	PFN5[2:0]			PKN3[4:0]					--
36h	PFN6[2:0]			PKN4[4:0]					--
37h	PFN7[2:0]			PKN5[4:0]					--
38h	0	0	0	PKN7[4:0]					--
39h	0	0	0	PFN0[4:0]					--
3Ah	0	0	0	PFN8[4:0]					--
3Bh	0	0	0	PFN9[4:0]					--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

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OTP COMMAND TABLE										
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--
02h	R/W	0	ID2[6:0]							--
03h	R/W	0	ID3[6:0]							--
05h	R/W	0	VMF[6:0]							40h
60h	W	0	1	0	0	0	1	OTPEN	0	44h
65h	W	OTPACK[7:0]								00h
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

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8.2 Command Table1 Register Description

8.2.1 GRB、DISP CONTROL (10h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h

Designation	Description
GRB	Reset register setting. GRB=0: reset all registers to default value GRB=1: normal operation
DISP	Display on/off control. DISP=0: standby mode DISP=1: normal mode

8.2.2 CONTRAST (11h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
11h	W	CONTRAST[7:0]								40h

Designation	Description
CONTRAST[7:0]	Set RGB contrast level, the range of gain is 0~3.984. CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 CONTRAST=FFh: contrast gain=3.984

8.2.3 BRIGHTNESS (14h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	W	BRIGHTNESS[7:0]								40h

Designation	Description
BRIGHTNESS[7:0]	Set RGB brightness level, the range of brightness is -64~+191. BRIGHTNESS=00h: -64 BRIGHTNESS=40h: 0 BRIGHTNESS=FFh: +191

8.2.4 H_BLANKING (17h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
17h	W	0	H_BLANKING[6:0]							08h

Designation	Description
H_BLANKING[6:0]	The HSYNC back porch setting of RGB interface.

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8.2.5 V_BLANKING (18h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	W	0	V_BLANKING[6:0]							08h

Designation	Description
V_BLANKING[6:0]	The VSYNC back porch setting of RGB interface.

8.2.6 OTP AUTO DOWNLOAD CONTROL (1Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	W	0	0	0	0	0	AUTODL	0	0	--

Designation	Description
AUTODL	OTP auto-refresh function control. AUTODL= 0: disable auto-refresh function AUTODL= 1: enable auto-refresh function

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8.3 Command Table2 Register Description

8.3.1 GVDD SETTING (40h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	VRHP[6:0]							--

Designation	Description
VRHP[6:0]	GVDD level setting

VRHP	GVDD	VRHP	GVDD	VRHP	GVDD	VRHP	GVDD
00	Reserved	20	5.696	40	5.184	60	4.672
01	Reserved	21	5.680	41	5.168	61	4.656
02	Reserved	22	5.664	42	5.152	62	4.640
03	Reserved	23	5.648	43	5.136	63	4.624
04	Reserved	24	5.632	44	5.120	64	4.608
05	Reserved	25	5.616	45	5.104	65	4.592
06	Reserved	26	5.600	46	5.088	66	4.576
07	Reserved	27	5.584	47	5.072	67	4.560
08	Reserved	28	5.568	48	5.056	68	4.544
09	Reserved	29	5.552	49	5.040	69	4.528
0A	Reserved	2A	5.536	4A	5.024	6A	4.512
0B	Reserved	2B	5.520	4B	5.008	6B	4.496
0C	Reserved	2C	5.504	4C	4.992	6C	4.480
0D	Reserved	2D	5.488	4D	4.976	6D	4.464
0E	Reserved	2E	5.472	4E	4.960	6E	4.448
0F	Reserved	2F	5.456	4F	4.944	6F	4.432
10	5.952	30	5.440	50	4.928	70	4.416
11	5.936	31	5.424	51	4.912	71	4.400
12	5.920	32	5.408	52	4.896	72	4.384
13	5.904	33	5.392	53	4.880	73	4.368
14	5.888	34	5.376	54	4.864	74	4.352
15	5.872	35	5.360	55	4.848	75	4.336
16	5.856	36	5.344	56	4.832	76	4.320
17	5.840	37	5.328	57	4.816	77	4.304
18	5.824	38	5.312	58	4.800	78	4.288
19	5.808	39	5.296	59	4.784	79	4.272
1A	5.792	3A	5.280	5A	4.768	7A	4.256
1B	5.776	3B	5.264	5B	4.752	7B	4.240
1C	5.760	3C	5.248	5C	4.736	7C	4.224
1D	5.744	3D	5.232	5D	4.720	7D	4.208

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	1E	5.728	3E	5.216	5E	4.704	7E	4.192
	1F	5.712	3F	5.200	5F	4.688	7F	4.176

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8.3.2 GVCL SETTING (41h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
41h	R/W	0	VRHN[6:0]							--

Designation	Description
VRHN[6:0]	GVCL level setting

VRHN	GVCL	VRHN	GVCL	VRHN	GVCL	VRHN	GVCL
00	Reserved	20	-4.496	40	-3.984	60	-3.472
01	Reserved	21	-4.480	41	-3.968	61	-3.456
02	Reserved	22	-4.464	42	-3.952	62	-3.440
03	Reserved	23	-4.448	43	-3.936	63	-3.424
04	Reserved	24	-4.432	44	-3.920	64	-3.408
05	Reserved	25	-4.416	45	-3.904	65	-3.392
06	Reserved	26	-4.400	46	-3.888	66	-3.376
07	Reserved	27	-4.384	47	-3.872	67	-3.360
08	Reserved	28	-4.368	48	-3.856	68	-3.344
09	Reserved	29	-4.352	49	-3.840	69	-3.328
0A	Reserved	2A	-4.336	4A	-3.824	6A	-3.312
0B	Reserved	2B	-4.320	4B	-3.808	6B	-3.296
0C	Reserved	2C	-4.304	4C	-3.792	6C	-3.280
0D	Reserved	2D	-4.288	4D	-3.776	6D	-3.264
0E	Reserved	2E	-4.272	4E	-3.760	6E	-3.248
0F	Reserved	2F	-4.256	4F	-3.744	6F	-3.232
10	Reserved	30	-4.240	50	-3.728	70	-3.216
11	Reserved	31	-4.224	51	-3.712	71	-3.200
12	Reserved	32	-4.208	52	-3.696	72	-3.184
13	Reserved	33	-4.192	53	-3.680	73	-3.168
14	Reserved	34	-4.176	54	-3.664	74	-3.152
15	Reserved	35	-4.160	55	-3.648	75	-3.136
16	Reserved	36	-4.144	56	-3.632	76	-3.120
17	Reserved	37	-4.128	57	-3.616	77	-3.104
18	Reserved	38	-4.112	58	-3.600	78	-3.088
19	Reserved	39	-4.096	59	-3.584	79	-3.072
1A	Reserved	3A	-4.080	5A	-3.568	7A	-3.056
1B	Reserved	3B	-4.064	5B	-3.552	7B	-3.040
1C	Reserved	3C	-4.048	5C	-3.536	7C	-3.024
1D	Reserved	3D	-4.032	5D	-3.520	7D	-3.008
1E	Reserved	3E	-4.016	5E	-3.504	7E	-2.992
1F	Reserved	3F	-4.000	5F	-3.488	7F	-2.976

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8.3.3 VGHS, VGL SETTING (45h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
45h	R/W	VGL[3:0]				VGHS[3:0]				--

<table>
<tr><th>Designation</th><th>Description</th></tr>
<tr><td>VGL[3:0]</td><td>VGL level setting
<table>
<tr><th>VGL[3:0]</th><th>VGL (V)</th></tr>
<tr><td>00</td><td>-6.6</td></tr>
<tr><td>01</td><td>-7</td></tr>
<tr><td>02</td><td>-7.43</td></tr>
<tr><td>03</td><td>-7.88</td></tr>
<tr><td>04</td><td>-8.22</td></tr>
<tr><td>05</td><td>-8.63</td></tr>
<tr><td>06</td><td>-9.05</td></tr>
<tr><td>07</td><td>-9.36</td></tr>
<tr><td>08</td><td>-9.66</td></tr>
<tr><td>09</td><td>-10.2</td></tr>
<tr><td>0A</td><td>-10.7</td></tr>
<tr><td>0B</td><td>-11</td></tr>
<tr><td>0C</td><td>-11.4</td></tr>
<tr><td>0D</td><td>-12</td></tr>
<tr><td>0E</td><td>Reserved</td></tr>
<tr><td>0F</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>VGHS[3:0]</td><td>VGH level setting
<table>
<tr><th>VGHS3:0]</th><th>VGH (V)</th><th>VGHS3:0]</th><th>VGH (V)</th></tr>
<tr><td>00</td><td>8</td><td>0C</td><td>Reserved</td></tr>
<tr><td>01</td><td>9</td><td>0D</td><td>Reserved</td></tr>
<tr><td>02</td><td>10</td><td>0E</td><td>Reserved</td></tr>
<tr><td>03</td><td>11</td><td>0F</td><td>Reserved</td></tr>
<tr><td>04</td><td>12</td><td></td><td></td></tr>
<tr><td>05</td><td>13</td><td></td><td></td></tr>
<tr><td>06</td><td>14</td><td></td><td></td></tr>
<tr><td>07</td><td>14.5</td><td></td><td></td></tr>
<tr><td>08</td><td>15</td><td></td><td></td></tr>
<tr><td>09</td><td>15.5</td><td></td><td></td></tr>
<tr><td>0A</td><td>16</td><td></td><td></td></tr>
<tr><td>0B</td><td>Reserved</td><td></td><td></td></tr>
</table></td></tr>
</table>

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8.4 Gamma Table Register Description

8.4.1 GAMMA SETTING (20h~29h, 30h~39h)

GAMMA COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	HRATIO[1:0]		VRF[5:0]						--
21h	PFP1[2:0]			PKP0[4:0]					--
22h	PFP2[2:0]			PKP1[4:0]					--
23h	PFP3[2:0]			PKP2[4:0]					--
24h	PFP4[2:0]			PKP3[4:0]					--
25h	PFP5[2:0]			PKP4[4:0]					--
26h	PFP6[2:0]			PKP5[4:0]					--
27h	PFP7[2:0]			PKP6[4:0]					--
28h	0	0	0	PKP7[4:0]					--
29h	0	0	0	PFP0[4:0]					--
2Ah	0	0	0	PFP8[4:0]					--
2Bh	0	0	0	PFP9[4:0]					--
30h	LRATIO[1:0]		VOS[5:0]						--
31h	PFN1[2:0]			PKN0[4:0]					--
32h	PFN2[2:0]			PKN0[4:0]					--
33h	PFN3[2:0]			PKN1[4:0]					--
34h	PFN4[2:0]			PKN2[4:0]					--
35h	PFN5[2:0]			PKN3[4:0]					--
36h	PFN6[2:0]			PKN4[4:0]					--
37h	PFN7[2:0]			PKN5[4:0]					--
38h	0	0	0	PKN7[4:0]					--
39h	0	0	0	PFN0[4:0]					--
3Ah	0	0	0	PFN8[4:0]					--
3Bh	0	0	0	PFN9[4:0]					--

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Designation	Description
PKP0[4:0]	V16 gamma selection
PKN0[4:0]	
PKP1[4:0]	V32 gamma selection
PKN1[4:0]	
PKP2[4:0]	V48 gamma selection
PKN2[4:0]	
PKP3[4:0]	V80 gamma selection
PKN3[4:0]	
PKP4[4:0]	V176 gamma selection
PKN4[4:0]	
PKP5[4:0]	V208 gamma selection
PKN5[4:0]	
PKP6[4:0]	V224 gamma selection
PKN6[4:0]	
PKP7[4:0]	V240 gamma selection
PKN7[4:0]	
VRF[5:0]	V8 gamma selection
VOS[5:0]	V248 gamma selection
PFP0[4:0]	V4 gamma selection
PFN0[4:0]	
PFP1[2:0]	V12 gamma selection
PFN1[2:0]	
PFP2[2:0]	V64 gamma selection
PFN2[2:0]	
PFP3[2:0]	V104 gamma selection
PFN3[2:0]	
PFP4[2:0]	V128 gamma selection
PFN4[2:0]	
PFP5[2:0]	V152 gamma selection
PFN5[2:0]	
PFP6[2:0]	V192 gamma selection
PFN6[2:0]	
PFP7[2:0]	V224 gamma selection
PFN7[2:0]	
PFP8[2:0]	V252 gamma selection
PFN8[2:0]	

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8.5 OTP Table Register Description

8.5.1 ID1 SETTING (01h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--

Designation	Description
ID1[6:0]	Built-in OTP for ID1 setting.

8.5.2 ID2 SETTING (02h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	R/W	0	ID2[6:0]							--

Designation	Description
ID2[6:0]	Built-in OTP for ID2 setting.

8.5.3 ID3 SETTING (03h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
03h	R/W	0	ID3[6:0]							--

Designation	Description
ID3[6:0]	Built-in OTP for ID3 setting.

8.5.4 VCOM OFFSET SETTING (05h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
05h	R/W	0	VMF[6:0]							40h

Designation	Description
VMF[6:0]	VCOM offset setting

VMF[6]	VMF[5:0]	VCOM”	GVDD	GVCL
0	000000	VCOM+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOM+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOM+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOM+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOM+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOM+0d	VRHP[6:0]	VRHN[6:0]
1	000001	VCOM-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOM-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|

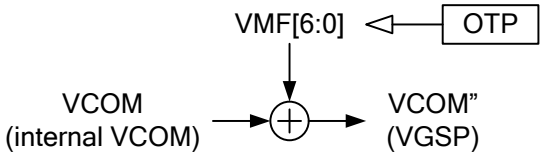
1	111110	VCOM-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
1	111111	VCOM-63d	VRHP[6:0]-63d	VRHN[6:0]-63d

Note: 1.d=12.5mV

2. Adjustable VCOM offset (OTP) can be used to compensate feedthrough tolerance and its limitation couldn't exceed the maximum voltage range of GVDD and GVCL.

3. VCOM" ≤ GVDD-Vop = GVCL+Vop

Vop is the operation voltage of liquid crystal.



8.5.5 OTP FUNCTION CONTROL (60h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	W	0	1	0	0	0	1	OTPEN	0	44h

Designation	Description
OTPEN	OTP programming function control. OTPEN = 0: disable OTP programming function OTPEN = 1: enable OTP programming function

8.5.6 OTP ACKNOWLEDGEMENT CONTROL (65h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
65h	W	OTPACK[7:0]								00h

Designation	Description
OTPACK[7:0]	OTP active selection.

OTPACK[7:0]	Description
31h	ID1 program
32h	ID2 program
33h	ID3 program
3Ah	VCOM offset program

8.5.7 ID1 PROGRAM TIMES (68h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--

Designation	Description
ID1 OTP TIME[2:0]	Read ID1 remaining programmable times.

8.5.8 ID2 PROGRAM TIMES (69h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--

Designation	Description
ID2 OTP TIME[2:0]	Read ID2 remaining programmable times.

8.5.9 ID3 PROGRAM TIMES (6Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--

Designation	Description
ID3 OTP TIME[2:0]	Read ID3 remaining programmable times.

8.5.10 VCOM OFFEST PROGRAM TIMES (6Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Designation	Description
VMF OTP TIME[2:0]	Read VMF remaining programmable times.

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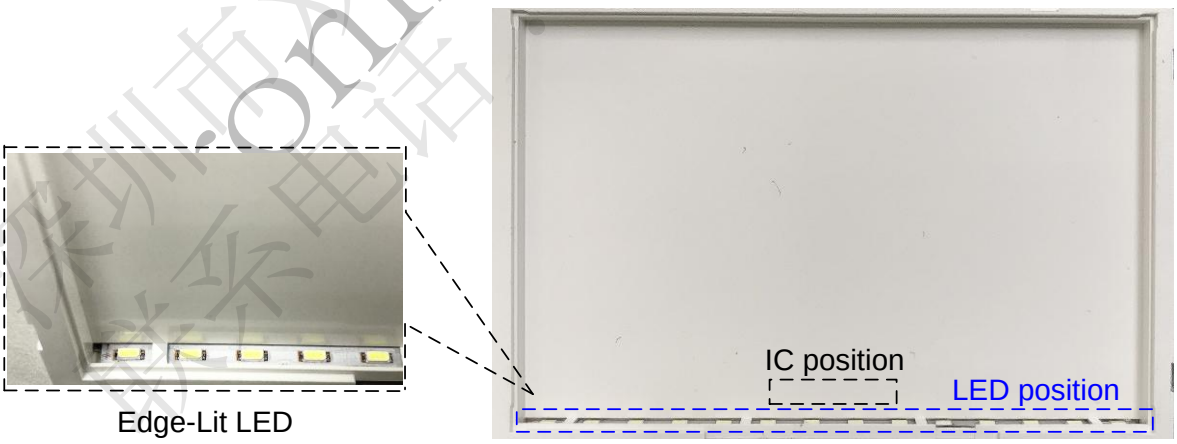
9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.0	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VOUT	-0.3 ~ VDDI + 0.3	V
Dirver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. *That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.*
2. *Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.*
3. *Insure the voltage levels of VDDI, VDD, PVDD always matches the correct relation:*
   3.2V ≦ VDDI ≦ VDD = PVDD ≦ 3.6V
4. *VIN should be less than or equal to 3.6V(VIN ≤ 3.6V).*
5. *Panel display quality depends on panel loading, and it may have the different performance at low/high temperature.*
6. *When the backlight LED is turned on which is the heat generation leads to the increasing temperature of the LCD module.*
   In order to protect the LCD driver IC against thermal effect, we advise that the positon of backlight LED should not be close to the driver IC. The edge-lit type LED is recommended.



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9.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

9.2.1 Recommended Operating Range

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.2	3.3	3.6	V	
IO Supply Voltage	VDDI	3.2	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.2	3.3	3.6	V	

9.2.2 DC Characteristics for Digital Circuit

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGH	8		16	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-12		-6.6	V	
Output Voltage Deviation	Vod	-	±40	±50	mV	
Standby Current	Isc	-	-	50	uA	
Operation Current	Ioc	-	40	-	mA	

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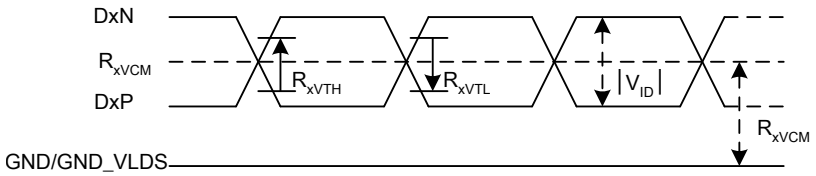
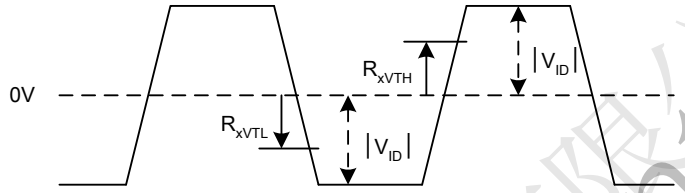
9.2.4 DC Characteristics for LVDS Receiver Circuit

Single end signals



Differential signals



DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold Voltage	R_{xVTH}	-	-	0.1	V	R_{xVCM} = 1.2V
Differential Input Low Threshold Voltage	R_{xVTL}	-0.1	-	-	V	
Input Voltage Range (Singled-End)	R_{xVIN}	0	-	VDD-1.0	V	
Differential Input Common Mode Voltage	R_{xVCM}	$\lvert V_{ID} \rvert$ /2	-	2.4-$\lvert V_{ID} \rvert$/2	V	
Differential Input Voltage	$\lvert V_{ID} \rvert$	0.2	-	0.6	V	
Differential Input Leakage Current	RV_{xliz}	-10	-	10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	
Differential Input Termination Resistance	R_{ID}	-	100	-	Ω	

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9.3 AC Characteristics

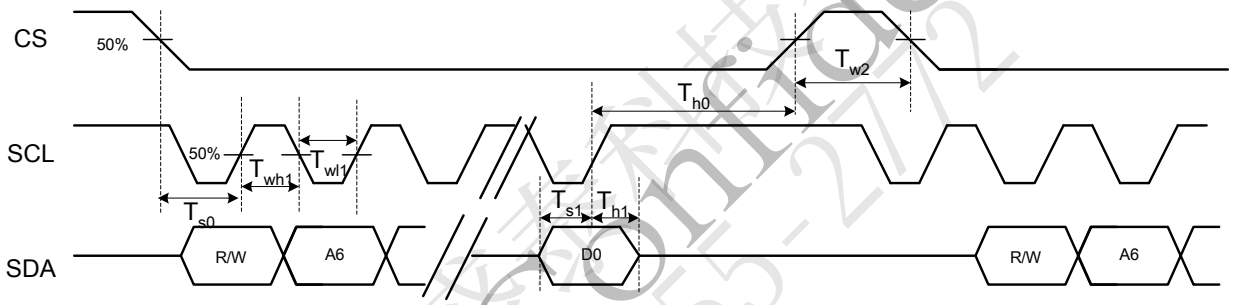
AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

9.3.1 System Operation AC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

9.3.2 System Bus Timing for 3-Wire SPI Interface

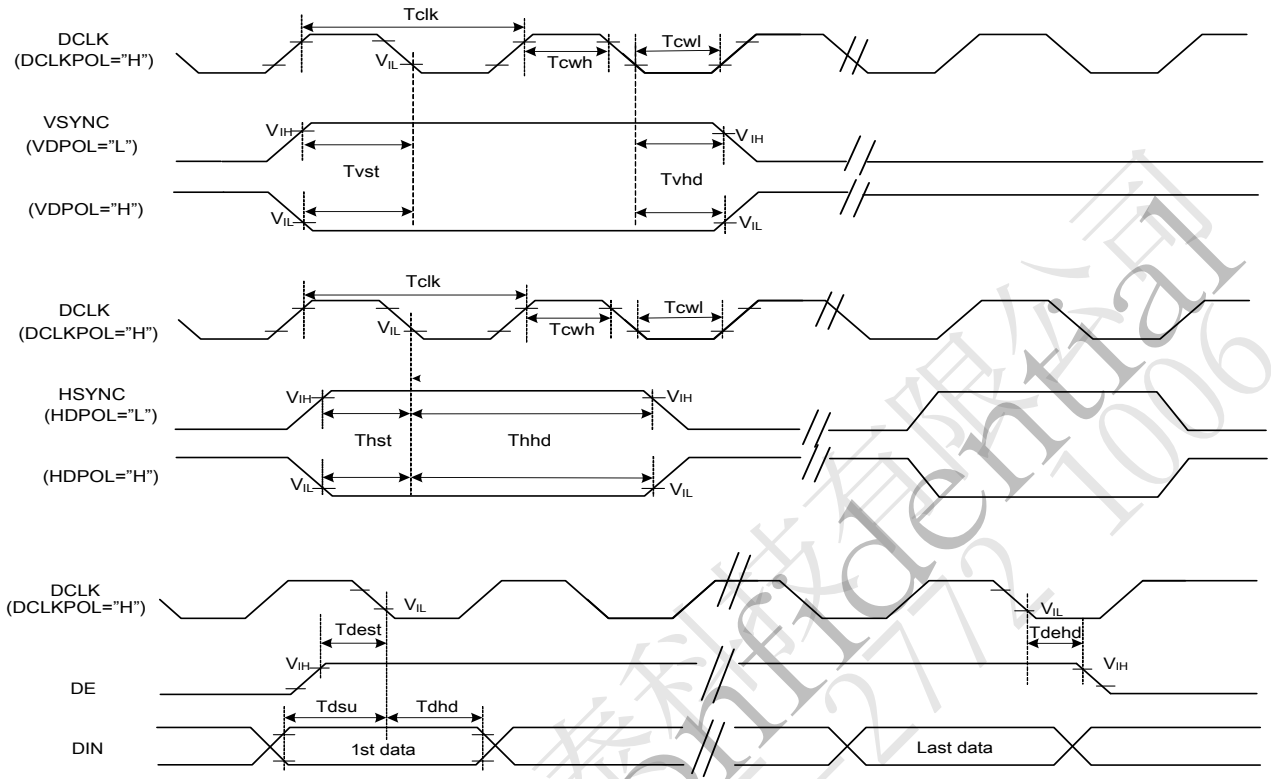


DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

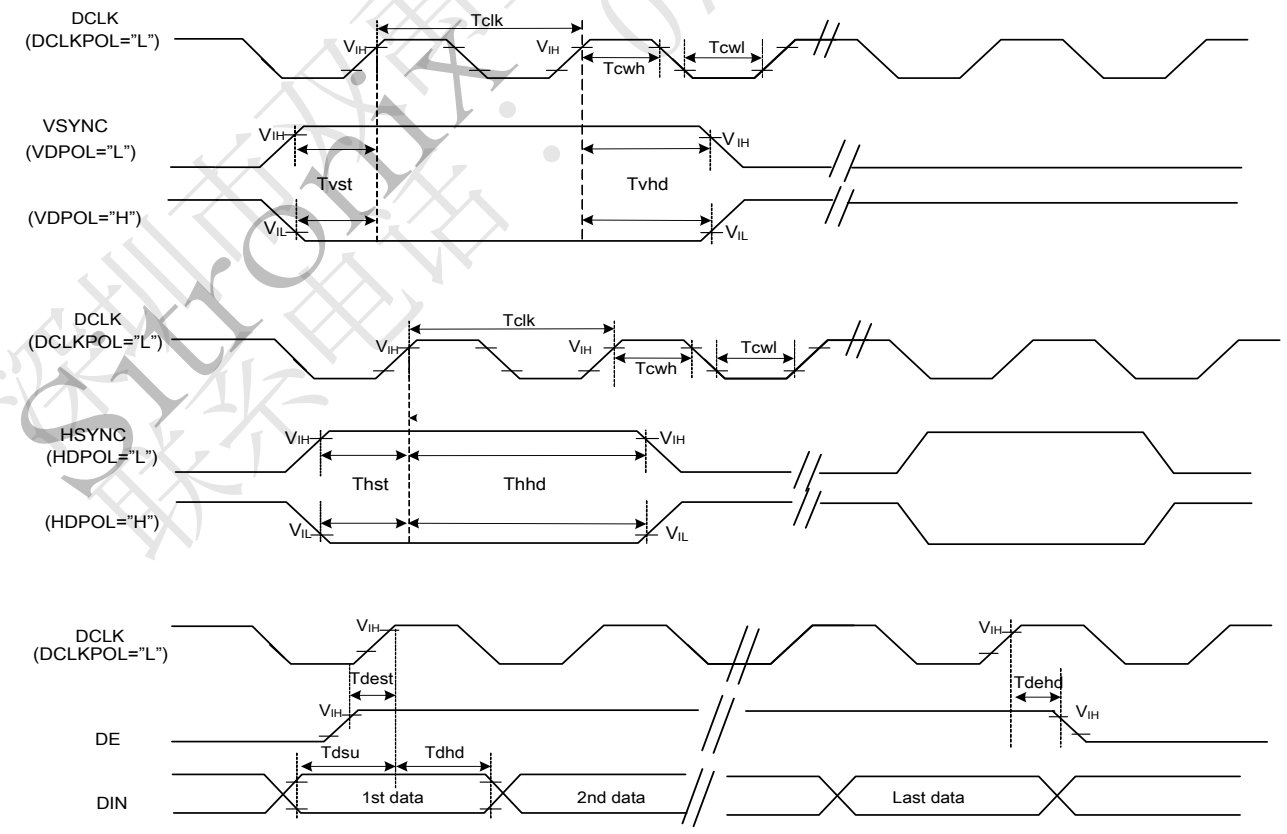
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	T_{s0}	50	-	-	ns	
Serial Data Input Setup Time	T_{s1}	50	-	-	ns	
CS Input Hold Time	T_{h0}	50	-	-	ns	
Serial Data Input Hold Time	T_{h1}	50	-	-	ns	
SCL Write Pulse High Width	T_{wh1}	50	-	2000	ns	
SCL Write Pulse Low Width	T_{wl1}	50	-	2000	ns	
SCL Read Pulse High Width	T_{rh1}	300	-	2000	ns	
SCL Read Pulse Low Width	T_{rl1}	300	-	2000	ns	
CS Pulse High Width	T_{w2}	400	-	-	ns	

9.3.3 System Bus Timing for RGB Interface

DCLK Neagtive Polarity (DCLPOL="H")



DCLK Positive Polarity (DCLPOL="L")



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DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tcw	40	50	60	%	
VSYNC Setup Time	Tvst	10	-	-	ns	
VSYNC Hold Time	Tvhd	10	-	-	ns	
HSYNC Setup Time	Thst	10	-	-	ns	
HSYNC Hold Time	Thhd	10	-	-	ns	
Data Setup Time	Tdsu	10	-	-	ns	
Data Hold Time	Tdhd	10	-	-	ns	
DE Setup Time	Tdest	10	-	-	ns	
DE Hold Time	Tdehd	10	-	-	ns	

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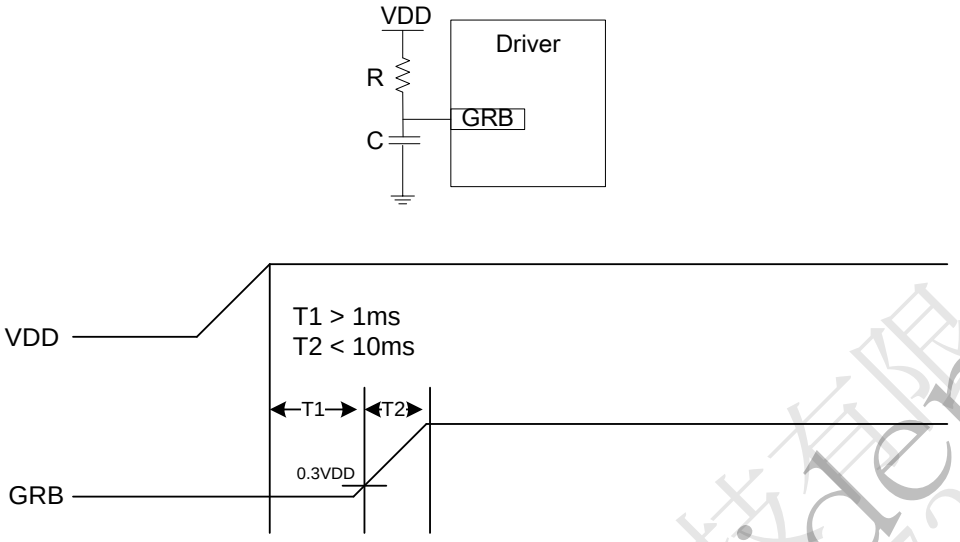
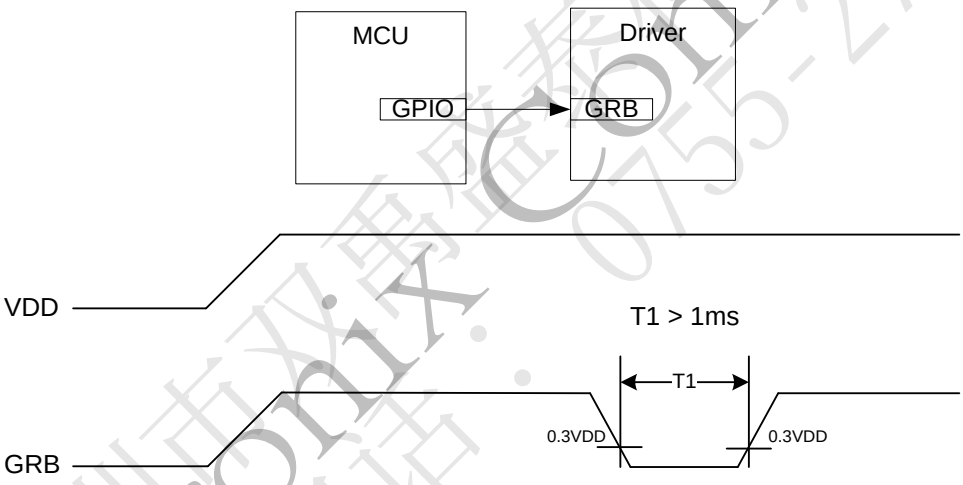
9.3.4 Reset timing

Setting GRB pin to “L” (hardware reset) can initialize internal function. Initialized by GRB pin is essential before operating. There are two suggestions for hardware reset connection.

(1) The GRB pin with external RC circuit.



(2) The GRB pin controlled by MCU.



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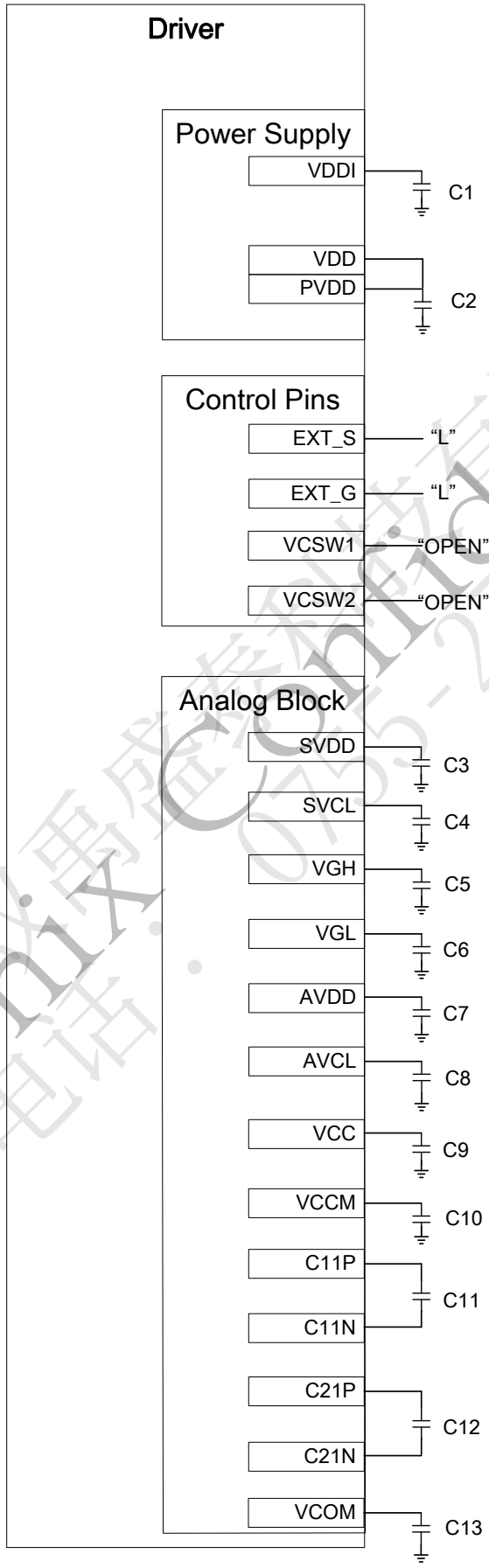
10. APPLICATION CIRCUIT

10.1 1 Power Mode



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10.1.1 Input Voltage

Pin Name	Voltage range	Note
VDDI	3.2~3.6V	
VDD	3.2~3.6V	
PVDD	3.2~3.6V	

10.1.2 External Component

Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	4.7	10	
C4	4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	
C11	4.7	10	
C12	4.7	10	
C13	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C13 is used when feedthrough voltage > 1.2V.

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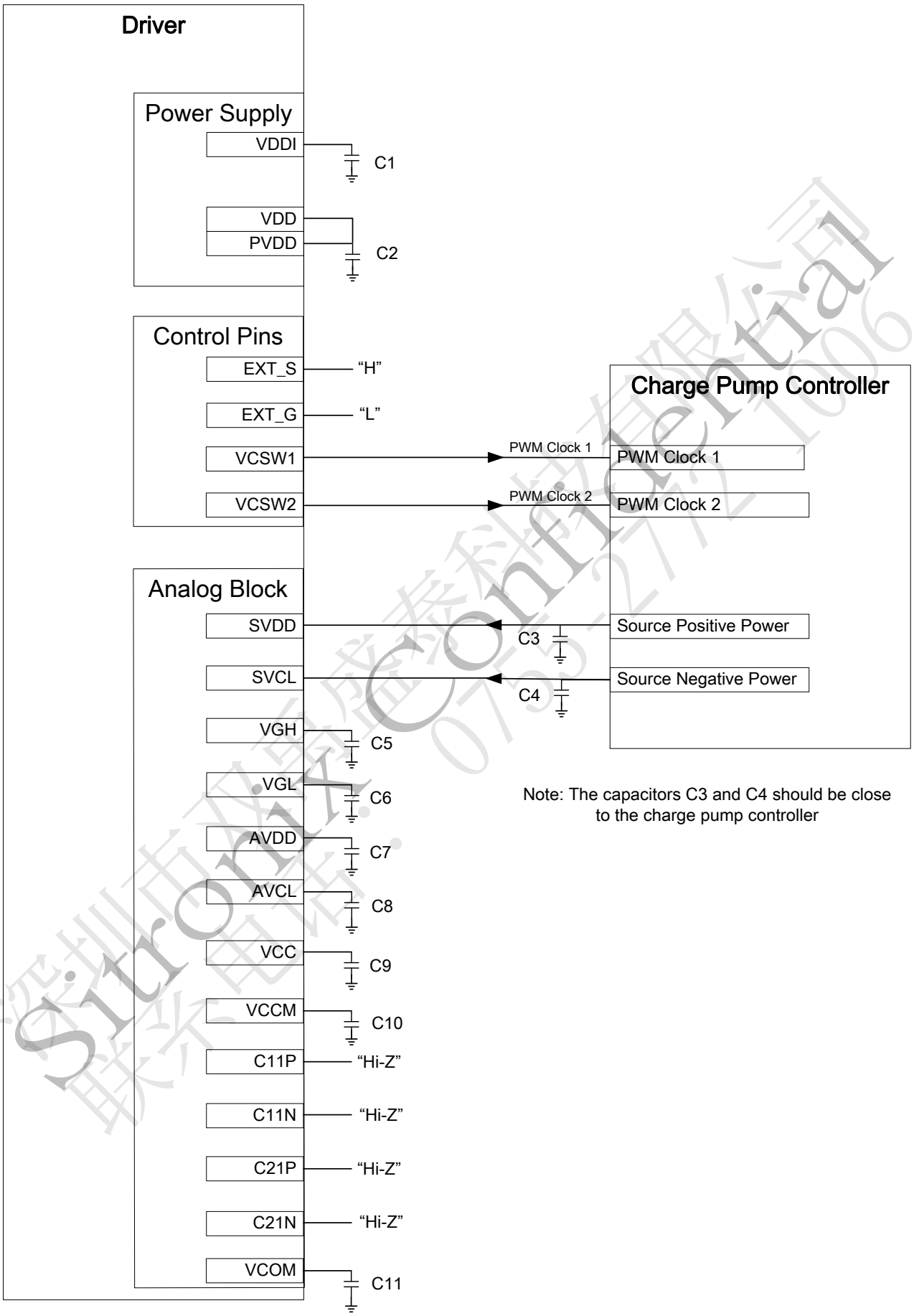
10.2 3 Power Mode with Charge Pump Controller



Note: The capacitors C3 and C4 should be close to the charge pump controller

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10.2.1 Input Voltage

Pin Name	Voltage range(V)	Note
VDDI	3.2~3.6	
VDD	3.2~3.6	
PVDD	3.2~3.6	
SVDD	6.4	External power supply by Charge Pump Controller
SVCL	-6.4	External power supply by Charge Pump Controller

10.2.2 External Component

Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	4.7	10	
C4	4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	
C11	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C11 is used when feedthrough voltage > 1.2V.

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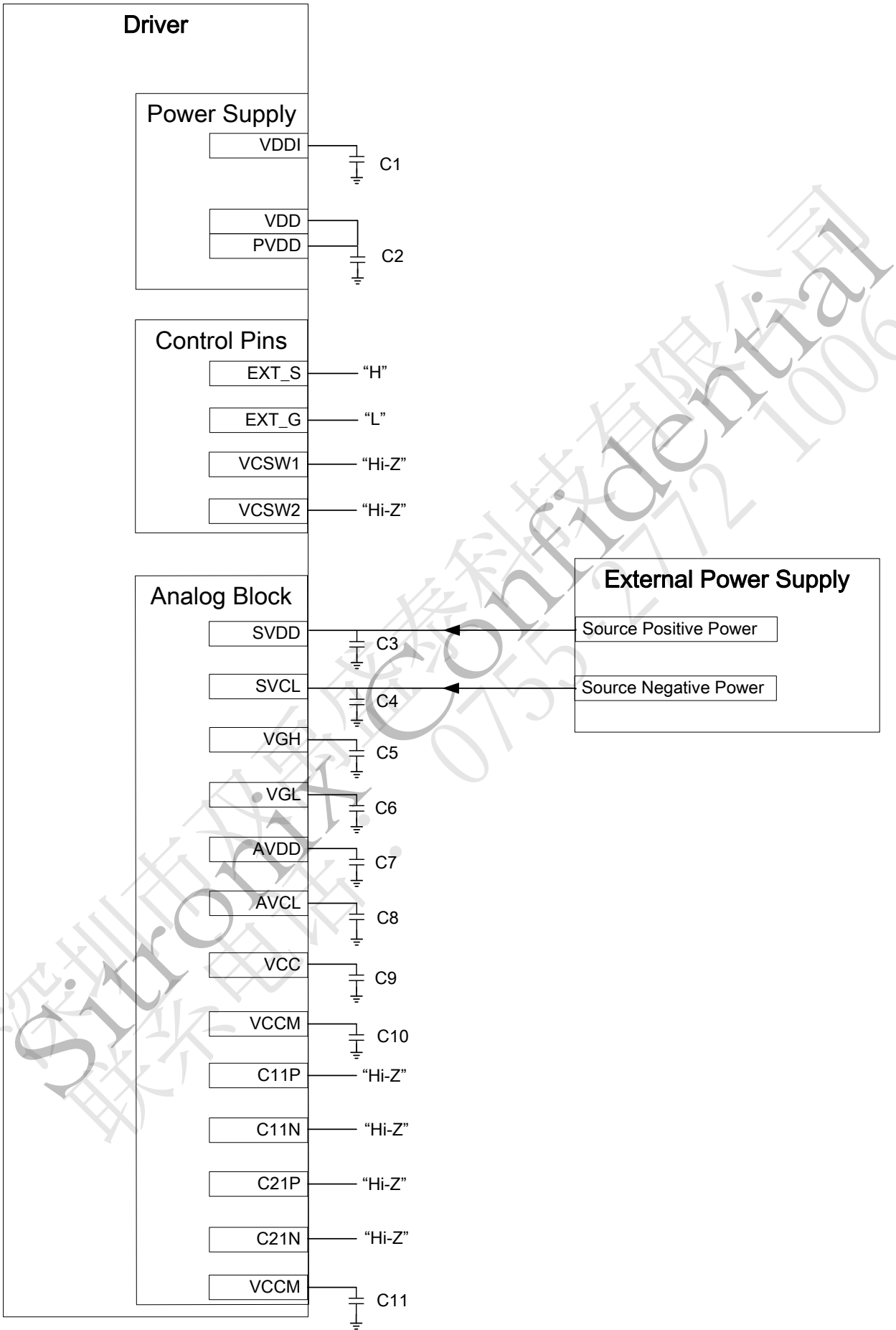
10.3 3 Power Mode with External Power Supply



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10.3.1 Input Voltage

Pin Name	Voltage range(V)	Note
VDDI	3.2~3.6	
VDD	3.2~3.6	
PVDD	3.2~3.6	
SVDD	6.4	External power supply
SVCL	-6.4	External power supply

10.3.2 External Component

Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	4.7	10	
C4	4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	
C11	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C11 is used when feedthrough voltage > 1.2V.

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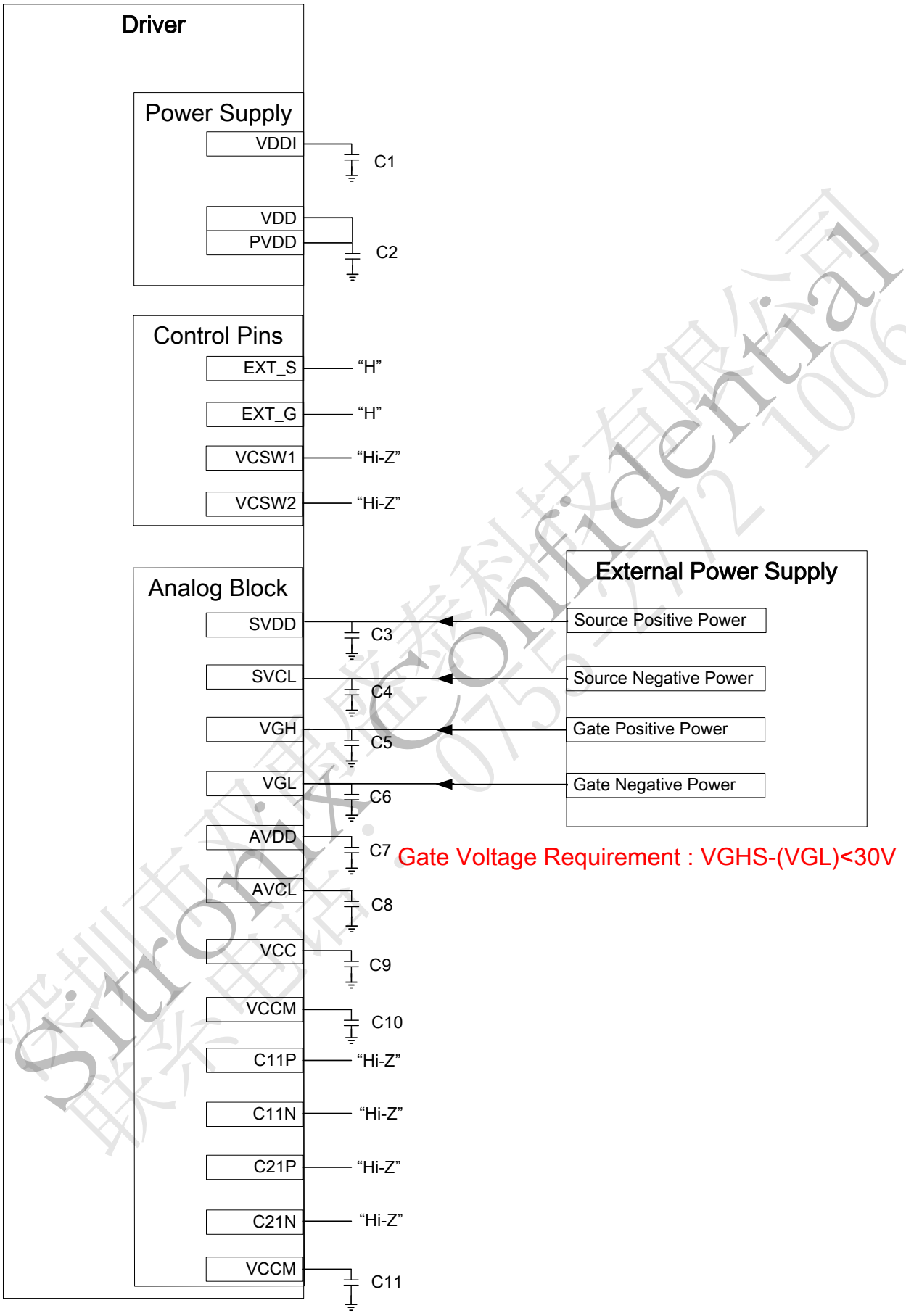
10.4 5 Power Mode with External Power Supply



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10.4.1 Input Voltage

Pin Name	Voltage range(V)	Note
VDDI	3.2~3.6	
VDD	3.2~3.6	
PVDD	3.2~3.6	
SVDD	6.4	External power supply
SVCL	-6.4	External power supply
VGH	8~16	External power supply , VGHS voltage is determined by panel design
VGL	-6.6~-12	External power supply , VGL voltage is determined by panel design

10.4.2 External Component

Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	4.7	10	
C4	4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	
C11	2.2~4.7	6	

Note:

1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C11 is used when feedthrough voltage > 1.2V. If the feedthrough voltage is greater than 1.2V, please contact Sitronix.

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10.4 Input Color Format Application Circuit

10.4.1 Pin Assignment for RGB Interface

Pin		Parallel RGB		
		888	666	565
VSYNC	SYNC Mode	VSYNC	VSYNC	VSYNC
	DE Mode	x	x	x
	SYNC DE Mode	VSYNC	VSYNC	VSYNC
HSYNC	SYNC Mode	HSYNC	HSYNC	HSYNC
	DE Mode	x	x	x
	SYNC DE Mode	HSYNC	HSYNC	HSYNC
DE	SYNC Mode	x	x	x
	DE Mode	DE	DE	DE
	SYNC DE Mode	DE	DE	DE
DCLK		DCLK	DCLK	DCLK
DR0		R0	x	x
DR1		R1	x	x
DR2		R2	R2	x
DR3		R3	R3	R3
DR4		R4	R4	R4
DR5		R5	R5	R5
DR6		R6	R6	R6
DR7		R7	R7	R7
DG0		G0	x	x
DG1		G1	x	x
DG2		G2	G2	G2
DG3		G3	G3	G3
DG4		G4	G4	G4
DG5		G5	G5	G5
DG6		G6	G6	G6
DG7		G7	G7	G7
DB0		B0	x	x
DB1		B1	x	x
DB2		B2	B2	x
DB3		B3	B3	B3
DB4		B4	B4	B4
DB5		B5	B5	B5
DB6		B6	B6	B6
DB7		B7	B7	B7

10.4.2 Data Format

Parallel RGB888					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	1'R0	2'R0	3'R0	…	N'R0
DR1	1'R1	2'R1	3'R1	…	N'R1
DR2	1'R2	2'R2	3'R2	…	N'R2
DR3	1'R3	2'R3	3'R3	…	N'R3
DR4	1'R4	2'R4	3'R4	…	N'R4
DR5	1'R5	2'R5	3'R5	…	N'R5
DR6	1'R6	2'R6	3'R6	…	N'R6
DR7	1'R7	2'R7	3'R7	…	N'R7
DG0	1'G0	2'G0	3'G0	…	N'G0
DG1	1'G1	2'G1	3'G1	…	N'G1
DG2	1'G2	2'G2	3'G2	…	N'G2
DG3	1'G3	2'G3	3'G3	…	N'G3
DG4	1'G4	2'G4	3'G4	…	N'G4
DG5	1'G5	2'G5	3'G5	…	N'G5
DG6	1'G6	2'G6	3'G6	…	N'G6
DG7	1'G7	2'G7	3'G7	…	N'G7
DB0	1'B0	2'B0	3'B0	…	N'B0
DB1	1'B1	2'B1	3'B1	…	N'B1
DB2	1'B2	2'B2	3'B2	…	N'B2
DB3	1'B3	2'B3	3'B3	…	N'B3
DB4	1'B4	2'B4	3'B4	…	N'B4
DB5	1'B5	2'B5	3'B5	…	N'B5
DB6	1'B6	2'B6	3'B6	…	N'B6
DB7	1'B7	2'B7	3'B7	…	N'B7

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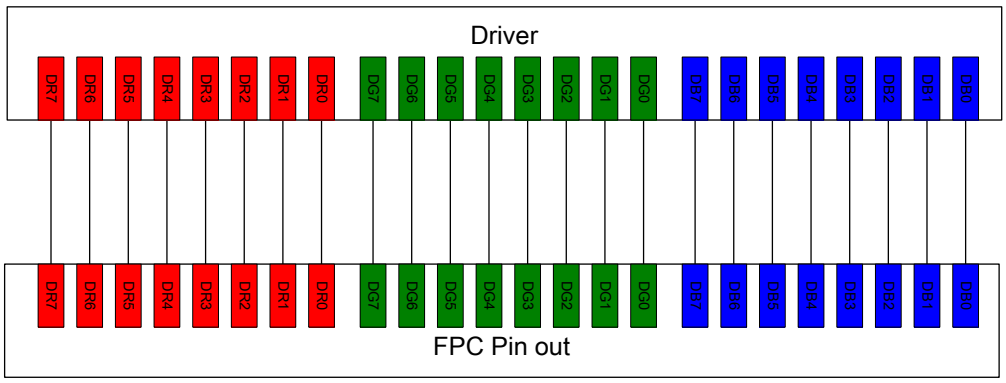
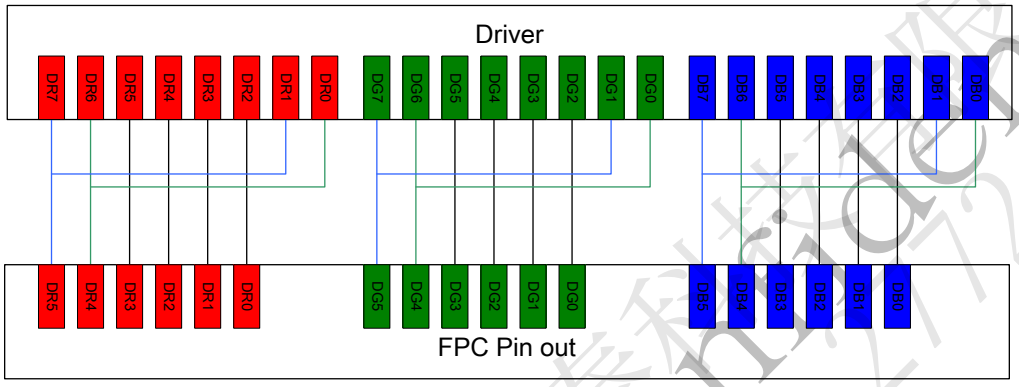
Parallel RGB666					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	1'R0	2'R0	3'R0	…	N'R0
DR3	1'R1	2'R1	3'R1	…	N'R1
DR4	1'R2	2'R2	3'R2	…	N'R2
DR5	1'R3	2'R3	3'R3	…	N'R3
DR6	1'R4	2'R4	3'R4	…	N'R4
DR7	1'R5	2'R5	3'R5	…	N'R5
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1'G0	2'G0	3'G0	…	N'G0
DG3	1'G1	2'G1	3'G1	…	N'G1
DG4	1'G2	2'G2	3'G2	…	N'G2
DG5	1'G3	2'G3	3'G3	…	N'G3
DG6	1'G4	2'G4	3'G4	…	N'G4
DG7	1'G5	2'G5	3'G5	…	N'G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	1'B0	2'B0	3'B0	…	N'B0
DB3	1'B1	2'B1	3'B1	…	N'B1
DB4	1'B2	2'B2	3'B2	…	N'B2
DB5	1'B3	2'B3	3'B3	…	N'B3
DB6	1'B4	2'B4	3'B4	…	N'B4
DB7	1'B5	2'B5	3'B5	…	N'B5

Parallel RGB565					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	x	x	x	…	x
DR3	1'R0	2'R0	3'R0	…	N'R0
DR4	1'R1	2'R1	3'R1	…	N'R1
DR5	1'R2	2'R2	3'R2	…	N'R2
DR6	1'R3	2'R3	3'R3	…	N'R3
DR7	1'R4	2'R4	3'R4	…	N'R4
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1'G0	2'G0	3'G0	…	N'G0
DG3	1'G1	2'G1	3'G1	…	N'G1
DG4	1'G2	2'G2	3'G2	…	N'G2
DG5	1'G3	2'G3	3'G3	…	N'G3
DG6	1'G4	2'G4	3'G4	…	N'G4
DG7	1'G5	2'G5	3'G5	…	N'G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	x	x	x	…	x
DB3	1'B0	2'B0	3'B0	…	N'B0
DB4	1'B1	2'B1	3'B1	…	N'B1
DB5	1'B2	2'B2	3'B2	…	N'B2
DB6	1'B3	2'B3	3'B3	…	N'B3
DB7	1'B4	2'B4	3'B4	…	N'B4

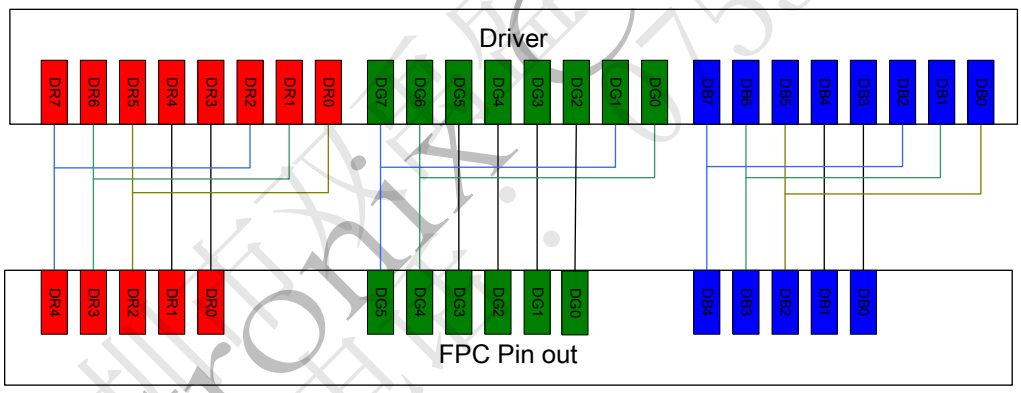
10.4.3 16.7M (R G B, 8 8 8) INPUT COLOR FORMAT



10.4.4 262K (R G B, 6 6 6) INPUT COLOR FORMAT



10.4.5 65K (R G B, 5 6 5) INPUT COLOR FORMAT



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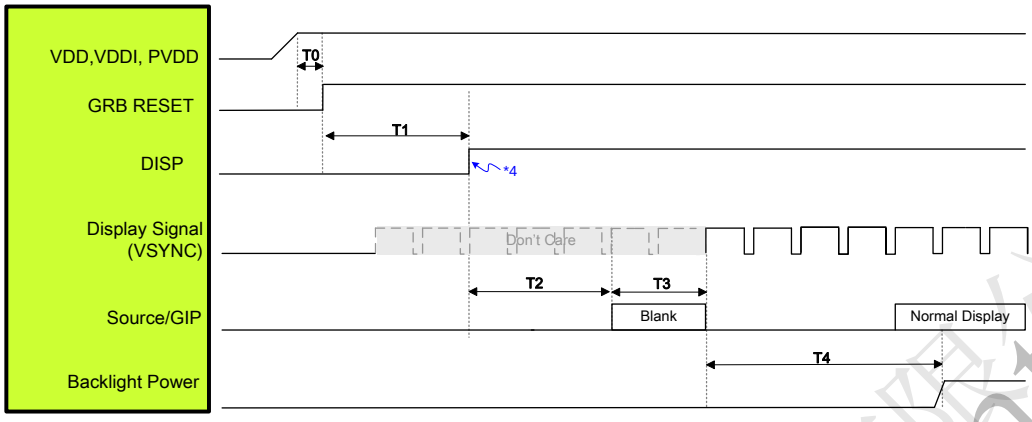
11. POWER ON/OFF SEQUENCE

11.1 Power On Sequence

11.1.1 1 Power Mode



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to DISP=“High”	≥10	ms
T2	DISP=“High” to Source/GIP scan blank	85	ms
T3	IC scan blanking signal	≥33	ms
T4	Display signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

4. When Display Signal is correct and stable(depends on system display data signal), wait for >1ms then DISP pulls high.

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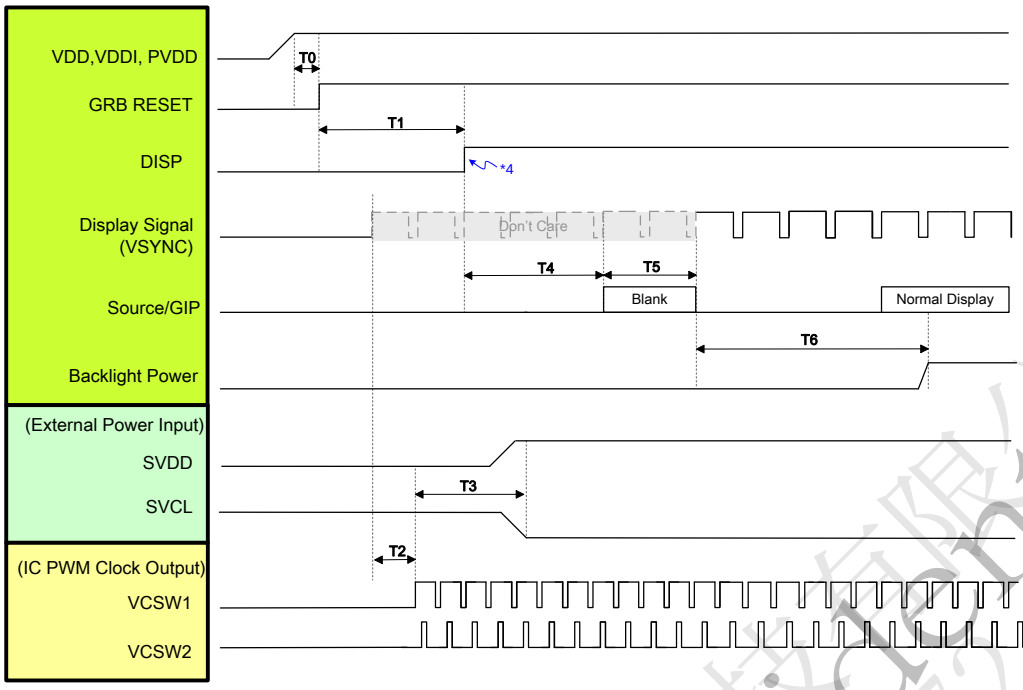
11.1.2 3 Power Mode with Charge Pump Controller



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to DISP= “High”	≥10	ms
T2	DISP=“High” to IC output PWM clock	1	ms
T3	PWM clock input to SVDD/SVCL stability	≤50	ms
T4	DISP=“High” to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

4. When Display Signal is correct and stable(depends on system display data signal), wait for >1ms then DISP pulls high.

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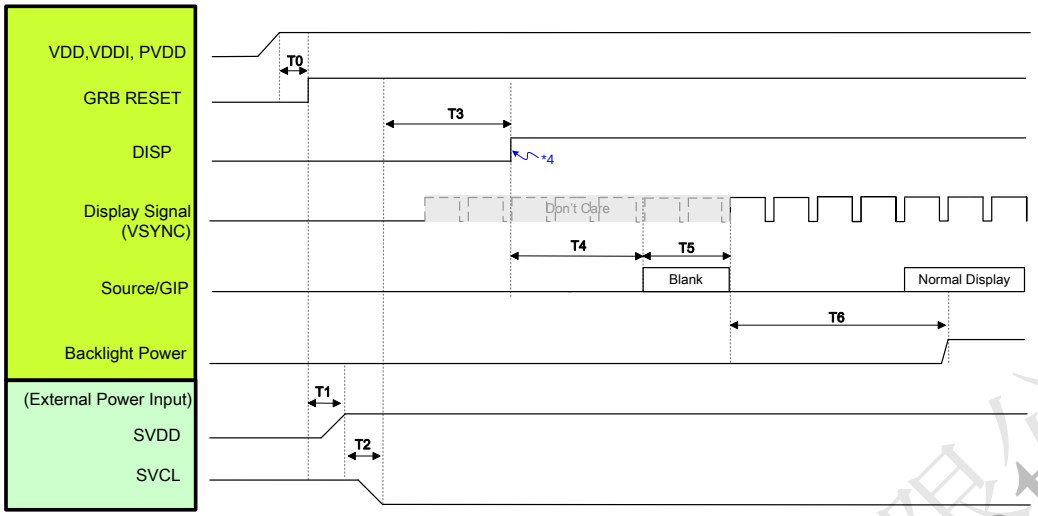
11.1.3 3 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to SVDD input	≥10	ms
T2	SVDD input to SVCL input	≥1	ms
T3	SVCL input to DISP=“High”	≥1	ms
T4	DISP=“High” to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

4. When Display Signal is correct and stable(depends on system display data signal), wait for >1ms then DISP pulls high.

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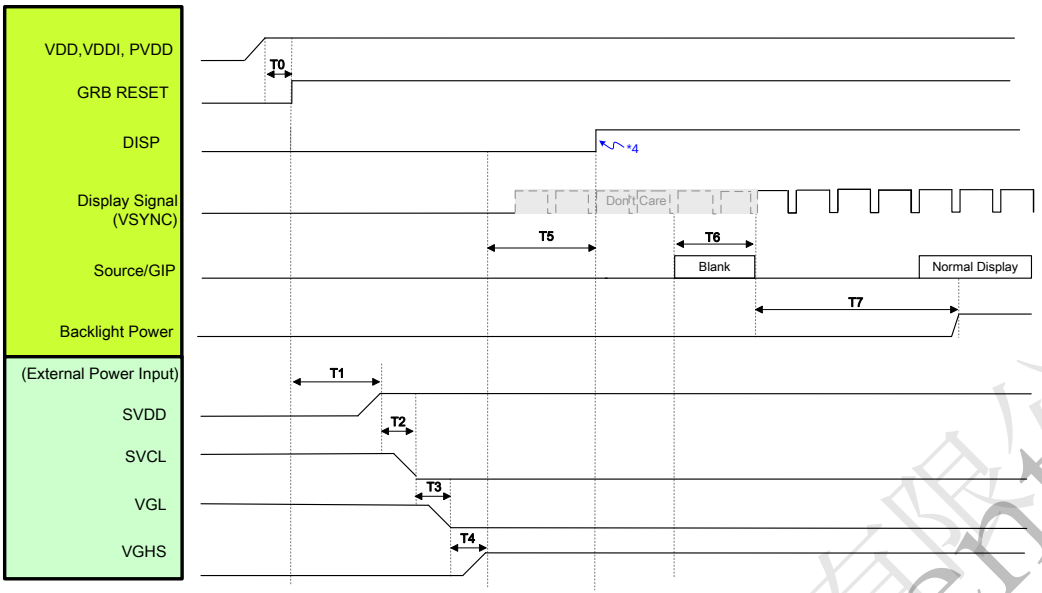
11.1.4 5 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to SVDD input	≥10	ms
T2	SVDD input to SVCL input	≥1	ms
T3	SVCL input to VGL input	≥1	ms
T4	VGL input to VGHS input	≥1	ms
T5	VGH Input to DISP=“High”	≥1	ms
T6	IC scan blanking signal	≥33	ms
T7	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

4. When Display Signal is correct and stable(depends on system display data signal), wait for >1ms then DISP pulls high.

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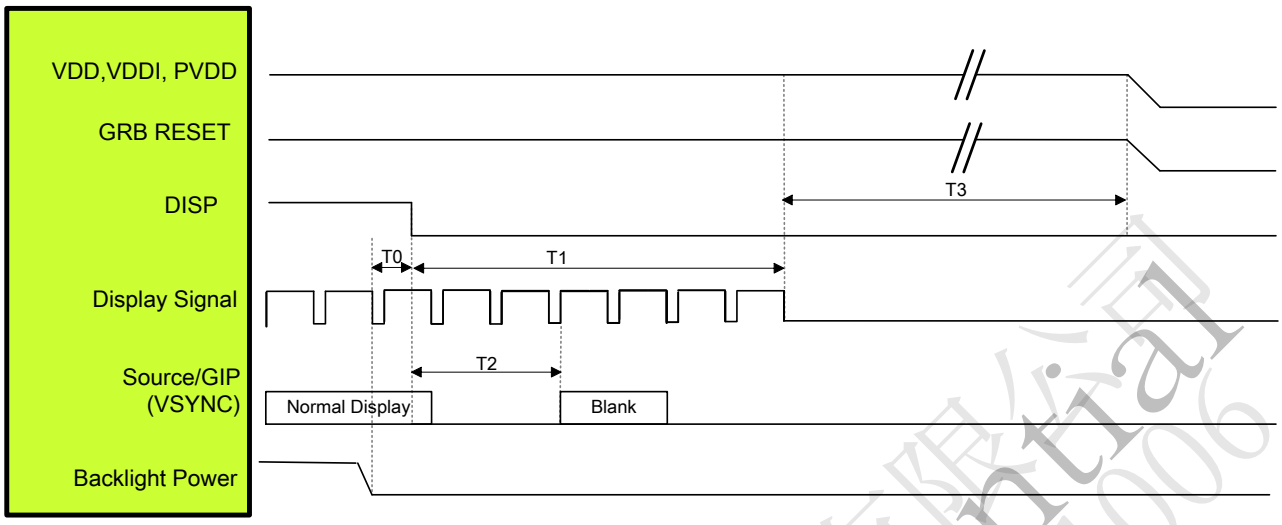
11.2 Power Off Sequence

11.2.1 1 Power Mode



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

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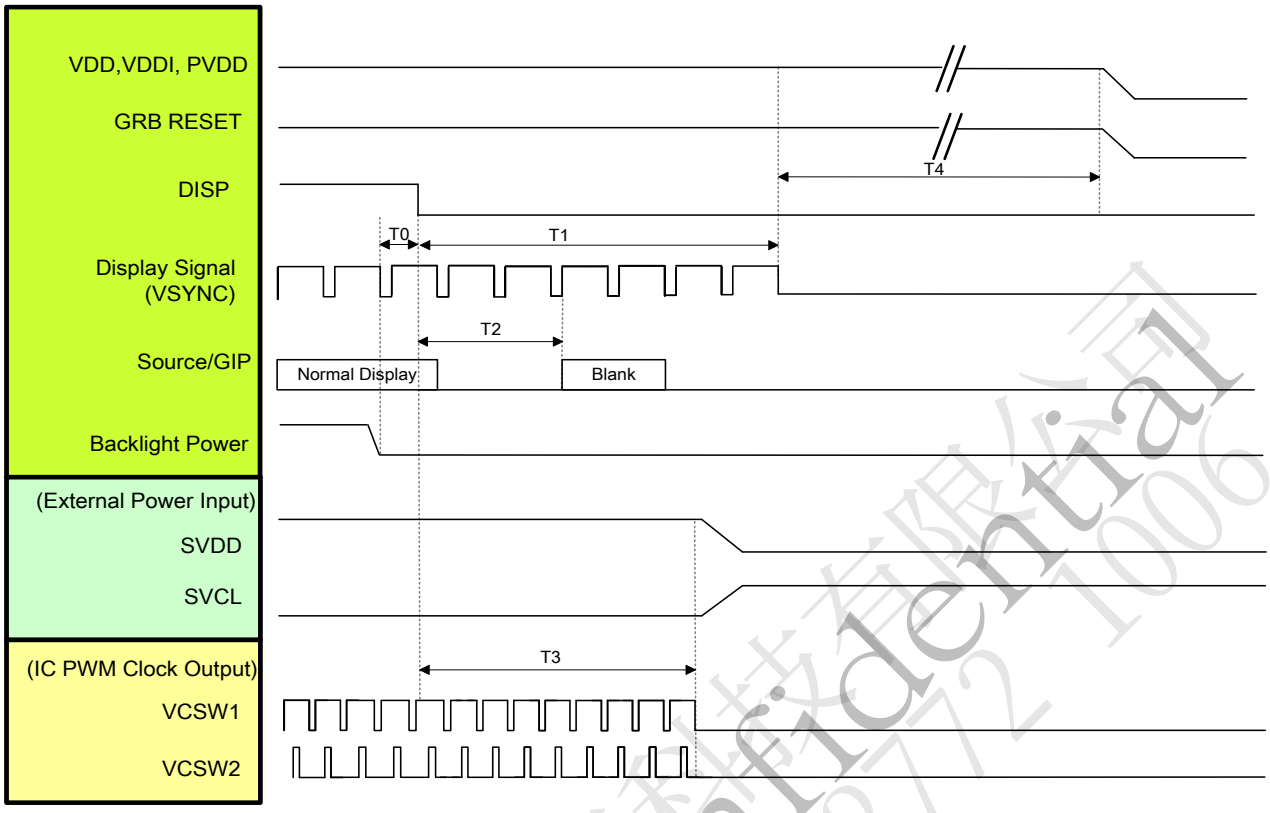
11.2.2 3 Power Mode with Charge Pump Controller



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to PWM clock stop (base on Display Signal Frame Rate 60Hz)	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

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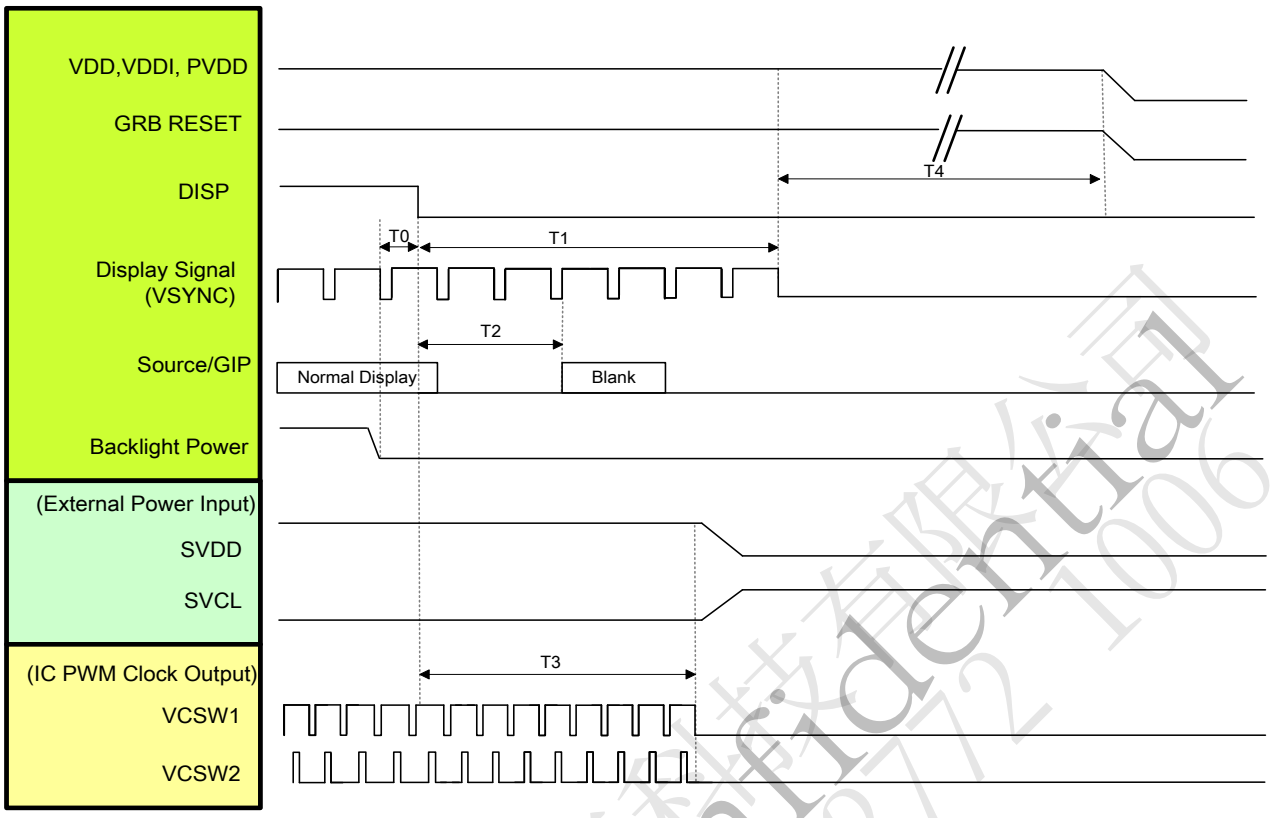
11.2.3 3 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to SVDD /SVCL Power off	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

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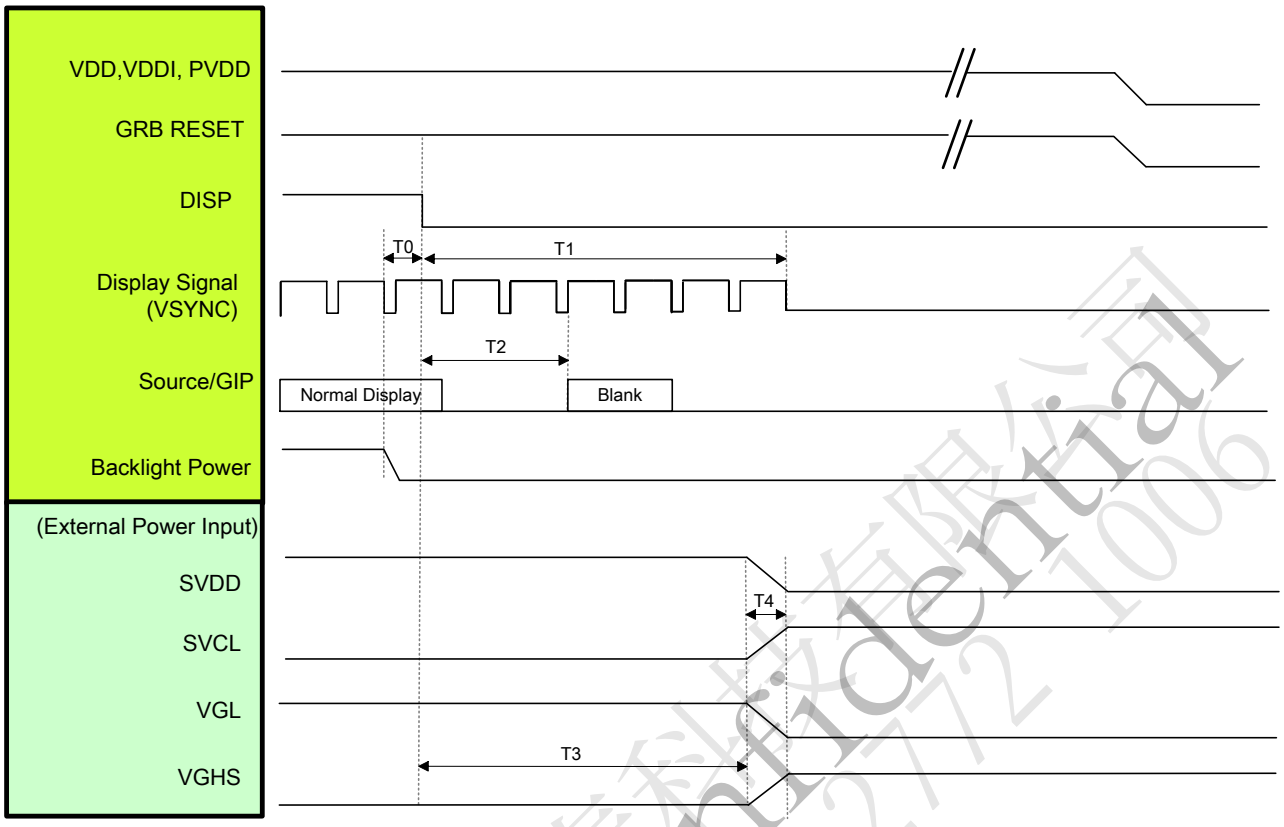
11.2.4 5 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to VGL /VGHS power off	≥85	ms
T4	VGL/VGHS power off to SVDD/SVCL power off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

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12. RECOMMENDED PANEL ROUTING RESISTANCE

The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

Pin Number	Pin Name	Unit: ohm
1	VDDI	<1
2	VDD	<1
3	VDD1	<1
4	PVDD	<1
5	DGND	<1
6	AGND	<1
7	SGND	<1
8	PGND	<1
9	C11P	<3
10	C11N	<3
11	C12P	<3
12	C12N	<3
13	SVCL	<3
14	SVDD	<3
15	VCOM	<3
16	VGH	<3
17	VGL	<3
18	GVDD	<50
19	GVCL	<50
20	VGSP	<50
21	VCC	<50
22	VCCM	<50
23	AVCL	<50
24	AVDD	<50
25	CS	<50
26	SDA	<50
27	SCL	<50
28	DISP	<50
29	GRB	<50
30	DCLKN	<50
31	DCLKP	<50

Pin Number	Pin Name	Unit: ohm
32	DR[7:0]	<50
33	DG[7:0]	<50
34	DB[7:0]	<50
35	DE	<50
36	VSYNC	<50
37	HSYNC	<50
38	CP	<50
39	CN	<50
40	DP0	<50
41	DN0	<50
42	DP1	<50
43	DN1	<50
44	AUTODL	<50
45	HDIR	<50
46	VDIR	<50
47	INTF	<50
48	VDPOL_LVDS_SEL	<50
49	HDPOL_LVDS_DSWAP	<50
50	DCLKPOL	<50
51	VPP	<50
52	BIST_EN	<50
53	LVDS_FMT	<50
54	EXT_S	<50
55	EXT_G	<50
56	SPI_ I^2C _SEL	<50
57	VCSW1	<50
58	VCSW2	<50
59	TESTI[4:0]	<50
60	DUMMY	<50

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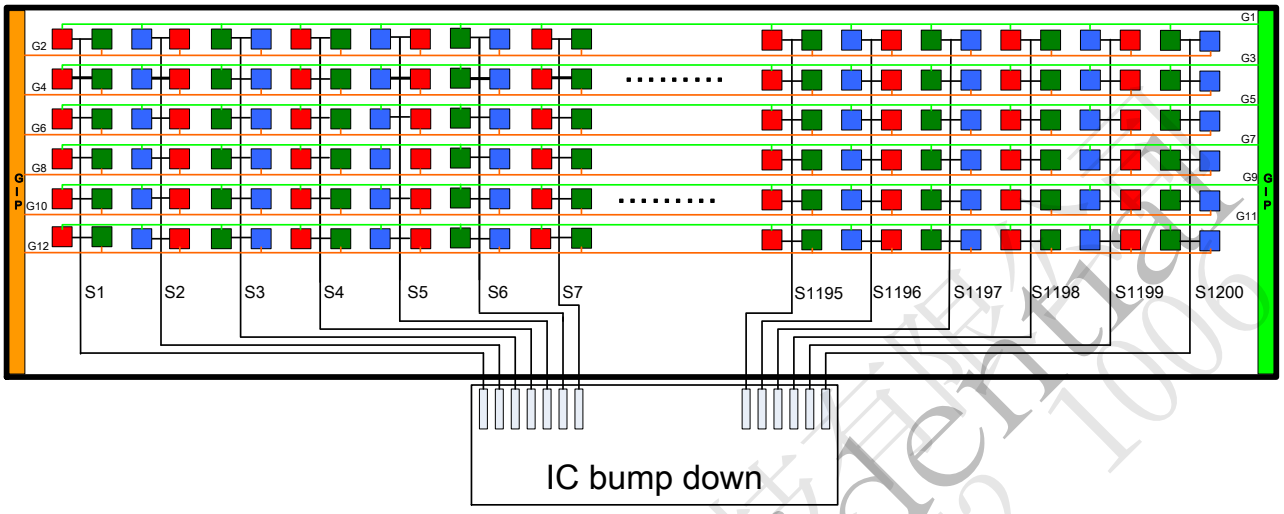
13. DISPLAY INVERSION TYPE

The IC supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.

13.1 2-dot inversion



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14. REVISION HISTORY

Revision	Description	Date
Preliminary V0.1	1st edition.	2026/07

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