DATA SHEET

凌陽科技
SUNPLUS

SPLC501C

132 x 65 Dot Matrix LCD Driver

JAN. 29, 2003

Version 1.5

Table of Contents

PAGE

132 x 65 DOT MATRIX LCD DRIVER

1. GENERAL DESCRIPTION

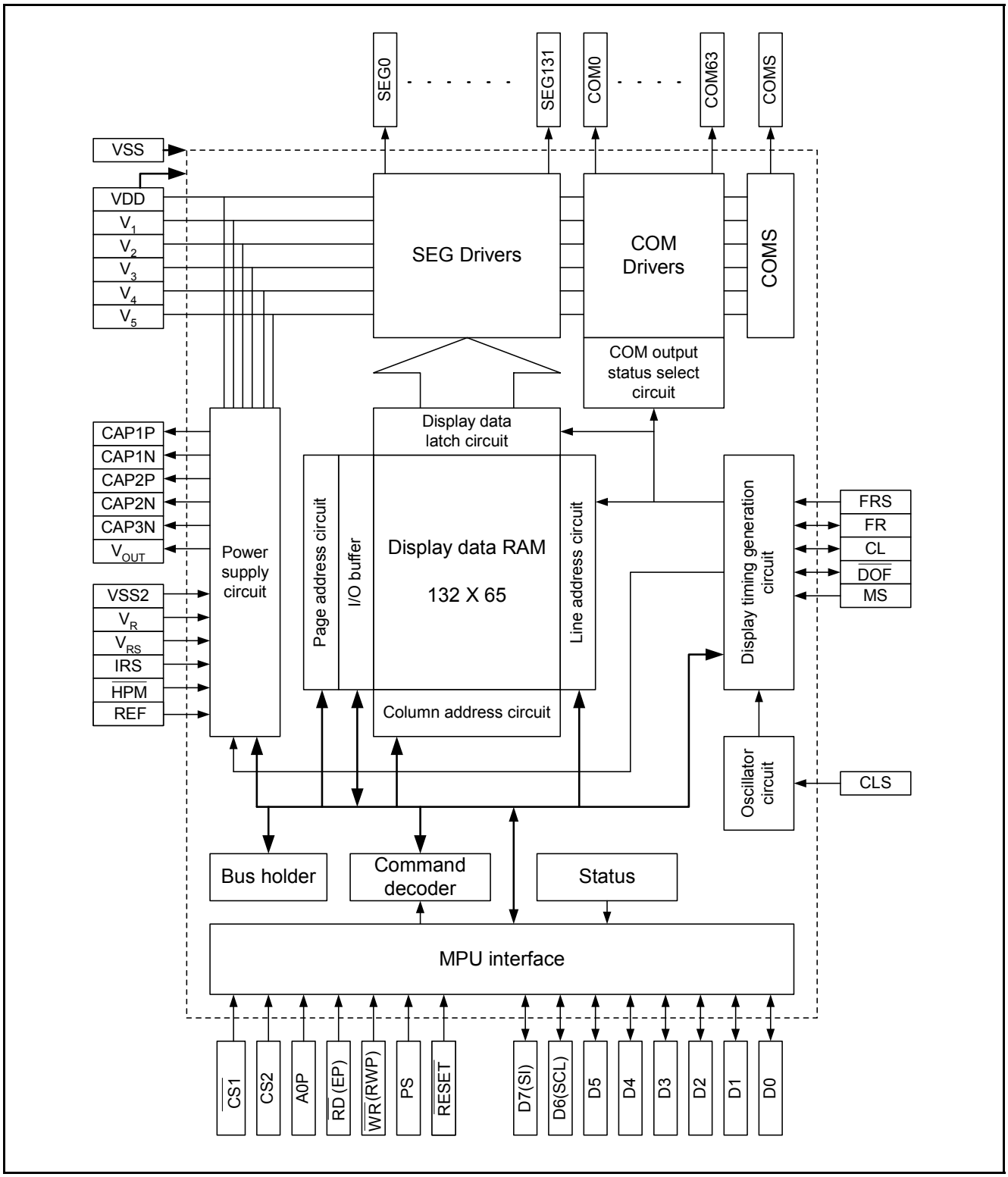
The SPLC501C, a single-chip dot matrix liquid crystal display drivers, is specially designed to connect directly with a microprocessor bus. The 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM. It generates a liquid crystal drive signal independent of the microprocessor. Since the SPLC501C contains a 65 X 132 bits of display data RAM, a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, it is able to enable displays with a high degree of flexibility. The SPLC501C contains 65 common output circuits, 132 segment output circuits and therefore, a single chip can drive a 65 X 132 dot display (capable of displaying 8 columns X 4 rows of a 16 X 16 dot kanji font). In addition, the capacity of the display can also be extended through the use of master/slave structures between chips. The chips can save a great amount of power because no external operating clock is required for the display data RAM to read and write operations. Since each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the SPLC501C can be used for creating the lowest power display system with the fewest components for high performance portable devices.

2. FEATURES

- Direct display of RAM data through the display data RAM.
  '1': Non-illuminated.
  '0': Illuminated.
- RAM capacity.
  65 X 132 = 8580 bits.
- Display driver circuits.
  SPLC501C: 65 common outputs and 132 segment outputs.
- Static drive circuit equipped internally for indicators.
  (1 system, with variable flashing speed.)
- These chips not designed for resistance to light or Resistance to radiation.
- High-speed 8-bit MPU interface (capability to be connected directly to the both the 80 X 86 series MPUs and the 68000 series MPUs)/Serial interface are supported.
- Wide range of operating temperatures.
- CMOS process
- CR oscillator circuit equipped internally
  (External clock can also be input).
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V_5 voltage regulation internal resistor ratio set.
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally).
  High-accuracy voltage adjustment circuit
  (Thermal gradient -0.05%/℃ or external input).
  V_5 voltage regulator resistors equipped internally,
  V_{4-1} voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- Driving Mode register provided for different size panel loading.
- Extremely low power consumption.
  Low operating power when the built-in power supply is used
- Power supply
  Operable on the low 2.4 voltage
  Logic power supply VDD - VSS = 2.4V to 5.5V
  Boost reference voltage: VDD - VSS2 = 2.4V to 6.0V
  Liquid crystal drive power supply: VDD - V_5 = 4.5V to 12V

Product Name	Duty	Bias	SEG Dr	COM Dr	VREG Temperature Gradient	Shipping Forms
SPLC501C	1/65	1/9, 1/7	132	65	-0.05%/℃	Bare Chip with Gold Bump

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

4.1. Power Supply PINs

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>12</td><td>P</td><td>VDD Shared with MPU power supply terminal VCC</td></tr>
<tr><td>VSS</td><td>11</td><td>P</td><td>0V terminal connected to the system GND.</td></tr>
<tr><td>VSS2</td><td>4</td><td>P</td><td>A reference power supply for the step-up voltage circuit for the liquid crystal drive</td></tr>
<tr><td>V_{RS}</td><td>1</td><td>P</td><td>The external-input V_{REG} power supply for the LCD power supply voltage regulator. These can only be enabled for the models with the V_{REG} external input option.</td></tr>
<tr><td>V_1, V_2, V_3, V_4, V_5</td><td>10</td><td>P</td><td>A multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.
VDD (= V_0) $\geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$
Master operation: When the power supply turns ON, the internal power supply circuits generate the V_1 to V_4 voltages shown below. The voltage settings are selected by the LCD bias command.
<table>
<tr><td></td><td colspan="2">SPLC501C</td></tr>
<tr><td>V_1</td><td>1/9 . V_5</td><td>1/7 . V_5</td></tr>
<tr><td>V_2</td><td>2/9 . V_5</td><td>2/7 . V_5</td></tr>
<tr><td>V_3</td><td>7/9 . V_5</td><td>5/7 . V_5</td></tr>
<tr><td>V_4</td><td>8/9 . V_5</td><td>6/7 . V_5</td></tr>
</table>
</td></tr>
</table>

P: Power Supply

4.2. LCD Power Supply Circuit Terminals

Mnemonic	PIN No.	Type	Description
CAP1P	2	O	DC/DC voltage converter. A capacitor is connected between this terminal and the CAP1N terminal.
CAP1N	2	O	DC/DC voltage converter. A capacitor is connected between this terminal and the CAP1P terminal.
CAP2P	2	O	DC/DC voltage converter. A capacitor is connected between this terminal and the CAP2N terminal.
CAP2N	2	O	DC/DC voltage converter. A capacitor is connected between this terminal and the CAP2P terminal.
CAP3N	2	O	DC/DC voltage converter. A capacitor is connected between this terminal and the CAP1P terminal.
V_{OUT}	3	O	DC/DC voltage converter. A capacitor is connected between this terminal and VSS.
V_R	2	I	Output voltage regulator terminal. Provides the voltage between VDD and V_5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = 'L'). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = 'H').

4.3. System Bus Connection Terminals

Mnemonic	PIN No.	Type	Description
DB7 - 0 (SI) (SCL)	8	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (PS = 'L'), DB7 serves as the serial data input terminal (SI) and DB6 serves as the serial clock input terminal (SCL). At the same time, DB5 - 0 are set to high impedance. When the chip select is inactive, DB0 to DB7 are set to high impedance.
A0P	1	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0P = 'H': Indicates DB7 - 0 is display data. A0P = 'L': Indicates DB7 - 0 is control data.
$\overline{\text{RESET}}$	1	I	When $\overline{\text{RESET}}$ is set to 'L', the settings are initialized. The $\overline{\text{RESET}}$ signal level performs the reset operation.
$\overline{\text{CS1}}$ CS2	2	I	This is the chip select signal. When $\overline{\text{CS1}}$ = 'L' and CS2 = 'H', the chip select becomes active, and data/command I/O is enabled.
$\overline{\text{RD}}$ (EP)	1	I	When connected to an 8080 MPU, this is LOW active. This pin is connected to the RD signal of the 8080 MPU, and the SPLC501C data bus is in an output status when this signal is 'L'. When connected to a 6800 Series MPU, this is HIGH active. This is the 68000 Series MPU enable clock input terminal.
$\overline{\text{WR}}$ (RWP)	1	I	When connected to an 8080 MPU, this is LOW active. This terminal connects to the 8080 MPU $\overline{\text{WR}}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{\text{WR}}$ signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When RWP = 'H': Read. When RWP = 'L': Write.
C86	1	I	This is the MPU interface switch terminal. C86 = 'H': 6800 Series MPU interface. C86 = 'L': 8080 MPU interface.
PS	1	I	This is the parallel data input/serial data input switch terminal. PS = 'H': Parallel data input. PS = 'L': Serial data input. The following applies depending on the PS status: PS / Data/Command / Data / Read/Write / Serial Clock 'H' / A0P / DB0 to DB7 / $\overline{\text{RD}}$, $\overline{\text{WR}}$ Write only / SCL (DB6) 'L' / A0P / SI(DB7) When PS = 'L', DB0 to DB5 are high impedance. DB0 to DB5 may be 'H', 'L' or Open. $\overline{\text{RD}}$ (EP) and $\overline{\text{WR}}$ (RWP) are fixed to either 'H' or 'L'. With serial data input, RAM display data reading is not supported.
CLS	1	I	Terminal to select whether to enable or disable the display clock internal oscillator circuit. CLS = 'H': Internal oscillator circuit is enabled. CLS = 'L': Internal oscillator circuit is disabled (requires external input). When CLS = 'L', input the display clock through the CL terminal.
FR	1	I/O	This is the liquid crystal alternating current signal I/O terminal. MS = 'H': Output MS = 'L': Input When the SPLC501C chip is used in master/slave mode, the various FR terminals must be connected.

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>MS</td><td>1</td><td>I</td><td>This terminal selects the master/slave operation for the SPLC501C chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
MS = ‘H’: Master operation
MS = ‘L’: Slave operation
The following is true depending on the MS and CLS status:
<table>
<tr><th>MS</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>$\overline{DOF}$</th></tr>
<tr><td>'H'</td><td>'H'</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td></td><td>'L'</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>'L'</td><td>'H'</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td></td><td>'L'</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the MS and CLS status.
<table>
<tr><th>MS</th><th>CLS</th><th>CL</th></tr>
<tr><td>'H'</td><td>'H'</td><td>Output</td></tr>
<tr><td></td><td>'L'</td><td>Input</td></tr>
<tr><td>'L'</td><td>'H'</td><td>Input</td></tr>
<tr><td></td><td>'L'</td><td>Input</td></tr>
</table>When the SPLC501C chips are used in master/slave mode, the various CL terminals must be connected.</td></tr>
<tr><td>$\overline{DOF}$</td><td>1</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
MS = ‘H’: Output
MS = ‘L’: Input
When the SPLC501C chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected.</td></tr>
<tr><td>FRS</td><td>1</td><td>O</td><td>This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td></tr>
<tr><td>IRS</td><td>1</td><td>O</td><td>This terminal selects the resistors for the V_5 voltage level adjustment.
IRS = ‘H’: Use the internal resistors.
IRS = ‘L’: Do not use the internal resistors.
The V_5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pin is enabled only when the master operation mode is selected. It is fixed to either ‘H’ or ‘L’ when the slave operation mode is selected.</td></tr>
<tr><td>$\overline{HPM}$</td><td>1</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{HPM}$ = ‘H’: Normal mode.
$\overline{HPM}$ = ‘L’: High power mode.
This pin is enabled only when the master operation mode is selected. It is fixed to either ‘H’ or ‘L’ when the slave operation mode is selected.</td></tr>
<tr><td>REF</td><td>1</td><td>I</td><td>This is the reference source select terminal for the power supply circuit for liquid crystal drive.
REF = “H”; external reference source from VRS terminal.
REF = “L”; internal reference source from SPLC501C terminal.
This pin is enable only when the master operation mode is selected. It is fixed to either “H” or “L” when the slave operation mode is selected.</td></tr>
</table>

4.4. Liquid Crystal Drive terminals

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG131 - 0</td><td>132</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from VDD, V_2, V_3, and V_5.
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>VDD</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>VDD</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>-</td><td colspan="2">VDD</td></tr>
</table></td></tr>
<tr><td>COM63 - 0</td><td>64</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>SPLC501C</td><td>COM63 -0</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VDD, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>VDD</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>-</td><td>VDD</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>2</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal. Leave these pins open if they are not used. When in master/slave mode, the same signal is output by both master and slave.</td></tr>
</table>

4.5. Test Terminals

Mnemonic	PIN No.	Type	Description
TEST	1	I	This is terminal for IC chip testing only.
TEST3, TEST4	2	I	These are terminals for IC chip testing only.
TEST5, TEST6	2	O	These are terminals for IC chip testing only.

5. FUNCTIONAL DESCRIPTIONS

5.1. The MPU Interface

5.1.1. Selecting the interface type

For SPLC501C, data transfers are accomplished through an 8-bit bi-directional data bus (DB7 - 0) or through a serial data input (SI). By selecting the PS terminal polarity to the 'H' or 'L', it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

PS	$\overline{CS1}$	CS2	A0P	$\overline{RD}$	$\overline{WR}$	C86	DB7	DB6	DB5 - 0
H: Parallel Input	$\overline{CS1}$	CS2	A0P	$\overline{RD}$	$\overline{WR}$	C86	DB7	DB6	DB5 - 0
L: Serial Input	$\overline{CS1}$	CS2	A0P	-	-	-	SI	SCL	(HiZ)

'-' indicates fixed to either 'H' or to 'L'

5.1.2. The parallel interface

When the parallel interface is selected (PS = 'H'), it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either 'H' or 'L'.

Table 2

C86	$\overline{CS1}$	CS2	A0P	$\overline{RD}$	$\overline{WR}$	DB7 - 0
H: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0P	EP	RWP	DB7 - 0
L: 8080 MPU Bus	$\overline{CS1}$	CS2	A0P	$\overline{RD}$	$\overline{WR}$	DB7 - 0

Data bus signals are recognized by a combination of A0P, $\overline{RD}$ (EP), $\overline{WR}$ (RWP) signals, shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0P	WRP	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read the display data
1	0	1	0	Write the display data
0	1	0	1	Read Status
0	0	1	0	Write control data (command)

5.1.3. The serial interface

When the serial interface is selected (PS = 'L') and when the chip is in active state ($\overline{CS1}$ = 'L' and CS2 = 'H'), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin at the rising edge of the serial clocks DB7, DB6 through DB0 in order. The data is converted to 8-bit parallel data at the rising edge of the eighth serial clock. The A0P input determines whether the serial data input is display data or command data; when A0P = 'H', the data is display data, and when A0P = 'L', the data is command data. The A0P input is read and used for detecting every 8th rising edge of the serial clock after the chip is active.

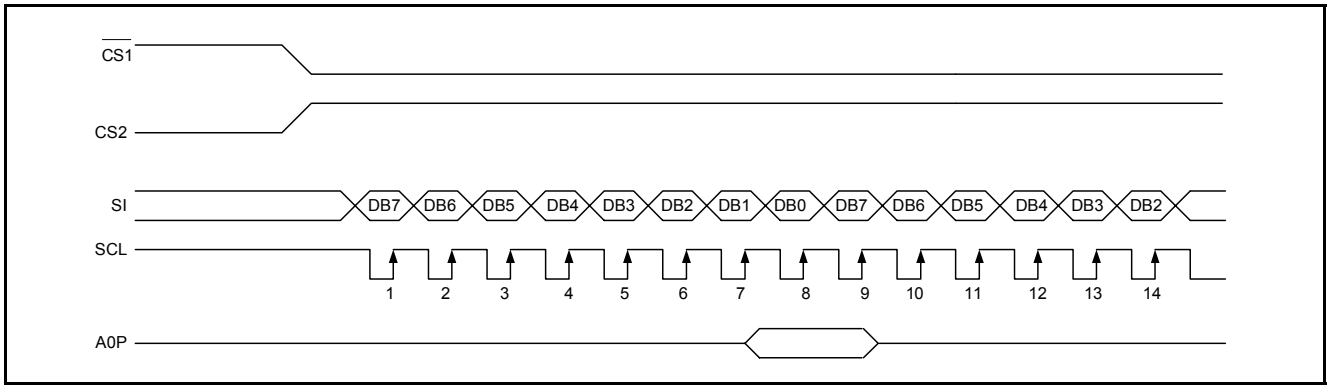


Figure 1: serial interface signal chart.

Note1: When the chip is not active, the shift registers and counter are reset to their initial states.
Note2: Reading is not acceptable in serial interface mode.
Note3: Caution is required on the SCL signal when it comes to line-end reflections and external noise. SUNPLUS recommends that operation should be rechecked on the actual equipment.

5.2. The Chip Select

The SPLC501C have two chip-select-terminals: $\overline{CS1}$ and CS2. The MPU interface or the serial interface is enabled only when $\overline{CS1}$ = 'L' and CS2 = 'H'.

When the chip select is inactive, DB7 - 0 enter into a high impedance state, and the A0P, $\overline{RD}$, and $\overline{WR}$ inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

5.3. Accessing the Display Data RAM and the Internal Registers

Data transferring at a high speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the SPLC501C. Wait time may not be considered. Also, in SPLC501C chips, each time data is sent from MPU. A type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. There is a certain restriction in the read sequence of the display data RAM. Note that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the addresses setup or write cycle operation is conducted. This relationship is shown in Figure 2.

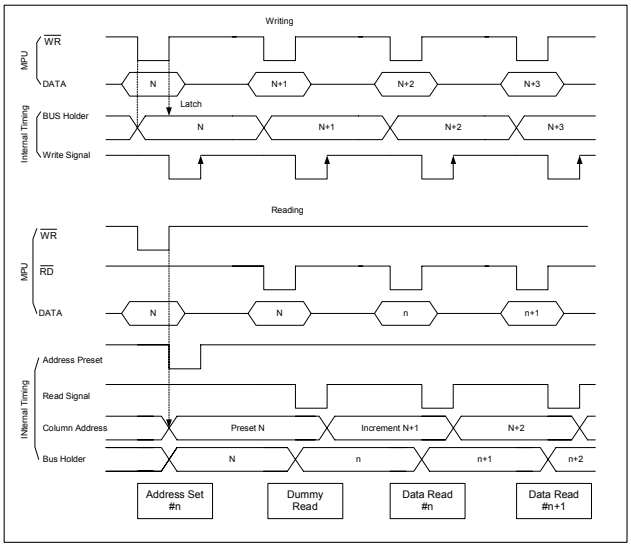


Figure2

5.4. The Busy Flag

When the busy flag is '1', it indicates that the SPLC501C is running internal processes. At this moment, no command aside from a status read will be received. The busy flag is outputted to DB7 pin with the read instruction. If the cycle time (t_{CYC}) is remained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

5.5. Display Data RAM

5.5.1. Display data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page x 8 bit +1) x 132-bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the DB7 - 0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple SPLC501C chips are used. Therefore, display structures can be created easily and with a high degree of freedom.

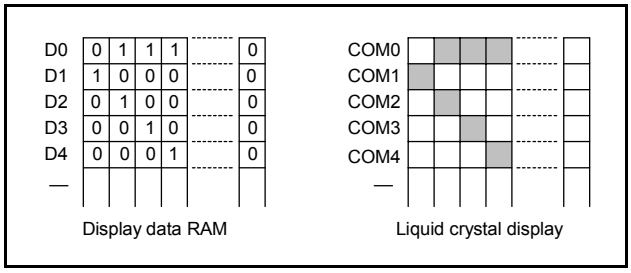


Figure 3

Moreover, reading from and writing to the display RAM in the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

5.5.2. The page address circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 (DB3, DB2, DB1, DB0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data DB0 is used.

5.5.3. The column addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column addresses stops with 83H. Because the column address depends on the page address, it is necessary to re-specify both the page address and the column address when moving, for example, from page 0 column 83H to page 1 column 00H. Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0 SEG131
ADC '0'	0 (H) → Column Address →83(H)
(DB0) '1'	83(H) ← Column Address ← 0(H)

5.5.4. The line address circuit

The line address circuit, as shown in Figure 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, which is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for SPLC501C when the common output mode is reversed. The display area is a 65-line area for the SPLC501C from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, …etc. can be performed.

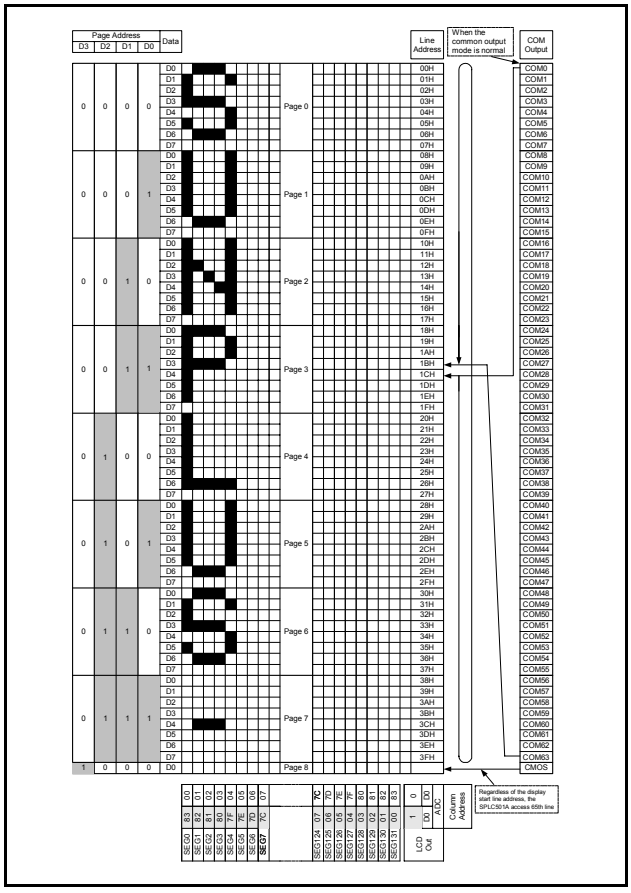


Figure 4

5.6. The Display Data Latch Circuit

The display data latch circuit temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

5.7. The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when MS = 'H' and CLS = 'H'. When CLS = 'L', the oscillation stops, and the display clock is input through the CL terminal.

5.8. The Common Output Status Select

In the SPLC501C chips, the COM output scan direction can be selected by the common output status select command (See Table 5.). Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 5

Status	COM Scan Direction
	SPLC501C
Normal	COM0→COM63
Reverse	COM63→COM0

5.9. Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display. Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive-wave form using a 2-frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive-wave form (SPLC501C)

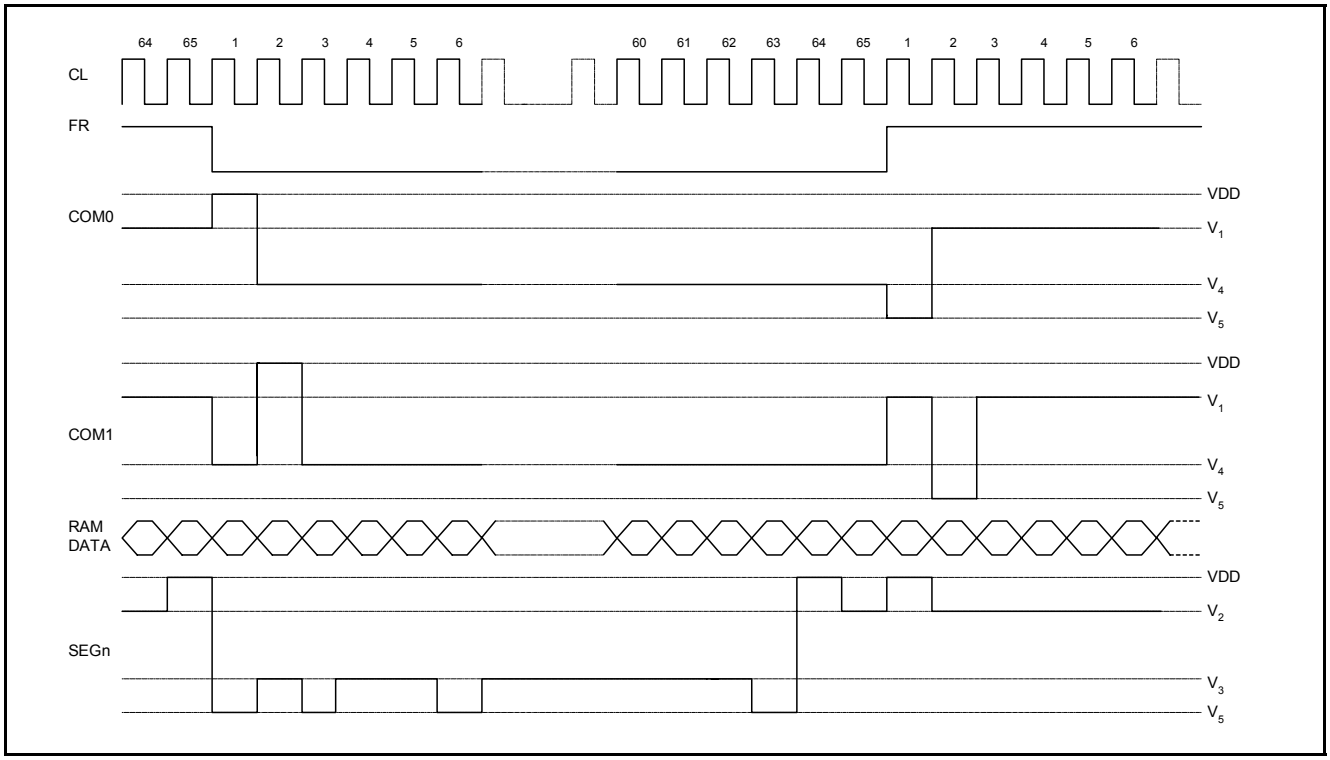


Figure 5

When multiple SPLC501C chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip(s). Table 6 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 6

Operating Mode	FR	CL	$\overline{DOF}$
Master (MS = 'H'):			
The internal oscillator circuit is enabled (CLS = 'H')	Output	Output	Output
The internal oscillator circuit is disabled (CLS = 'L')	Output	Input	Output
Slave (MS = 'L'):			
The internal oscillator circuit is enabled (CLS = 'H')	Input	Input	Input
The internal oscillator circuit is disabled (CLS = 'L')	Input	Input	Input

5.10. The Liquid Crystal Driver Circuits

These are a 197-channel (SPLC501C) that generates four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signals, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows examples of the SEG and COM output waveform.

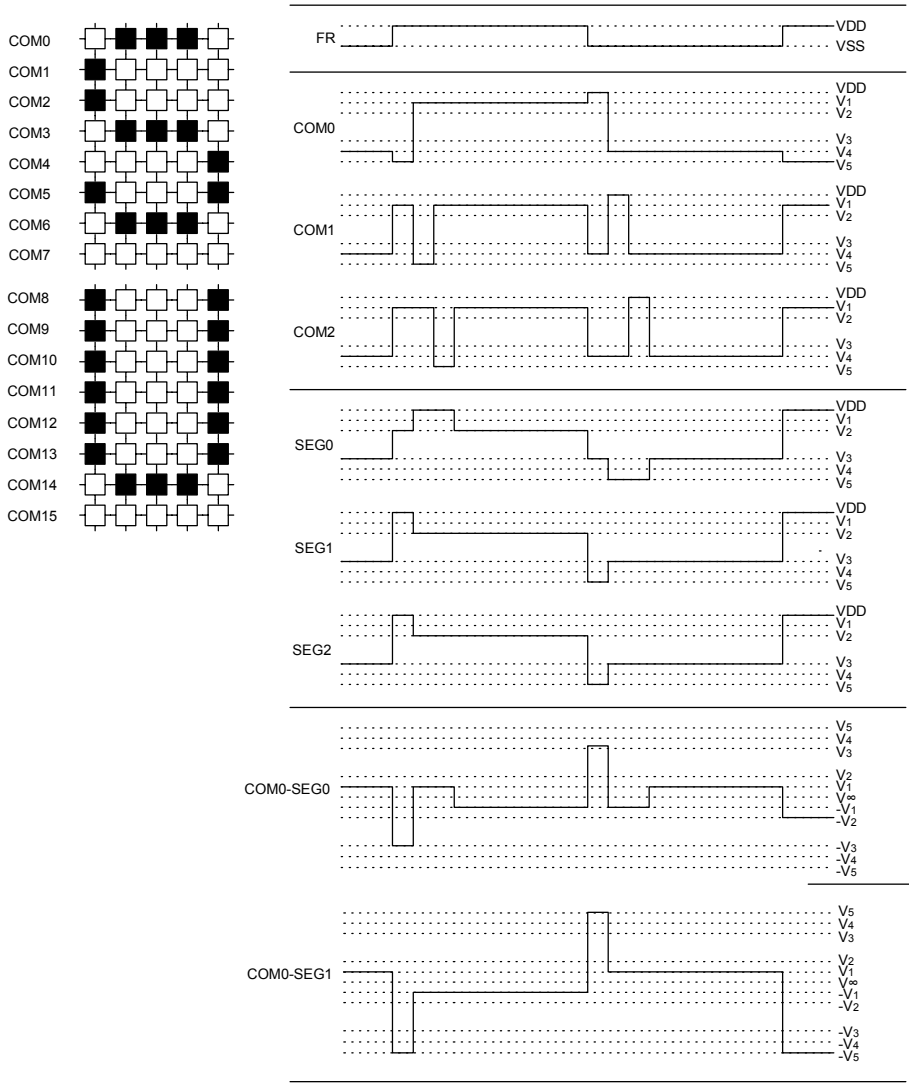


Figure 6

5.11. The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function in parallel. Table 7 shows the Power Control Set Command 3-bit data control functions, and Table 8 shows reference combinations.

Table 7 The Control Details of Each Bit of the Power Control Set Command

Item	Status	
	'1'	'0'
DB2 Booster circuit control bit	ON	OFF
DB1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
DB0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference Combinations

Use Settings	DB0	DB1	DB0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up Voltage SystemTerminal
Only the internal power supply is used	1	1	1	O	O	O	VSS2	Used
Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, VSS2	Open
Only the V/F circuit is used	0	0	1	X	X	O	V_5, VSS2	Open
Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

Note1: The 'step-up system terminals' refer CAP1P, CAP1N, CAP2P, CAP2N, and CAP3N.
Note2: While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

5.11.1. The step-up voltage circuits

Using the step-up voltage circuits equipped within the SPLC501C chips, it is possible to product a Quad step-up, a Triple step-up, and a Double step-up of the VDD - VSS2 voltage levels.

Quad step-up: Connect capacitor C1 between CAP1P and CAP1N, between CAP2P and CAP2N, between CAP1P and CAP3N, and between VSS2 and VOUT, to produce a voltage level in the negative direction at the VOUT terminal that is 4 times the voltage level between VDD and VSS2.

Triple step-up: Connect capacitor C1 between CAP1P and CAP1N, between CAP2P and CAP2N and between VSS2 and VOUT, and short between CAP3N and VOUT to produce a voltage level in the negative direction at the VOUT terminal that is 3 times the voltage difference between VDD and VSS2.

Double step-up: Connect capacitor C1 between CAP1P and CAP1N, and between VSS2 and VOUT, leave CAP2P open, and short between CAP2N, CAP3N and VOUT to produce a voltage in the negative direction at the VOUT terminal that is twice the voltage between VDD and VSS2.

The step-up voltage relationships are shown in Figure 7.

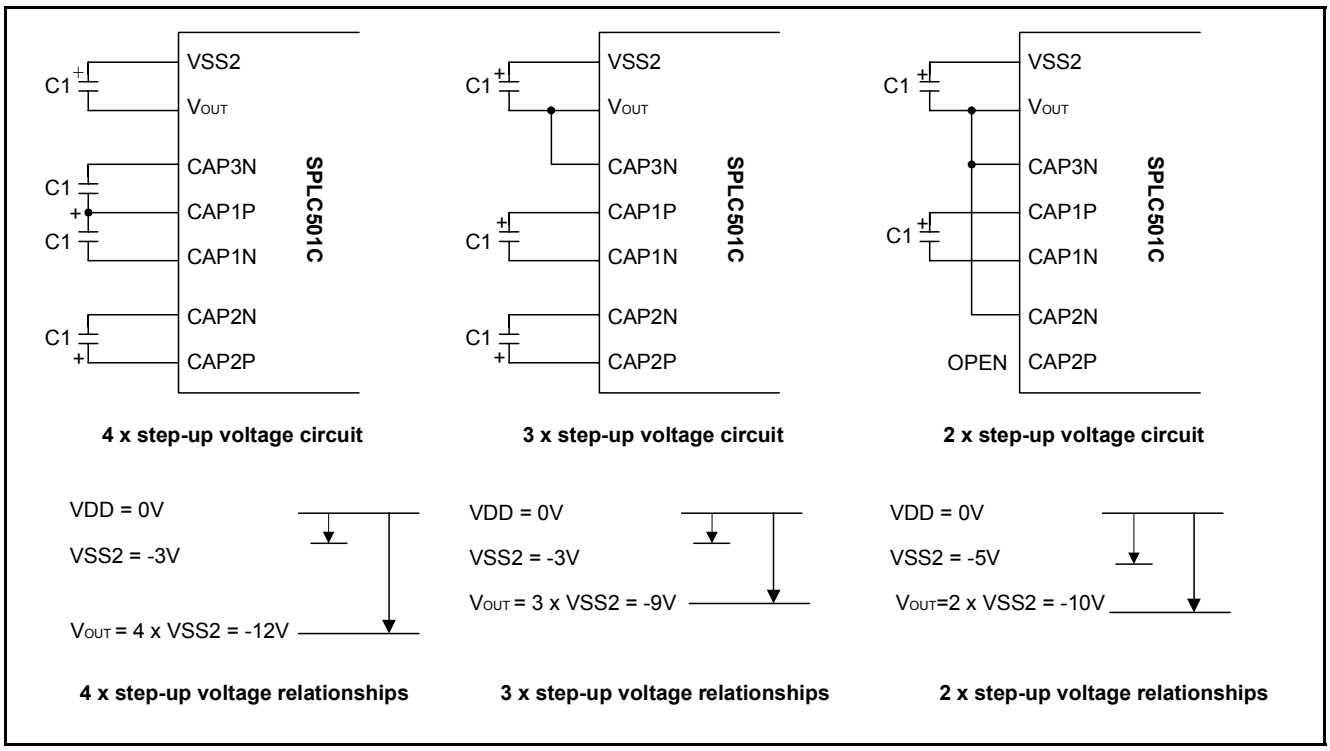


Figure 7

Note: The VSS2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rate.

5.11.2. The voltage regulator circuit

The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit. Because the SPLC501C chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. Moreover, in the SPLC501C, two types of thermal gradients have been prepared as V_{REG} options: (1) approximately -0.05%/℃ and (2) external input (supplied to the VRS terminal).

5.11.2.1. When the V_5 voltage regulator internal resistors are used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function, the liquid crystal power supply voltage, V_5, can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left\{1+\frac{Rb}{Ra}\right\} \bullet V_{EN}$$

$$= \left\{1+\frac{Rb}{Ra}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet V_{REG}$$

$$\left[\because V_{EN} = (1-\alpha/162) \bullet V_{REG}\right] \qquad \text{Equation A-1}$$

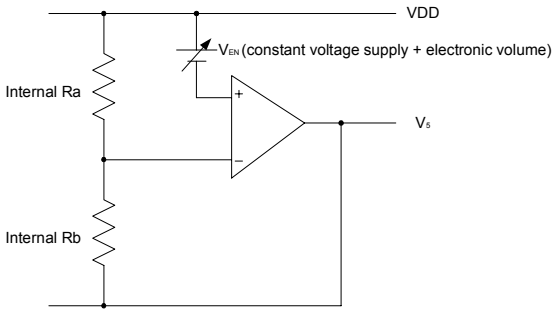


Figure 8

V_{REG} is the IC-internal fixed voltage supply, and its voltage at T_A = 25℃ is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
(1) Internal Power Supply	-0.05	[%/℃]	-2.1	[V]
(2) External Input	-	-	VRS	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for depending on the electronic volume register settings.

Table 10

DB5	DB4	DB3	DB2	DB1	DB0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
:	:	:	:	:	:	:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V_5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V_5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V_5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			SPLC501C Equipment Type by Thermal Gradient [Units: %/℃]	
DB2	DB1	DB0	(1) -0.05	(2) VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

5.11.2.2. When an external resistance is used (i.e., The V_5 Voltage Regulator Internal Resistors are not used) (1)

The liquid crystal power supply voltage V_5 can also be set without using the V_5 voltage regulator internal resistors (IRS terminal = 'L') by adding resistors Ra' and Rb' between VDD and VR, and between VR and V_5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where $|V_5| < |V_{OUT}|$, the V_5 voltage can be calculated using equation B-1 based on the external resistance, Ra' and Rb'.

$$V_5 = \left\{1+\frac{Rb'}{Ra'}\right\} \bullet V_{EN}$$

$$= \left\{1+\frac{Rb'}{Ra'}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet V_{REG}$$

$$\left[\because V_{EN} = (1-\alpha/162) \bullet V_{REG}\right] \qquad \text{Equation B-1}$$

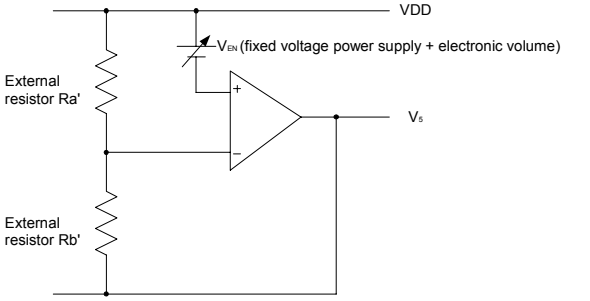


Figure 9

Setup example: When selecting T_A = 25℃ and V_5 = -7.0V for an SPLC501C model where the temperature gradient = -0.05%/℃. When the central value of the electron volume register is (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = -2.1V. According to equation B-1:

$$V_5 = \left\{1+\frac{Rb'}{Ra'}\right\} \bullet V_{EN}$$

$$-7.0V = \left\{1+\frac{Rb'}{Ra'}\right\} \bullet \left\{1-\frac{\alpha}{162}\right\} \bullet (-2.1) \qquad \text{Equation B-2}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{Equation B-3}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V_5 voltage variable range and notch width, based on the electron volume function, is as given in Table 12.

Table 12

V_5	Min.	Typ.	Max.	Units
Variable Range	-8.6 (63 levels)	-7.0 (central value)	-5.3 (0 level)	[V]
Notch width	-	52	-	[mV]

5.11.2.3. When external resistors are used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments ($\triangle$R2).

$$V_5 = \left\{1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right\} \bullet V_{EN}$$

$$= \left\{1 + \frac{R_3 + R_2 + \Delta R_2}{R_1 + \Delta R_2}\right\} \bullet \left\{1 - \frac{\alpha}{162}\right\} \bullet (V_{REG})$$

$$\left[\because V_{EN} = (1 - \alpha/162) \bullet V_{REG}\right] \qquad \text{Equation C-1}$$

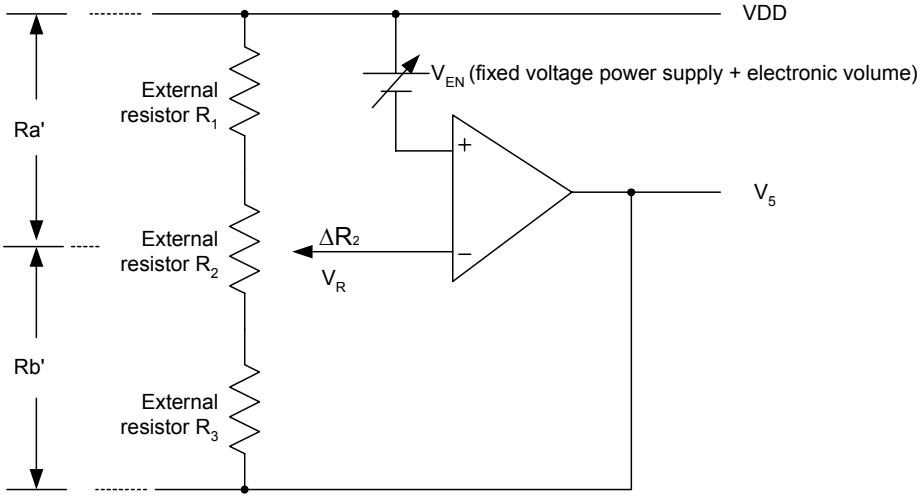


Figure 10

Setup example: When selecting T_A = 25℃ and V_5 = -5.0V to -9.0V (using R2) for an SPLC501C model where the temperature gradient = -0.05%/℃.

When the central value for the electronic volume register is set at (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0),

α = 31
V_{REG} = -2.1V

so, according to equation C-1, when △R2 = 0Ω , in order to make V_5 = -9.0V,

$$-9.0V = \left\{1+\frac{R_3+R_2}{R_1}\right\} \bullet \left\{1-\frac{31}{162}\right\} \bullet (-2.1) \qquad \text{Equation C-2}$$

When △R2 = R2, in order to make V = -5.0V,

$$-5.0V = \left\{1+\frac{R_3}{R_1+R2}\right\} \bullet \left\{1-\frac{31}{162}\right\} \bullet (-2.1) \qquad \text{Equation C-3}$$

Moreover, when the current flowing VDD and V_5 is set to 5μA,

R1 + R2 + R3 = 1.4MΩ Equation C-4

With this, according to equation C-2, C-3 and C-4,

R1 = 264kΩ
R2 = 211kΩ
R3 = 925kΩ

At this time, the V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 13.

Table 13

V_5	Min.	Typ.	Max.	Units
Variable Range	-8.6 (63 levels)	-7.0 (central value)	-5.3 (0 level)	[V]
Notch width	-	53	-	[mV]

Note1: When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.

Note2: The VR terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = 'L'). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = 'H'), the VR terminal is left open.

Note3: Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

5.11.3. The liquid crystal voltage generator circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for SPLC501C can be selected.

5.12. High Power Mode

The power supply circuit equipped in the SPLC501C chips has very low power consumption (normal mode: $\overline{HPM}$ = 'H'). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to 'L' (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, it is necessary to add a liquid crystal drive power supply externally.

5.13. The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 11 is recommended for shutting down the internal power supply. First place the power supply in power saver mode and then turn the power supply OFF.

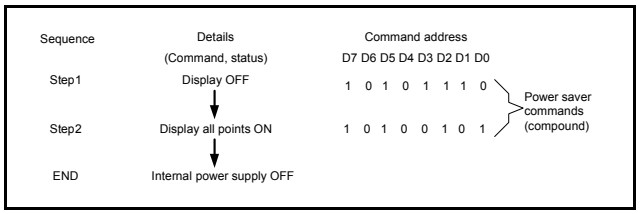


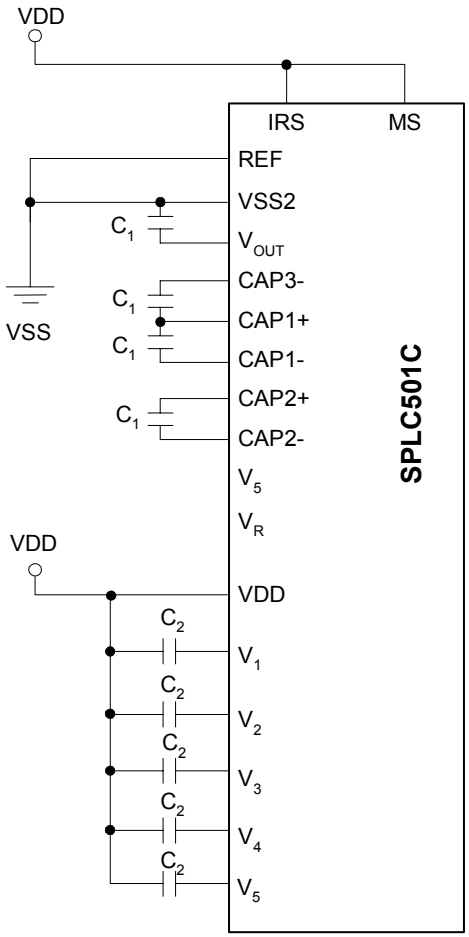
Figure 11

5.14. Reference Circuit Examples

Figure 12 shows reference circuit examples.

5.14.1.1. When using all of the step-up circuit, voltage regulating circuit and V/F circuit

A. When the voltage regulator internal resistor is used.
Example where VSS2 = VSS, with 4x step-up



B. When the voltage regulator internal resistor is not used.
Example where VSS2 = VSS, with 4x step-up

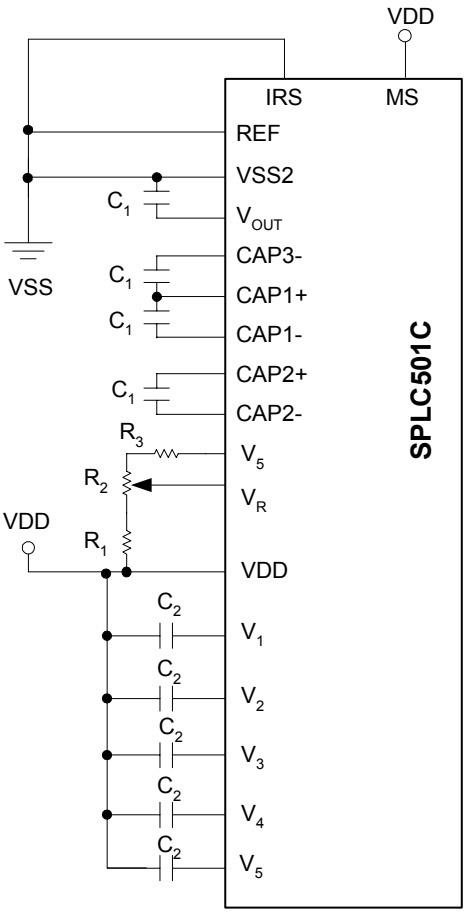
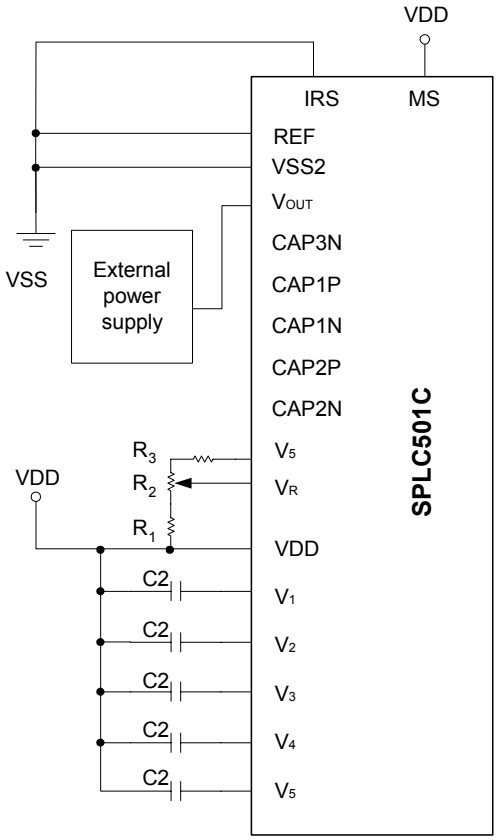


Figure 12

5.14.1.2. When the voltage regulator circuit and V/F circuit alone are used

A. When the V_5 voltage regulator internal resistor is not used.



B. When the voltage regulator internal resistor is used.

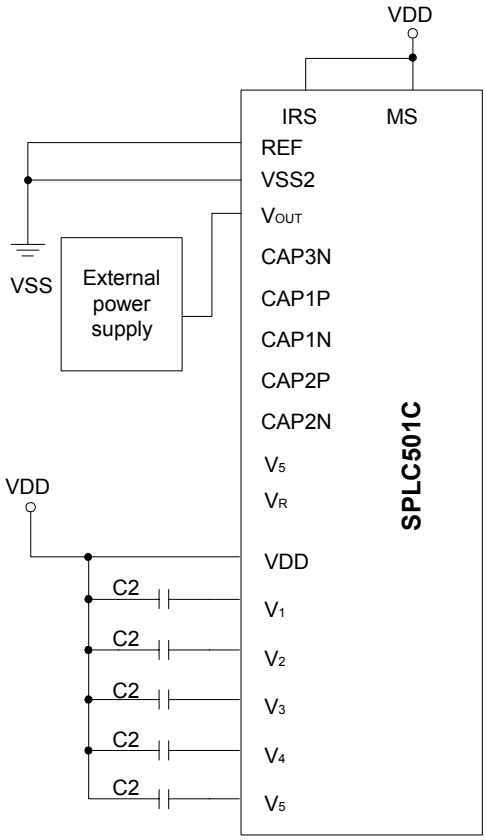
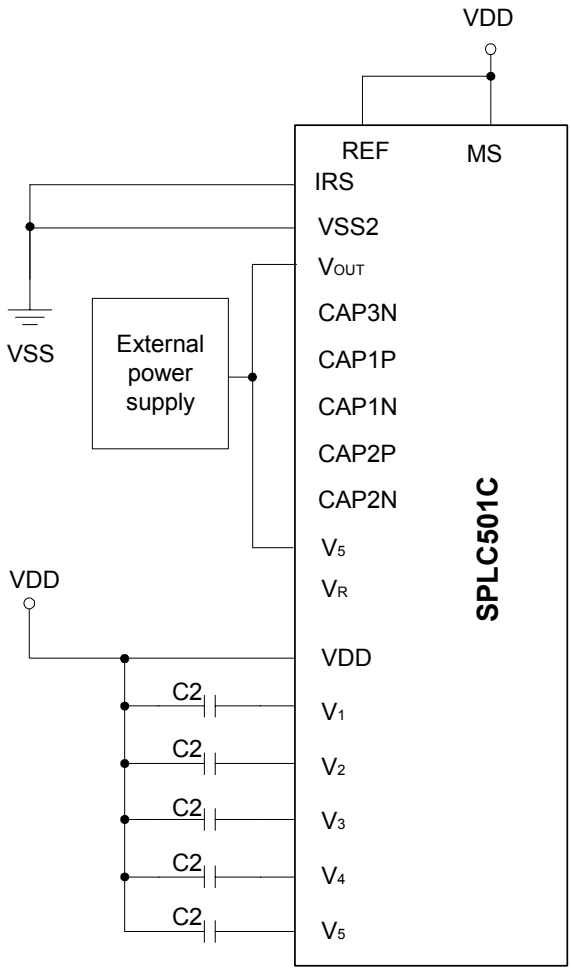


Figure 13

C. When the V/F circuit alone are used.



D. When the built-in power is not used.

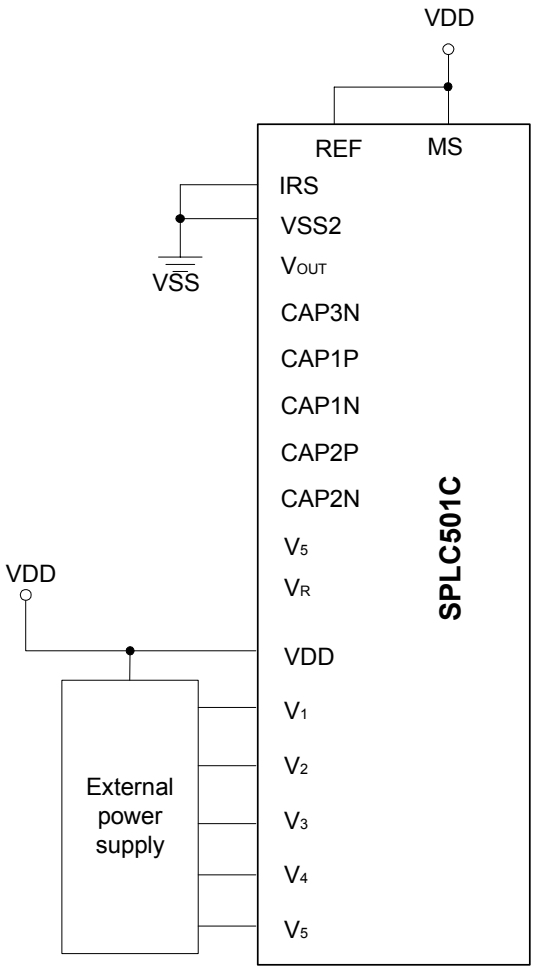


Figure 14

5.15. The Reset Circuit

When the $\overline{\text{RESET}}$ input comes to the 'L' level, these LSIs return to the default state. Their default states are as follows:

1). Display OFF
2). Normal display
3). ADC select: Normal (ADC command DB0 = 'L')
4). Power control register: (DB2, DB1, DB0) = (0, 0, 0)
5). Serial interface internal register data clear
6). LCD power supply bias rate:
SPLC501C.....1/9 bias
7). All-indicator lamps-on OFF (All-indicator lamps ON/OFF command DB0 = 'L')
8). Power saving clear
9). V_5 voltage regulator internal resistors, Ra and Rb, are connected.
10). Output conditions of SEG and COM terminals
SEG: VDD, COM: VDD
11). Read modify write OFF
12). Static indicator OFF
Static indicator register: (DB1, DB2) = (0, 0)
13). Display start line set to first line
14). Column address set to Address 0
15). Page address set to Page 0
16). Common output status normal
17). V5 voltage regulator internal resistor ratio set mode clear
18). Electronic volume register set mode clear
Electronic volume register: (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0. 0, 0, 0, 0)
19). Test mode clear
20). Driving mode register: (DB7, DB6)=(0, 0)

On the other hand, when the reset command is used, only above default settings from 11 to 19 are executed. When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the $\overline{\text{RESET}}$ terminal. After the initialization, each input terminal should be controlled normally. Moreover, when the control signal from the MPU is in the high impedance, an over-current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state. If the internal liquid crystal power supply circuit is not used on SPLC501C, it is necessary that $\overline{\text{RESET}}$ is 'H' when the external liquid crystal power supply is turned on. This IC has the function to discharge V_5 when $\overline{\text{RESET}}$ is 'L,' and the external power supply short-circuits to VDD when $\overline{\text{RESET}}$ is 'L.'. While $\overline{\text{RESET}}$ is 'L,' the oscillator and the display timing generator stop, and the CL, FR, FRS and $\overline{\text{DOF}}$ terminals are fixed to 'H'. The terminals DB7 - 0 are not affected. The VDD level is output from the SEG and COM output terminals. It means that an internal resistor is connected between VDD and V_5. When the internal liquid crystal power supply circuit is not used on other models of SPLC501C, it is necessary that $\overline{\text{RESET}}$ is 'L' when the external liquid crystal power supply is turned on. While $\overline{\text{RESET}}$ is 'L,' the oscillator works, but the display timing generator stops, and the CL, FR, FRS and $\overline{\text{DOF}}$ terminals are fixed to 'H'. The terminals DB7 - 0 are not affected.

6. COMMANDS

The SPLC501C chips identify the data bus signals by a combination of A0P, $\overline{\text{RD}}$ (EP), $\overline{\text{WR}}$ (RWP) signals. Command interpretation and execution do not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{\text{RD}}$ terminal for reading, and inputting a low pulse to the $\overline{\text{WR}}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when a 'H' signal is input to the RWP terminal. It is placed in a write mode when a 'L' signal is input to the RWP terminal. Then, the command is launched by inputting a high pulse to the EP terminal (See '10. Timing Characteristics' regarding the timing). Consequently, the 6800 Series MPU interface is different from the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read $\overline{\text{RD}}$ (EP) becomes '1(H)'. In the explanations below, the commands are explained using the 8080 Series MPU interface as the example. When the serial interface is selected, the data is inputted in the sequence starting from DB7.

<Explanation of Commands>

6.1. Display ON/OFF

This command turns the display ON and OFF.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed and when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

6.2. Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details, see the explanation of this function in 'The Line Address Circuit'.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Line Address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

6.3. Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the page address circuit in the Function Description (page 12) for the detail.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

6.4. Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically incremented (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in 'The Column Address Circuit' for details.

	A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A7	A6	A5	A4	A3	A2	A1	A0	Column Address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	0	0	130
												1	0	0	0	0	0	1	1	131

6.5. Status Read

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	BUSY	ADC	ON/OFF	$\overline{RESET}$	0	0	0	0

BUSY	When BUSY = '1', it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = '0', if the cycle time can be satisfied, there is no need to check for BUSY condition.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n⇔SEG n) 1: Normal (column address n⇔SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
$\overline{RESET}$	This indicates that the chip is in the process of initialization either because of a $\overline{RESET}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

6.6. Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by one after the write, the MPU can write the display data.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	Write data							

6.7. Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by one after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address being set. See the function explanation in “Display Data RAM” for the explanation of accessing the internal registers. When the serial interface is used, reading the display data becomes unavailable.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Read Data							

6.8. ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (page 12) for the detail. Increment of the column address (by ‘1’) accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

6.9. Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done, the display data RAM contents are maintained.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data ‘H’ LCD ON voltage (normal
										1	RAM Data ‘L’ LCD ON voltage (reverse)

6.10. Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For more details, see the Power Save Section.

6.11. LCD Bias Set

This command selects the voltage bias ratio for the liquid crystal display.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Select Status SPLC501C
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

6.12. Read/Modify/Write

This command is used paired with the 'END' command. Once this command has been inputted, the display data read command does not change the column address, but only the display data write command increment (+1) the column address. This mode remains until the END command is inputted. When the END command is inputted, the column address returns to the address at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there is repeating data changes in a specified display region, such as when there is a blanking cursor.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	0	0

Note: Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.

6.12.1. The sequence for cursor display

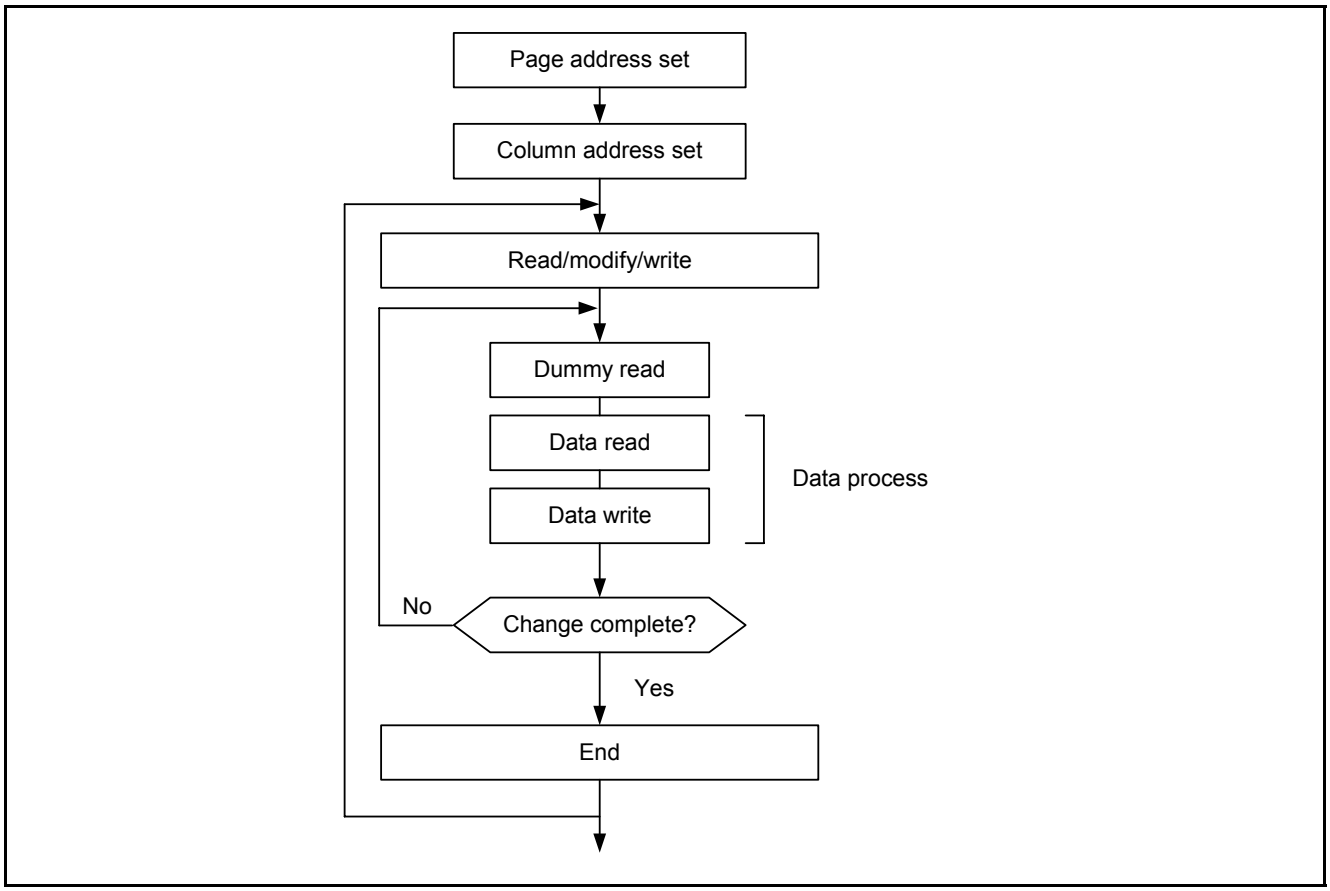


Figure 15

6.13. END

This command releases the read / modify / write mode, and returns the column address to the address at when the mode was entered.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	1	1	1	0

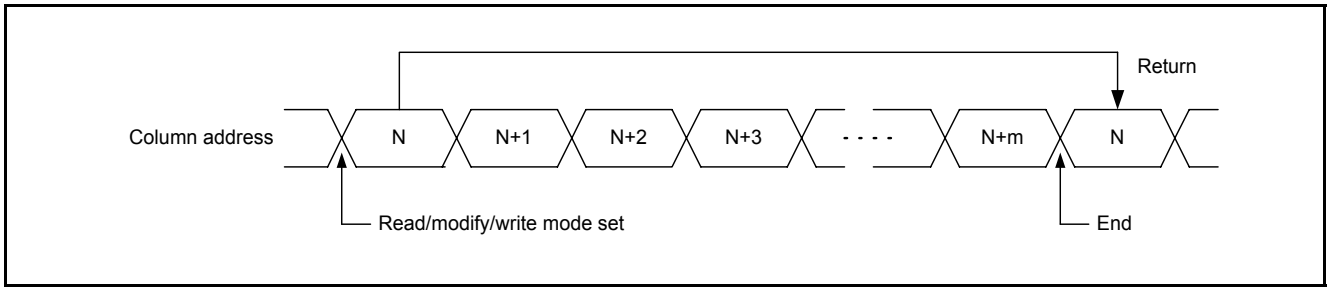


Figure 16

6.14. RESET

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details. The reset operation is performed after the reset command is entered.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	0

The initialization must be done through applying a reset signal to the $\overline{RESET}$ terminal when the power supply is applied.

6.15. Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit”.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Select Status SPLC501C	
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0 --> COM63
							1				Reverse	COM63 --> COM0

Note: *Disabled bit

6.16. Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit” for more details.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit :OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

Note: Display off command masks the power control circuits

6.17. V_5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the function explanation in "The Power Supply Circuits".

A0P	EP / RD	RWP / WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Setting
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

6.18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V_5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two bytes command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

6.18.1. The electronic volume mode set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, the electronic volume mode is released.

A0P	EP / RD	RWP / WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	0	0	0	0	1

6.18.2. Electronic volume register set

By using this command to set six bits of data to the electronic volume register, the liquid crystal driving voltage, V_5, assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0P	EP / RD	RWP / WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	| V5|
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

Note: *Inactive bit

6.18.3. The electronic volume register set sequence

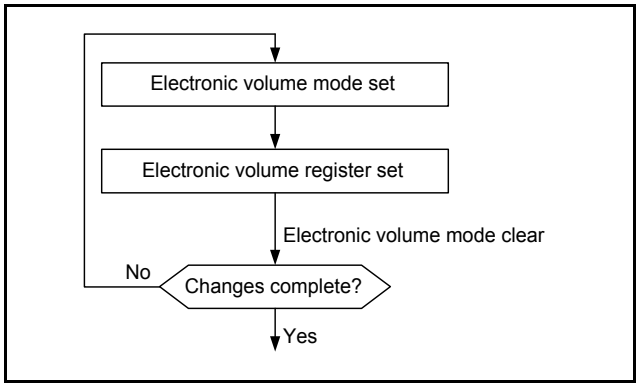


Figure 17

6.19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent from other display control commands. This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes. The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. The static indicator OFF command is a single byte command.

6.19.1. Static indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command is entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

6.19.2. Static indicator register set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Static Indicator
0	1	0	*	*	*	*	*	*	0	0	OFF
			*	*	*	*	*	*	0	1	ON (blinking at approximately 0.5 second intervals)
			*	*	*	*	*	*	1	0	ON (blinking at approximately one second intervals)
			*	*	*	*	*	*	1	1	ON (constantly on)

Note: *Disabled bit

6.20. Page Blinking (Double Byte Command)

6.20.1. The page blinking mode set

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	0	1

6.20.2. Page blinking register set

Set either bit to '1' will set corresponding PAGE0 - PAGE7 to blink.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Blinking Page
0	1	0	1	0	0	0	0	0	0	0	PAGE 7 blink
			0	1	0	0	0	0	0	0	PAGE 6 blink
			0	0	1	0	0	0	0	0	PAGE 5 blink
						↓					
			0	0	0	0	0	0	0	1	PAGE 0 blink

6.20.3. Page blinking indicator register set sequence

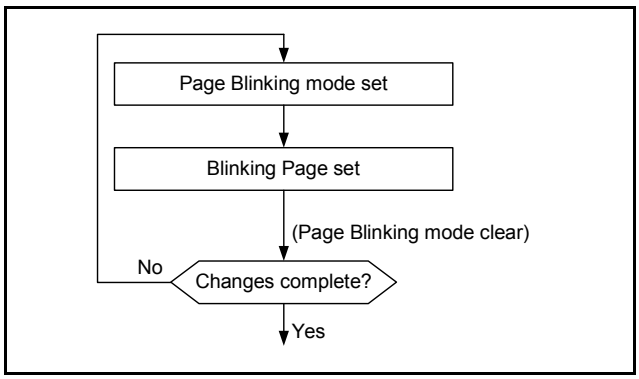


Figure 18

6.21. Set Driving Mode (Double Byte Command)

This command makes it possible to reduce the power consumption by instruction command for using different liquid crystal panel. User can select the appropriate mode for their liquid crystal panel and display pattern. The driving capability sequence is Mode1>Mode2>Mode3>Mode4, and so as the current consumption.

6.21.1. The driving mode set

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	0	1	0	0	1	0

6.21.2. Mode selection register set

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Driving Duty Selection
0	1	0	1	1	0	0	0	0	0	0	Mode 1
			0	0	0	0	0	0	0	0	Mode 2
			0	1	0	0	0	0	0	0	Mode 3
			1	0	0	0	0	0	0	0	Mode 4

Note1: DB5 - DB0 6 bits must fill 0.
Note2: Mode2 (DB7, DB6)=(0,0) is default.
Note3: Driving capability Mode1>Mode2>Mode3>Mode4.

6.22. Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered and therefore, it reduces a great amount of power. The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, the sleep mode is entered. When the static indicator is ON, the standby mode is entered. In the sleep mode and standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM. Refer to figure 19 for power save off sequence.

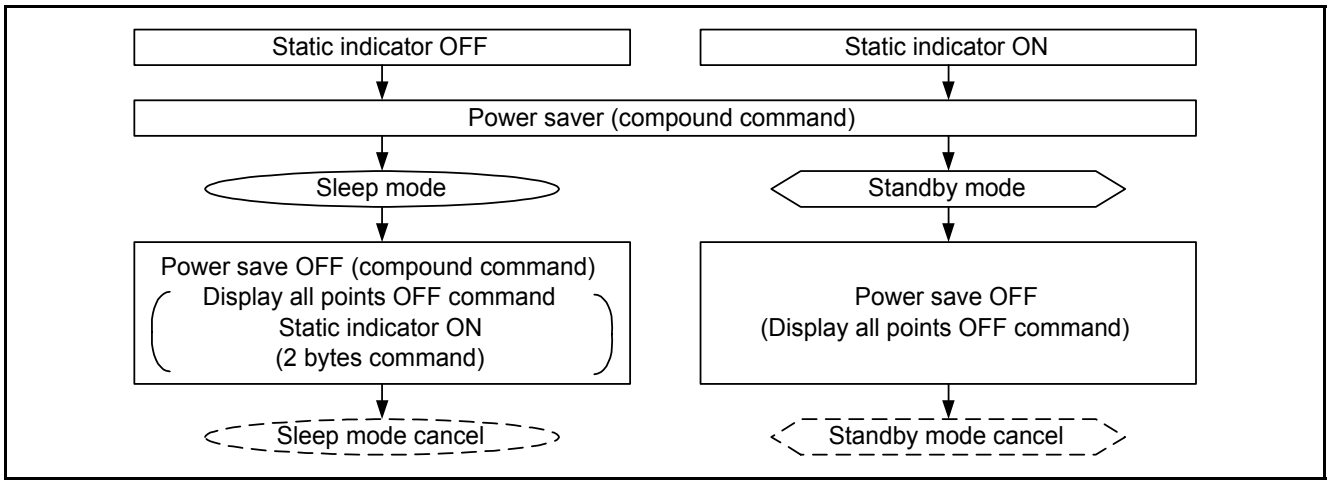


Figure 19

6.22.1. Sleep mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value close to the static current. The internal modes during sleep mode are as follows:

1). The oscillator circuit and the LCD power supply circuit are halted.
2). All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VDD level.

6.22.2. Standby mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

1). The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2). The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs a VDD level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

Note1: When an external power supply is used, it is recommended that the functions of the external power supply circuit should be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The SPLC501C chips have a liquid crystal display blanking control terminal $\overline{DOF}$. This terminal enters a 'L' state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.

Note2: When the master is turned on, the oscillator circuit is operable immediately after the power on.

6.23. NOP

Non-Operation Command

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	1

6.24. TEST

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a 'L' signal to the $\overline{RESET}$ input by the reset command or by using a NOP.

A0P	EP $\overline{RD}$	RWP $\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	1	*	*	*	*
0	1	0	1	1	0	1	0	0	1	0
0	1	0	1	1	0	1	0	1	0	0

Note: The SPLC501C chips maintain their operating modes until some conditions occurred to change them. Consequently, excessive external noise, etc., can change the internal modes of the SPLC501C chip. Thus, in the packaging and system design, it is necessary to suppress the noise or take measurement to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects.

6.25. Table 13 Table of SPLC501C Commands

Command	Command Code											Function
	A0P	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1). Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
2). Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
3). Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
4). Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Set the least significant 4 bits of the display RAM column address.
5). Status read	0	0	1	Status				0	0	0	0	Reads the status data
6). Display data write	1	1	0	Write data								Writes to the display RAM
7). Display data read	1	0	1	Read data								Reads from the display RAM
8). ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1:reverse
9). Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1:reverse
10). Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
11). LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD driver voltage bias ratio SPLC501C…….0:1/9, 1:1/7
12). Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
13). End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
14). Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
15). Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
16). Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
17). V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
18). Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V_5 output voltage electronic volume register
Electronic volume register set	0	1	0	*	*	Electronic volume value						

Command	Command Code										Function
	A0P	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
19). Static indicator ON/OFF				1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static indicator Register set				*	*	*	*	*	*	Mode		Set the flashing mode
20). Page Blink	0	1	0	1	1	0	1	0	1	0	1	
Page selection	0	1	0	P7	P6	P5	P4	P3	P2	P1	P0	P7 - 0: 1 - blinking page 0 - no blinking, normal display
21). Driving Mode Set	0	1	0	1	1	0	1	0	0	1	0	Set the driving mode register
Mode selection	0	1	0	D1	D0	0	0	0	0	0	0	Driving capability (D1, D0): (1,1)>(0,0)>(0,1)>(1,0)
22). Power saver												Display OFF and display all points ON compound command
23). NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
24). Test	0	1	0	1 1	1 1	1 0	1 1	* 0	* 1	* 0	* 0	Command for IC test. Do not use this command

7. COMMAND DESCRIPTION

7.1. Instruction Setup: Reference (Reference)

7.1.1. Initialization

Note: When the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V_{5-1}) and the VDD pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

1). When the built-in power is being used immediately after turning on the power:

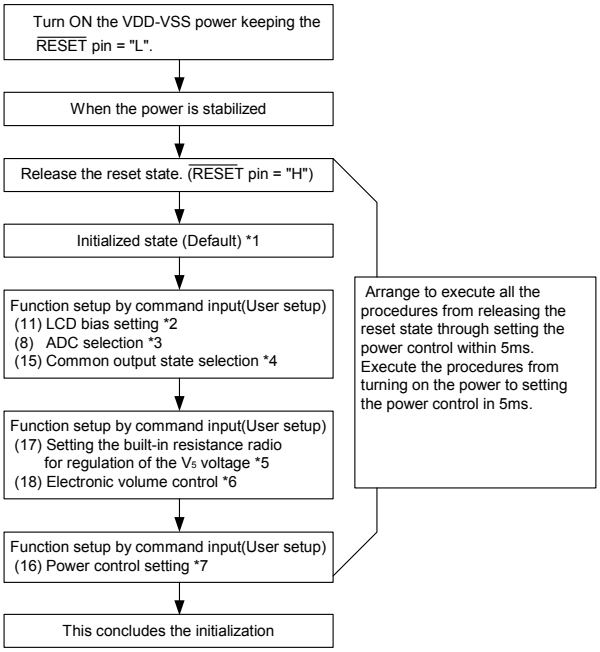


Figure 20

Note1: The target time of 5ms varied depending on the panel characteristics and the capacitance of the smoothing apacitor. Therefore, we suggest users to conduct an operation check using the actual equipment.

Note2: Refer to respective sections or paragraphs listed below.

*1:Description of functions; Reset circuit
*2:Command description; LCD bias setting
*3:Command description; ADC selection
*4:Command description; Common output state selection
*5:Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_5 voltage
*6:Description of functions; Power circuit & Command description; Electronic volume control
*7:Description of functions; Power circuit & Command description; Power control setting.

2). When the built-in power is not being used immediately after turning on the power:

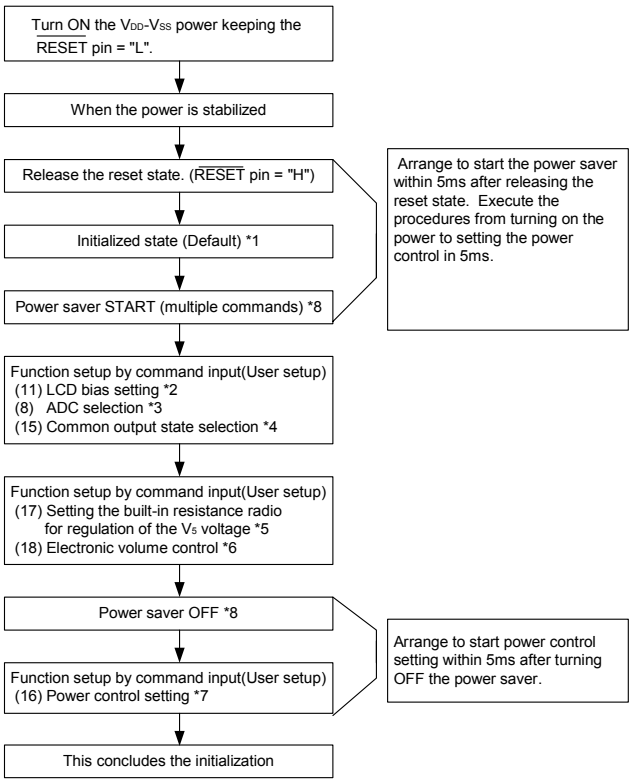


Figure 21

Note1: The target time of 5ms varied depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest users to conduct an operation check using the actual equipment.

Note2: Refer to respective sections or paragraphs listed below.

*1:Description of functions; Resetting circuit
*2:Command description; LCD bias setting
*3:Command description; ADC selection
*4:Command description; Common output state selection
*5:Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_5 voltage
*6:Description of functions; Power circuit & Command description; Electronic volume control
*7:Description of functions; Power circuit & Command description; Power control setting
*8:The power saver ON state can either be in sleep state or stand-by state. Command description; Power saver START (multiple commands)

7.1.2. Data display

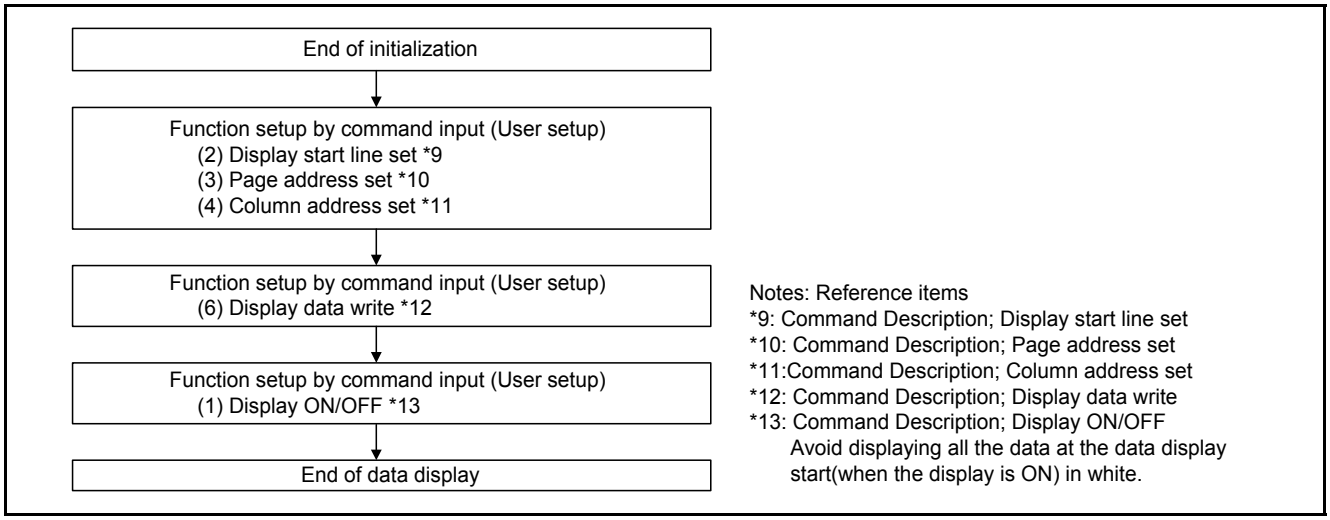


Figure 22

7.1.3. Power OFF *14

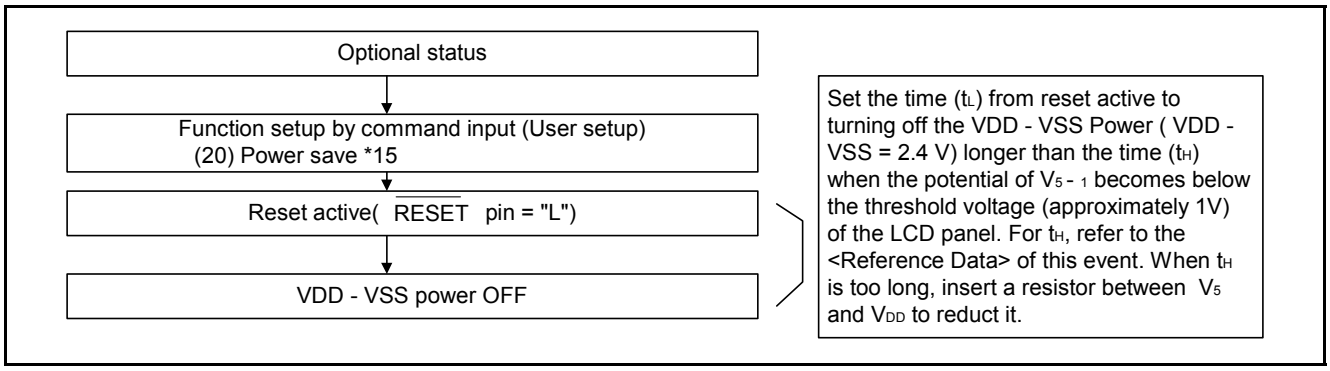


Figure 23

Note: Reference items

*14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VDD - V_5. Therefore, if the power supply VDD - VSS is cut off when the LCD power supply VDD - V_5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:

• After turning off the internal power supply, make sure that the potential V_{5-1} has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS).

Refer to "6. Description of Function, Power Circuit" for more information.

*15: After inputting the power save command, be sure to reset the function using the $\overline{\text{RESET}}$ terminal until the power supply VDD - VSS is turned off. Refer to " 7. Command Description, (20) Power Save" for more information.

7.2. Precautions ON Turning OFF The Power

7.2.1. Power save (the LCD powers (VDD - V_5) are off.) → Reset input → Power (VDD - VSS) OFF

1). Observe $t_L > t_H$.

2). When $t_L < t_H$, an irregular display may occur.

Set t_L on the MPU according to the software. t_H is determined according to the external capacity C2 (smoothing capacity of V_{5-1}) and the driver's discharging capacity.

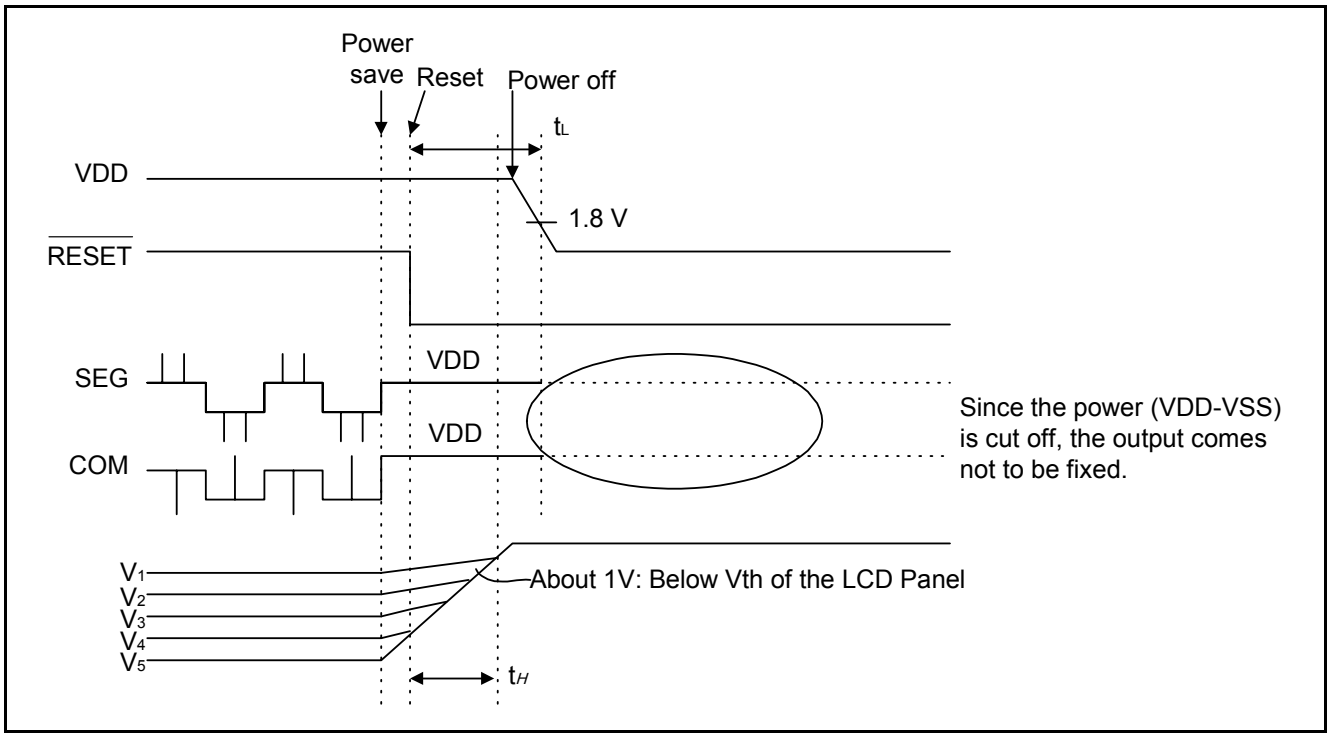

Power
save
Reset
Power off
tL
VDD
1.8 V
RESET
SEG
VDD
VDD
COM
Since the power (VDD-VSS) is cut off, the output comes not to be fixed.
V1
V2
V3
V4
V5
About 1V: Below Vth of the LCD Panel
tH

Figure 24

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

(Unless otherwise noted, VSS = 0V)

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	-0.3 to + 7.0	V
Power supply voltage (2) (VDD standard)	With Triple step-up	VSS2	-7.0 to +0.3 -4.0 to +0.3	V
	With Quad step-up		-3.0 to +0.3	
Power supply voltage (3) (VDD standard)		V_5, V_{OUT}	-12.0 to +0.3	V
Power supply voltage (4) (VDD standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	-0.3 to VDD +0.3	V
Output voltage		V_O	-0.3 to VDD +0.3	V
Operating temperature		T_{OPR}	-40 to +85	℃
Storage temperature	Bare chip	T_{STR}	-55 to +125	℃

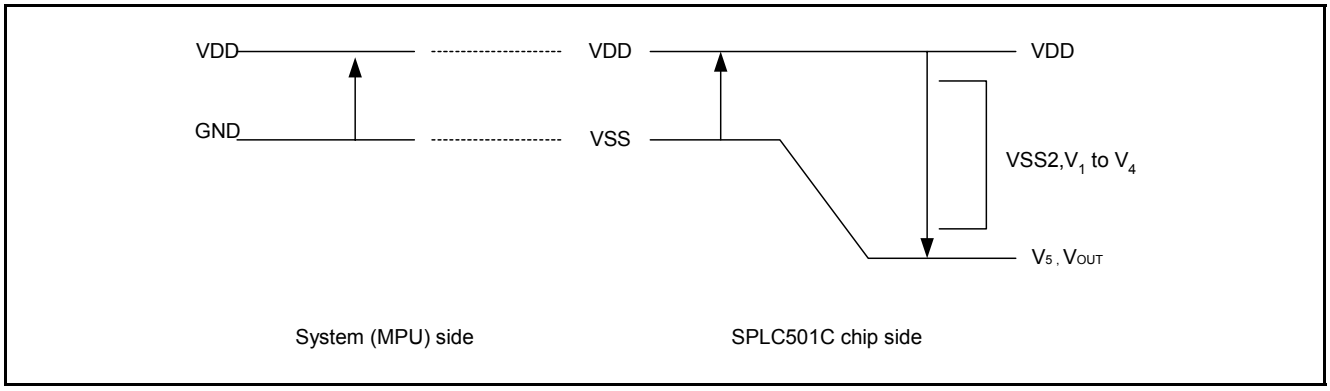


Figure 25

Notes and Cautions:

1. The VSS2, V_1 to V_5 and VOUT are relative to the VDD = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that VDD≧V_1≧V_2≧V_3≧V_4≧V_5.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

8.2. DC Characteristics

(Unless otherwise specified, VSS = 0V, VDD = 3.0V±10%, T_A = 25℃)

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable PIN
Operating Voltage (1)	Recommended Voltage	VDD			2.7	-	3.3	V	VDD*1
	Possible Operating Voltage				2.4	-	5.5	V	VDD*1
Operating Voltage (2)	Recommended Voltage	VSS2	(Relative to VDD)		-3.3	-	-2.7	V	VSS2
	Possible Operating Voltage	VSS2	(Relative to VDD)		-6.0	-	-1.8	V	VSS2
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to VDD)		-12.0	-	-4.5	V	V_5*2
	Possible Operating Voltage	V_1, V_2	(Relative to VDD)		0.4 x V_5	-	VDD	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to VDD)		V_5	-	0.6 x V_5	V	V_3, V_4
High-level Input Voltage		V_{IHC}			0.8 x VDD	-	VDD	V	*3
Low-level Input Voltage		V_{ILC}			VSS	-	0.2 x VDD	V	*3
High-level Input Voltage		V_{OHC}	I_{OH} = -0.5mA		0.8 x VDD	-	VDD	V	*4
Low-level Input Voltage		V_{OLC}	I_{OL} = 0.5mA		VSS	-	0.2 x VDD	V	*4
Input leakage current		I_{LI}	V_{IN} = VDD or VSS		-1.0	-	1.0	μA	*5
Output leakage current		I_{LO}			-3.0	-	3.0	μA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	T_A = 25℃ (Relative To VDD)	V_5 = -12V	-	2.0	3.5	KΩ	SEGn
				V_5 = -8.0V	-	3.2	5.4	KΩ	COMn*7
Static Consumption Current		I_{SSQ}			-	0.01	5.0	μA	VSS, VSS2
Output Leakage Current		I_{5Q}	V_5 = -12V (Relative to VDD)		-	0.01	15	μA	V_5
Input Terminal Capacitance		C_{IN}	T_A = 25℃ f = 1.0MHz		-	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	T_A = 25℃		18	22	26	KHz	*8
	External Input	f_{CL}	SPLC501C		18	22	26	KHz	CL

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Application PIN
Internal Power	Input Voltage	VSS2	With Triple (Relative to VDD)		-4.0	-	-2.4	V	VSS2
		VSS2	With Quad (Relative to VDD)		-3.0	-	-2.4	V	VSS2
	Supply Setup-up output voltage Circuit	V_{OUT}	(Relative to VDD)		-12	-	-	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to VDD)		-12	-	-6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to VDD)		-12	-	-4.5	V	V_5 *9
	Base Voltage	V_{REG0}	T_A = 25℃ (Relative to VDD)	-0.05%/℃	-2.28	-2.22	-2.16	V	*10

Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF.
Current consumed by total ICs when an external power supply is used.

8.3. Display Pattern OFF

(T_A = 25℃)

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SPLC501C	I_{DD}(1)	VDD = 5.0V, V_5 - VDD = -11V	-	4.6	12.6	μA	*11
		VDD = 3.0V, V_5 - VDD = -11V	-	2.9	5.8		

8.4. Display Pattern Checker

(T_A = 25℃)

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SPLC501C	I_{DD}(1)	VDD = 5.0V, V_5 - VDD = -11V	-	8.2	15	μA	*11
		VDD = 3.0V, V_5 - VDD = -11V	-	5.0	7.5		

Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

8.5. Display Pattern Checker

(T_A = 25℃)

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SPLC501C	I_{DD}(2)	VDD = 5.0V, Double step-up voltage. V_5 - VDD = -9.0V	Normal Mode	-	130	220	μA	*12
			High-Power Mode	-	140	280		
		VDD = 3.0V, Quad step-up voltage. V_5 - VDD = -9.0V	Normal Mode	-	200	270		
			High-Power Mode	-	250	320		

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep Mode SPLC501C	I_{DDS1}	-	-	0.01	5.0	μA	

Item		f_{CL}	f_{FR}
SPLC501C *8	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4x65}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{260}$

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the VDD system and the V_5 system is applied when the external power supply is being used.

*3 The A0P, DB0 to DB5, DB6 (SCL), DB7 (SI), $\overline{RD}$ (EP), $\overline{WR}$ (RWP), $\overline{CS1}$, CS2, CLS, CL, FR, MS, C86, PS, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*4 The DB0 to DB7, FR, FRS, $\overline{DOF}$, and CL terminals.

*5 The A0P, $\overline{RD}$ (EP), $\overline{WR}$ (RWP), $\overline{CS1}$, CS2, CLS, MS, C86, PS, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*6 Applies when the DB0 to DB5, DB6 (SCL), DB7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range.
R_{ON} = 0.1V/ △I (Where △I is the current that flows when 0.1V is applied while the power supply is ON.)

*8 The relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

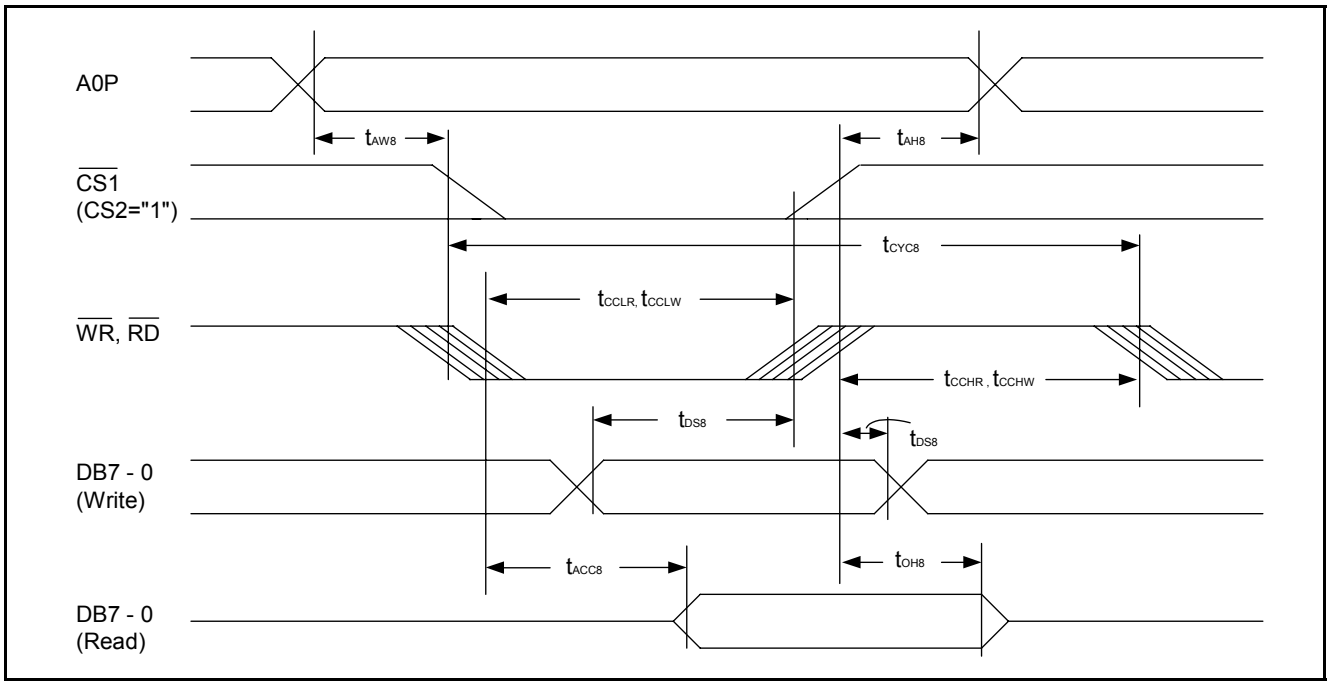
*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the SPLC501C, the temperature range can come in three types as VREG options: (1) approximately –0.05%/C, and (2) external input.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
The SPLC501C is 1/9 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.

*12 It is the value on a model having the V_{REG} option temperature gradient is –0.05%/C when the V_5 voltage regulator internal resistor is used.

8.6. Timing Characteristics

8.6.1. System bus read/write characteristics 1 (For the 8080 Series MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		166	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	-	ns
Data setup time	DB7 - 0	t_{DS8}		30	-	ns
Address hold time		t_{DH8}		10	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	70	ns
Output disable time		t_{OH8}		5.0	50	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		300	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	-	ns
Data setup time	DB7 - 0	t_{DS8}		40	-	ns
Address hold time		t_{DH8}		15	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

(VDD = 2.4V to 2.7V, T_A = 25℃)

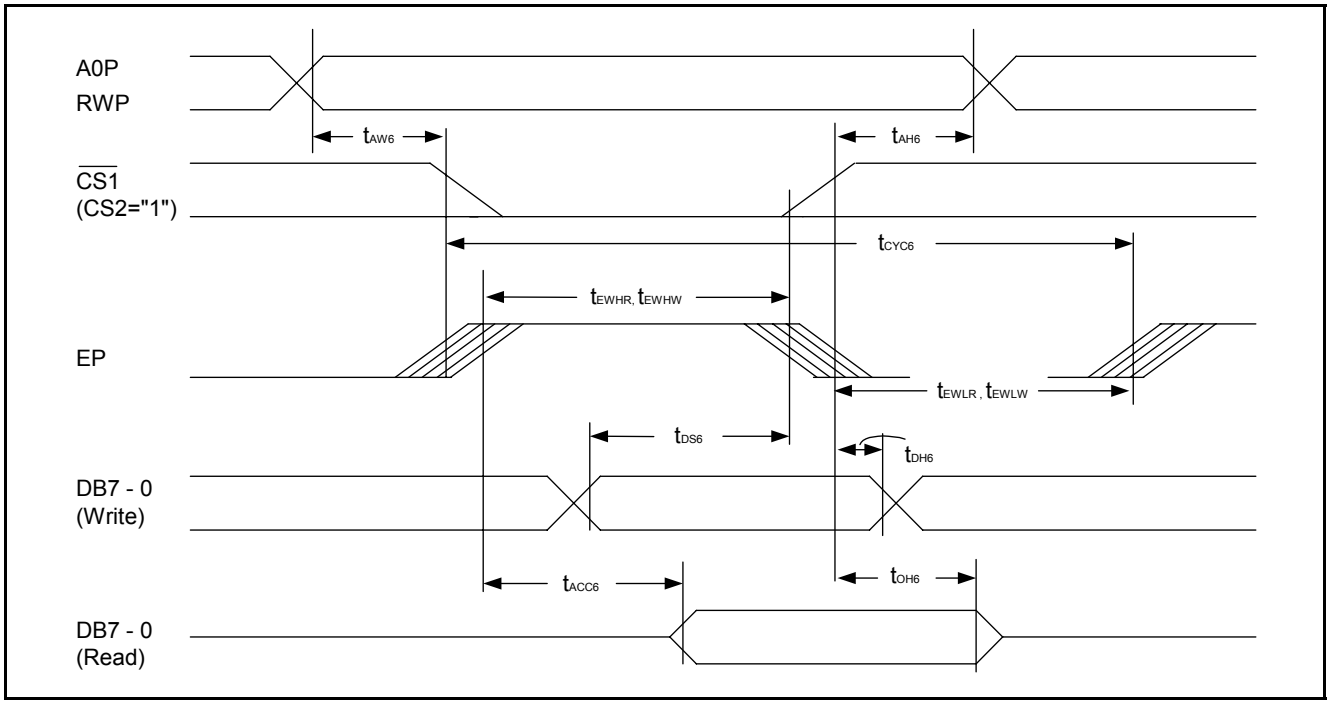
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		1000	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	-	ns
Data setup time	DB7 - 0	t_{DS8}		80	-	ns
Address hold time		t_{DH8}		30	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	280	ns
Output disable time		t_{OH8}		10	200	ns

Note1: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being 'L' ($\overline{CS2}$ = 'H') and $\overline{WR}$ and $\overline{RD}$ being at the 'L' level.

8.6.2. System bus read/write characteristics 2 (6800 series MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		166	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	30	-	ns
Data hold time			t_{DH6}		10	-	ns
Access time			t_{ACC6}		-	70	ns
Output disable time			t_{OH6}		10	50	ns
Enable H pulse time	Read	EP	t_{EWHR}		70	-	ns
	Write		t_{EWHW}		30	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		30	-	ns
	Write		t_{EWLW}		30	-	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		300	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	40	-	ns
Data hold time			t_{DH6}		15	-	ns
Access time			t_{ACC6}		-	140	ns
Output disable time			t_{OH6}		10	100	ns
Enable H pulse time	Read	EP	t_{EWHR}		120	-	ns
	Write		t_{EWHW}		60	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		60	-	ns
	Write		t_{EWLW}		60	-	ns

(VDD = 2.4V to 2.7V, T_A = 25℃)

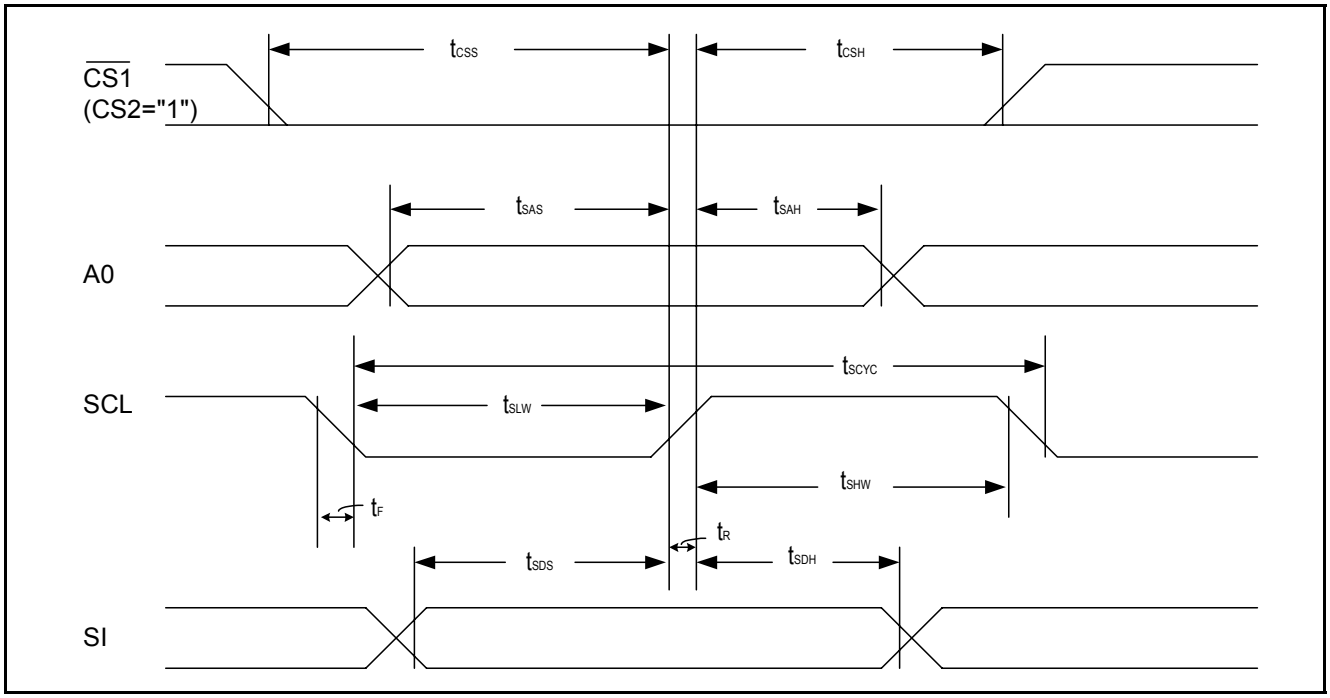
Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		1000	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	80	-	ns
Data hold time			t_{DH6}		30	-	ns
Access time			t_{ACC6}		-	280	ns
Output disable time			t_{OH6}		10	120	ns
Enable H pulse time	Read	EP	t_{EWHR}		240	-	ns
	Write		t_{EWHW}		120	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		120	-	ns
	Write		t_{EWLW}		120	-	ns

Note1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and EP.

8.6.3. The serial interface



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	-	200	-	ns
SCL 'H' pulse width		t_{SHW}	-	75	-	ns
SCL 'L' pulse width		t_{SLW}	-	75	-	ns
Address setup time	A0P	t_{SAS}	-	50	-	ns
Address hold time		t_{SAH}	-	100	-	ns
Data setup time	SI	t_{SDS}	-	50	-	ns
Data hold time		t_{SDH}	-	50	-	ns
CS-SCL time	CS	t_{CSS}	-	100	-	ns
		t_{CSH}	-	100	-	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	250	-	ns
SCL 'H' pulse width		tSHW	-	100	-	ns
SCL 'L' pulse width		tSLW	-	100	-	ns
Address setup time	A0P	tSAS	-	150	-	ns
Address hold time		tSAH	-	150	-	ns
Data setup time	SI	tSDS	-	100	-	ns
Data hold time		tSDH	-	100	-	ns
CS-SCL time	CS	tCSS	-	150	-	ns
		tCSH	-	150	-	ns

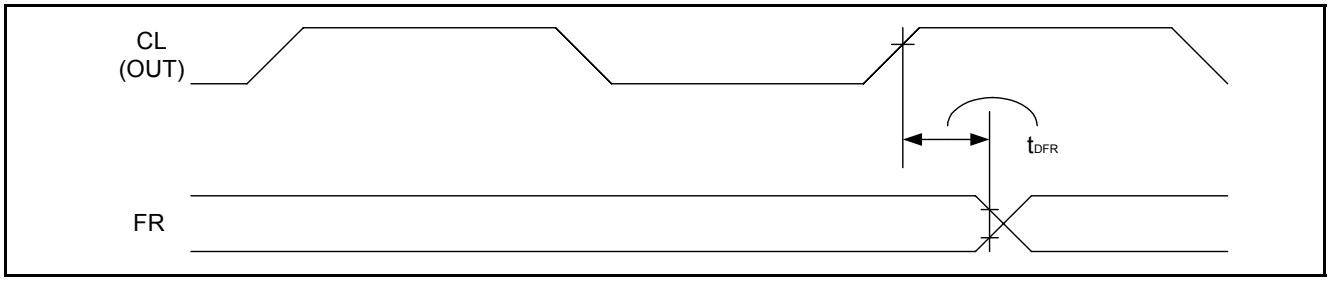
(VDD = 2.4V to 2.7V, TA = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	-	400	-	ns
SCL 'H' pulse width		t_{SHW}	-	150	-	ns
SCL 'L' pulse width		t_{SLW}	-	150	-	ns
Address setup time	A0P	t_{SAS}	-	250	-	ns
Address hold time		t_{SAH}	-	250	-	ns
Data setup time	SI	t_{SDS}	-	150	-	ns
Data hold time		t_{SDH}	-	150	-	ns
CS-SCL time	CS	t_{CSS}	-	250	-	ns
		t_{CSH}	-	250	-	ns

Note1: The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.

Note2: All timing is specified using 20% and 80% of VDD as the standard.

8.6.4. Display control output timing



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	-	10	40	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	-	20	80	ns

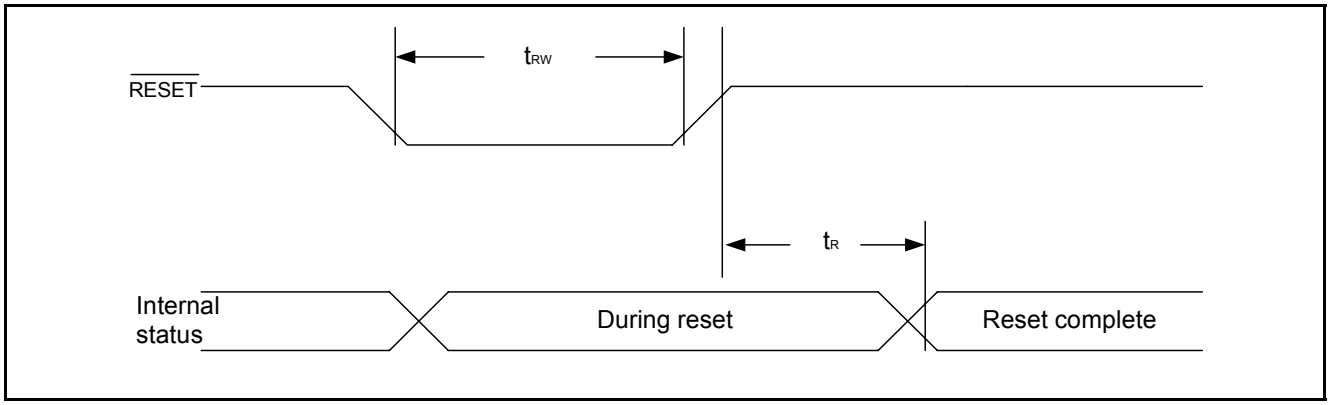
(VDD = 2.4V to 2.7V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	-	50	200	ns

Note1: Valid only when the master mode is selected.

Note2: All timing is based on 20% and 80% of VDD.

8.6.5. Reset timing



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	0.5	μs
Reset 'L' pulse width	RES	t_{RW}		0.5	-	-	μs

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	1.0	μs
Reset 'L' pulse width	RES	t_{RW}		1.0	-	-	μs

(VDD = 2.4V to 2.7V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	1.5	μs
Reset 'L' pulse width	RES	t		1.5	-	-	μs

Note: All timing is specified with 20% and 80% of VDD as the standard.

8.7. The MPU Interface (Reference Examples)

The SPLC501C can be connected to either 80 X 86 Series MPUs or to 68000 Series MPUs. Moreover, The serial interface is possible to operate the SPLC501C chips with fewer signal lines. The display area can be enlarged by using multiple SPLC501C chips. When this is done, the chip select signal can be used to select the individual ICs to access.

8.7.1. 8080 series MPUs

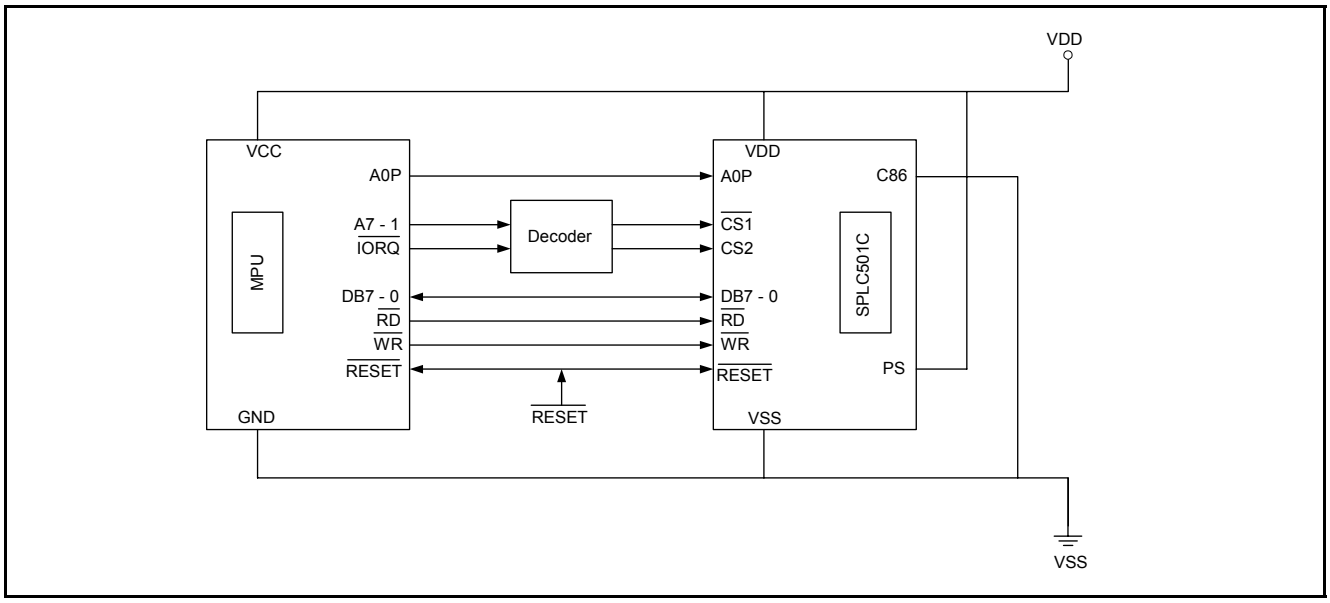


Figure 26

8.7.2. 6800 series MPUs

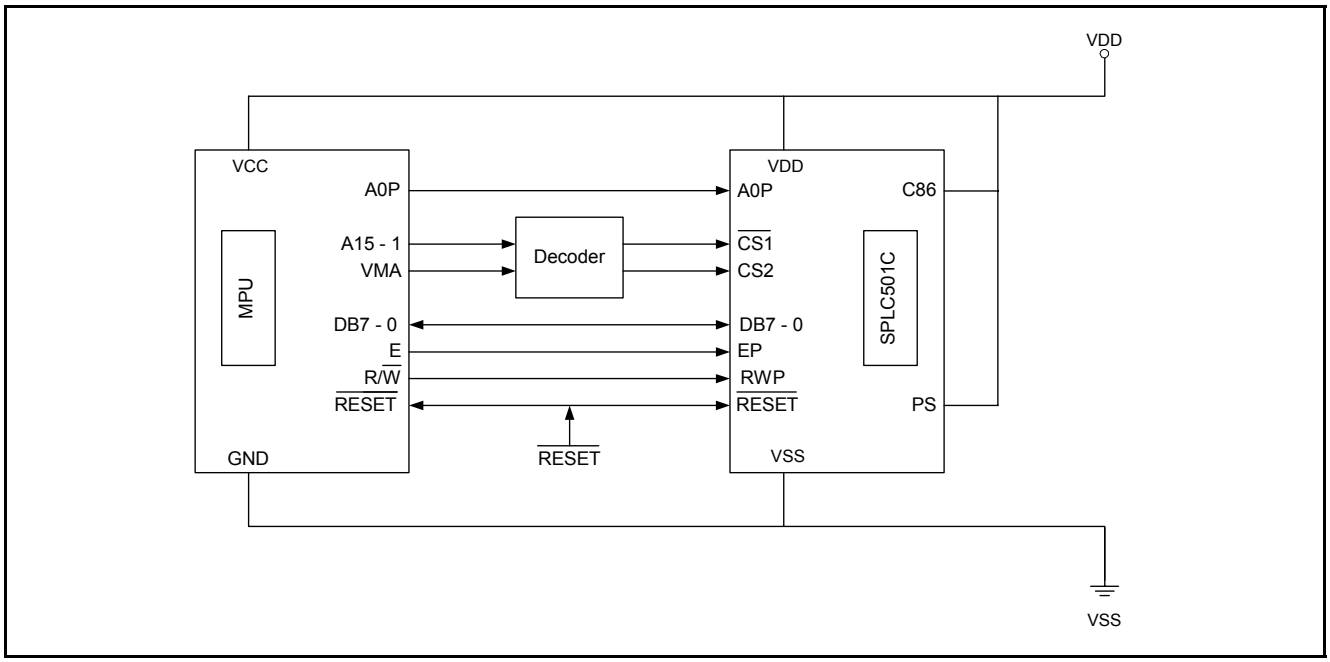


Figure 27

8.7.3. Using the serial interface

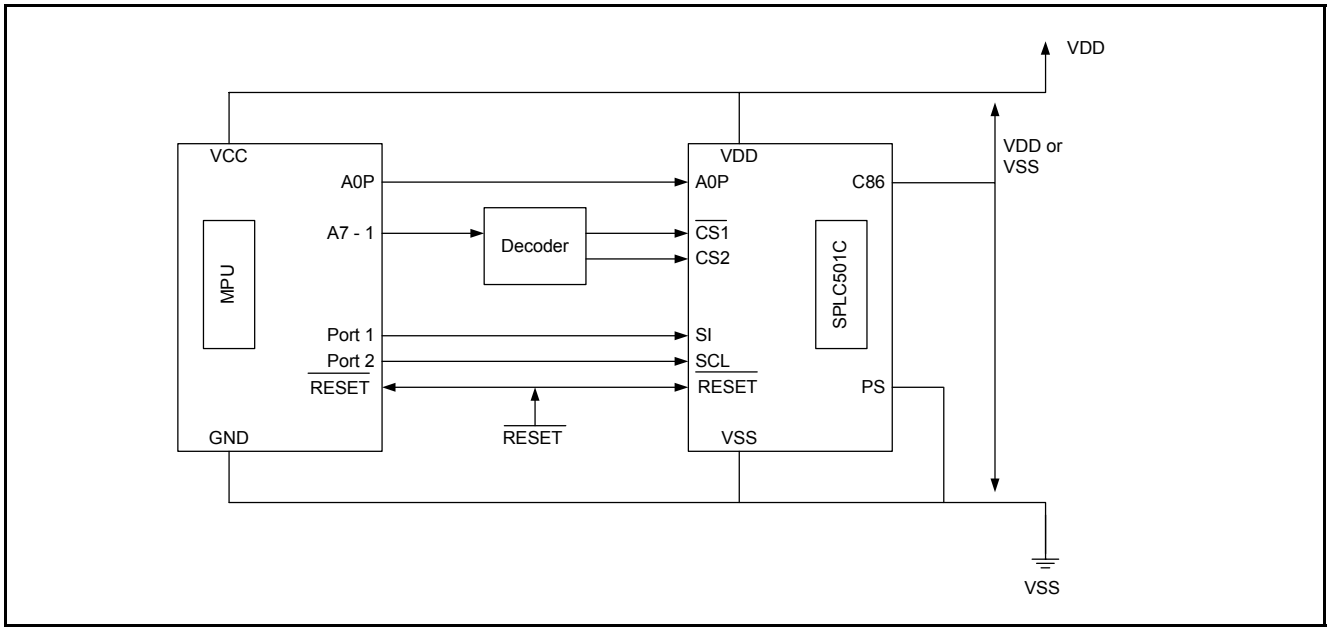


Figure 28

8.8. Connections Between LCD Drivers (Reference Example)

The liquid crystal display area can be enlarged with ease through the use of multiple SPLC501C chips. Use a same equipment type.

8.8.1. SPLC501C (Master)<->SPLC501C (Slave)

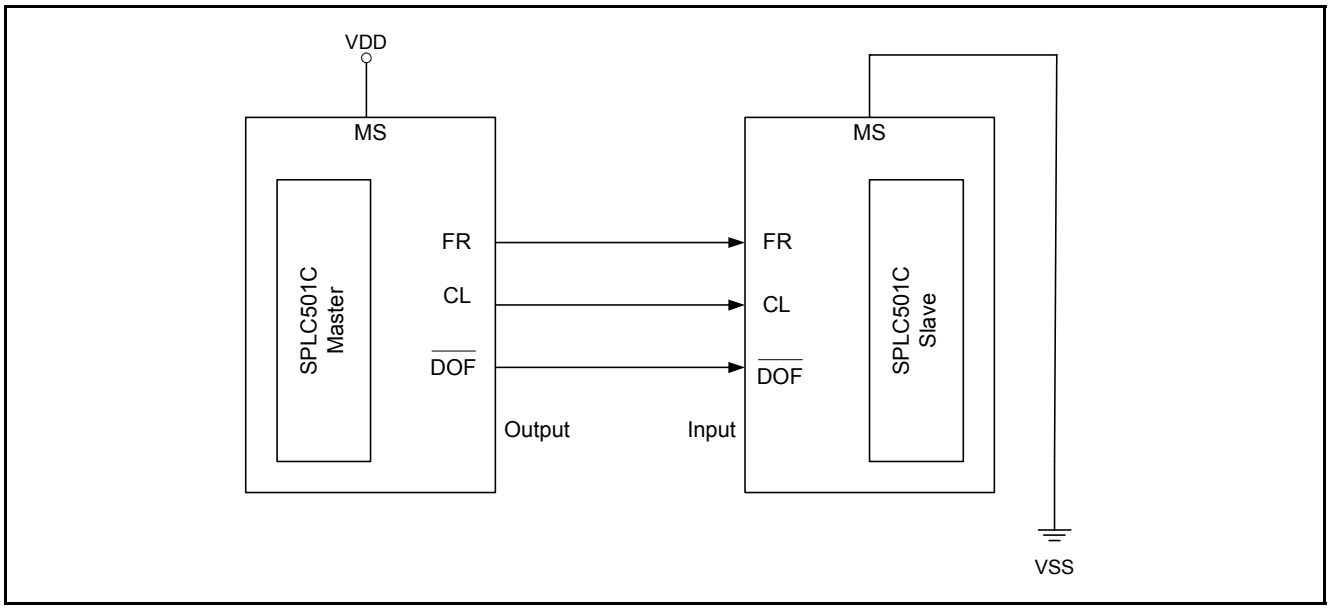


Figure 29

8.9. Connections Between LCD Drivers (Reference Examples)

The liquid crystal display area can be enlarged with ease through the use of multiple SPLC501C chips. Use a same equipment type, in the composition of these chips.

8.9.1. Single-chip structure

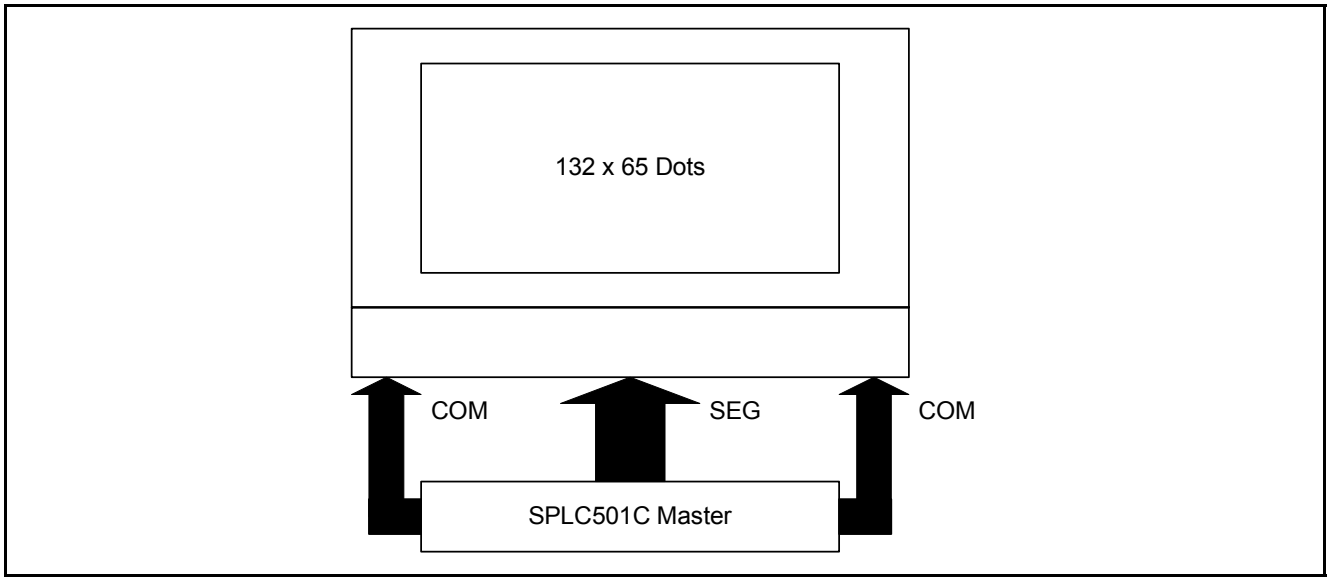
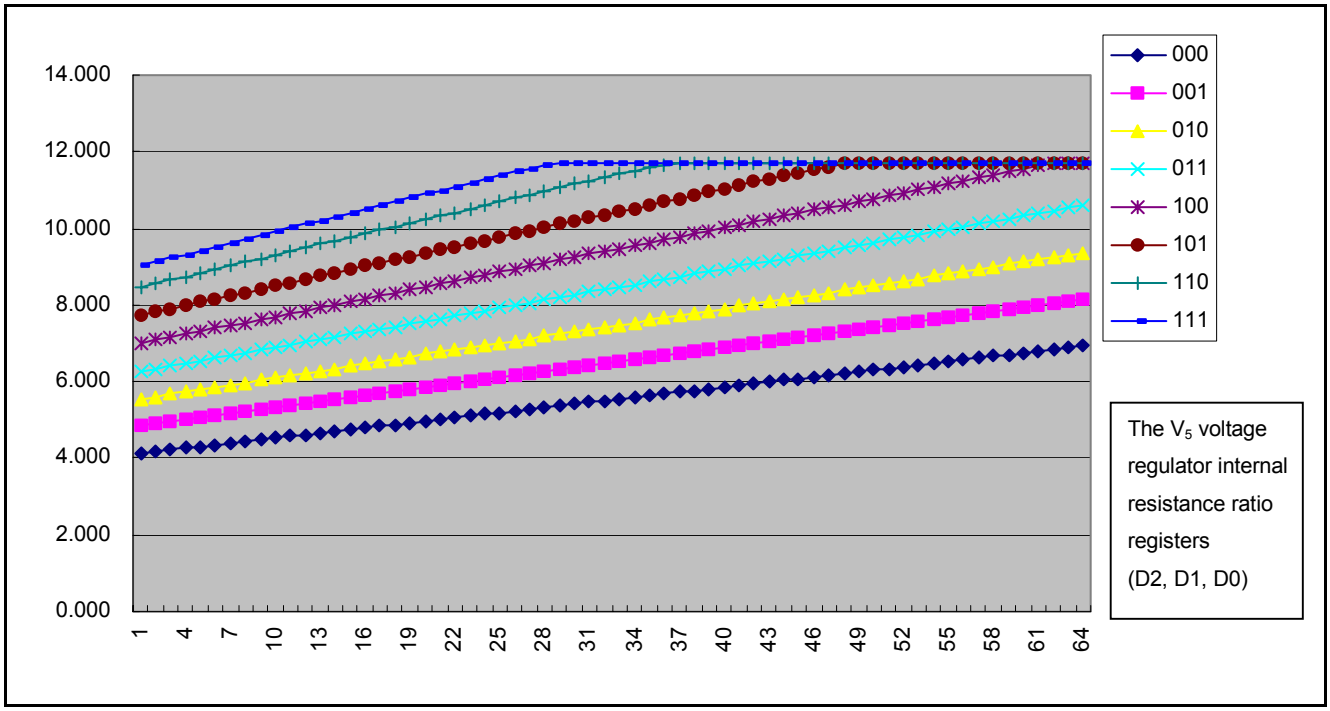


Figure 30

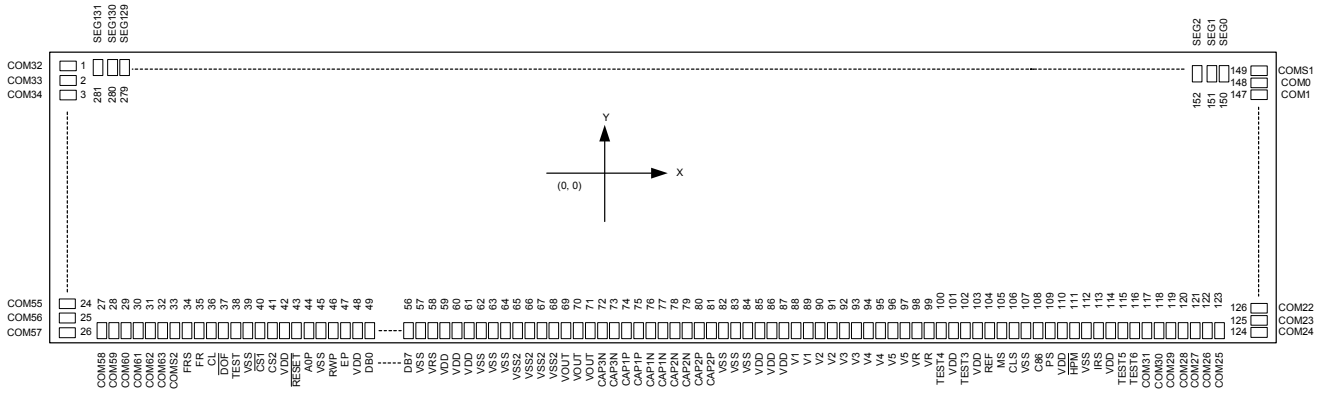
8.10. VLCD Voltage (Voltage between VDD to V_5) relationship of V_5 Voltage Regulator Internal Resistor Ratio Register and Electronic Volume Control Register



Note: Use External V_{OUT} Power Supply.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 8290μm x 1720μm

This IC substrate should be connected to VDD

Bump Pitch	60μm(Min.)	Size		Unit
		X	Y	
Bump Size	PAD No. 1 ~ 26	90	40	μm
	PAD No. 27 ~ 123	40	105	
	PAD No. 150 ~ 281	40	90	
	PAD No. 124 ~ 149	90	40	
Bumped PAD height	ALL PAD	18		

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD, VSS, AVDD and AVSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPLC501C-nnnnV-C	Chip form with Gold Bump

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	COM32	-4020	761	45	VSS	-2268	-724
2	COM33	-4020	701	46	RWP	-2181	-724
3	COM34	-4020	641	47	EP	-2073	-724
4	COM35	-4020	581	48	VDD	-1941	-724
5	COM36	-4020	521	49	DB0	-1853	-724
6	COM37	-4020	461	50	DB1	-1746	-724
7	COM38	-4020	401	51	DB2	-1639	-724
8	COM39	-4020	341	52	DB3	-1532	-724
9	COM40	-4020	281	53	DB4	-1426	-724
10	COM41	-4020	221	54	DB5	-1318	-724
11	COM42	-4020	161	55	DB6	-1212	-724
12	COM43	-4020	101	56	DB7	-1105	-724
13	COM44	-4020	41	57	VSS	-972	-724
14	COM45	-4020	-19	58	VRS	-884	-724
15	COM46	-4020	-79	59	VDD	-796	-724
16	COM47	-4020	-139	60	VDD	-736	-724
17	COM48	-4020	-199	61	VDD	-629	-724
18	COM49	-4020	-259	62	VSS	-569	-724
19	COM50	-4020	-319	63	VSS	-509	-724
20	COM51	-4020	-379	64	VSS	-402	-724
21	COM52	-4020	-439	65	VSS2	-342	-686
22	COM53	-4020	-499	66	VSS2	-282	-686
23	COM54	-4020	-559	67	VSS2	-222	-686
24	COM55	-4020	-619	68	VSS2	-162	-686
25	COM56	-4020	-679	69	VOUT	-102	-686
26	COM57	-4020	-739	70	VOUT	-42	-686
27	COM58	-3932	-724	71	VOUT	18	-686
28	COM59	-3872	-724	72	CAP3N	78	-686
29	COM60	-3812	-724	73	CAP3N	138	-686
30	COM61	-3752	-724	74	CAP1P	198	-686
31	COM62	-3692	-724	75	CAP1P	258	-686
32	COM63	-3632	-724	76	CAP1N	318	-686
33	COMS2	-3572	-724	77	CAP1N	378	-686
34	FRS	-3484	-724	78	CAP2N	438	-686
35	FR	-3377	-724	79	CAP2N	498	-686
36	CL	-3271	-724	80	CAP2P	558	-686
37	$\overline{\text{DOF}}$	-3163	-724	81	CAP2P	618	-686
38	TEST	-3057	-724	82	VSS	678	-686
39	VSS	-2969	-724	83	VSS	738	-686
40	CS1N	-2836	-724	84	VSS	798	-686
41	CS2	-2729	-724	85	VDD	858	-686
42	VDD	-2596	-724	86	VDD	918	-686
43	$\overline{\text{RESET}}$	-2508	-724	87	VDD	978	-686
44	A0P	-2401	-724	88	V1	1038	-686

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
89	V1	1098	-686	134	COM14	4016	-139
90	V2	1158	-686	135	COM13	4016	-79
91	V2	1218	-686	136	COM12	4016	-19
92	V3	1278	-686	137	COM11	4016	41
93	V3	1338	-686	138	COM10	4016	101
94	V4	1398	-686	139	COM9	4016	161
95	V4	1458	-686	140	COM8	4016	221
96	V5	1518	-686	141	COM7	4016	281
97	V5	1578	-686	142	COM6	4016	341
98	VR	1638	-686	143	COM5	4016	401
99	VR	1698	-686	144	COM4	4016	461
100	TEST4	1758	-686	145	COM3	4016	521
101	VDD	1852	-686	146	COM2	4016	581
102	TEST3	1946	-686	147	COM1	4016	641
103	VDD	2006	-724	148	COM0	4016	701
104	REF	2139	-724	149	COMS1	4016	761
105	MS	2246	-724	150	SEG0	3928	736
106	CLS	2353	-724	151	SEG1	3868	736
107	VSS	2436	-724	152	SEG2	3808	736
108	C86	2574	-724	153	SEG3	3748	736
109	PS	2681	-724	154	SEG4	3688	736
110	VDD	2814	-724	155	SEG5	3628	736
111	$\overline{\text{HPM}}$	2901	-724	156	SEG6	3568	736
112	VSS	2989	-724	157	SEG7	3508	736
113	IRS	3122	-724	158	SEG8	3448	736
114	VDD	3210	-724	159	SEG9	3388	736
115	TEST5	3343	-724	160	SEG10	3328	736
116	TEST6	3450	-724	161	SEG11	3268	736
117	COM31	3568	-724	162	SEG12	3208	736
118	COM30	3628	-724	163	SEG13	3148	736
119	COM29	3688	-724	164	SEG14	3088	736
120	COM28	3748	-724	165	SEG15	3028	736
121	COM27	3808	-724	166	SEG16	2968	736
122	COM26	3868	-724	167	SEG17	2908	736
123	COM25	3928	-724	168	SEG18	2848	736
124	COM24	4016	-739	169	SEG19	2788	736
125	COM23	4016	-679	170	SEG20	2728	736
126	COM22	4016	-619	171	SEG21	2668	736
127	COM21	4016	-559	172	SEG22	2608	736
128	COM20	4016	-499	173	SEG23	2548	736
129	COM19	4016	-439	174	SEG24	2488	736
130	COM18	4016	-379	175	SEG25	2428	736
131	COM17	4016	-319	176	SEG26	2368	736
132	COM16	4016	-259	177	SEG27	2308	736
133	COM15	4016	-199	178	SEG28	2248	736

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
179	SEG29	2188	736	224	SEG74	-512	736
180	SEG30	2128	736	225	SEG75	-572	736
181	SEG31	2068	736	226	SEG76	-632	736
182	SEG32	2008	736	227	SEG77	-692	736
183	SEG33	1948	736	228	SEG78	-752	736
184	SEG34	1888	736	229	SEG79	-812	736
185	SEG35	1828	736	230	SEG80	-872	736
186	SEG36	1768	736	231	SEG81	-932	736
187	SEG37	1708	736	232	SEG82	-992	736
188	SEG38	1648	736	233	SEG83	-1052	736
189	SEG39	1588	736	234	SEG84	-1112	736
190	SEG40	1528	736	235	SEG85	-1172	736
191	SEG41	1468	736	236	SEG86	-1232	736
192	SEG42	1408	736	237	SEG87	-1292	736
193	SEG43	1348	736	238	SEG88	-1352	736
194	SEG44	1288	736	239	SEG89	-1412	736
195	SEG45	1228	736	240	SEG90	-1472	736
196	SEG46	1168	736	241	SEG91	-1532	736
197	SEG47	1108	736	242	SEG92	-1592	736
198	SEG48	1048	736	243	SEG93	-1652	736
199	SEG49	988	736	244	SEG94	-1712	736
200	SEG50	928	736	245	SEG95	-1772	736
201	SEG51	868	736	246	SEG96	-1832	736
202	SEG52	808	736	247	SEG97	-1892	736
203	SEG53	748	736	248	SEG98	-1952	736
204	SEG54	688	736	249	SEG99	-2012	736
205	SEG55	628	736	250	SEG100	-2072	736
206	SEG56	568	736	251	SEG101	-2132	736
207	SEG57	508	736	252	SEG102	-2192	736
208	SEG58	448	736	253	SEG103	-2252	736
209	SEG59	388	736	254	SEG104	-2312	736
210	SEG60	328	736	255	SEG105	-2372	736
211	SEG61	268	736	256	SEG106	-2432	736
212	SEG62	208	736	257	SEG107	-2492	736
213	SEG63	148	736	258	SEG108	-2552	736
214	SEG64	88	736	259	SEG109	-2612	736
215	SEG65	28	736	260	SEG110	-2672	736
216	SEG66	-32	736	261	SEG111	-2732	736
217	SEG67	-92	736	262	SEG112	-2792	736
218	SEG68	-152	736	263	SEG113	-2852	736
219	SEG69	-212	736	264	SEG114	-2912	736
220	SEG70	-272	736	265	SEG115	-2972	736
221	SEG71	-332	736	266	SEG116	-3032	736
222	SEG72	-392	736	267	SEG117	-3092	736
223	SEG73	-452	736	268	SEG118	-3152	736

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
269	SEG119	-3212	736	276	SEG126	-3632	736
270	SEG120	-3272	736	277	SEG127	-3692	736
271	SEG121	-3332	736	278	SEG128	-3752	736
272	SEG122	-3392	736	279	SEG129	-3812	736
273	SEG123	-3452	736	280	SEG130	-3872	736
274	SEG124	-3512	736	281	SEG131	-3932	736
275	SEG125	-3572	736				

9.4. Align Key Locations

X	Y	Description
-3456	385	Marked with 68μm diameter spot
3452	385	Marked with 68μm diameter spot

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JUN. 12, 2001	0.1	Original	
JUL, 30, 2001	1.0	1. Delete "*PRELIMINARY*" 2. Change title 3. Add REF pin description in "4.3. *System Bus Connection Terminals*" 4. Modify base voltage	 4 9 41
NOV. 06, 2001	1.1	1. Modify Boost reference voltage: VDD - VSS2 = 2.4V to -6.0V to 2.4V to 6.0V 2. Modify Liquid crystal drive power supply: VDD - V_5 = -4.5V to -12V to 4.5V to 12V 3. Add "Driving Mode register provided for different size panel loading" in the "*2. FEATURES*" 4. Modify Mnemonic:COM64 - 0 to COM63 - 0, PIN No.: 64 to 64 5. Add "20.) Driving mode register: (DB7, DB6)=(0, 0)" in the "*5.15 The Reset Circuit*" 6. Add Note1 and Note2 in the "*6.21.2 Mode selection register set*" 7. Add "Driving capability (D1, D0): (1,1)>(0,0)>(0,1)>(1,0)" in the "*6.25 Table 13 Table of SPLC501C Commands*" 8. Add "*8.10 VLCD Voltage (Voltage between VDD to V_5) relationship of V_5 Voltage Regulator Internal Resistor Ratio Register and Electronic Volume Control Register*" 9. Modify "75μm(Min.)" to "60μm(Min.)" in the "*9.1 PAD Assignment*" 10. Add Note4 in the "*9.1 PAD Assignment*"	4 4 4 9 23 32 36 52 53 53
APR. 04, 2002	1.2	1. Add REF pin in "*3. BLOCK DIAGRAM*" 2. Add REF pin description at "*4.3 System Bus Connection Terminal*" 3. Add REF pin connection in 5.14.1.1 and 5.14.1.2	5 8 20 - 22
NOV. 07, 2002	1.3	Delete " *8.5 Display Pattern Checker* / Standby Mode SPLC501C "	42
NOV. 15, 2002	1.4	Correct "*Note4: Gold Bump Height 17μm* " to 18μm	53
JAN. 29, 2003	1.5	Correct type error	4