

HIGH-VOLTAGE MIXED-SIGNAL IC

UC1610

128 x 160 4S STN LCD Controller-Driver



Preliminary Specifications
Revision 0.11

July 30, 2003

ULTRACHIP

The Coolest LCD Driven Ever!!

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UC1610

*Single-Chip, Ultra-Low Power
128COM x 160SEG Matrix
Passive Color LCD Controller-Driver*

INTRODUCTION

UC1610 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1610 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x160 matrix STN LCD with 4 gray shades.
- One software readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row ordered and column ordered display buffer RAM access
- Support industry standard 2-wire, 3-wire, 4-wire serial bus (I²C, S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates up to 130Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 4 temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command, make RST pin optional.
- Self-configuring 8x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S9 or I²C) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range: 1.8V ~ 3.3V
V_{DD} (analog) range: 2.4V ~ 3.3V
LCD V_{OP} range: 5.0V ~ 15V
- Available in COF and gold bump dies
Bump pitch: 50uM
Bump gap: 17uM.
Bump surface: 3,000uM²

ORDERING INFORMATION

Part Number	Versions	Description
UC1610XGAA	Gold Bumped Die	Bare die with gold bumps
UC1610iGAA	Gold Bumped Die	Bare die with gold bumps with I ² C interface
UC1610XFAA	COF	IC in the COF packaging
UC1610iFAA	COF	IC in the COF packaging with I ² C interface

General Notes**APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

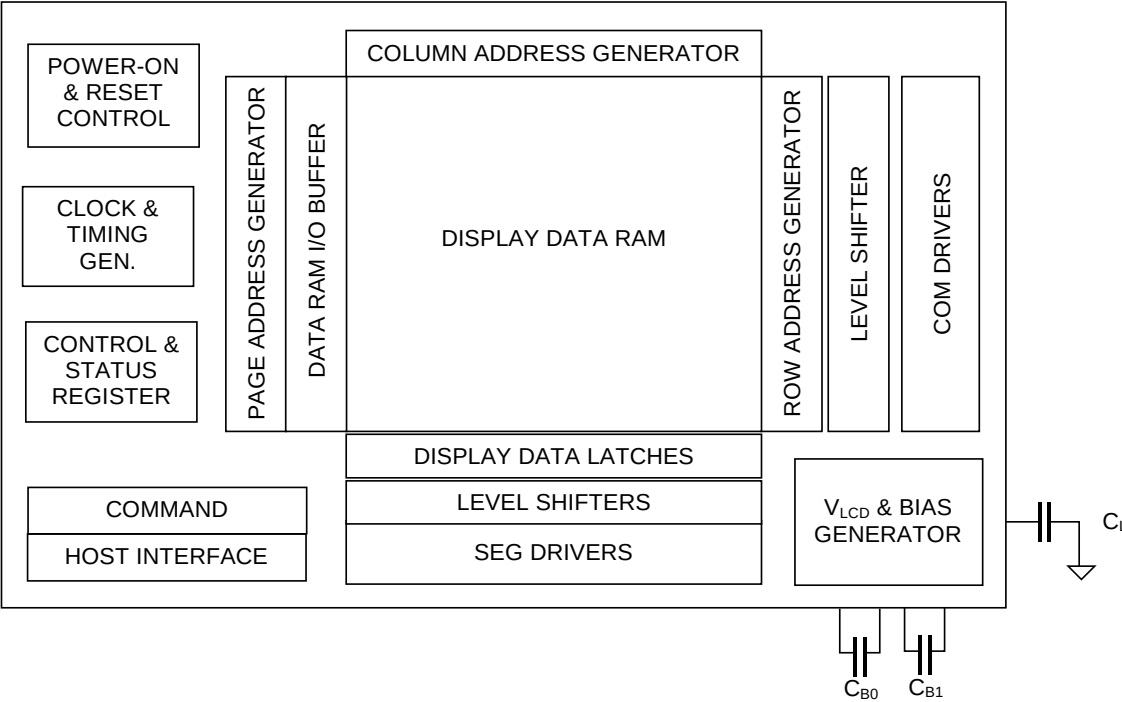
USE OF I²C

The implementation of I²C is already included and tested in all silicon. However, unless I²C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I²C applications. Unless I²C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR		V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND		Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{BIAS}	I		This is the reference voltage to generate the actual SEG driving voltage. V_{BIAS} can be used to fine tune V_{LCD} by external variable resistors. Internal resistor network has been provided to simplify external trimming circuit. The following network is sufficient for most applications. The diagram shows a variable resistor (potentiometer) connected between V_{DD2}/V_{DD3} and ground. The wiper of the potentiometer is connected to the V_{BIAS} pin. The potentiometer has a 330K resistor between V_{DD2}/V_{DD3} and the wiper, and a 1M/VR resistor between the wiper and ground. An internal RC filter is provided to filter noise on the V_{BIAS} pin. When not use, it is OK to leave V_{BIAS} open circuit. If noise starts to cause problem, connect a small bypass capacitor between V_{BIAS} and V_{SS}.
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR		LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR		High voltage LCD Power Supply. Connect these pins together. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the trace resistance under 300 Ohm.

NOTE

- Recommended capacitor values:
 C_B : 150~250x LCD load capacitance or 2uF (2V), whichever is higher.
 C_L : 0.06uF~0.3uF (16V) is appropriate for most applications.

Name	Type	Pins	Description																																													
HOST INTERFACE																																																
BM0 BM1	I		Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:																																													
			<table><tr><td>BM[1:0]</td><td>D[7:6]</td><td>Mode</td></tr><tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr><tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr><tr><td>01</td><td>00</td><td>6800/4-bit</td></tr><tr><td>00</td><td>00</td><td>8080/4-bit</td></tr><tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token (S9: conventional)</td></tr><tr><td>01</td><td>11</td><td>2-wire I²C</td></tr><tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token (S8: conventional)</td></tr><tr><td>00</td><td>11</td><td>3-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)</td></tr></table>	BM[1:0]	D[7:6]	Mode	11	Data	6800/8-bit	10	Data	8080/8-bit	01	00	6800/4-bit	00	00	8080/4-bit	01	10	3-wire SPI w/ 9-bit token (S9: conventional)	01	11	2-wire I ² C	00	10	4-wire SPI w/ 8-bit token (S8: conventional)	00	11	3-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)																		
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CS1/A2 CS0/A3	I	2	Chip Select. Chip is selected when CS1="H" and CS0 = "L". When the chip is not selected, D[7:0] will be high impedance. In I ² C mode, these two pins indicate the I ² C bus address' bit 2 and bit 3.																																													
RST	I		When RST="L", all control registers are re-initialized by their default states. Since UC1610 has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V _{DD} .																																													
CD	I		Select Control data or Display data for read/write operation. In S9 and I ² C modes, CD pin is not used. Connect CD to V _{SS} when not used. "L": Control data "H": Display data																																													
ID	I		ID pin is for production control. The connection will affect the content of D[7] when using <i>Get Status</i> command. Connect to V _{DD} for "H" or V _{SS} for "L".																																													
WR0 WR1	I		WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail. In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V _{SS} .																																													
D0~D7	I/O		Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,																																													
			<table><tr><td></td><td>BM=1x (Parallel)</td><td>BM=0x (Parallel)</td><td>BM=01 (S9/I²C)</td><td>BM=00 (S8/S8uc)</td></tr><tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr><tr><td>D1</td><td>D1</td><td>D1/D5</td><td>—</td><td>—</td></tr><tr><td>D2</td><td>D2</td><td>D2/D6</td><td>—</td><td>—</td></tr><tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr><tr><td>D4</td><td>D4</td><td>—</td><td>—</td><td>—</td></tr><tr><td>D5</td><td>D5</td><td>—</td><td>—</td><td>—</td></tr><tr><td>D6</td><td>D6</td><td>—</td><td>S9/I²C</td><td>S8/S8uc</td></tr><tr><td>D7</td><td>D7</td><td>0</td><td>1</td><td>1</td></tr></table>		BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9/I ² C)	BM=00 (S8/S8uc)	D0	D0	D0/D4	SCK	SCK	D1	D1	D1/D5	—	—	D2	D2	D2/D6	—	—	D3	D3	D3/D7	SDA	SDA	D4	D4	—	—	—	D5	D5	—	—	—	D6	D6	—	S9/I ² C	S8/S8uc	D7	D7	0	1	1
				BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9/I ² C)	BM=00 (S8/S8uc)																																									
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			D1	D1	D1/D5	—	—																																									
			D2	D2	D2/D6	—	—																																									
			D3	D3	D3/D7	SDA	SDA																																									
			D4	D4	—	—	—																																									
			D5	D5	—	—	—																																									
			D6	D6	—	S9/I ² C	S8/S8uc																																									
D7	D7	0	1	1																																												
Connect unused pins to V _{SS} .																																																

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG160	HV		SEG (column) driver outputs. Support up to 160 pixels. Leave unused drivers open-circuit.
COM1 ~ COM128	HV		COM (row) driver outputs. Support up to 128 rows. Leave unused COM drivers open-circuit.
MISC. PINS			
V _{DDX}			Auxiliary V _{DD} . These pins are connected to the main V _{DD} bus on chip. They are provided to facilitate chip configurations in COG and COF applications. These pins should not be used to provide V _{DD} power to the chip. It is not necessary to connect V _{DDX} to main V _{DD} externally.
TST4	I		Test control. Connect TST4 to V _{SS} during normal use.
TST2	I/O		Test I/O pin. Leave these pins open during normal use.
TP[5:1]	I		Test control. Leave these pins open during normal use.

Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM_X or SEG_X will correspond to index X-1, and the value ranges for those index registers will be 0~127 for COM and 0~159 for SEG.

CONTROL REGISTERS

UC1610 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1610 will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.

Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127–2xFL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable. When partial display mode is activated, the display of these 2xFL lines are also controlled by LC[0].
CR	8	0H	Return Column Address. Useful for cursor implementation.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	5	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS} . 00b: 5 01b: 10 10b: 11 11b: 12
TC	2	0H	Temperature Compensation (per °C) 00b: -0.05% 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	B2H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
OM	2	–	Operating Modes (Read only) 10b: Sleep 11b: Normal 01b: (Not used) 00b: Reset
ID	1	PIN	Access the connected status of ID pin.
RS	1		Reset in progress. Host Interface not ready
PC	4	DH	Power Control. PC[1:0]: 00b: LCD: ≤ 16nF 01b: LCD: 16~21nF 10b: LCD: 21~28nF 11b: LCD: 28~38nF PC[3:2]: 00b: External V_{LCD} 01b: Internal V_{LCD} (6X pump, low V_{LCD} , only used when BR=5) 10b: Internal V_{LCD} (7X pump) 11b: Internal V_{LCD} (8X pump, standard)
DC	3	00H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default 0: OFF) DC[1]: APO: All Pixels ON (Default 0: OFF) DC[2]: Display ON/OFF (Default 0: OFF)

Name	Bits	Default	Description
AC	5	01H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default 1: ON) AC[1]: Auto-Increment order 0: Column (CA) first 1: Row (PA) first AC[2]: PID: PA (Page Address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, (Default 0: OFF) when CUM=1, CA increment on write only, wrap around suspended AC[4]: Window Program Enable 0 : Disable 1 : Enable
WPC0	8	00H	Window program starting column address. Value range: 0~159.
WPP0	5	00H	Window program starting Page Address. Value range: 0~31.
WPC1	8	9FH	Window program ending column address. Value range: 0~159.
WPP1	5	1FH	Window program ending Page Address. Value range: 0~31.
CEN DST DEN	7 7 7	7FH 00H 7FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ≥ DEN ≥ DST+ 9
LC	9	008H	LCD Control: LC[0]: Enable the first FLx2 lines in partial display mode (Default OFF). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: OFF) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: OFF) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 12.1 Klps (95fps) 01b: 13.4 Klps (105fps) 10b: 14.7 Klps (115fps) 11b: 16.6 Klps (130fps) (Frame-Rate = Line-Rate / Mux-Rate, Frame rate at 128 is listed) LC[6:5]: Gray-Shade control. Control the difference of percentage between data "01" to data "10" 00b: 20% 01b: 24% 10b: 28% 11b: 32% LC[8:7]: Partial Display Control 00b: Disable Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enable Mux-Rate = CEN+1 11b: Enabled Mux-Rate = DEN-DST+1
APC0 APC1	8 8	0DH 36H	Advanced Product Configuration. For UltraChip only. Please do not use.

COMMAND SUMMARY

The following is a list of host commands supported by UC1610

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Page Address	0	0	0	1	1	#	#	#	#	#	Set PA[4:0]	0
11	Set V _{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	B2H
		0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[8:7]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set LCD Gray Shade	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	00b
21	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
22	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
23	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
24	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
25	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
26	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
31	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[4:0]	0
		0	0	-	-	-	#	#	#	#	#		
32	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
33	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[4:0]	31
		0	0	-	-	-	#	#	#	#	#		
34	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

* All other bit patterns other than the commands listed above may result in undefined behavior.

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to DDRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from DDRAM							

Write/Read Data Byte (command 1,2) operation use internal Page Address register (PA) and Column Address register (CA). Four rows of LCD pixel image are defined as one page in DDRAM. Each column of pixel corresponds to one column of DDRAM data. PA and CA registers can be programmed by issuing *Set Page Address* and *Set Column Address* commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of PA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and PA will be incremented or decremented, depending on the setting of Row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1

Status flag definitions:

ID: Provide access to ID pin connection status.

MX: Status of register LC[1], mirror X.

MY: Status of register LC[2], mirror Y.

WA: Status of register AC[0]. Automatic column/page wrap around.

DE: Display enable flag. DE=1 when display is enabled

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	0	0	0	1	CA7	CA6	CA5	CA4

Set DDRAM column address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: 0~159

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.05%/°C **01b**= -0.10%/°C **10b**= -0.15%/°C **11b**= -0.20%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: **00b**=<16nF **01b**=16~21nF **10b**=21~28nF **11b**=28~38nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	0	0	1	0	1	1	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External VLCD **01b**= Internal VLCD (6X pump, for BR=5)
01b= Internal VLCD (7X pump) **11b**= Internal VLCD (8X pump, standard)

(8) SET ADVANCED PRODUCT CONFIGURATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R]	0	0	0	0	1	1	0	0	0	R
(Double byte command)	0	0	APC register parameter							

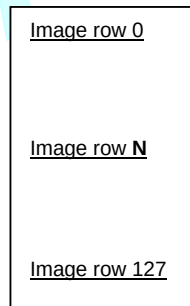
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

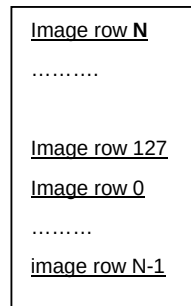
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	0	1	0	1	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and (127-2xFL). FL is the register value programmed by *Set Fixed Lines* command.



SL=0



SL=N

(10) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA [4:0]	0	0	0	1	1	PA4	PA3	PA2	PA1	PA0

Set DDRAM Page Address for read/write access.

Possible value = **0~31**

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double byte command)	0	0	1	0	0	0	0	0	0	1
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [8:7]	0	0	1	0	0	0	0	1	LC8	LC7

This command is used to enable partial display function.

LC[8:7] : 00b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)

10b: Enable Partial Display, Mux-Rate = CEN+1

11b: Enable Partial Display, Mux-Rate = DEN-DST+1

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.

0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary

1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1]: Auto-Increment order

0 : column (CA) increment (+1) first until CA reaches CA boundary, then PA will increment by (+/-1).

1 : row (PA) increment (+/-1) first until PA reach PA boundary, then CA will increment by (+1) .

AC[2]: PID, Page Address (PA) auto increment direction (0/1 = +/- 1)

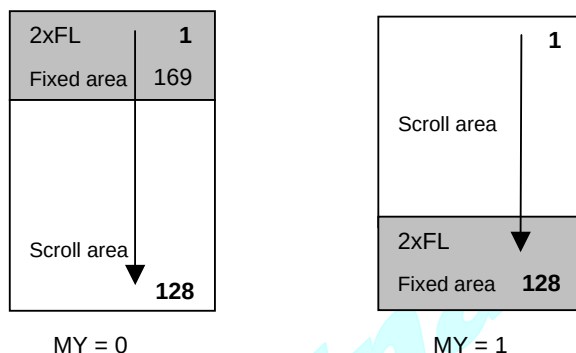
When WA=1 and CA reaches CA boundary, PID controls whether Page Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and PA. When Window Program is enabled (AC[4]=ON), see command description (32) ~ (36) for more details. When Window Program is disabled (AC[4]=OFF), the behavior of CA, PA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[4]=ON.

(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	1	0	0	1	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.

**(15) SET LINE RATE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 1/2 and 1/4 at Mux-Rate = 56 and 24.

The following are line rates at Mux Rate = 57~128.

LC[4:3]: 00b: 12.1 Klps
 01b: 13.4 Klps
 10b: 14.7 Klps
 11b: 16.6 Klps (Klps: Kilo-Line-per-second)

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(18) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [2]	0	0	1	0	1	0	1	1	1	DC2

This command is for programming register DC[2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1610 will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

(19) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for program LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~2xFL) is display or not during partial display mode.

(20) SET LCD GRAY SHADE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade [6:5]	0	0	1	1	0	1	0	0	LC6	LC5

Program gray scale register (LC[6:5]). This register controls the voltage RMS separation between the two gray shade levels (data "01" and data "10")

00b=20% 01b=24% 10b=28% 11b=32%

(21) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(22) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

(23) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(Double byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(24) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b = 5 01b = 10 10b = 11 11b = 12

(25) RESET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode AC[3]=0 CA=CR	0	0	1	1	1	0	1	1	1	AC3

This command is used to reset cursor update mode function.

(26) SET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	1	1	1	0	1	1	1	AC3

This command is used for set cursor update mode function. When cursor update mode sets, UC1610 will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation.

The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when reset cursor update mode.

The purpose of this pair of commands and their features is to support “write after read” function for cursor implementation.

(27) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	1	1	1	1	0	0	0	1
(Double byte command)	0	0	CEN register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

(28) SET DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	1	1	1	1	0	0	1	0
(Double byte command)	0	0	DST register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

(29) SET DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN (Double byte command)	0	0	1	1	1	1	0	0	1	1
			DEN register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

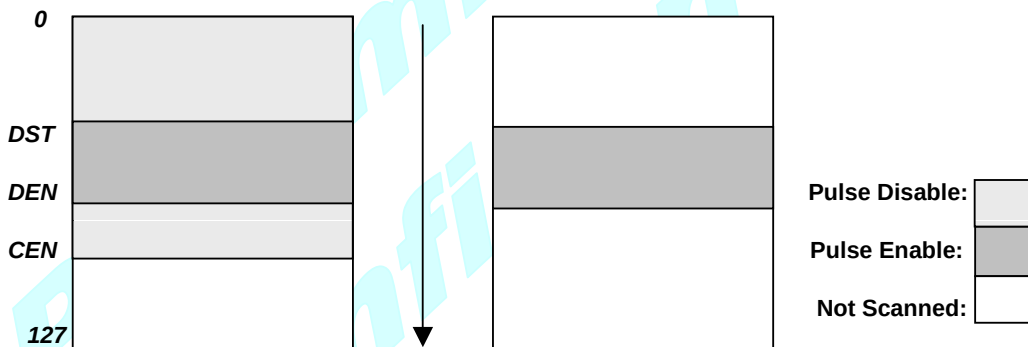
CEN, DST, DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1, two partial display modes are possible with UC1610:

LC[7]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ≤ 32 , set BR=5, PC[3:2]=01b).

LC[7]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[8:7]=11b, the Mux-Rate is narrowed down to just the range between DST and DEN. When Mux-Rate is under 32, set BR=5, PC[3:2]=01b, and adjust PM to reduce VLCD and achieve the lowest power consumption. When LC[8:7]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly. In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.


(30) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double byte command)	0	0	1	1	1	1	0	1	0	0
			WPC0[7:0] register parameter							

This command is to program the starting column address of RAM program window.

(31) SET WINDOW PROGRAM STARTING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double byte command)	0	0	1	1	1	1	0	1	0	1
			WPP0[4:0] register parameter							

This command is to program the starting Page Address of RAM program window.

(32) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double byte command)	0	0	1	1	1	1	0	1	1	0
			WPC1[7:0] register parameter							

This command is to program the ending column address of RAM program window.

(33) SET WINDOW PROGRAM ENDING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double byte command)	0	0	1	1	1	1	0	1	1	1
			WPP1[4:0] register parameter							

This command is to program the ending Page Address of RAM program window.

(34) SET WINDOW PROGRAM ENABLE

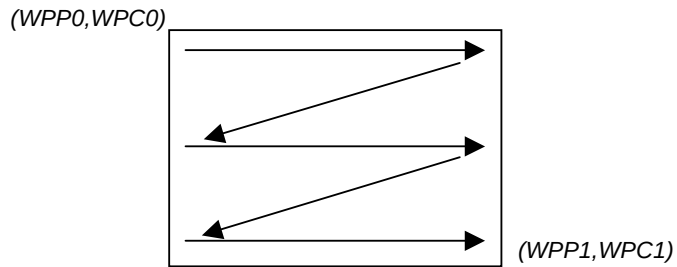
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[4]	0	0	1	1	1	1	1	0	0	AC4

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

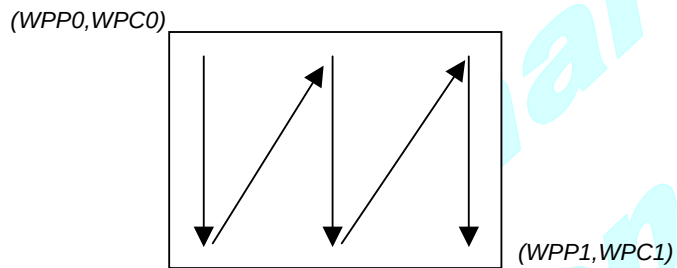
Window Program Function can be used to refresh the RAM data in a specified window of DDRAM address. When window programming is enabled, the CA and PA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row / column after reaching the specified window column / row boundary. PID controls the RAM address incrementing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address incrementing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

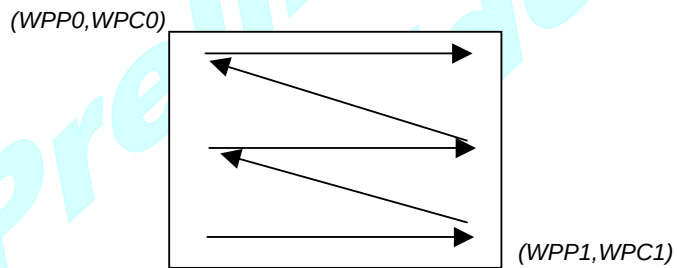
Auto-increment order = 0 MX=0 PID = 0



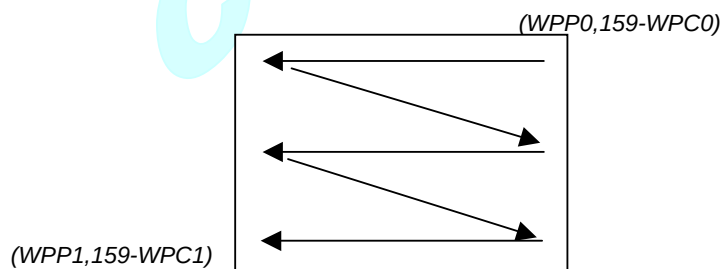
Auto-increment order = 1 MX=0 PID = 0



Auto-increment order = 0 MX=0 PID = 1

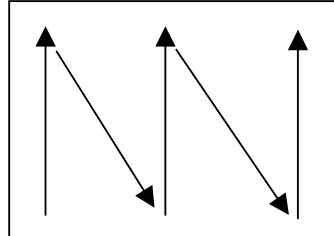


Auto-increment order = 0 MX=1 PID = 0



Auto-increment order = 1 MX=0 PID = 1

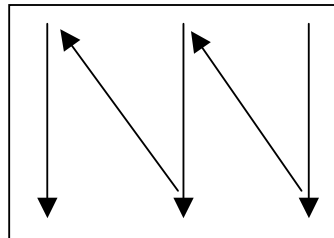
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=1 PID = 0

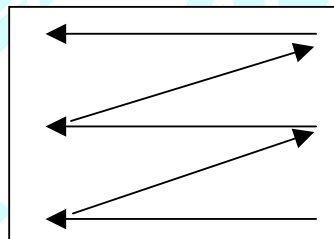
(WPP0,159-WPC0)



(WPP1,159-WPC1)

Auto-increment order = 0 MX=1 PID = 1

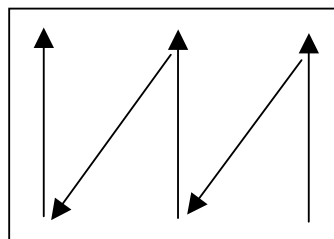
(WPP0,159-WPC0)



(WPP1,159-WPC1)

Auto-increment order = 1 MX=1 PID = 1

(WPP0,159-WPC0)



(WPP1,159-WPC1)

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1610 via registers CEN, DST, DEN, and partial display control LC[8:7].

Combined with low power partial display mode and a low bias ratio of 5, UC1610 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS} , i.e.

$$BR = V_{LCD} / V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux} + 1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1610 supports four *BR* as listed below. *BR* can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 15V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T \%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of *BR* register, as illustrated in the table on the next page,

PM is the numerical value of *PM* register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by *TC* register.

V_{LCD} FINE TUNING

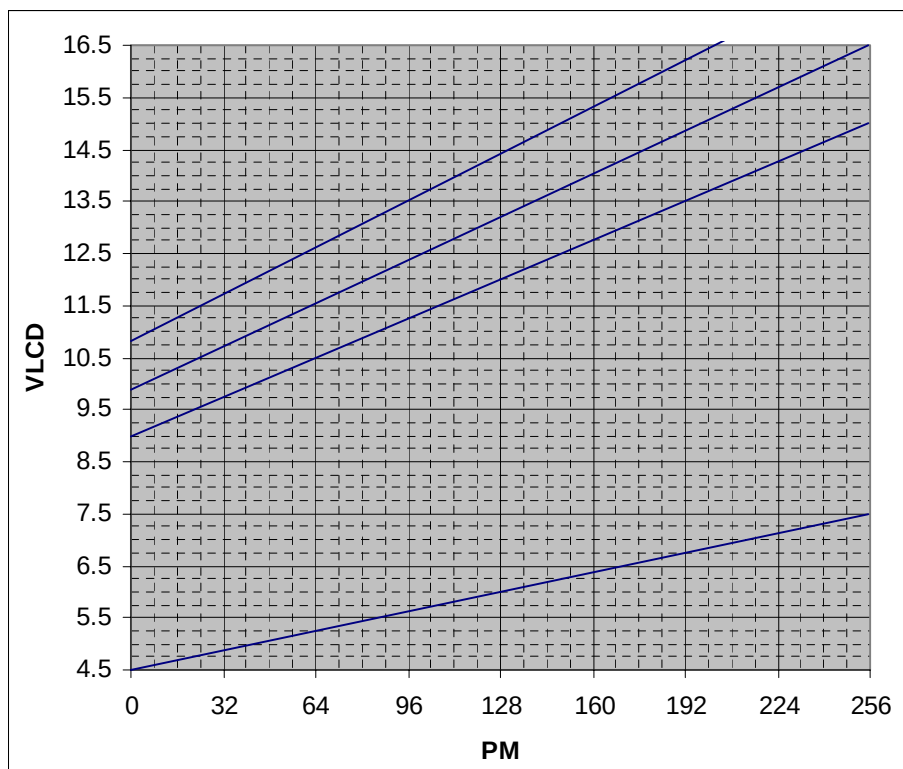
Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different vendors. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning.

For applications where mechanical manual fine tuning of V_{LCD} becomes necessary, then V_{BIAS} pin may be used with an external trim pot to fine tune the V_{LCD} . Please refer to Application Notes for more detailed discussion on this subject.

LOAD DRIVING STRENGTH

The power supply circuit of UC1610 is designed to handle LCD panels with load capacitance up to ~30nF when $V_{DD2} = 2.5V$. 30nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels use higher V_{DD} and COF packaging.

V_{LCD} QUICK REFERENCEV_{LCD} relationship to BR and PM at 25 °C

BR	C _{V0} (V)	C _{PM} (mV)	PM	V _{LCD} (V)
5	4.500	11.77	0	4.50
			255	7.50
10	9.000	23.53	0	9.00
			255	15.00
11	9.900	25.88	0	9.90
			255	16.50
12	10.800	28.24	0	10.80
			255	18.00

Note: For best reliability, keep V_{LCD} under 15V over all temperature.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

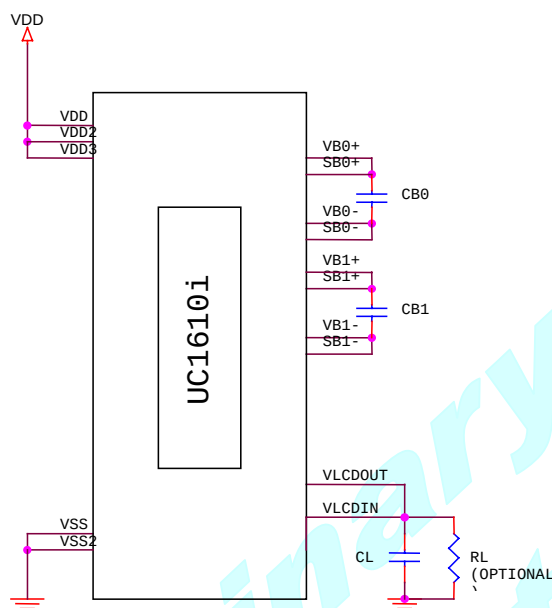


FIGURE 1: Reference circuit using internal Hi-V generator circuit

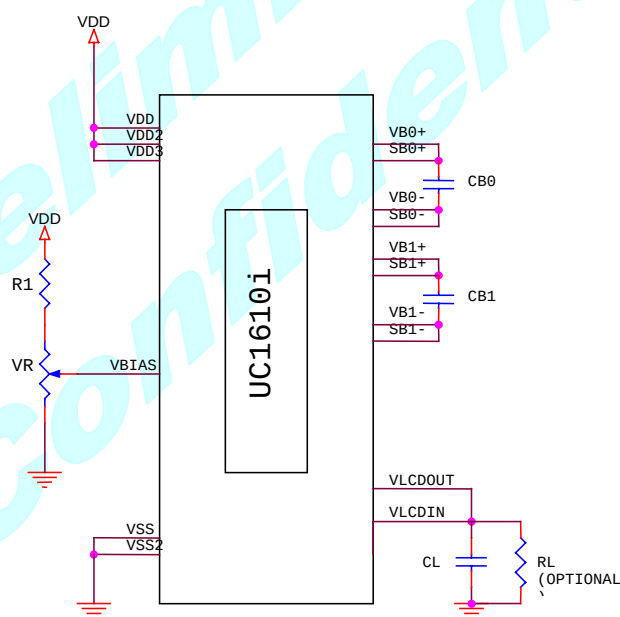


FIGURE 2: Reference circuit using external Bias source

Note

- Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)
 - C_B: 150 ~ 250x LCD load capacitance or 2uF (2V), whichever is higher.
 - C_L: 0.06uF ~ 0.3uF (16V) is appropriate for most applications.
 - R_L: 10MΩ. Acts as a draining circuit when the power is abnormally shut down.
 - VR: 1MΩ.
 - R1: 330KΩ

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1610 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 56, frame rate is calculated as:

$$\text{Frame Rate} = \text{Line-Rate} / \text{Mux-Rate}.$$

When Mux-Rate is lowered to 56 (and 24), line rate will be scaled down by 2 (and 4) times automatically to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with $(t_r + t_f) < 160\text{ms}$ is used, faster line rate may be required under 8-shade mode to maintain good contrast ratio at operating temperature $>50^\circ\text{C}$.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to V_{SS} .

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where $x=1\sim128$, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1610 will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1610 will first exit from Sleep Mode, restore the power (V_{LCD} , V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1610 provides flexible control of Mux Rate and active display area. Please refer to command description (28) ~ (30) for more detail.

GRAY-SHADE MODULATION

UC1610 uses a proprietary frame rate modulation scheme to generate 4 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[6:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

LAYOUT CONSIDERATIONS FOR COM SIGNALS

Since the COM scanning pulse of UC1610 can be as short as 60us, it is critical to control the RC delay of COM signal to minimize distortion of COM scanning pulse.

For the best image quality, it is recommended to limit the worst case COM signal RC delay as calculated below.

$$(R_{\text{ROW}} / 3 + R_{\text{COM}} + R_{\text{OUT}}) \times C_{\text{ROW}} < 4.0\mu\text{S}$$

where

C_{ROW} : LCD loading capacitance of one row of pixels. It can be calculated by $C_{\text{LCD}}/\text{Mux-Rate}$, where C_{LCD} is the LCD panel capacitance.

R_{ROW} : ITO resistance over one row of pixels within the active area

R_{COM} : COM routing resistance from IC to the active area

R_{OUT} : COM output impedance

In case such RC_{MAX} exceed the above constraint significantly, please make sure

$$|RC_{\text{MAX}} - RC_{\text{MIN}}| < 2.0\mu\text{S}$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

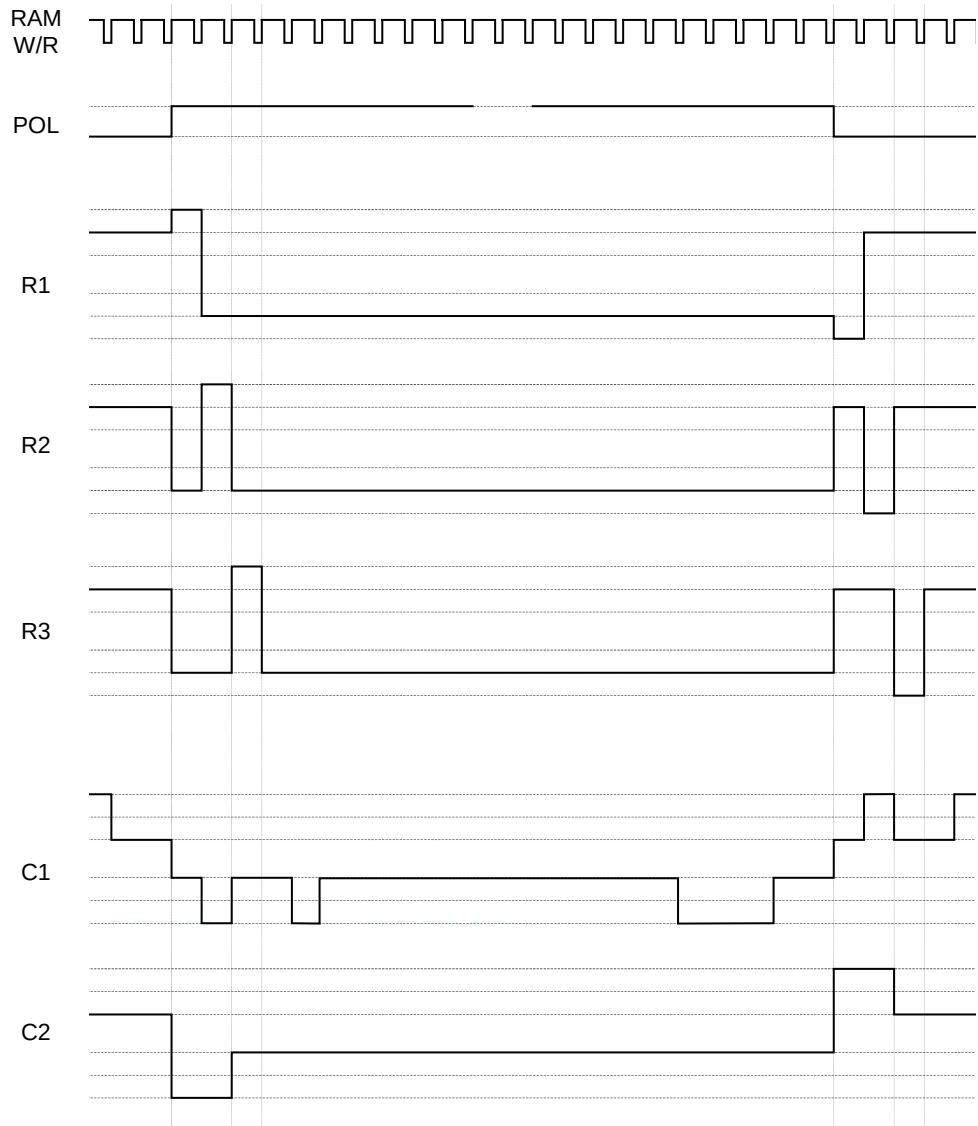


FIGURE 3: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1610 supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and four serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type	8080		6800		S8 (4wr)	S8uc (3wr)	S9 (3wr)	I ² C
Width	8-bit	4-bit	8-bit	4-bit	Serial			
Access	Read/Write				Write Only			R/W
Control & Data Pins	BM[1:0]	10	00	11	01	00	01	
	D[7:6]	Data	00	Data	00	10	11	11
	CS[1:0]	Chip Select						A[3:2]
	CD	Control/Data						–
	WR0	$\overline{\text{WR}}$		$\text{R}/\overline{\text{W}}$		–		
	WR1	$\overline{\text{RD}}$		EN		–		
	D[5:4]	Data	–	Data	–	–		
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1610 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA*, or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT & 4-BIT BUS OPERATION

UC1610 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time Chip-Select or CD pin changes state.

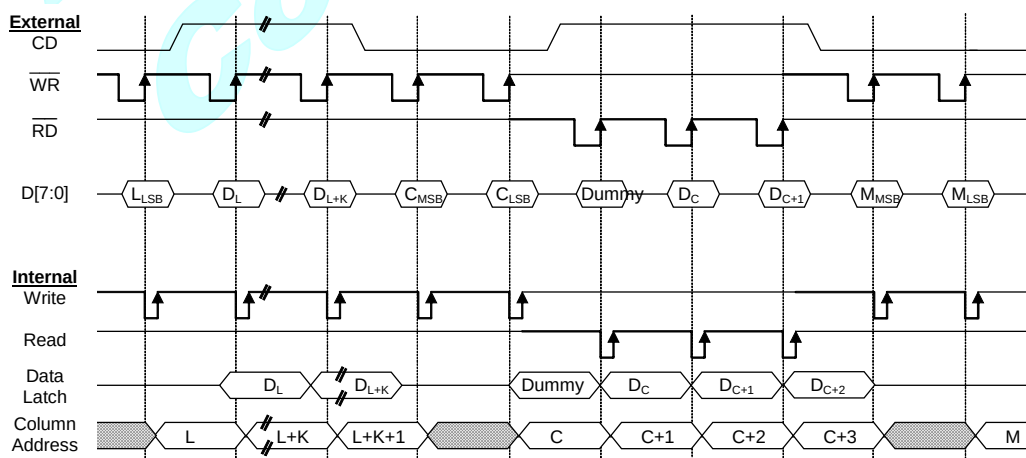


FIGURE 4: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

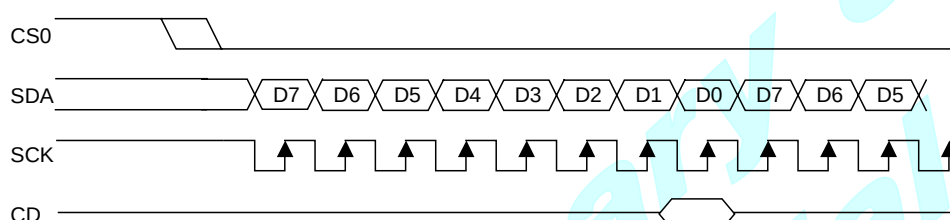
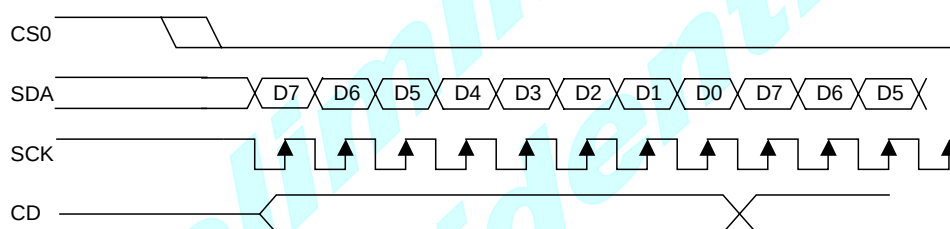
UC1610 supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the

content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

**FIGURE 5.a: 4-wire Serial Interface (S8)****FIGURE 5.b: 3/4-wire Serial Interface (S8uc)****S8UC (3/4-WIRE) INTERFACE**

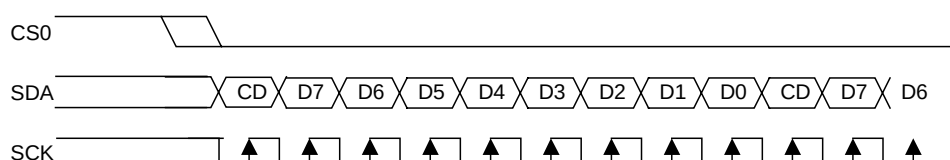
Only write operations are supported in this 3/4-wire serial mode. The data format is identical as S8. However, in addition to CS pins, CD pin transitions will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS} . The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

**FIGURE 5.c: 3-wire Serial Interface (S9)**

2-WIRE SERIAL INTERFACE (I²C)

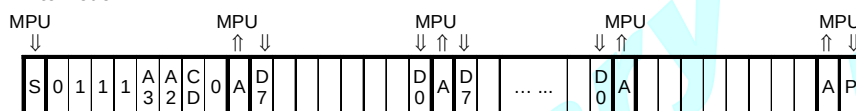
When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1610 is configured as an I²C bus signaling protocol compliant slave device. Please refer to I²C standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1610's device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I²C mode.

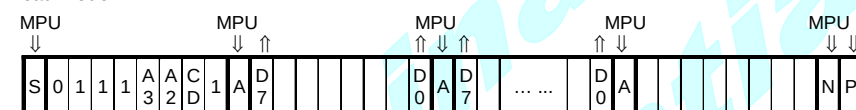
Each UC1610 I²C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I²C mode and should be connected to V_{SS}.

Write Mode



Read Mode



The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R↔W) or the content type (C↔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1610 will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1610) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.

HOST INTERFACE REFERENCE CIRCUIT

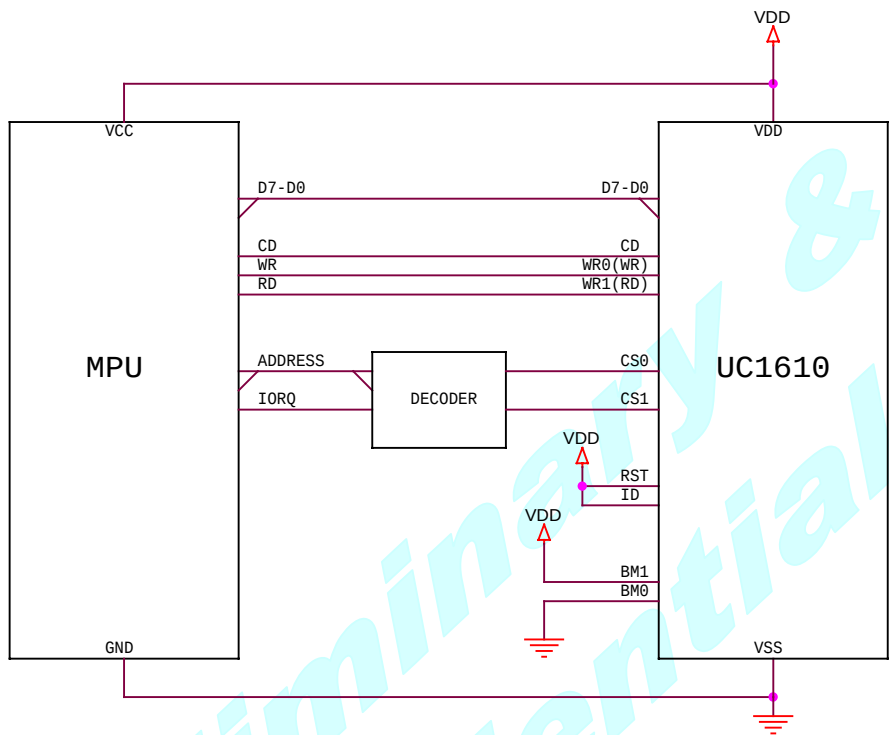


FIGURE 6: 8080/8bit parallel mode reference circuit

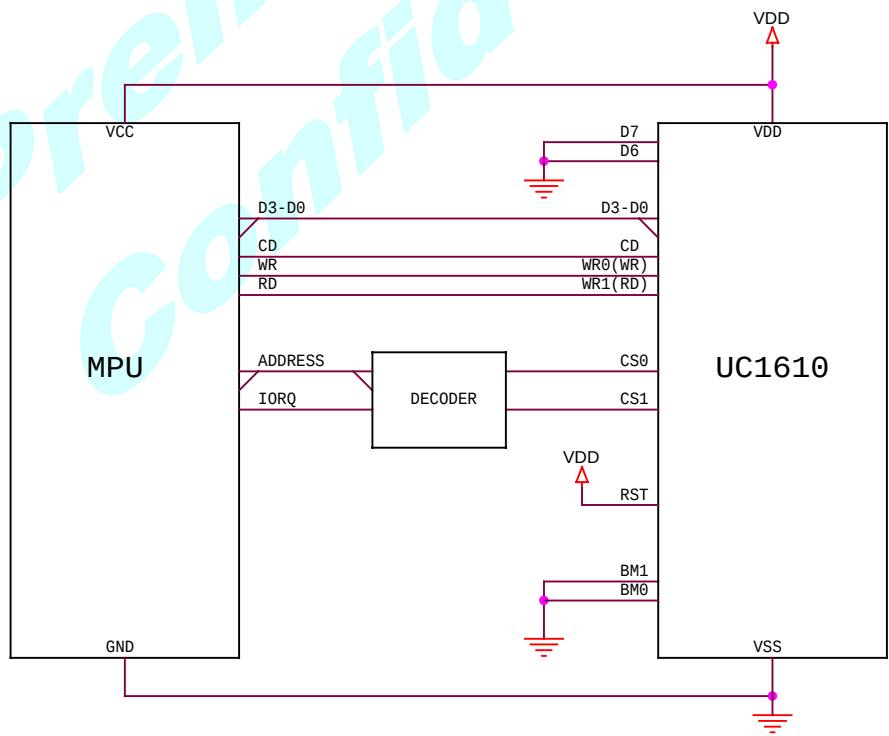


FIGURE7: 8080/4bit parallel mode reference circuit

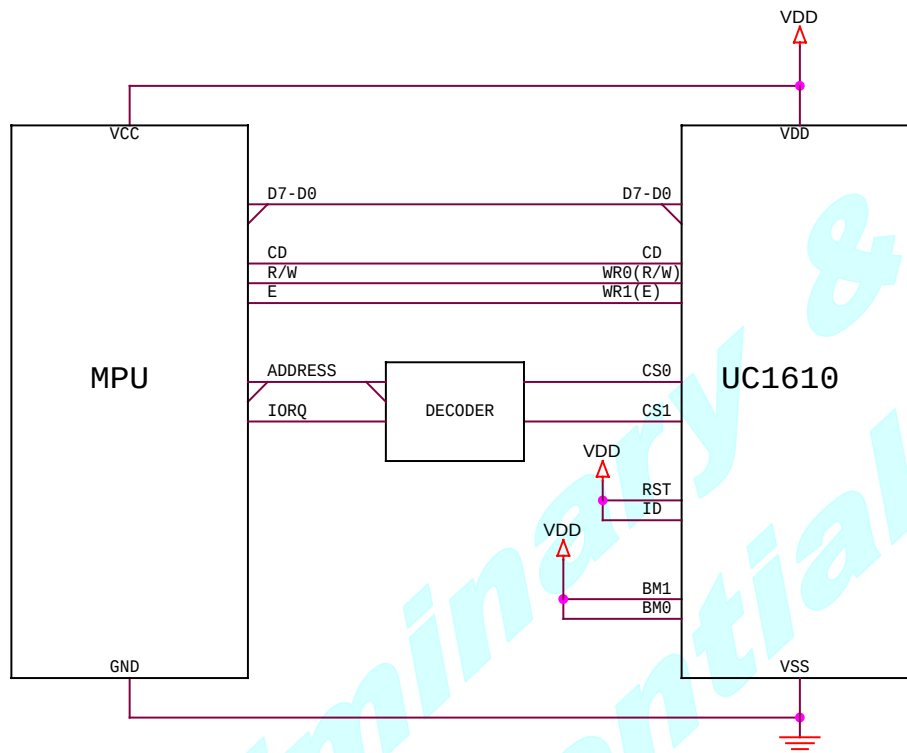


FIGURE 8: 6800/8bit parallel mode reference circuit

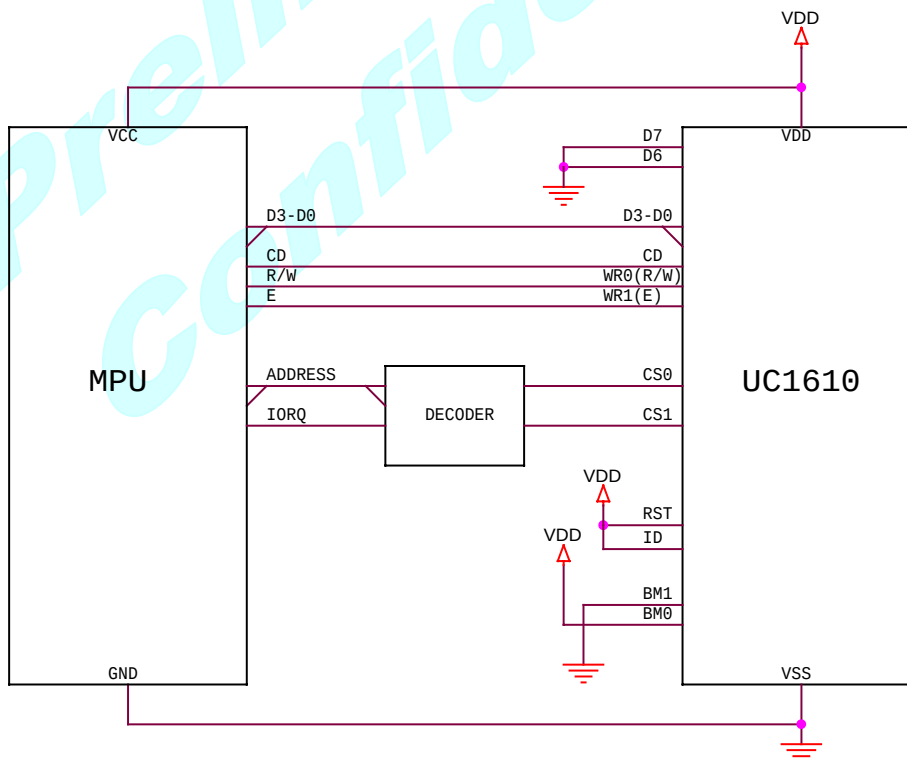


FIGURE 9: 6800/4bit parallel mode reference circuit

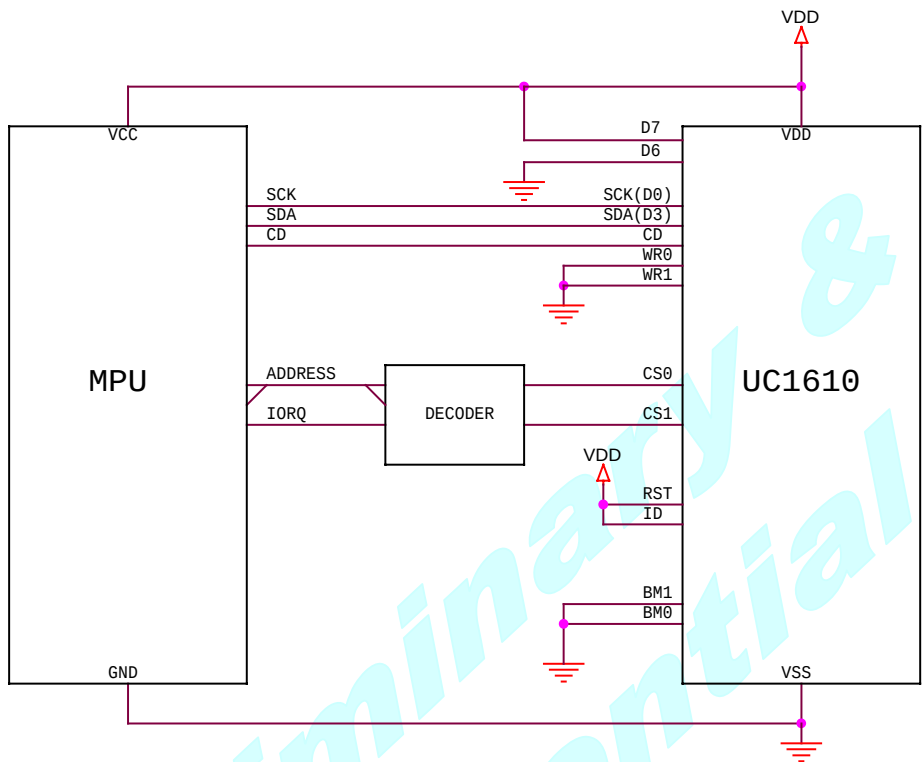


FIGURE 10: 4-Wires SPI (S8) serial mode reference circuit

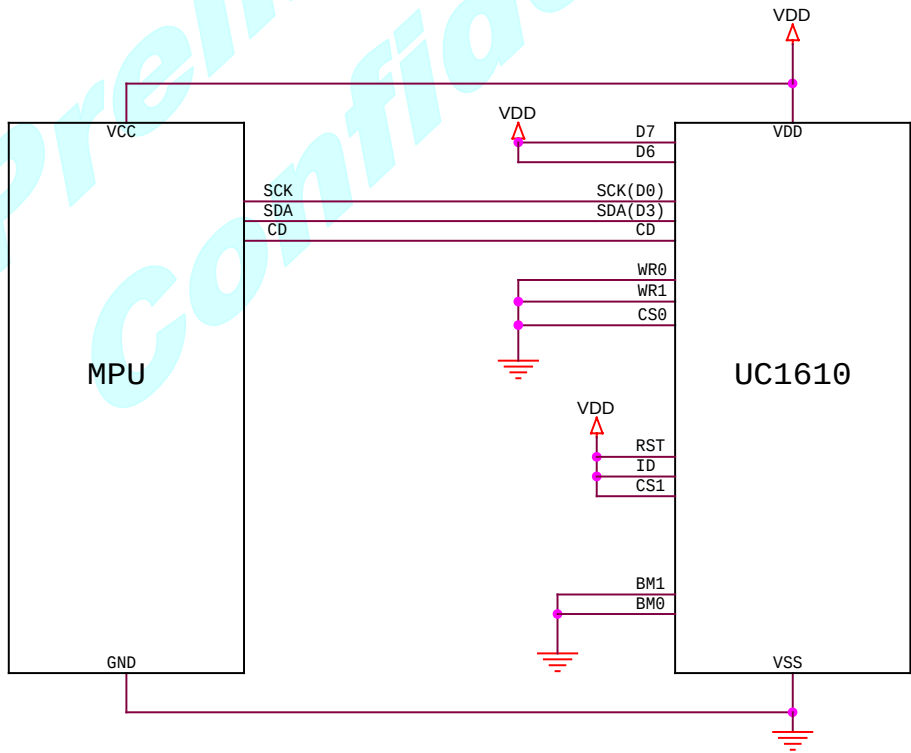
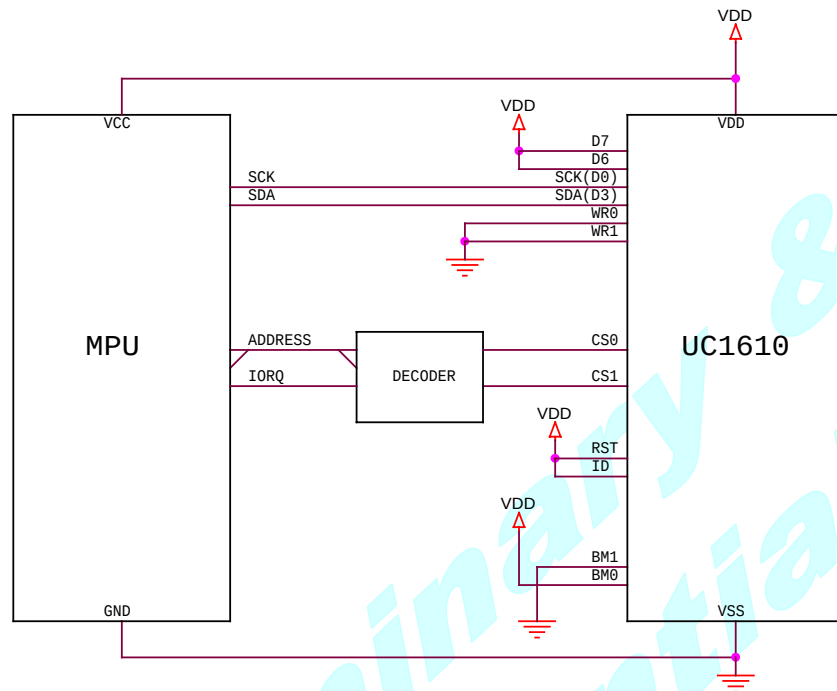
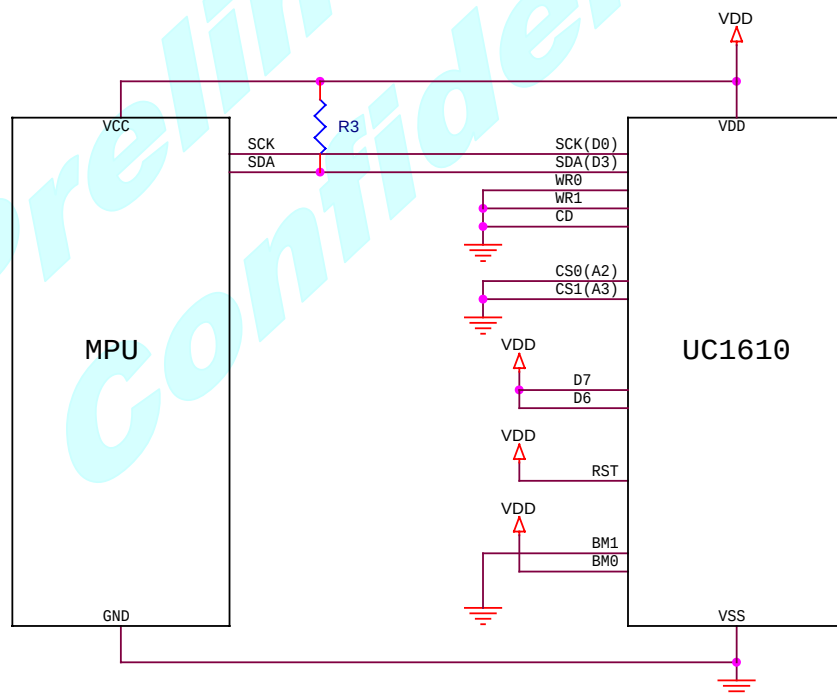


FIGURE 11: 3/4-Wires SPI (S8uc) serial mode reference circuit


FIGURE 12: 3-Wires SPI (S9) serial mode reference circuit

FIGURE 13: I²C serial mode reference circuit

Note

- ID pin is for production control. The connection will affect the content of D[7] when using *Get Status* command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x160x2.

After setting CA and PA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, DDRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

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DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (127), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (159-CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the

display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FL) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by SL rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display DDRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

$$Line = SL$$

Otherwise

$$Line = \text{Mod}(Line+1, 128)$$

Where Mod is the modular operator, and Line is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above Line generation formula produces the "loop around" effect as it effectively resets Line to 0 when Line+1 reaches 128. Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

$$Line = \text{Mod}(SL + MUX-1, 128)$$

$$\text{where } MUX = CEN + 1$$

Otherwise

$$Line = \text{Mod}(Line-1, 128)$$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

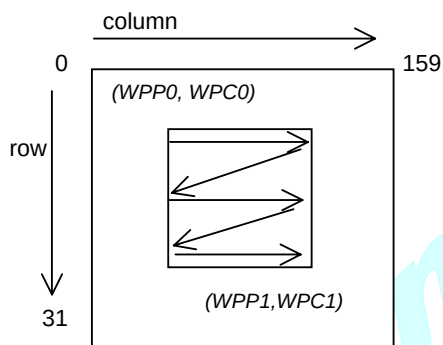
WINDOW PROGRAM

Window program is designed for data write in a specified window range of DDRAM address. The procedure should start with window boundary registers setting ($WPP0$, $WPP1$, $WPC0$ and $WPC1$) and then enable $AC[4]$. After $AC[4]$ sets, data can be written to DDRAM within the window address range which is specified by ($WPP0$, $WPC0$) and ($WPP1$, $WPC1$). $AC[4]$ should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

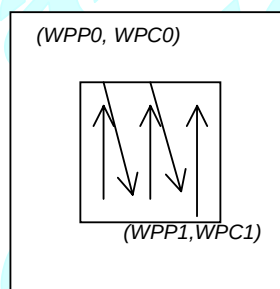
The data write direction will be determined by $AC[2:0]$ and MX settings. When $AC[0]=1$, the data write can be consecutive within the range of the specified window. $AC[1]$ will control the data write in either column or row direction. $AC[2]$ will result the data write starting either from row $WPP0$ or $WPP1$. MX is for the initial column address either from $WPC0$ to $WPC1$ or from ($MC-WPC0$ to $MC-WPC1$).

Example1:

$AC[2:0] = 001$ $MX=0$


Example 2:

$AC[2:0] = 111$ $MX = 0$



		RAM																MY=0				MY=1					
Data		Line Addresss																SL=0		SL=8		SL=0		SL=8			
D1/0	00H																	R1	R113	R128	R16						
D3/2	01H																	R2	R114	R127	R15						
D5/4	02H																	R3	R115	R126	R14						
D7/6	03H																	R4	R116	R125	R13						
D1/0	04H																	R5	R117	R124	R12						
D3/2	05H																	R6	R118	R123	R11						
D5/4	06H																	R7	R119	R122	R10						
D7/6	07H																	R8	R120	R121	R9						
D1/0	08H																	R9	R121	R120	R8						
D3/2	09H																	R10	R122	R119	R7						
D5/4	0AH																	R11	R123	R118	R6						
D7/6	0BH																	R12	R124	R117	R5						
D1/0	0CH																	R13	R125	R116	R4						
D3/2	0DH																	R14	R126	R115	R3						
D5/4	0EH																	R15	R127	R114	R2						
D7/6	0FH																	R16	R128	R113	R1						
D1/0	10H																	R17	R1	R112	R128						
D3/2	11H																	R18	R2	R111	R127						
D5/4	12H																	R19	R3	R110	R126						
D7/6	13H																	R20	R4	R109	R125						
D1/0	14H																	R21	R5	R108	R124						
D3/2	15H																	R22	R6	R107	R123						
D5/4	16H																	R23	R7	R106	R122						
D7/6	17H																	R24	R8	R105	R121						
D1/0	18H																	R25	R9	R104	R120						
D3/2	19H																	R26	R10	R103	R119						
D5/4	1AH																	R27	R11	R102	R118						
D7/6	1BH																	R28	R12	R101	R117						
D1/0	68H																	R105	R89	R24	R40						
D3/2	69H																	R106	R90	R23	R39						
D5/4	6AH																	R107	R91	R22	R38						
D7/6	6BH																	R108	R93	R21	R37						
D1/0	6CH																	R109	R93	R20	R36						
D3/2	6DH																	R110	R94	R19	R35						
D5/4	6EH																	R111	R95	R18	R34						
D7/6	6FH																	R112	R96	R17	R33						
D1/0	70H																	R113	R97	R16	R32						
D3/2	71H																	R114	R98	R15	R31						
D5/4	72H																	R115	R99	R14	R30						
D7/6	73H																	R116	R100	R13	R29						
D1/0	74H																	R117	R101	R12	R28						
D3/2	75H																	R118	R102	R11	R27						
D5/4	76H																	R19	R103	R10	R26						
D7/6	77H																	R120	R104	R9	R25						
D1/0	78H																	R121	R105	R8	R24						
D3/2	79H																	R122	R106	R7	R23						
D5/4	7AH																	R123	R107	R6	R22						
D7/6	7BH																	R124	R108	R5	R21						
D1/0	7CH																	R125	R109	R4	R20						
D3/2	7DH																	R126	R110	R3	R19						
D5/4	7EH																	R127	R111	R2	R18						
D7/6	7FH																	R128	R112	R1	R17						
																						128		128			
																						MUX					
MX	1	0	C160	C1	C2	C3	C4	C5	C6	C7	C8							C5	C156	C4	C157	C3	C158	C2	C159	C1	C160

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1610 has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1610 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1610 has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

For maximum energy utilization, Sleep Mode is designed to retain charges stored in external capacitors C_{B0} , C_{B1} , and C_L . To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11
Reset command or RST_pin pulled "L" Power ON Reset	Reset	00

Table 5: OM changes

Even though UC1610 consumes very little energy in Sleep mode (typically 5uA or less); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1610 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1610 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1610 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~10 ms before the CPU starting to issue commands to UC1610. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD} , $V_{DD2/3}$ should be started not later than V_{DD} .

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 13-1.

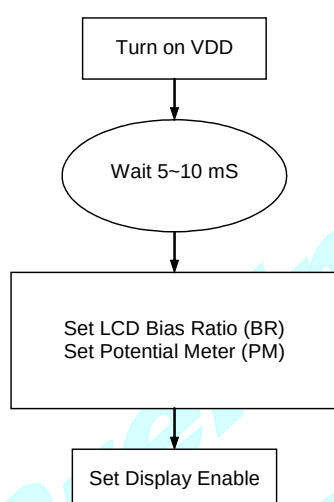


Figure 14: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+} , C_{BX-} , and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+} . It is recommended to wait $3 \times RC$ for V_{LCD} and $1.5 \times RC$ for V_{B+} . For example, if C_L is 10nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1610 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD} .

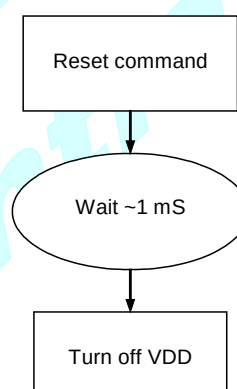


Figure 15: Reference Power-Down Sequence

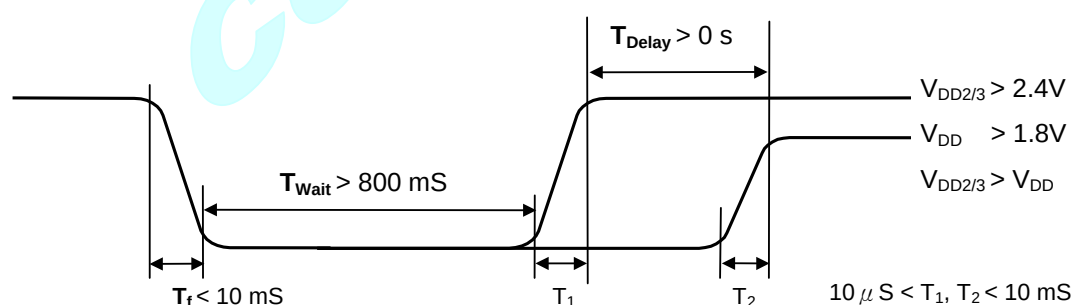


Figure 14-1: Delay allowance between V_{DD} and $V_{DD2/3}$

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required

Customer: These items are not necessary if customer parameters are the same as default

Advanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait 5~10ms after V _{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(15) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	(22) Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	(26) Set Bias Ratio	LCD specific operating voltage setting
R	0	0	1	0	0	0	0	0	0	1	(11) Set V _{BIAS} Potentiometer	
O	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(23) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1ms before V _{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(18) Set Display Disable	
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* This is only recommended for very brief display OFF (under 10mS).

If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset.	C _{B1} , C _{B1} , C _{LCD} discharged.
–	–	–	–	–	–	–	–	–	–	–		Extended display OFF Z z z z . . .
–	–	–	–	–	–	–	–	–	–	–		System waking up
R											Repeat power-up sequence	Repeat power up register setting sequence
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON Reset* is replaced by *System Reset* command, and an extended idle time in between.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Logic Supply voltage	-0.3	+4.0	V
V _{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V _{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V _{LCD}	LCD Generated voltage (-30°C ~ +80°C)	-0.3	+18.0	V
V _{IN}	Digital input signal	-0.4	V _{DD} + 0.5	V
T _{OPR}	Operating temperature range	-30	+85	°C
T _{STR}	Storage temperature	-55	+125	°C

Notes

1. V_{DD} based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

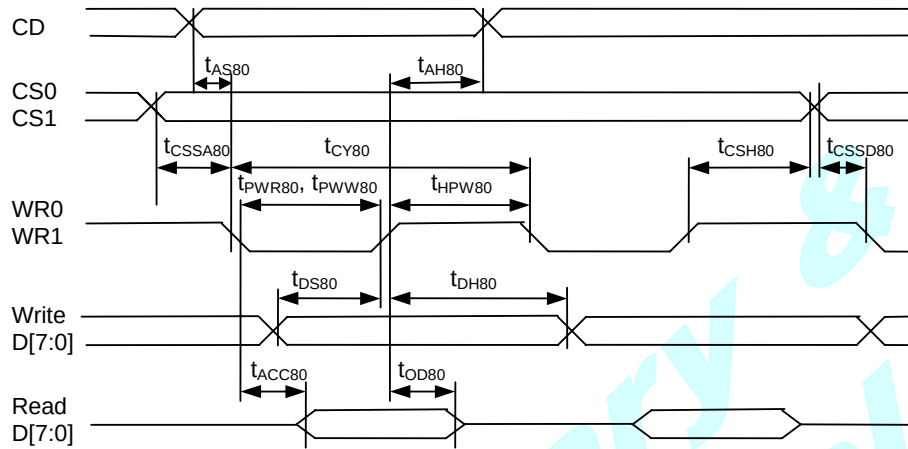
DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.8		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq 2.4V, 25^{\circ}C$		13.5	15	V
V_D	LCD data voltage	$V_{DD2/3} \geq 2.4V, 25^{\circ}C$	0.9		1.5	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{0(SEG)}$	SEG output impedance	$V_{LCD} = 13.5V$		2.0	4.0	$k\Omega$
$R_{0(COM)}$	COM output impedance	$V_{LCD} = 13.5V$		1.2	2.5	$k\Omega$
f_{LINE}	Average Line rate	$LC[4:3] = 11b$		16.6		kHz

POWER CONSUMPTION

V_{DD} = (TBD), Bias Ratio = (TBD), Gain = (TBD), PM = (TBD), Line Rate = (TBD), P_L = (TBD), MR = (TBD), Bus mode = (TBD), C_L = (TBD), C_B = (TBD). All outputs are open circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	(TBD),	(TBD),
2-pixel checker	Bus = idle	(TBD),	(TBD),

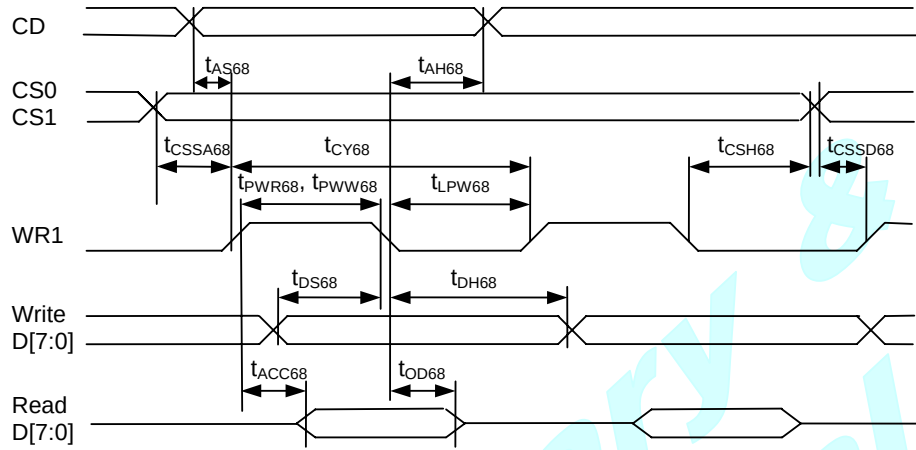
AC CHARACTERISTICS

FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

 ($V_{DD}=2.5V$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 20	—	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	—	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 65	—	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	—	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		65 35 65 35	—	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 20	—	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	$C_L = 100pF$	— 12	60 20	ns
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, T_a= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS80} t _{AH80}	CD	Address setup time Address hold time		0 30	—	ns
t _{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		210 120 210 120	—	ns
t _{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		100 100	—	ns
t _{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		55 55	—	ns
t _{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		100 55 100 55	—	ns
t _{DS80} t _{DH80}	D0~D7	Data setup time Data hold time		45 30	—	ns
t _{ACC80} t _{OD80}		Read access time Output disable time	C _L = 100pF	- 20		ns
t _{CSSA80} t _{CSSD80} t _{CSH80}	CS1/CS0	Chip select setup time		15 15 30		ns

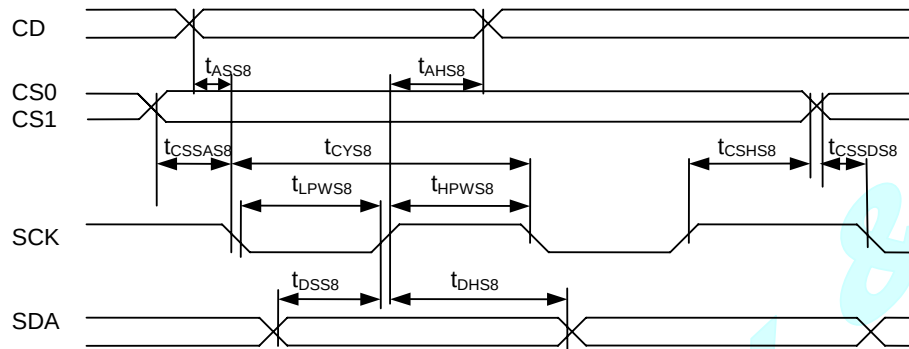

FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

 ($V_{DD}=2.5V$ to $3.3V$, $T_a = -30$ to $+85^{\circ}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	—	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	—	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 65	—	ns
t_{PPWW68}		Pulse width 8 bits (write) 4 bits		35 35	—	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		65 35 65 35	—	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 20	—	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	$C_L = 100pF$	— 12	60 20	ns
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, T_a= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS68} t _{AH68}	CD	Address setup time Address hold time		0 30	—	ns
T _{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		210 120 210 120	—	ns
t _{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		100 100	—	ns
t _{PWW68}		Pulse width 8 bits (write) 4 bits		55 55	—	ns
t _{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		100 55 100 55	—	ns
t _{DS68} t _{DH68}	D0~D7	Data setup time Data hold time		45 30	—	ns
t _{ACC68} t _{OD68}		Read access time Output disable time	C _L = 100pF	- 20		ns
T _{CSSA68} T _{CSSD68} T _{CSH68}	CS1/CS0	Chip select setup time		15 15 30		ns


FIGURE 17: Serial Bus Timing Characteristics (for S8)

($V_{DD}=2.5V$ to $3.3V$, $T_a = -30$ to $+85^{\circ}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		20	–	ns
t_{CYS8}	SCK	System cycle time		140	–	ns
t_{LPWS8}		Low pulse width		65	–	ns
t_{HPWS8}		High pulse width		65	–	ns
t_{DSS8}	SDA	Data setup time		30	–	ns
t_{DHS8}		Data hold time		20	–	ns
t_{CSSAS8}	CS1/CS0	Chip select setup time		10		ns
t_{CSSDS8}				10		ns
t_{CSHS8}				20		ns

($V_{DD}=1.8V$ to $2.5V$, $T_a = -30$ to $+85^{\circ}C$)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		30	–	ns
t_{CYS8}	SCK	System cycle time		210	–	ns
t_{LPWS8}		Low pulse width		100	–	ns
t_{HPWS8}		High pulse width		100	–	ns
t_{DSS8}	SDA	Data setup time		45	–	ns
t_{DHS8}		Data hold time		30	–	ns
t_{CSSAS8}	CS1/CS0	Chip select setup time		15		ns
t_{CSSDS8}				15		ns
t_{CSHS8}				30		ns

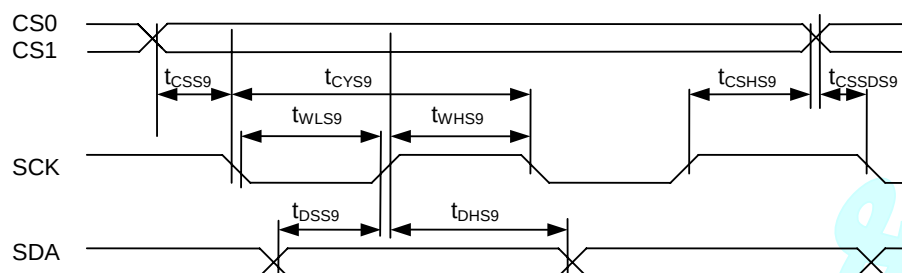


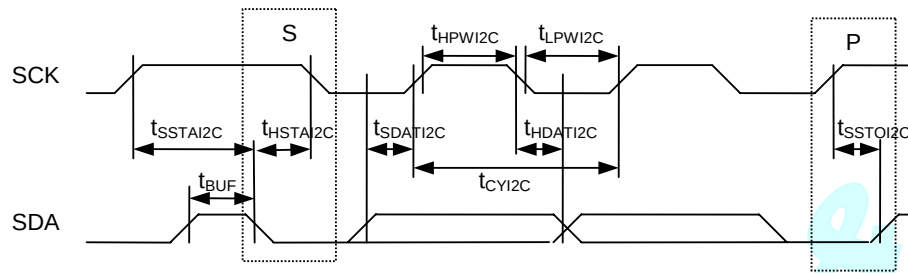
FIGURE 18: Serial Bus Timing Characteristics (for S9)

(V_{DD}=2.5V to 3.3V, T_a= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{CYS9}	SCK	System cycle time		140	–	ns
t _{LPWS9}		Low pulse width		65	–	ns
t _{HPWS9}		High pulse width		65	–	ns
t _{DSS9} t _{DHS9}	SDA	Data setup time Data hold time		30 20	–	ns
t _{CSSAS9} t _{CSSDS9} t _{CHS9}		Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, T_a= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{CYS9}	SCK	System cycle time		210	–	ns
t _{LPWS9}		Low pulse width		100	–	ns
t _{HPWS9}		High pulse width		100	–	ns
t _{DSS9} t _{DHS9}	SDA	Data setup time Data hold time		45 30	–	ns
t _{CSSAS9} t _{CSSDS9} t _{CHS9}		Chip select setup time		15 15 30		ns


FIGURE 19 Serial bus timing characteristics (for I²C)

 (V_{DD}=2.5V to 3.3V, T_a= -30 to +85^o C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{CYI2C}	SCK	SCK cycle time	tr+tf ≤ 100ns	250	—	ns
t _{LPWI2C}		Low pulse width		65	—	ns
t _{HPWI2C}		High pulse width		65	—	ns
tr, tf	SCK SDA	Rise time and fall time		—	—	ns
t _{SSDAI2C}		Data setup time		30	—	ns
t _{HDAI2C}		Data hold time		10	—	ns
t _{SSTAI2C}		START Setup time		30	—	ns
t _{HSTAI2C}		STAR Hold time		10	—	ns
t _{SSTOI2C}		STOP setup time		30	—	ns

 (V_{DD}=1.8V to 2.5V, T_a= -30 to +85^o C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{CYI2C}	SCK	SCK cycle time	tr+tf ≤ 100ns	300	—	ns
t _{LPWI2C}		Low pulse width		100	—	ns
t _{HPWI2C}		High pulse width		100	—	ns
tr, tf	SCK SDA	Rise time and fall time		—	—	ns
t _{SSDAI2C}		Data setup time		45	—	ns
t _{HDAI2C}		Data hold time		15	—	ns
t _{SSTAI2C}		START Setup time		45	—	ns
t _{HSTAI2C}		STAR Hold time		15	—	ns
t _{SSTOI2C}		STOP setup time		45	—	ns



FIGURE 20: Reset Characteristics

(V_{DD} =1.8V to 3.3V, T_a = -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		15	–	uS

PHYSICAL DIMENSIONS

DIE SIZE:
1.372mm x 11.384mm

DIE THICKNESS:
0.5mm

BUMP HEIGHT:
17µm ±1µm (within die)

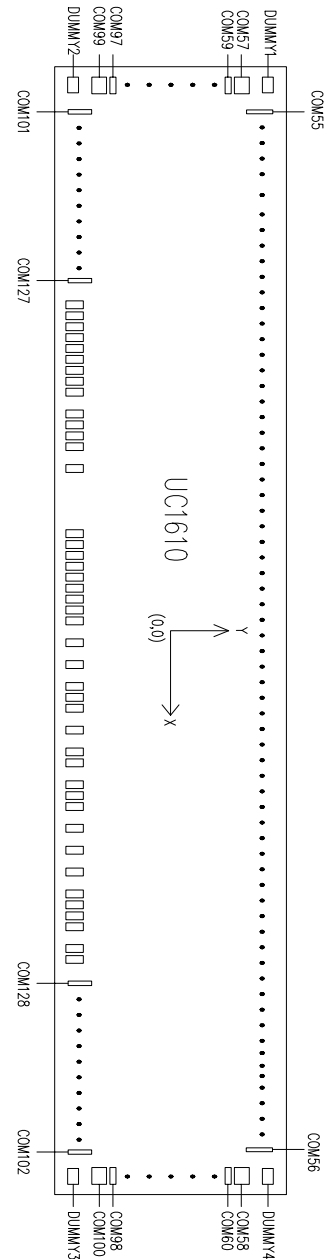
MINIMUM BUMP PITCH:
SEG: 50µm
COM: 50µm

MINIMUM BUMP GAP:
17µm

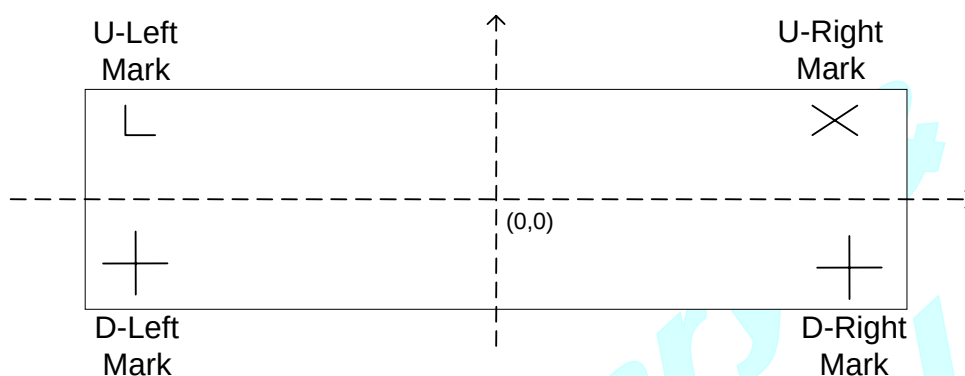
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

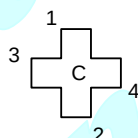
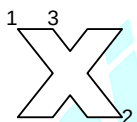
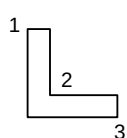
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



COORDINATES:

	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-5496.315	623.800	5430.360	625.900
2	-5480.690	591.875	5497.760	578.575
3	-5449.465	576.375	5452.059	625.900

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-5474.315	-590.975	5467.935	-590.975
2	-5463.315	-646.025	5478.935	-646.025
3	-5496.315	-613.000	5445.935	-613.000
4	-5441.265	-624.000	5500.985	-624.000
C	-5468.815	-618.500	5473.435	-618.500

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

#	PAD Name	X	Y	W	H
1	DUMMY	-5588.92	568.575	99	53
2	COM57	-5588.92	508.45	99	33
3	COM59	-5588.92	458.45	99	33
4	COM61	-5588.92	408.45	99	33
5	COM63	-5588.92	358.45	99	33
6	COM65	-5588.92	308.45	99	33
7	COM67	-5588.92	258.45	99	33
8	COM69	-5588.92	208.45	99	33
9	COM71	-5588.92	158.45	99	33
10	COM73	-5588.92	108.45	99	33
11	COM75	-5588.92	58.45	99	33
12	COM77	-5588.92	8.45	99	33
13	COM79	-5588.92	-41.55	99	33
14	COM81	-5588.92	-91.55	99	33
15	COM83	-5588.92	-141.55	99	33
16	COM85	-5588.92	-191.55	99	33
17	COM87	-5588.92	-241.55	99	33
18	COM89	-5588.92	-291.55	99	33
19	COM91	-5588.92	-341.55	99	33
20	COM93	-5588.92	-391.55	99	33
21	COM95	-5588.92	-441.55	99	33
22	COM97	-5588.92	-491.55	99	33
23	COM99	-5588.92	-541.55	99	33
24	DUMMY	-5588.92	-601.425	99	53
25	COM101	-5395.02	-593.025	33	99
26	COM103	-5345.02	-593.025	33	99
27	COM105	-5295.02	-593.025	33	99
28	COM107	-5245.02	-593.025	33	99
29	COM109	-5195.02	-593.025	33	99
30	COM111	-5145.02	-593.025	33	99
31	COM113	-5095.02	-593.025	33	99
32	COM115	-5045.02	-593.025	33	99
33	COM117	-4995.02	-593.025	33	99
34	COM119	-4945.02	-593.025	33	99
35	COM121	-4895.02	-593.025	33	99
36	COM123	-4845.02	-593.025	33	99
37	COM125	-4795.02	-593.025	33	99
38	COM127	-4745.02	-593.025	33	99
39	D0	-4667.52	-600.025	50	80
40	D1	-4597.52	-600.025	50	80
41	D2	-4527.52	-600.025	50	80
42	D3	-4457.52	-600.025	50	80
43	D4	-4387.52	-600.025	50	80
44	D5	-4317.52	-600.025	50	80
45	D6	-4247.52	-600.025	50	80
46	D7	-4177.52	-600.025	50	80
47	RST_	-4105.92	-600.025	50	80
48	CS0	-3846.79	-600.025	50	80
49	VDDX	-3775.87	-600.025	50	80
50	CS1	-3705.19	-600.025	50	80
51	ID	-3450.19	-600.025	50	80
52	CD	-3378.59	-600.025	50	80
53	WR0	-3123.59	-600.025	50	80

#	PAD Name	X	Y	W	H
54	WR1	-3051.99	-600.025	50	80
55	TST4	-2796.99	-600.025	50	80
56	BM0	-2725.39	-600.025	50	80
57	VDDX	-2554.39	-600.025	50	80
58	BM1	-2383.39	-600.025	50	80
59	TST2	-2312.47	-600.025	50	80
60	TP[5]	-2128.39	-600.025	50	80
61	TP[4]	-1867.99	-600.025	50	80
62	VSS	-1797.74	-600.025	50	80
63	VSS	-1727.74	-600.025	50	80
64	VSS	-1657.74	-600.025	50	80
65	VSS	-1587.74	-600.025	50	80
66	VSS	-1517.74	-600.025	50	80
67	VSS	-1447.74	-600.025	50	80
68	VSS2	-1264.32	-600.025	50	80
69	VSS2	-1194.32	-600.025	50	80
70	VSS2	-1124.32	-600.025	50	80
71	VSS2	-1054.32	-600.025	50	80
72	VSS2	-984.315	-600.025	50	80
73	VDD2	-914.315	-600.025	50	80
74	VDD2	-844.315	-600.025	50	80
75	VDD2	-774.315	-600.025	50	80
76	VDD3	-407.615	-600.025	50	80
77	VDD3	-336.365	-600.025	50	80
78	VDD3	-266.365	-600.025	50	80
79	VDD	104.685	-600.025	50	80
80	VDD	174.935	-600.025	50	80
81	VDD	244.935	-600.025	50	80
82	VDD	314.935	-600.025	50	80
83	VDD	384.935	-600.025	50	80
84	TP[3]	558.635	-600.025	50	80
85	TP[2]	628.885	-600.025	50	80
86	TP[1]	889.285	-600.025	50	80
87	VB0-	960.46	-600.025	50	80
88	VB0-	1030.46	-600.025	50	80
89	VB0-	1100.46	-600.025	50	80
90	VB0-	1170.46	-600.025	50	80
91	VB0-	1240.46	-600.025	50	80
92	VB0-	1310.46	-600.025	50	80
93	VB0-	1380.46	-600.025	50	80
94	VB0-	1450.46	-600.025	50	80
95	VB0-	1520.46	-600.025	50	80
96	VB1-	1871.46	-600.025	50	80
97	VB1-	1941.71	-600.025	50	80
98	VB1-	2010.11	-600.025	50	80
99	VB1-	2078.51	-600.025	50	80
100	VB1-	2146.91	-600.025	50	80
101	VB1-	2215.31	-600.025	50	80
102	VB1-	2283.71	-600.025	50	80
103	VB1-	2352.11	-600.025	50	80
104	VB1-	2420.51	-600.025	50	80
105	VB1+	2490.51	-600.025	50	80

#	PAD Name	X	Y	W	H
106	VB1+	2558.91	-600.025	50	80
107	VB1+	2627.31	-600.025	50	80
108	VB1+	2695.71	-600.025	50	80
109	VB1+	2764.11	-600.025	50	80
110	VB1+	2832.51	-600.025	50	80
111	VB1+	2900.91	-600.025	50	80
112	VB1+	2969.31	-600.025	50	80
113	VB1+	3039.31	-600.025	50	80
114	VB0+	3388.31	-600.025	50	80
115	VB0+	3458.56	-600.025	50	80
116	VB0+	3526.96	-600.025	50	80
117	VB0+	3595.36	-600.025	50	80
118	VB0+	3663.76	-600.025	50	80
119	VB0+	3732.16	-600.025	50	80
120	VB0+	3800.56	-600.025	50	80
121	VB0+	3868.96	-600.025	50	80
122	VB0+	3937.36	-600.025	50	80
123	VLCDIN	4007.36	-600.025	50	80
124	VLCDIN	4077.36	-600.025	50	80
125	VLCDOUT	4426.36	-600.025	50	80
126	VLCDOUT	4496.61	-600.025	50	80
127	VBIAS	4566.61	-600.025	50	80
128	COM128	4742.66	-593.025	33	99
129	COM126	4792.66	-593.025	33	99
130	COM124	4842.66	-593.025	33	99
131	COM122	4892.66	-593.025	33	99
132	COM120	4942.66	-593.025	33	99
133	COM118	4992.66	-593.025	33	99
134	COM116	5042.66	-593.025	33	99
135	COM114	5092.66	-593.025	33	99
136	COM112	5142.66	-593.025	33	99
137	COM110	5192.66	-593.025	33	99
138	COM108	5242.66	-593.025	33	99
139	COM106	5292.66	-593.025	33	99
140	COM104	5342.66	-593.025	33	99
141	COM102	5392.66	-593.025	33	99
142	DUMMY	5588.91	-601.425	99	53
143	COM100	5588.91	-541.55	99	33
144	COM98	5588.91	-491.55	99	33
145	COM96	5588.91	-441.55	99	33
146	COM94	5588.91	-391.55	99	33
147	COM92	5588.91	-341.55	99	33
148	COM90	5588.91	-291.55	99	33
149	COM88	5588.91	-241.55	99	33
150	COM86	5588.91	-191.55	99	33
151	COM84	5588.91	-141.55	99	33
152	COM82	5588.91	-91.55	99	33
153	COM80	5588.91	-41.55	99	33
154	COM78	5588.91	8.45	99	33
155	COM76	5588.91	58.45	99	33
156	COM74	5588.91	108.45	99	33
157	COM72	5588.91	158.45	99	33
158	COM70	5588.91	208.45	99	33
159	COM68	5588.91	258.45	99	33

#	PAD Name	X	Y	W	H
160	COM66	5588.91	308.45	99	33
161	COM64	5588.91	358.45	99	33
162	COM62	5588.91	408.45	99	33
163	COM60	5588.91	458.45	99	33
164	COM58	5588.91	508.45	99	33
165	DUMMY	5588.91	568.575	99	53
166	COM56	5375.01	593.025	33	99
167	COM54	5325.01	593.025	33	99
168	COM52	5275.01	593.025	33	99
169	COM50	5225.01	593.025	33	99
170	COM48	5175.01	593.025	33	99
171	COM46	5125.01	593.025	33	99
172	COM44	5075.01	593.025	33	99
173	COM42	5025.01	593.025	33	99
174	COM40	4975.01	593.025	33	99
175	COM38	4925.01	593.025	33	99
176	COM36	4875.01	593.025	33	99
177	COM34	4825.01	593.025	33	99
178	COM32	4775.01	593.025	33	99
179	COM30	4725.01	593.025	33	99
180	COM28	4675.01	593.025	33	99
181	COM26	4625.01	593.025	33	99
182	COM24	4575.01	593.025	33	99
183	COM22	4525.01	593.025	33	99
184	COM20	4475.01	593.025	33	99
185	COM18	4425.01	593.025	33	99
186	COM16	4375.01	593.025	33	99
187	COM14	4325.01	593.025	33	99
188	COM12	4275.01	593.025	33	99
189	COM10	4225.01	593.025	33	99
190	COM8	4175.01	593.025	33	99
191	COM6	4125.01	593.025	33	99
192	COM4	4075.01	593.025	33	99
193	COM2	4025.01	593.025	33	99
194	SEG1	3975.01	593.025	33	99
195	SEG2	3925.01	593.025	33	99
196	SEG3	3875.01	593.025	33	99
197	SEG4	3825.01	593.025	33	99
198	SEG5	3775.01	593.025	33	99
199	SEG6	3725.01	593.025	33	99
200	SEG7	3675.01	593.025	33	99
201	SEG8	3625.01	593.025	33	99
202	SEG9	3575.01	593.025	33	99
203	SEG10	3525.01	593.025	33	99
204	SEG11	3475.01	593.025	33	99
205	SEG12	3425.01	593.025	33	99
206	SEG13	3375.01	593.025	33	99
207	SEG14	3325.01	593.025	33	99
208	SEG15	3275.01	593.025	33	99
209	SEG16	3225.01	593.025	33	99
210	SEG17	3175.01	593.025	33	99
211	SEG18	3125.01	593.025	33	99
212	SEG19	3075.01	593.025	33	99
213	SEG20	3025.01	593.025	33	99

#	PAD Name	X	Y	W	H
214	SEG21	2975.01	593.025	33	99
215	SEG22	2925.01	593.025	33	99
216	SEG23	2875.01	593.025	33	99
217	SEG24	2825.01	593.025	33	99
218	SEG25	2775.01	593.025	33	99
219	SEG26	2725.01	593.025	33	99
220	SEG27	2675.01	593.025	33	99
221	SEG28	2625.01	593.025	33	99
222	SEG29	2575.01	593.025	33	99
223	SEG30	2525.01	593.025	33	99
224	SEG31	2475.01	593.025	33	99
225	SEG32	2425.01	593.025	33	99
226	SEG33	2375.01	593.025	33	99
227	SEG34	2325.01	593.025	33	99
228	SEG35	2275.01	593.025	33	99
229	SEG36	2225.01	593.025	33	99
230	SEG37	2175.01	593.025	33	99
231	SEG38	2125.01	593.025	33	99
232	SEG39	2075.01	593.025	33	99
233	SEG40	2025.01	593.025	33	99
234	SEG41	1975.01	593.025	33	99
235	SEG42	1925.01	593.025	33	99
236	SEG43	1875.01	593.025	33	99
237	SEG44	1825.01	593.025	33	99
238	SEG45	1775.01	593.025	33	99
239	SEG46	1725.01	593.025	33	99
240	SEG47	1675.01	593.025	33	99
241	SEG48	1625.01	593.025	33	99
242	SEG49	1575.01	593.025	33	99
243	SEG50	1525.01	593.025	33	99
244	SEG51	1475.01	593.025	33	99
245	SEG52	1425.01	593.025	33	99
246	SEG53	1375.01	593.025	33	99
247	SEG54	1325.01	593.025	33	99
248	SEG55	1275.01	593.025	33	99
249	SEG56	1225.01	593.025	33	99
250	SEG57	1175.01	593.025	33	99
251	SEG58	1125.01	593.025	33	99
252	SEG59	1075.01	593.025	33	99
253	SEG60	1025.01	593.025	33	99
254	SEG61	975.01	593.025	33	99
255	SEG62	925.01	593.025	33	99
256	SEG63	875.01	593.025	33	99
257	SEG64	825.01	593.025	33	99
258	SEG65	775.01	593.025	33	99
259	SEG66	725.01	593.025	33	99
260	SEG67	675.01	593.025	33	99
261	SEG68	625.01	593.025	33	99
262	SEG69	575.01	593.025	33	99
263	SEG70	525.01	593.025	33	99
264	SEG71	475.01	593.025	33	99
265	SEG72	425.01	593.025	33	99
266	SEG73	375.01	593.025	33	99
267	SEG74	325.01	593.025	33	99

#	PAD Name	X	Y	W	H
268	SEG75	275.01	593.025	33	99
269	SEG76	225.01	593.025	33	99
270	SEG77	175.01	593.025	33	99
271	SEG78	125.01	593.025	33	99
272	SEG79	75.01	593.025	33	99
273	SEG80	25.01	593.025	33	99
274	SEG81	-24.99	593.025	33	99
275	SEG82	-74.99	593.025	33	99
276	SEG83	-124.99	593.025	33	99
277	SEG84	-174.99	593.025	33	99
278	SEG85	-224.99	593.025	33	99
279	SEG86	-274.99	593.025	33	99
280	SEG87	-324.99	593.025	33	99
281	SEG88	-374.99	593.025	33	99
282	SEG89	-424.99	593.025	33	99
283	SEG90	-474.99	593.025	33	99
284	SEG91	-524.99	593.025	33	99
285	SEG92	-574.99	593.025	33	99
286	SEG93	-624.99	593.025	33	99
287	SEG94	-674.99	593.025	33	99
288	SEG95	-724.99	593.025	33	99
289	SEG96	-774.99	593.025	33	99
290	SEG97	-824.99	593.025	33	99
291	SEG98	-874.99	593.025	33	99
292	SEG99	-924.99	593.025	33	99
293	SEG100	-974.99	593.025	33	99
294	SEG101	-1024.99	593.025	33	99
295	SEG102	-1074.99	593.025	33	99
296	SEG103	-1124.99	593.025	33	99
297	SEG104	-1174.99	593.025	33	99
298	SEG105	-1224.99	593.025	33	99
299	SEG106	-1274.99	593.025	33	99
300	SEG107	-1324.99	593.025	33	99
301	SEG108	-1374.99	593.025	33	99
302	SEG109	-1424.99	593.025	33	99
303	SEG110	-1474.99	593.025	33	99
304	SEG111	-1524.99	593.025	33	99
305	SEG112	-1574.99	593.025	33	99
306	SEG113	-1624.99	593.025	33	99
307	SEG114	-1674.99	593.025	33	99
308	SEG115	-1724.99	593.025	33	99
309	SEG116	-1774.99	593.025	33	99
310	SEG117	-1824.99	593.025	33	99
311	SEG118	-1874.99	593.025	33	99
312	SEG119	-1924.99	593.025	33	99
313	SEG120	-1974.99	593.025	33	99
314	SEG121	-2024.99	593.025	33	99
315	SEG122	-2074.99	593.025	33	99
316	SEG123	-2124.99	593.025	33	99
317	SEG124	-2174.99	593.025	33	99
318	SEG125	-2224.99	593.025	33	99
319	SEG126	-2274.99	593.025	33	99
320	SEG127	-2324.99	593.025	33	99
321	SEG128	-2374.99	593.025	33	99

#	PAD Name	X	Y	W	H
322	SEG129	-2424.99	593.025	33	99
323	SEG130	-2474.99	593.025	33	99
324	SEG131	-2524.99	593.025	33	99
325	SEG132	-2574.99	593.025	33	99
326	SEG133	-2624.99	593.025	33	99
327	SEG134	-2674.99	593.025	33	99
328	SEG135	-2724.99	593.025	33	99
329	SEG136	-2774.99	593.025	33	99
330	SEG137	-2824.99	593.025	33	99
331	SEG138	-2874.99	593.025	33	99
332	SEG139	-2924.99	593.025	33	99
333	SEG140	-2974.99	593.025	33	99
334	SEG141	-3024.99	593.025	33	99
335	SEG142	-3074.99	593.025	33	99
336	SEG143	-3124.99	593.025	33	99
337	SEG144	-3174.99	593.025	33	99
338	SEG145	-3224.99	593.025	33	99
339	SEG146	-3274.99	593.025	33	99
340	SEG147	-3324.99	593.025	33	99
341	SEG148	-3374.99	593.025	33	99
342	SEG149	-3424.99	593.025	33	99
343	SEG150	-3474.99	593.025	33	99
344	SEG151	-3524.99	593.025	33	99
345	SEG152	-3574.99	593.025	33	99
346	SEG153	-3624.99	593.025	33	99
347	SEG154	-3674.99	593.025	33	99
348	SEG155	-3724.99	593.025	33	99
349	SEG156	-3774.99	593.025	33	99
350	SEG157	-3824.99	593.025	33	99
351	SEG158	-3874.99	593.025	33	99
352	SEG159	-3924.99	593.025	33	99
353	SEG160	-3974.99	593.025	33	99
354	COM1	-4024.99	593.025	33	99
355	COM3	-4074.99	593.025	33	99
356	COM5	-4124.99	593.025	33	99
357	COM7	-4174.99	593.025	33	99
358	COM9	-4224.99	593.025	33	99
359	COM11	-4274.99	593.025	33	99
360	COM13	-4324.99	593.025	33	99
361	COM15	-4374.99	593.025	33	99
362	COM17	-4424.99	593.025	33	99
363	COM19	-4474.99	593.025	33	99
364	COM21	-4524.99	593.025	33	99
365	COM23	-4574.99	593.025	33	99
366	COM25	-4624.99	593.025	33	99
367	COM27	-4674.99	593.025	33	99
368	COM29	-4724.99	593.025	33	99
369	COM31	-4774.99	593.025	33	99
370	COM33	-4824.99	593.025	33	99
371	COM35	-4874.99	593.025	33	99
372	COM37	-4924.99	593.025	33	99
373	COM39	-4974.99	593.025	33	99
374	COM41	-5024.99	593.025	33	99
375	COM43	-5074.99	593.025	33	99

#	PAD Name	X	Y	W	H
376	COM45	-5124.99	593.025	33	99
377	COM47	-5174.99	593.025	33	99
378	COM49	-5224.99	593.025	33	99
379	COM51	-5274.99	593.025	33	99
380	COM53	-5324.99	593.025	33	99
381	COM55	-5374.99	593.025	33	99

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COF INFORMATION

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REVISION HISTORY

Version	Contents	Date of Rev.
0.0	Preliminary specification	May 22, 2003
0.1	(1) Ordering Information is prepared.	Jul. 18, 2003
	(2) Overall pin name changes: $V_{LCD-IN} \rightarrow V_{LCDIN}$ $TST[2] \rightarrow TST2$ $PS<0/1> \rightarrow BM0/1$ $VDD \rightarrow VDDX$ (page52, # 49/57)	
	$VLCD-OUT \rightarrow VLCDOUT$ $PRG4/3/2/1/0 \rightarrow TP[5/4/3/2/1]$ $CS[0/1] \rightarrow CS0/1$ $V_{REF} \rightarrow V_{BIAS}$	
	(3) The value for C_L is provided in Note paragraphs: $C_L: 0.06\mu F \sim 0.3\mu F$ (Section "Pin Description", pages 4; "Hi-v Generator and bias reference circuit", page 22)	
	(4) Default value for register PM is corrected from "96H" to "B2H" (Section "Control Register", page 7)	
	(5) "10b" is added as possible values for PC[3:2]. (Section "Control Register", page 7; "Command Description", page 11)	
	(6) Default values are corrected. (Section "Command Table", page 9; "Command Description, Pp 10-17)	
	(7) I ² C related information are added: Figure 13 "I ² C serial mode reference circuit" is add. (Section "Host interface reference circuit", page 32)	
0.11	(8) Figure 14-1 is added to illustrate Delay allowance between V_{DD} and V_{DD23} . (Section "Reset & Power Management", page 37)	July 30, 2003
	(1) The description for entry "TST4" is updated: Connect TST4 to V_{SS} when normal use. (Section "Pin Description", page 6)	
	(2) Some minor typo errors are corrected: (4) Set Column Address : $CA[6:4] \rightarrow CA[7:4]$ (8) Set Advanced Product Configuration : $APC[1:0] \rightarrow APC[R]$ (25) Reset Cursor Update Mode : value of D0: $0 \rightarrow AC3$ (26) Set Cursor Update Mode : value of D0: $1 \rightarrow AC3$ (Section "Command Description", pages 10, 11, 14, 15)	
	(3) Alignment marks and shapes are corrected. (Section "Alignment Mark Information", page 51)	