HIGH-VOLTAGE ANALOG-SIGNAL IC

UC1671

4BPx40SEG Dot Matrix LCD Controller/Driver

ES Specifications
Datasheet Revision 0.62

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ULTRACHIP

The Coolest LCD Driver, Ever!!

Table of Content

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4BPx40SEG Dot Matrix LCD Controller/Driver

INTRODUCTION

The UC1671 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 SEGs. It can be easily cascaded for larger LCD applications. The UC1671 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware sub-addressing, and by display memory switching (static and duplex drive modes).

MAIN APPLICATIONS

- Battery-operated hand held devices
- Portable instruments

FEATURE HIGHLIGHTS

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Display bias: static, $\frac{1}{2}$, or $\frac{1}{3}$ Selectable frame frequency: 64Hz, 82Hz, 110Hz, or 200Hz

  400Hz is supported when using external oscillator, (Max.: 9.6KHz.)
- 40 SEG drives:
  - Up to twenty 7-SEG alphanumeric characters
  - Up to ten 14-SEG alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device sub-address boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 2.5 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 11.0V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- Extended temperature range up to 85 ^oC
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Manufactured in silicon gate CMOS process

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

ORDERING INFORMATION

Part Number	I²C	Package	Description
UC1671cGAD	Yes	COG	Gold bumped die. Bump Height: 9uM.

General Notes

APPLICATION INFORMATION
For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I²C
The implementation of I²C is already included and tested in all silicon.

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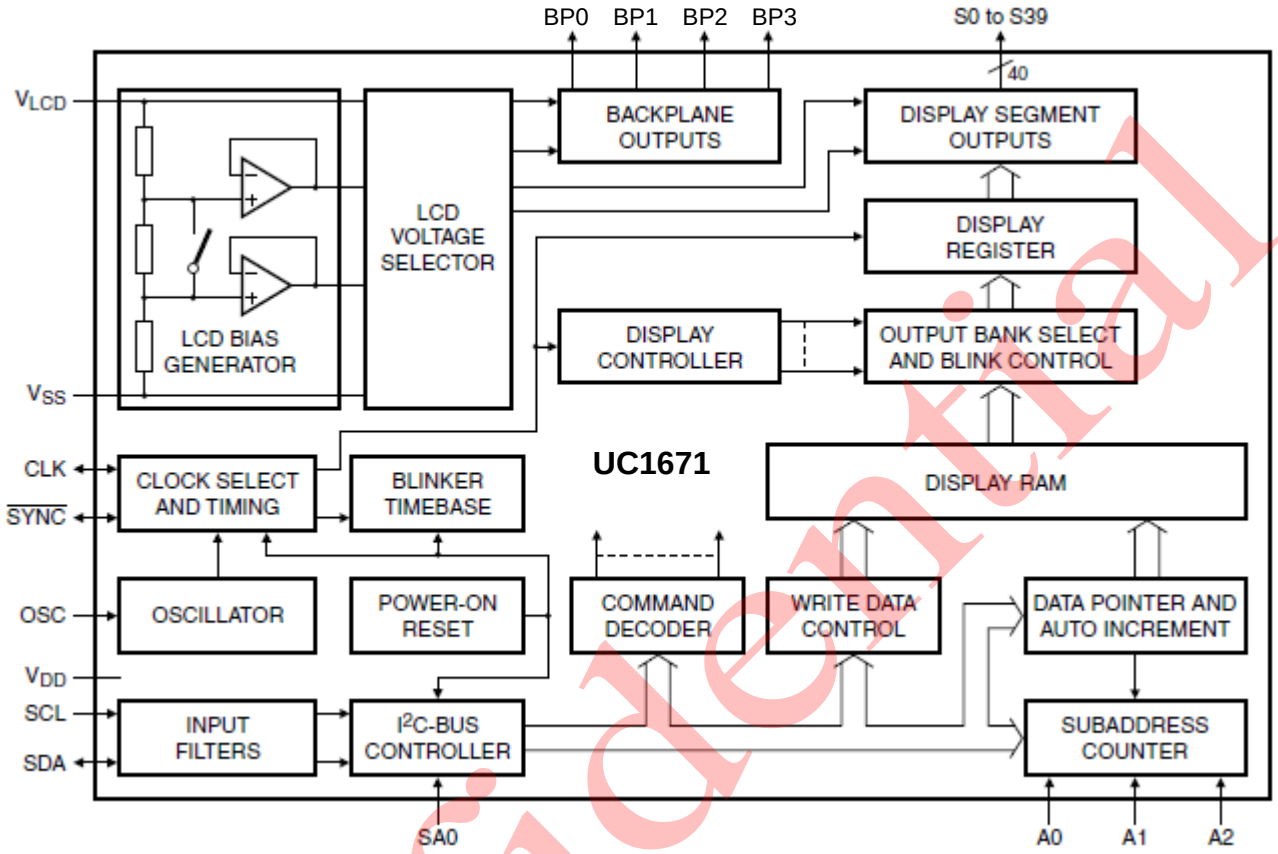
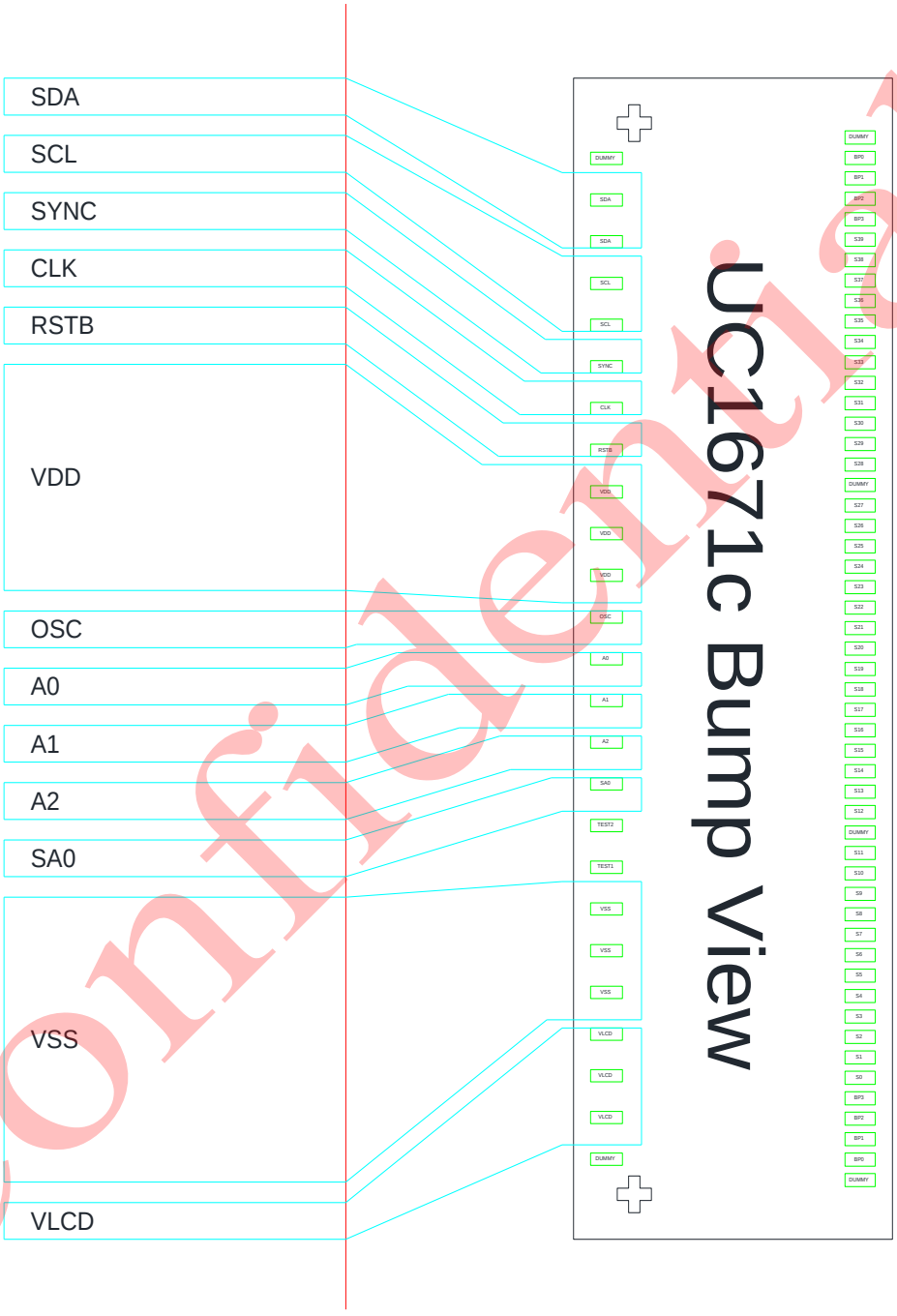
BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Pad No.	Type	Description
SDA	2~3	I/O	I^2C bus serial data input
SCL	4~5	I	I^2C bus serial clock input
$\overline{SYNC}$	6	I/O	Cascade synchronization input and output. Leave it open when cascade function is not used.
CLK	7	I/O	Clock input and output When OSC pin is Low: Leave it open. When OSC pin is High: External clock is input.
RSTB	8	I	Reset pin Reset if set to Low. Connect to V_{DD} or keep it floating if not used.
V_{DD}	9~11	PWR	Supply voltage
OSC	12	I	Oscillator selection. Low: Built-in oscillator is used. High: Built-in oscillator is stopped. External clock via the CLK pin is used.
A0~A2	13~15	I	Hardware device address selection for cascading. Connect to V_{SS} for logic 0, V_{DD} for logic 1. Connect to V_{SS} when the cascade function is not used.
SA0	16	I	I^2C bus slave address selection. Connect to V_{SS} for logic 0, V_{DD} for logic 1. When not used, connect to V_{SS}.
TEST2~1	17~18	–	Test pins, for UC's use only. Not Connected. Keep floating, neither short nor connecting to High/Low.
Vss	19~21	PWR	Ground supply voltage.
V_{LCD}	22~24	PWR	LCD supply voltage.
BP0~BP3	27~30, 73~76	O	LCD backplane outputs.
S0~S39	31~42, 44~59, 61~72	O	LCD SEG outputs.
Dummy	1, 25, 26, 43, 60, 77	–	Dummy pins. Not Connected. Keep floating. Neither short nor connecting to High/Low.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=2.5V (min.), should be satisfied under all operating conditions. UC1671c's peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1671c's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 2.5V and cause the IC to malfunction.

CONTROL REGISTERS

Register	# of Bits	Description
PS	1	Display power saving mode selection When OSC pin is Low, 0: internal clock is ON 1: internal clock is OFF When OSC pin is High, internal clock is OFF.
E	1	Display Status 0: Display disabled (blank) 1: Display enabled
B	1	LCD bias configuration 0: 1/3 bias 1: 1/2 bias
M[1:0]	2	LCD drive mode selection 00b: 1:4 multiplex; BP0~3 01b: static; 1 backplane; BP0 10b: 1:2 multiplex; BP0~1 11b: 1:3 multiplex; BP0~2
DP[5:0]	6	Display RAM addresses. Value range: 00 0000b~10 0111b (0~39d)
FR[1:0]	2	Frame Rate 00b: 64Hz 01b: 82Hz 10b: 110Hz 11b: 200Hz
A[2:0]	3	Device sub-address counter
I	1	Input bank selection 0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)
O	1	Output bank selection 0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)
A	1	Blink mode selection 0: Normal blinking. Normal blinking can only be selected when multiplex drive mode=1:3 or 1:4. 1: Blinking by alternating display RAM banks. Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.
BF[1:0]	2	Blink frequency selection 00b: OFF 01b: Blink mode 1 10b: Blink mode 2 11b: Blink mode 3

COMMAND TABLE

D7-D0: **C:** Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control byte continues; next byte will be a command, too.

#	Command	D7	D6	D5	D4	D3	D2	D1	D0	Action
1	Mode-set	C	**1**	**0**	PS	E	B	M1	M0	Set Display Mode
2	Load-data-pointer	C	**0**	DP5	DP4	DP3	DP2	DP1	DP0	
3	Frame-Rate-select	C	**1**	**1**	**0**	**1**	**0**	FR1	FR0	Select Frame Rate
4	Device-select	C	**1**	**1**	**0**	**0**	A2	A1	A0	Select Device
5	Bank-select	C	**1**	**1**	**1**	**1**	**0**	I	O	Select Bank
6	Blink-select	C	**1**	**1**	**1**	**0**	A	BF1	BF0	Select Blink Mode

COMMAND DESCRIPTION

D7-D0: **C:** Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control bytes continue; next byte will be a command too.

(1) Mode-Set

Action	D7	D6	D5	D4	D3	D2	D1	D0
Set mode	C	1	0	PS	E	B	M1	M0

PS: Display power saving mode switch.
0: Internal clock ON 1: Internal clock OFF, (for Power Saving).
The power saving mode is ON only when the OSC pin is Low and the display is disabled (E=0).

E: Display status
0: Display disabled (blank) 1: Display enabled

B: LCD bias configuration
0: 1/3 bias 1: 1/2 bias

M[1:0]: LCD drive mode selection
00b: 1:4 multiplex; BP0~3 01b: static; 1 backplane; BP0
10b: 1:2 multiplex; BP0~1 11b: 1:3 multiplex; BP0~2
To increase driving capabilities, refer to section “Backplane Outputs” on page 19 and its illustration on page 21.

(2) Load-Data-Pointer

Action	D7	D6	D5	D4	D3	D2	D1	D0
Load data pointer	C	0	DP5	DP4	DP3	DP2	DP1	DP0

DP[5:0]: Display RAM addresses. Value range: 00 0000b~10 0111b, that is 0~39 in decimal. The value will be transferred to the data pointer to define one of 40 Display RAM addresses.

(3) Frame-Rate-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Frame Rate	C	1	1	0	1	0	FR1	FR0

FR[1:0]: Frame rate 00b: 64Hz 01b: 82Hz 10b: 110Hz 11b: 200Hz

(4) Device-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Device	C	1	1	0	0	A2	A1	A0

A[2:0]: 3-bit binary value of 0 to 7, transferred to the sub-address counter to define one of 8 hardware sub-addresses.

D7-D0: **C:** Continuation bit. C=0: last control byte in the transfer; next byte will be regarded as display data.
C=1: control bytes continue; next byte will be a command too.

(5) Bank-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select RAM I/O	C	1	1	1	1	0	I	O

I: Input bank selection 0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)

	Storage of Arriving Display Data	
	Static	1:2 multiplex
I=0	RAM bit 0	RAM bits 0 and 1
I=1	RAM bit 2	RAM bits 2 and 3

O: Output bank selection 0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)

	Retrieval of LCD Display Data	
	Static	1:2 multiplex
O=0	RAM bit 0	RAM bits 0 and 1
O=1	RAM bit 2	RAM bits 2 and 3

This command has no effect in 1:3 or 1:4 multiplex drive mode.

(6) Blink-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select blink	C	1	1	1	0	A	BF1	BF0

A: Blink mode selection

0: Normal blinking. Normal blinking can only be selected when multiplex drive mode=1:3 or 1:4.
1: Blinking by alternating display RAM banks
Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

BF[1:0]: Blink frequency selection

00b: OFF 01b: Blink mode 1 10b: Blink mode 2 11b: Blink mode 3

See the Blink Frequency table for detailed description about each blink mode on page 22.

FUNCTION DESCRIPTION

The UC1671 is a versatile peripheral device designed to interface any microprocessor or microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 40 SEGs.

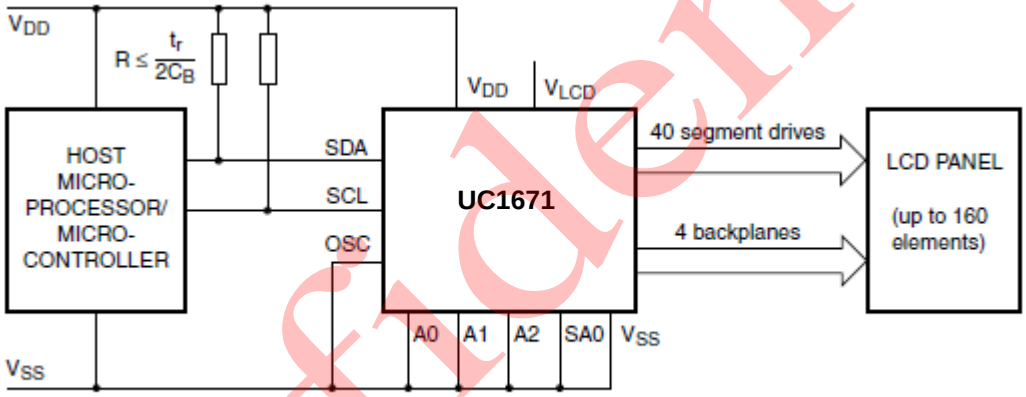
The possible display configurations of the UC1671 depend on the number of active backplane outputs required. A selection of display configurations is shown in the table below:

Possible Display Configurations

# of Backplanes	# of Elements	7-SEG alphanumeric		14-SEG alphanumeric		Dot matrix
		Digits	Indicator Symbols	Characters	Indicator Symbols	
4	160	20	20	10	20	160 dots (4 x 40)
3	120	15	15	8	8	120 dots (3 x 40)
2	80	10	10	5	10	80 dots (2 x 40)
1	40	5	5	2	12	40 dots (1 x 40)

All of the display configurations can be implemented in a typical system as shown in following figure:

Typical System Configuration



The resistance of the power lines must be kept to a minimum.

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the UC1671. The internal oscillator is enabled by connecting pin OSC to pin VSS. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, Vss, and V_{LCD}) and the LCD panel chosen for the application.

Power-ON Reset

At power-ON, the UC1671 resets to the following starting conditions:

- All backplane and SEG outputs are set to V_{LCD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched OFF.
- Input and output bank selectors are reset.
- The I²C-bus interface is initialized.
- The data pointer and the sub-address counter are cleared (set to logic 0).
- Display is disabled.

Remark: Do not transfer data on the I²C bus for at least 1mS after a power-ON to allow the reset action to complete.

LCD Bias Generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of 3 series resistors between V_{LCD} and Vss. The center resistor is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration is selected.

LCD Voltage Selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the `Mode-Set` command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in table below:

LCD Drive Mode	# of Backplanes	# of Levels	LCD Bias Configuration	$\frac{V_{OFF(RMS)}}{V_{LCD}}$	$\frac{V_{ON(RMS)}}{V_{LCD}}$	$D=\frac{V_{ON(RMS)}}{V_{OFF(RMS)}}$
static	1	2	static	0	1	∞
1:2 multiplex	2	3	1/2	0.354	0.791	2.236
1:2 multiplex	2	4	1/3	0.333	0.745	2.236
1:3 multiplex	3	4	1/3	0.333	0.638	1.915
1:4 multiplex	4	4	1/3	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{OFF(RMS)}$ with a defined LCD threshold voltage (Vth), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{LCD} > 3Vth$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated with $\frac{1}{1+a}$,

where a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{ON(RMS)}$) for the LCD is calculated with Equation (1) below:

$$V_{ON(RMS)} = V_{LCD}\sqrt{\frac{a^2+2a+n}{n\,x(1+a)^2}} \quad \ldots\ldots\ldots\ldots (1)$$

where n = 1 for static mode
n = 2 for 1:2 multiplex
n = 3 for 1:3 multiplex
n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{OFF(RMS)}$) for the LCD is calculated with Equation (2):

$$V_{OFF(RMS)} = V_{LCD}\sqrt{\frac{a^2-2a+n}{n\,x(1+a)^2}} \quad \ldots\ldots\ldots\ldots (2)$$

Discrimination is the ratio of $V_{ON(RMS)}$ to $V_{OFF(RMS)}$ and is determined from Equation (3):

$$D = \frac{Von(rms)}{Voff(rms)} = \sqrt{\frac{(a+1)^2+(n-1)}{(a-1)^2+(n-1)}} \quad \ldots\ldots\ldots (3)$$

where the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3}$ =1.732 and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3}$ =1.528.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD}, shown as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias):

  $V_{LCD} = \sqrt{6}$ x $V_{OFF(RMS)}$ = 2.449 $V_{OFF(RMS)}$

- 1:4 multiplex ($\frac{1}{2}$ bias):

  $V_{LCD} = [\frac{(4x\sqrt{3})}{3}]$ = 2.309 $V_{OFF(RMS)}$

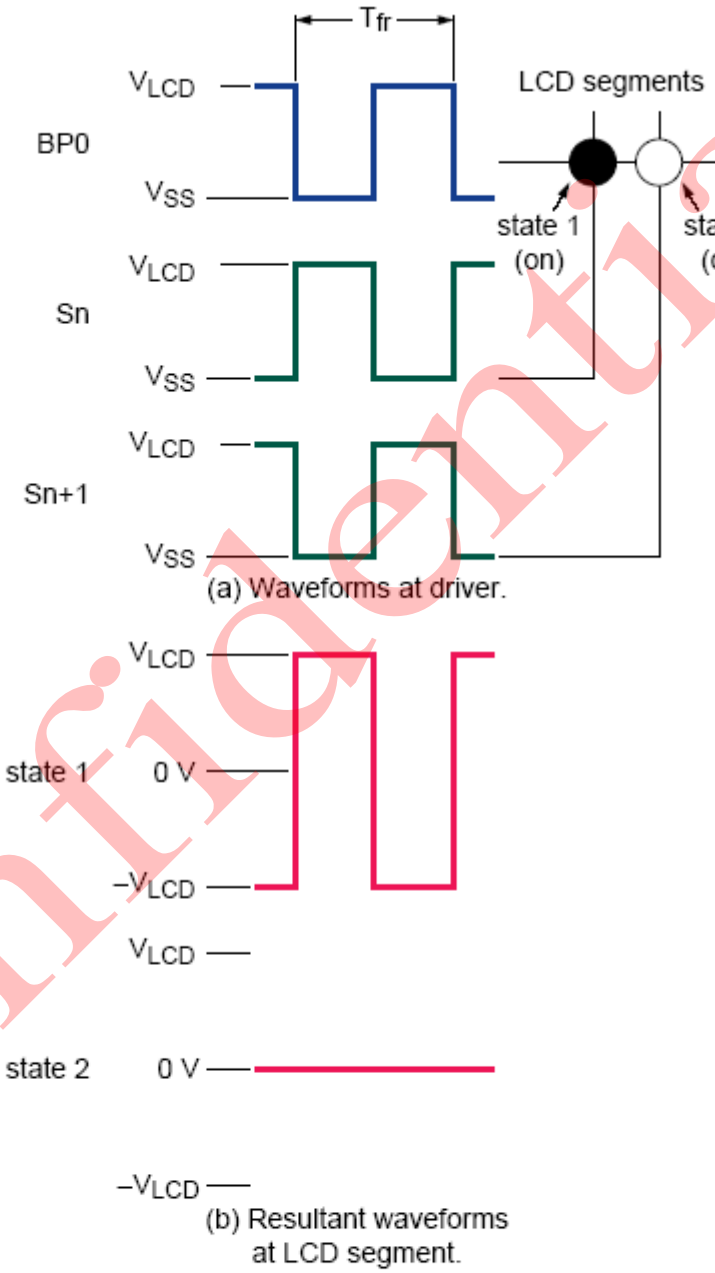
These compare with V_{LCD}=3 $V_{OFF(RMS)}$ when $\frac{1}{3}$ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

LCD Drive Mode Waveforms – Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and SEG drive waveforms for this mode are shown in the figure below:

Static Drive Mode Waveforms



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

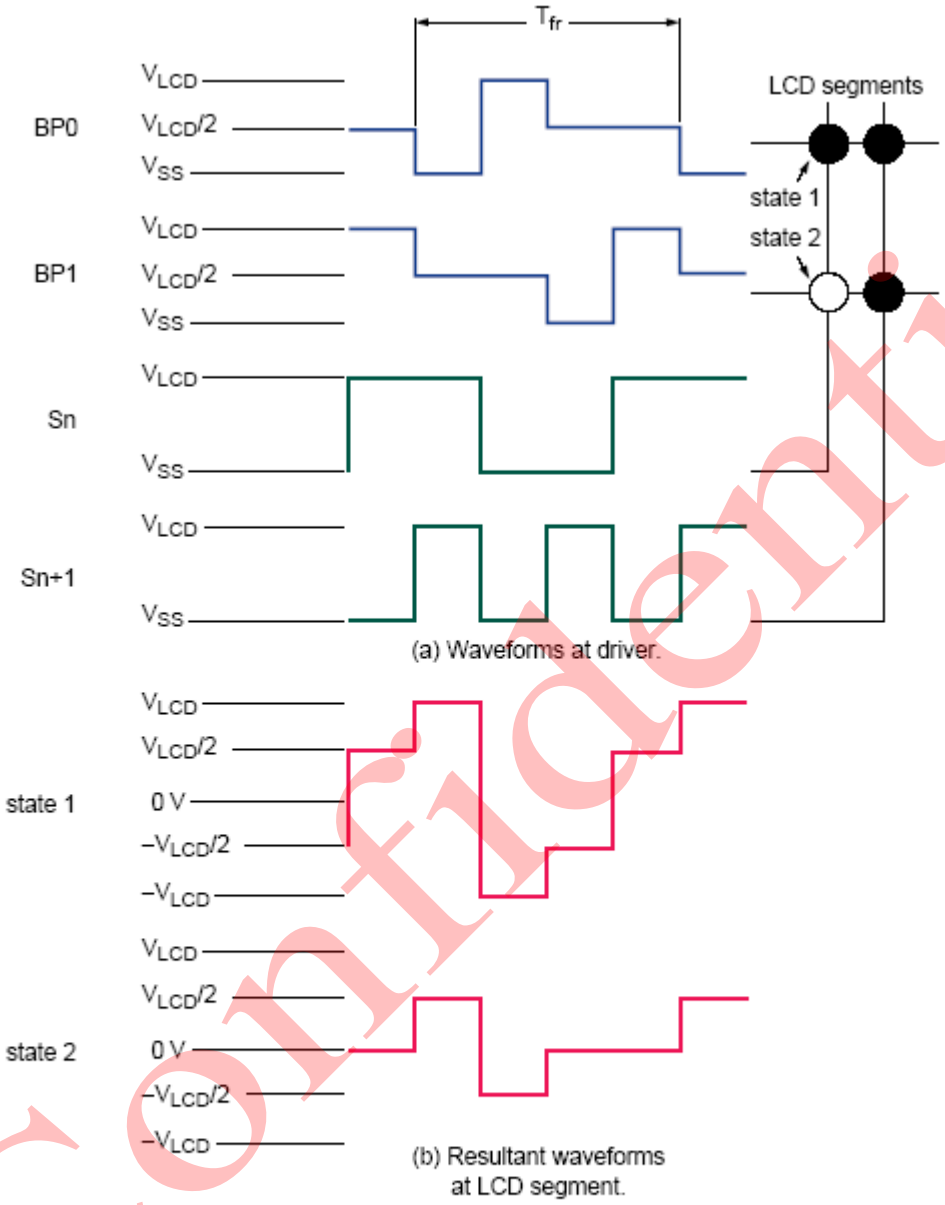
$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

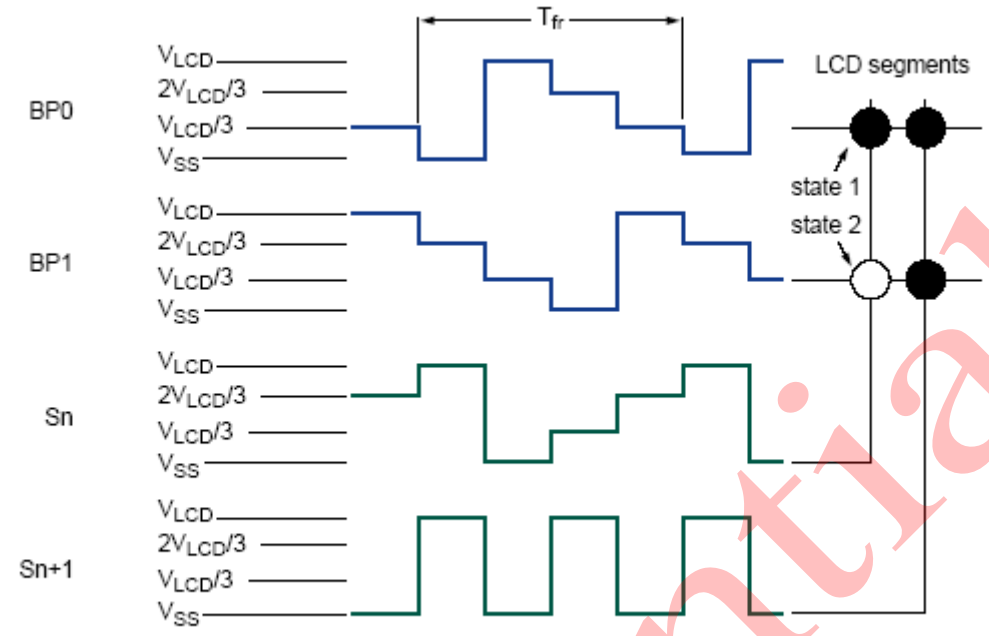
LCD Drive Mode Waveforms – 1:2 Multiplex drive mode

When 2 backplanes are provided in the LCD, the 1:2 multiplex mode applies. The UC1671 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in the following 2 figures.

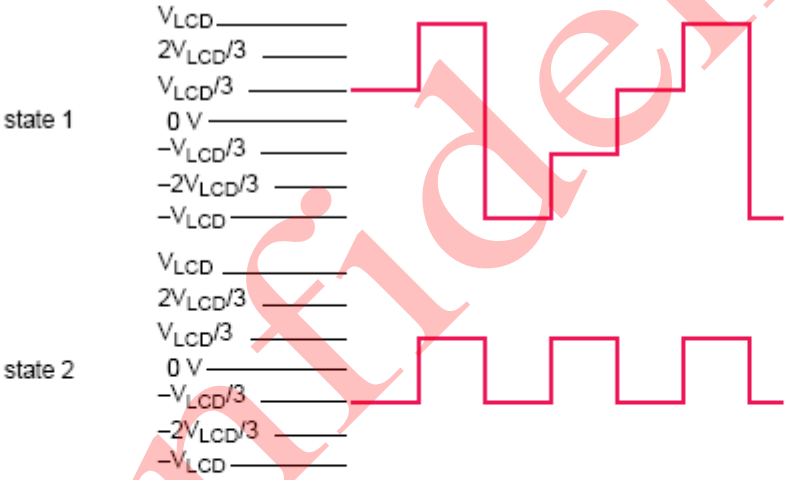


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{on(RMS)} = 0.791V_{LCD}$.
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{off(RMS)} = 0.354V_{LCD}$.

Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

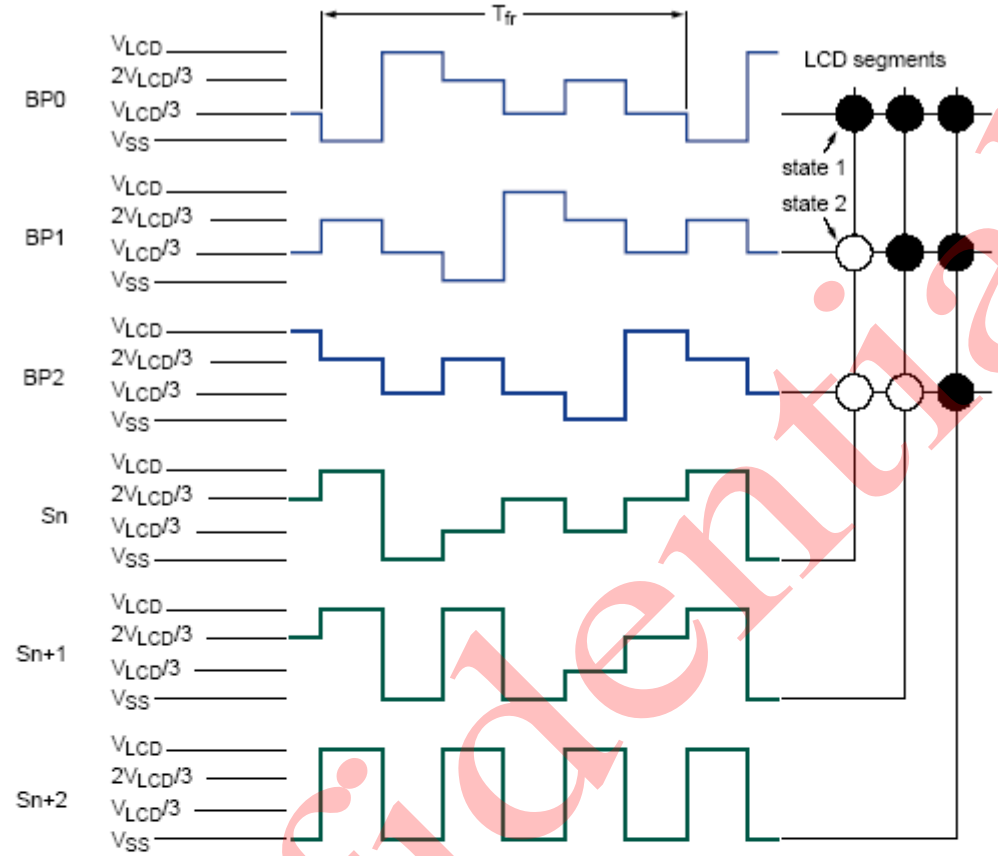
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

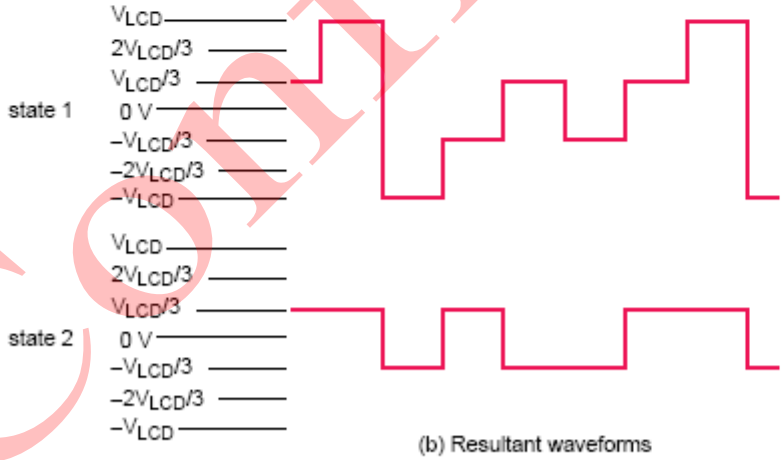
Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

LCD Drive Mode Waveforms – 1:3 Multiplex drive mode

When 3 backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in the figure below:



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

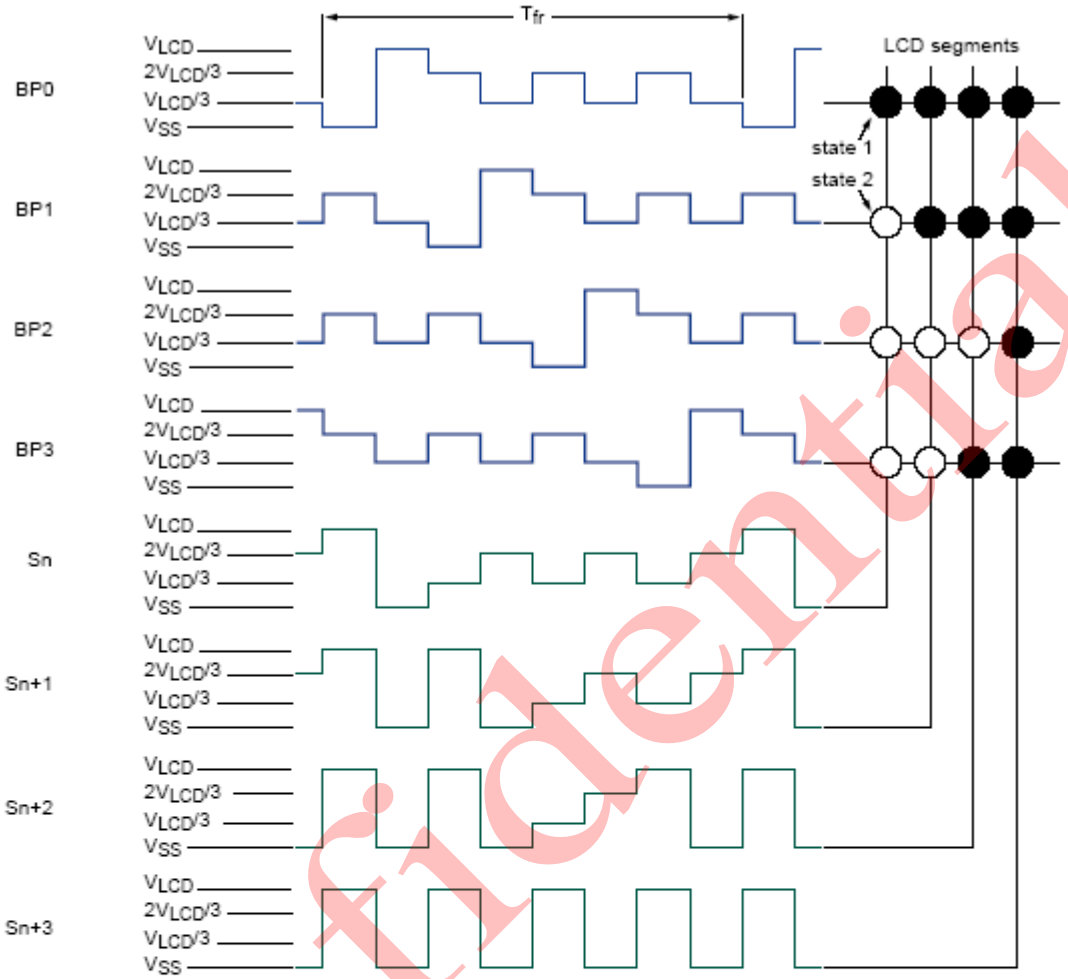
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

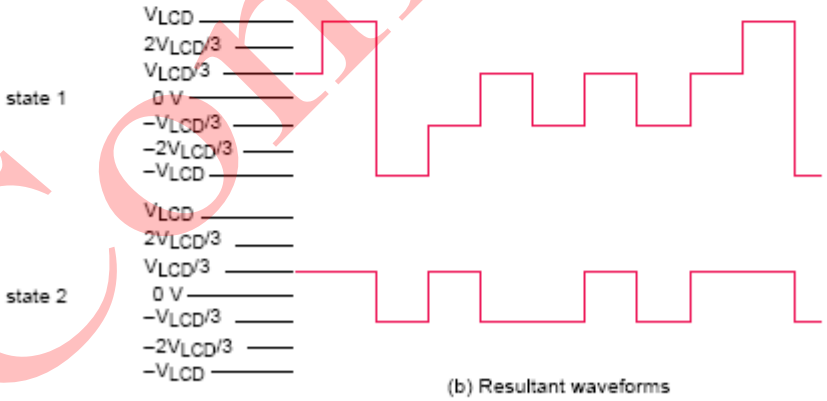
Waveforms for the 1:3 multiplex drive mod with $\frac{1}{3}$ bias

LCD Drive Mode Waveforms – 1:4 Multiplex drive mode

When 4 backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in the figure below:



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Waveforms for the 1:4 multiplex drive mod with $\frac{1}{3}$ bias

Oscillator

The internal logic of the UC1671 and its LCD drive signals are timed either by its internal oscillator or by an external clock.

Internal Clock

The internal oscillator is enabled by connecting pin OSC to pin Vss. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several UC1671 in the system that are connected in cascade.

External Clock

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

Timing and Frame Frequency

The UC1671 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each UC1671 in the system is maintained by the synchronization signal at pin $\overline{SYNC}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock:

$$f_{FR} = \frac{f_{CLK}}{24}$$

The internal clock frequency, f_{CLK}, can be selected using command Frame-Rate-select. As a result, 4 frame frequencies are available: 64Hz, 82Hz, 110Hz, or 200Hz:

FR[1:0]	Typical Clock Freq.	LCD Frame Freq.
00b	1536 Hz	64 Hz
01b	1970 Hz	82 Hz
10b	2640 Hz	110 Hz
11b	4800 Hz	200 Hz

However, 400Hz of frame frequency is supported when using external Oscillator, (Maximum: 9.6KHz.)

The timing of the UC1671 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display SEG outputs. In cascaded applications, the synchronization signal (SYNC) maintains the correct timing relationship between all the UC1671 in the system.

Display Register

The display register holds the display data while the corresponding multiplex signals are generated.

SEG Outputs

The LCD drive section includes 40 SEG outputs (S0 to S39), which must be connected directly to the LCD. The SEG output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 SEG outputs are required the unused SEG outputs must be left open-circuit.

Backplane Outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than 4 backplane outputs are required, the unused outputs can be left open-circuit.

static	The same signal is carried by all four (4) backplane outputs; and they can be connected in parallel for very high drive requirements.
1:2 multiplex	BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities.
1:3 multiplex	BP3 carries the same signal as BP1 does; therefore, these 2 adjacent outputs can be tied together to give enhanced drive capabilities.
1:4 multiplex	BP0~ BP3 must be connected directly to the LCD.

Display RAM

The display RAM is a static 40x4-bit RAM, which stores LCD data.

There is a one-to-one correspondence between
- the bits in the RAM bitmap and the LCD elements.
- the RAM columns and the SEG outputs
- the RAM rows and the backplane output.

A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the OFF-state.

The display RAM bit map figure below shows rows 0 to 3, which correspond with the backplane outputs BP0 to BP3, and columns 0 to 39, which correspond with the SEG outputs S0 to S39. In multiplexed LCD applications, the SEG data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3, respectively.

Display RAM Bit Map

Columns→ / Rows↓	Display RAM Addressed / SEG output (S)											
	0	1	2	3	4	…	…	…	36	37	38	39
Display RAM Rows / backplane outputs (BP) 0												
1												
2												
3												

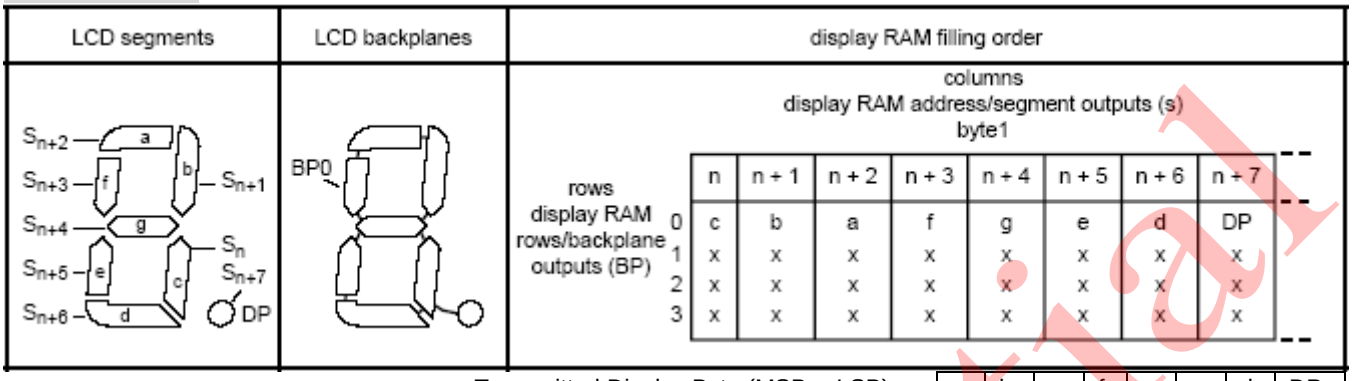
This display RAM bitmap shows the direct relationship between the display RAM addresses and the SEG outputs and between the bits in a RAM word and the backplane output.

When display data are transmitted to the UC1671, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data are stored singularly, in pairs, triples or quadruples.

To illustrate the filling order, an example of a 7-SEG numeric display showing all drive modes is given in the figure below; the RAM filling organization depicted applies equally to other LCD types.

Relationship between LCD Layout, Drive Mode, Display RAM Filling Order and Display Data transmitted over the I²C bus

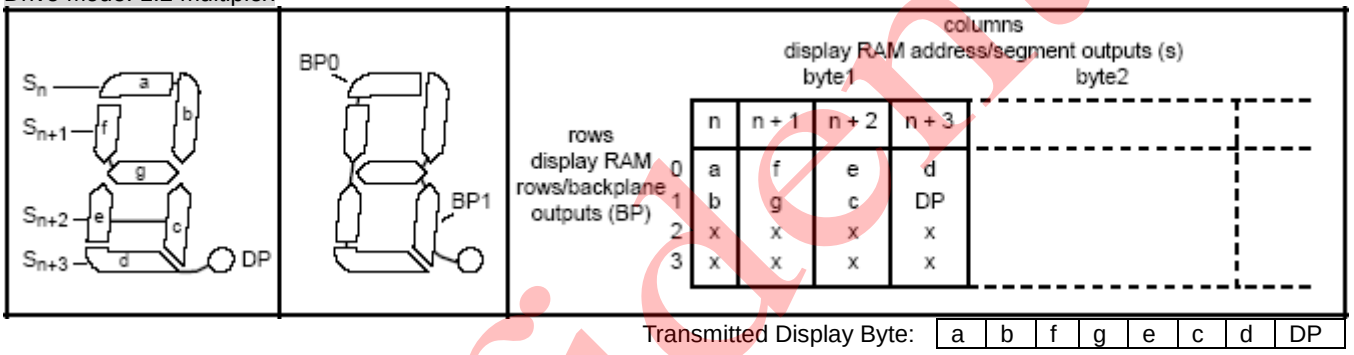
Drive Mode: Static



Transmitted Display Byte (MSB -- LSB):

c	b	a	f	g	e	d	DP

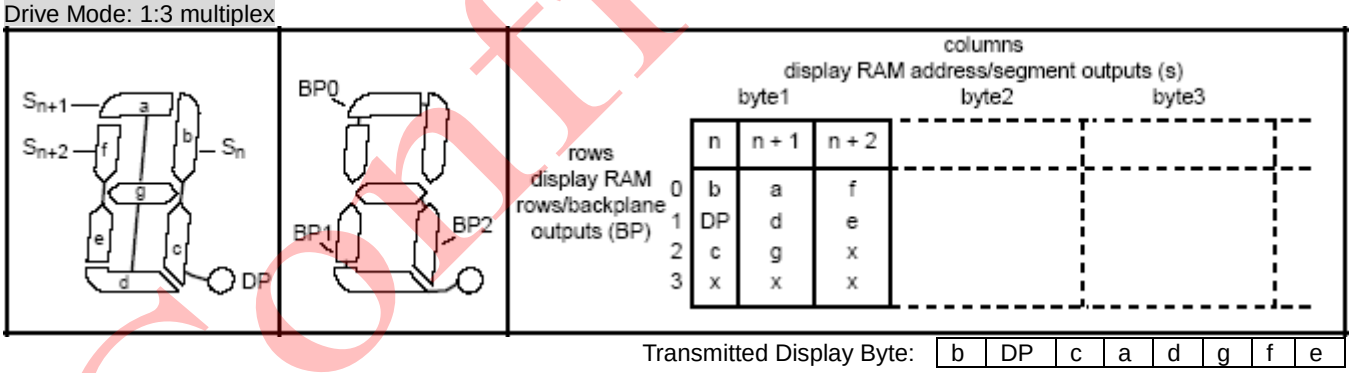
Drive Mode: 1:2 multiplex



Transmitted Display Byte:

a	b	f	g	e	c	d	DP

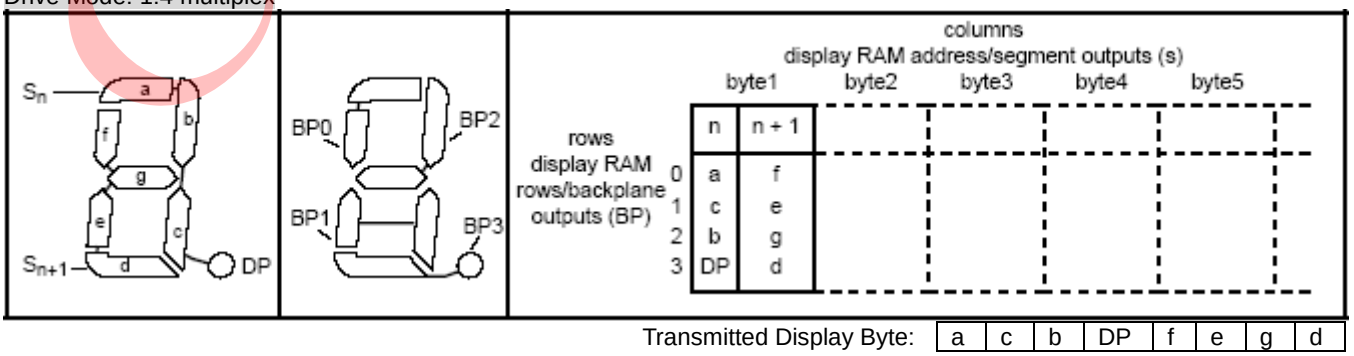
Drive Mode: 1:3 multiplex



Transmitted Display Byte:

b	DP	c	a	d	g	f	e

Drive Mode: 1:4 multiplex



Transmitted Display Byte:

a	c	b	DP	f	e	g	d

Remark: x = data bit unchanged

The following applies to the figure on last page:

Mode	Description
static	the 8 transmitted data bits are placed into row 0 of 8 successive 4-bit RAM words.
1:2 multiplex	the 8 transmitted data bits are placed in pairs into rows 0 and 1 of 4 successive 4-bit RAM words.
1:3 multiplex	the 8 bits are placed in triples into row 0, 1 and 2 of 3 successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
1:4 multiplex	the 8 transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of 2 successive 4-bit RAM words.

Data Pointer

The addressing mechanism for the display RAM is realized using a data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command.

Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in the Figure on the previous page.

After each byte is stored, the content of the data pointer is automatically increased by a value dependent on the selected LCD drive mode:

Mode	Content of Data Pointer
Static	Increased by eight (8)
1:2 multiplex	Increased by four (4)
1:3 multiplex	Increased by three (3)
1:4 multiplex	Increased by two (2)

If an I^2C-bus data access is terminated early then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

Sub-address Counter

The storage of display data is conditioned by the content of the sub-address counter. Storage is allowed only when the content of the sub-address counter match with the hardware sub-address applied to A0, A1, and A2. The sub-address counter value is defined by the device-select command (see command (4) Device-select). If the content of the sub-address counter and the hardware sub-address do not match, then data storage is inhibited but the data pointer is increased as if data storage had taken place. The sub-address counter is also increased when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next UC1671 occurs when the last RAM address is exceeded. Sub-addressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware sub-address must not be changed whilst the device is being accessed on the I^2C -bus interface.

Output bank selector

The output bank selector selects one of the 4 rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

Mode	Rows selected for Transfer
Static	Row 0 is selected
1:2 multiplex	Rows 0 and 1 are selected
1:3 multiplex	Rows 0, 1, and 2 are selected sequentially
1:4 multiplex	All RAM addresses of row 0 are selected, which are followed by the contents of row 1, row 2, and then row 3.

The UC1671 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input Bank Selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

Blinking

The display blinking capabilities of the UC1671 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see command (6) Blink-select). The blink frequencies are fractions of the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected:

Blink mode	Blink frequency Equation
OFF	–
1	fblink = fclk / 768
2	fblink = fclk / 1536
3	fblink = fclk / 3072

An additional feature is for an arbitrary selection of LCD SEGs to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available; groups of LCD SEGs can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the typical blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the `Mode-set` command (See `Command Description` section for more details).

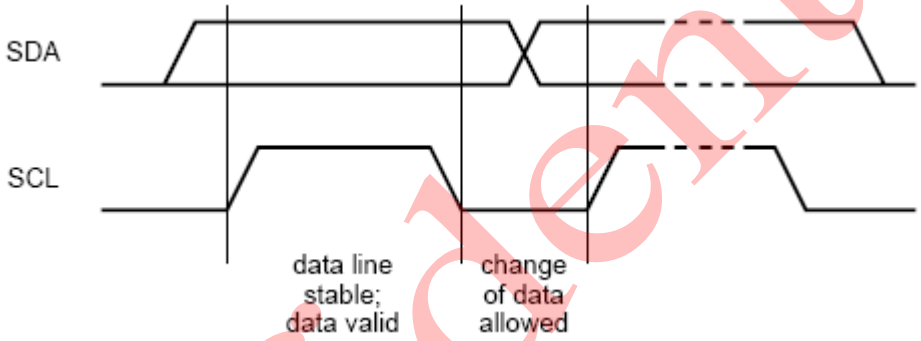
Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Bit Transfer



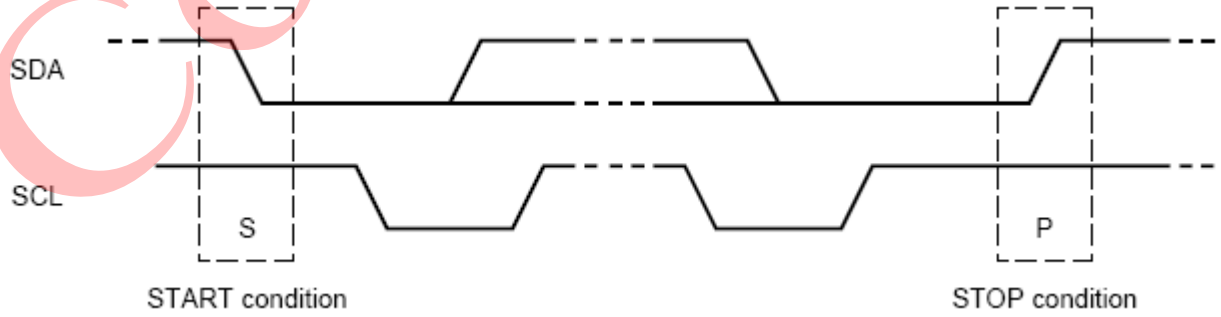
START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy.

A High-to-Low change of the data line, while the clock is High, is defined as the START condition (S).

A Low-to-High change of the data line, while the clock is High, is defined as the STOP condition (P).

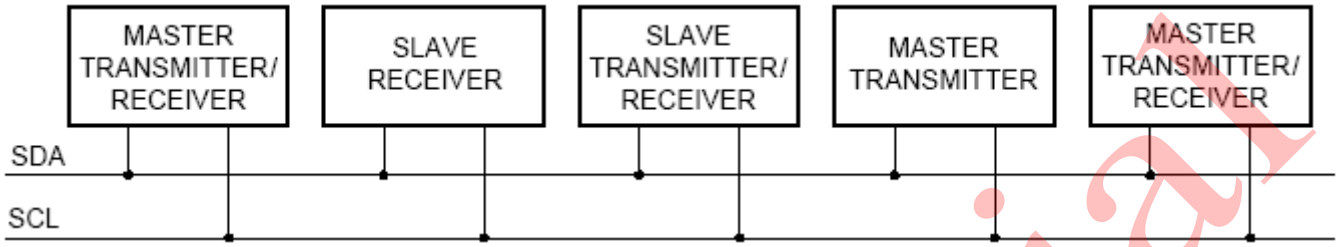
START/STOP Definition



System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves.

System Configuration

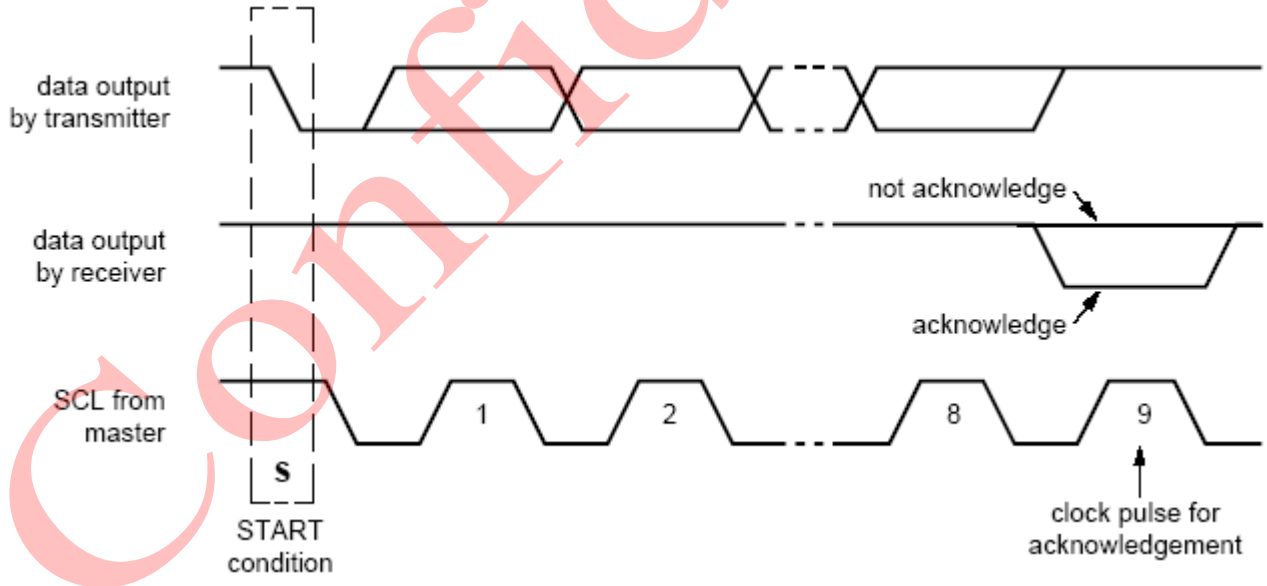


Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus



I²C-bus Controller

The UC1671 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the UC1671 are the acknowledge signals from the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data, and on the hardware sub-address.

In single device applications, the hardware sub-address inputs A0, A1, and A2 are normally tied to Vss which defines the hardware sub-address 0.

In multiple device applications A0, A1, and A2 are tied to Vss or VDD using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware sub-address.

Input Filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus Protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the UC1671.

I²C Slave address byte

(MSB)			Slave Address				(LSB)
7	6	5	4	3	2	1	0
0	1	1	1	0	0	SA0	R/$\overline{W}$

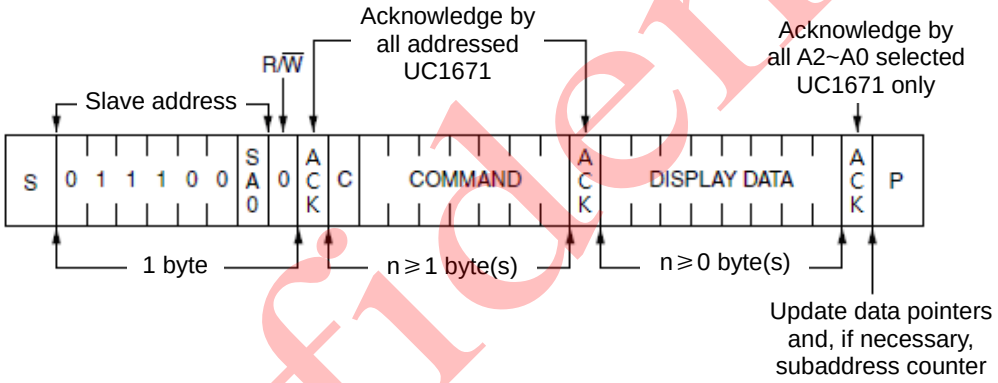
The UC1671 is a write/read access device. When performing write action, bit 0 should be logic 0. When performing read action, bit 0 should be logic 1. Bit 1 of the slave address that a UC1671 will respond to, is defined by the level tied at input SA0 input (Vss for logic 0, and VDD for logic 1).

Having 2 reserved slave addresses allows the followings on the same I²C-bus:

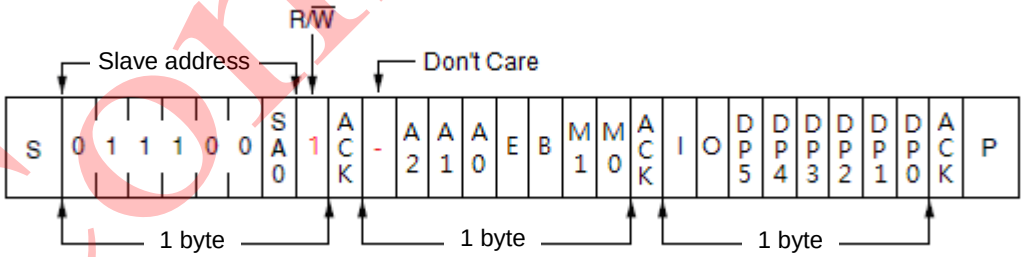
- Up to 16 UC1671 for very large LCD applications
- The use of two types of LCD multiplex drive

See the figure below for the I²C-bus protocol. The sequence is initiated with a START condition (**S**) from the I²C-bus master which is followed by 1 of 2 possible UC1671 slave addresses available. All UC1671s whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledgement (**A**) in parallel. This I²C-bus transfer is ignored by all UC1671 whose SA0 inputs are set to the alternative level.

I²C-bus Protocol (for Write)



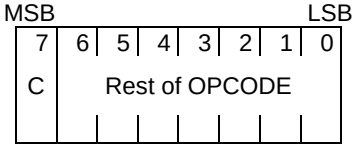
I²C-bus Protocol (for Read)



After acknowledgement, one or more command bytes follow that define the status of each addressed UC1671.

The last command byte sent is identified by resetting its most significant bit (MSB), continuation bit C. (as below)

Format of Command byte



The command bytes are also acknowledged by all addressed UC1671 connected to the bus.

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the sub-address counter. Both data pointer and sub-address counter are automatically updated and the data directed to the intended UC1671 device.

An acknowledgement after each byte is asserted only by UC1671 that are addressed via address lines A0, A1, and A2. After the last display byte, the I²C-bus master asserts a STOP

condition (**P**). Alternatively a START may be asserted to restart an I²C-bus access.

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The commands available to the UC1671 are defined in the “Command Table” and “Command Description” sections.

Display Controller

The display controller executes the commands identified by the command decoder. It contains the status registers and coordinates their effects. The display controller is also responsible for loading the display data into the display RAM in the correct filling order.

POWER MANAGEMENT

Power-Up Sequence

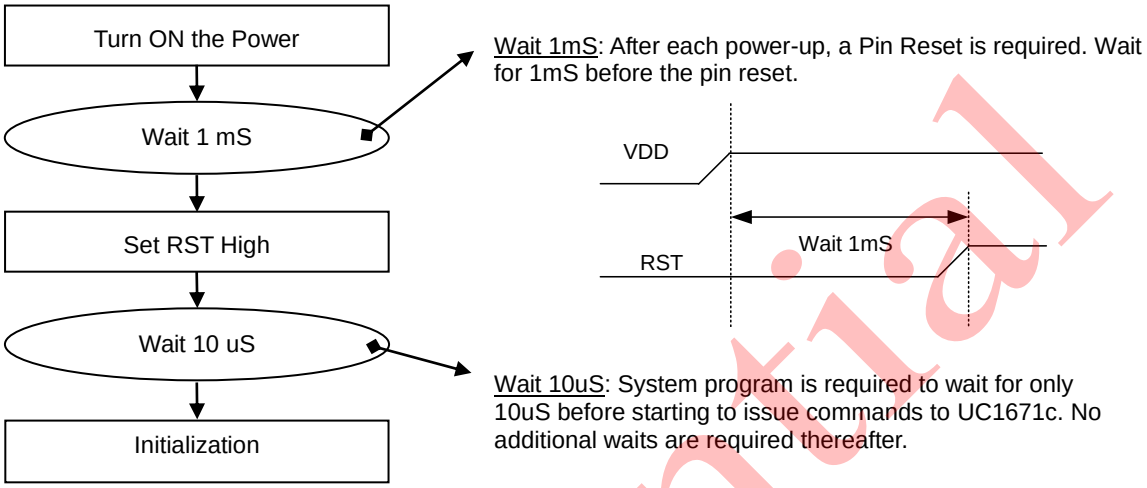


Figure 8: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD}:

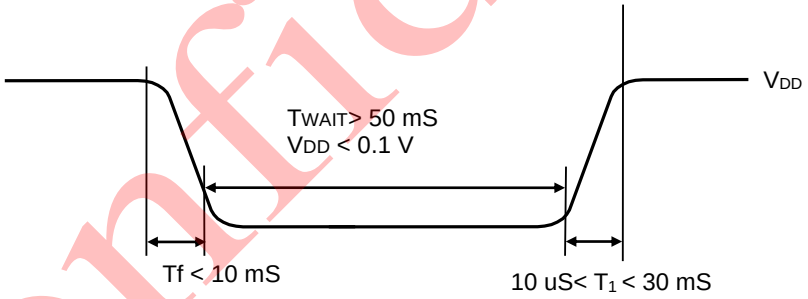


Figure 9: Power Off-On Sequence

Sample Power Management Command Sequences

The following tables are examples of command sequence for power-up and power-down operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type	Required:	These items are required
	Customized:	These items are not necessary if customer parameters are the same as default
	Advanced:	We recommend new users to skip these commands and use default values.
	Optional:	These commands depend on what users want to do.
D7 - D0	C: Continuation bit.	C=0: last control byte in the transfer; next byte will be regarded as display data. C=1: control bytes continue; next byte will be a command too.

Power-Up

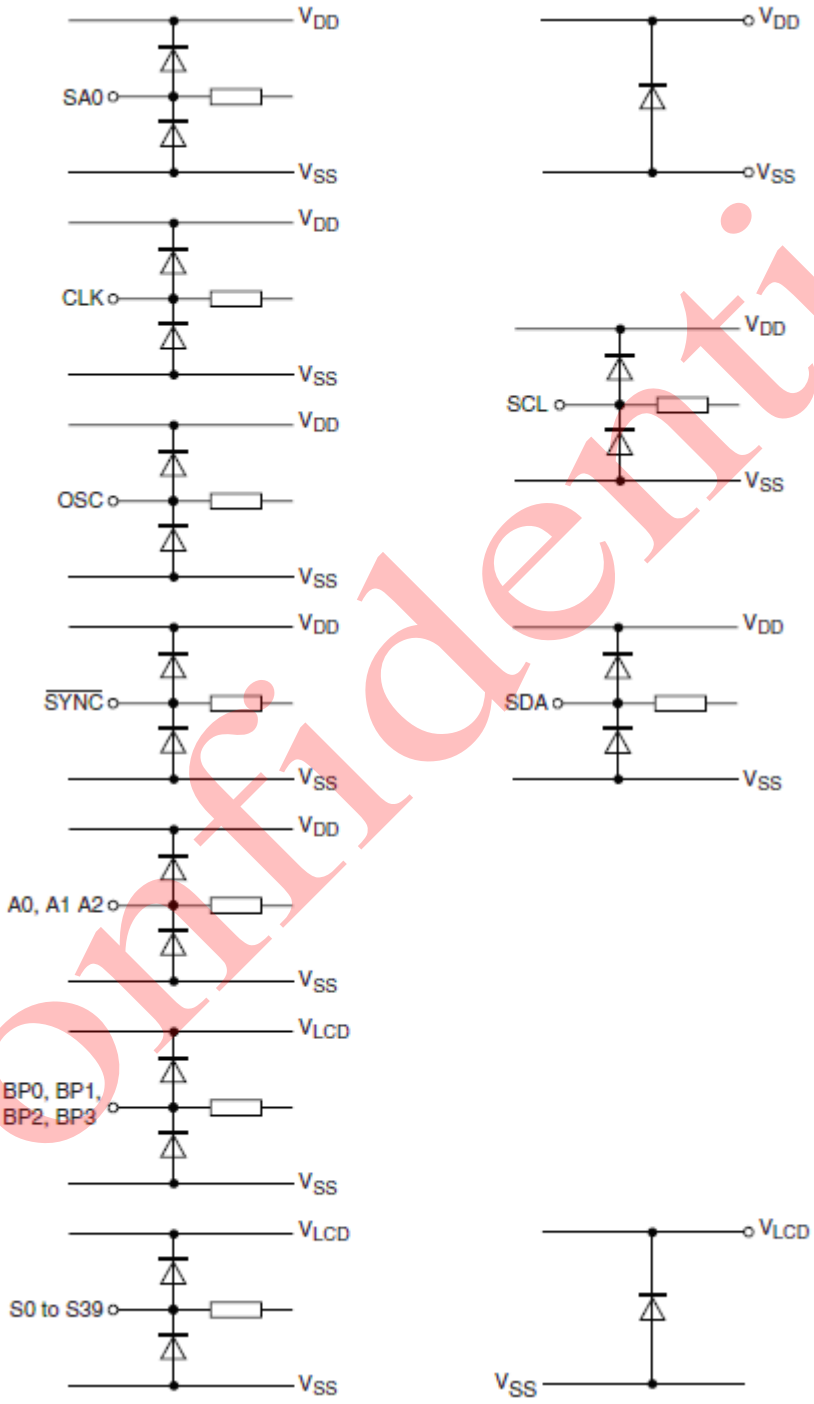
Type	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	Turn on V_{DD} and V_{LCD}	Wait until V_{DD}, V_{LCD} are stable
R	–	–	–	–	–	–	–	–	Wait 1mS	
R	–	–	–	–	–	–	–	–	Set RST pin High	Wait 10uS after RST is High.
R	C	1	1	0	1	#	#	#	Select Frame Rate	
R	C	1	1	0	0	#	#	#	Select Device	
R	C	1	1	1	1	0	#	#	Select Bank	
R	C	1	1	1	0	#	#	#	Select Blink Mode	
R	C	0	#	#	#	#	#	#	Set load data pointer	
O	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM Bit Map	Set up display image
R	C	1	0	0	1	0	0	0	Set Display Mode	Set display enable

Power-Down

Type	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	C	1	0	0	0	0	0	0	Set Display Mode	Set display disable
R	–	–	–	–	–	–	–	–		V_{DD} and V_{LCD} OFF

INTERNAL CIRCUITRY

Device Protection Circuits



ABSOLUTE MAXIMUM RATING

In accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DD}	Supply voltage		–0.5	+6.05	V
V_{LCD}	LCD supply voltage		–0.5	+12.1	V
Vi	Input Voltage	On each of the pins: CLK, SDA, SCL, $\overline{SYNC}$, SA0, OSC, A0 to A2	–0.5	+6.05	V
Vo	Output Voltage	On each of the pins: S0 to S39, BP0 to BP3	–0.5	+12.1	V
Ii	Input current		–10	+10	mA
Io	Output current		–10	+10	mA
I_{DD}	Supply current		–50	+50	mA
$I_{DD(LCD)}$	LCD supply current		–50	+50	mA
Iss	Ground supply current		–50	+50	mA
P_{TOT}	Total power dissipation		–	400	mW
Po	Output Power		–	100	mW
t_{STG}	Storage temperature		-55	+125	°C
t_{OPR}	Operation temperature		-40	+85	°C

Note: Static voltages across the liquid crystal display (LCD) can build up when the LCD supply voltage (V_{LCD}) is ON while the IC supply voltage (V_{DD}) is OFF, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

DC CHARACTERISTICS

V_{DD}=2.5V~5.5V, Vss=0V, V_{LCD}=2.5V~11.0V, Ta=–40°C~+85°C; unless otherwise specified.

Symbol	Characteristics	Condition		Min.	Typical	Max.	Unit
Supply							
V_{DD}	Supply voltage			2.5	–	5.5	V
V_{LCD}	LCD supply voltage	[1]		2.5	–	11.0	V
I_{DD}	Supply current	$f_{CLK(EXT)}$=1536Hz [2]		–	–	20	uA
$I_{DD(LCD)}$	LCD supply current	$f_{CLK(EXT)}$=1536Hz [2]		–	–	60	uA
Logic							
V_{POR}	Power-on reset voltage			1.0	1.3	1.6	V
V_{IL}	Input voltage – low	on pins CLK, $\overline{SYNC}$, OSC, A0~A2, SA0, SCL, SDA [3] [4]		Vss	–	0.2 V_{DD}	V
V_{IH}	Input voltage – high			0.8 V_{DD}	–	V_{DD}	V
I_{OL}	Output current – low	Output sink current; V_{OL}=0.4V, V_{DD}=5V	On pins CLK and $\overline{SYNC}$	1	–	–	mA
			On pin SDA	3	–	–	mA
$I_{OH(CLK)}$	Output current – high	Output source current; V_{OH}=4.6V, V_{DD}=5V		+1	–	–	mA
I_L	Leakage current	on pins CLK, SCL, SDA, A0~A2, SA0, V_I=V_{DD} or Vss.		–1	–	+1	uA
$I_{L(OSC)}$	Leakage current	V_I=V_{DD}		–1	–	+1	uA
C_I	Input capacitance	[5]		–	–	7	pF
LCD outputs							
ΔVo	Output voltage variation	on pin BP0~BP3 and S0~S39		-100	–	+100	mV
Ro	Output resistance	V_{LCD}=5V, on pin BP0~BP3 [6]		–	1.5	–	kΩ
		V_{LCD}=5V, on pin S0~S39 [6]		–	6.0	–	kΩ

Note:

[1] V_{LCD} > 3V for 1/3 bias

[2] LCD outputs are open-circuit; inputs at Vss or V_{DD}; external clock with 50% duty factor; I^2C bus inactive.

[3] When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in the “Absolute Maximum Rating” section on last page.

[4] Propagation delay of driver between clock (CLK) and LCD driving signals.

[5] Periodically sampled, not 100% tested.

[6] Outputs measured one at a time.

AC CHARACTERISTICS

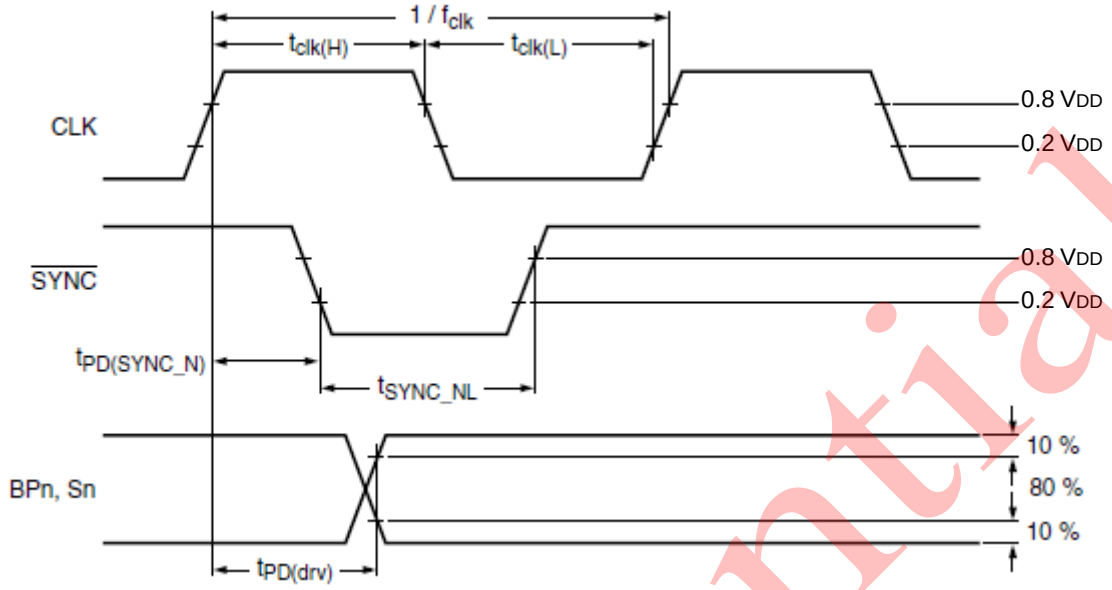


Figure: Driver Timing Waveform

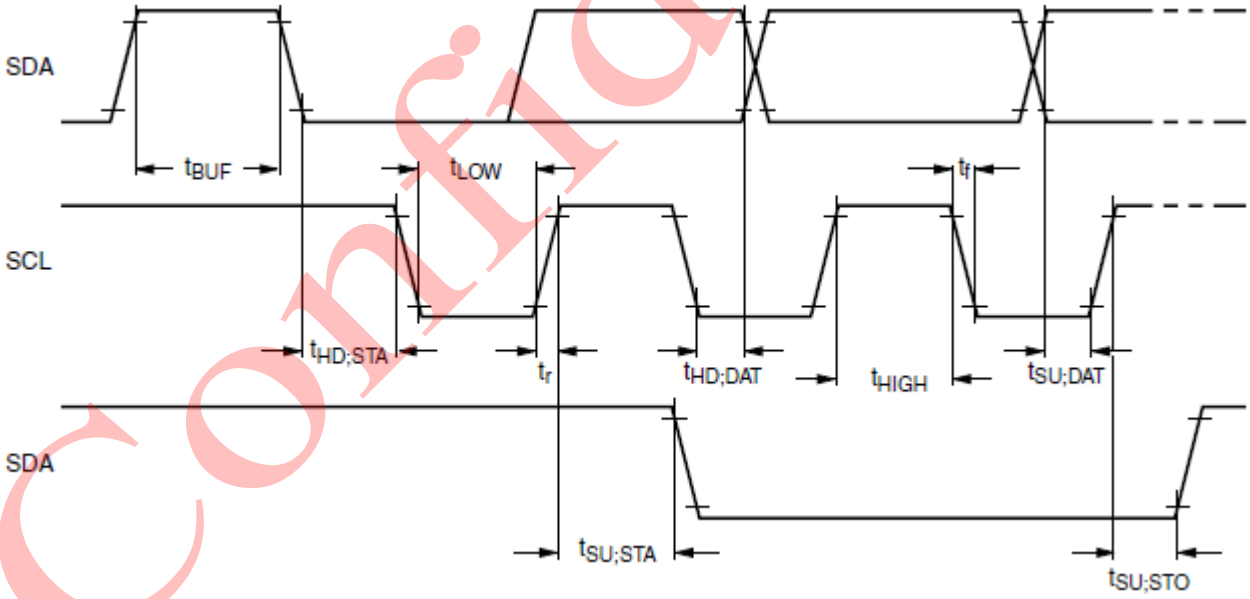


Figure: I²C Bus Timing Waveform

V_{DD}=2.5V~5.5V, Vss=0V, V_{LCD}=2.5V~11.0V, T_{AMB}= –40°C~+85°C; unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock						
$f_{CLK\ (INT)}$	Internal clock frequency	[1]	-25%	1536 1970 **2640** 4800	+25%	Hz
$f_{CLK\ (EXT)}$	External clock frequency		800	–	9600	Hz
$f_{FR\ (INT)}$	Internal clock Frame frequency		-25%	64 82 **110** 200	+25%	Hz
$f_{FR\ (EXT)}$	External clock Frame frequency		33	–	400	
$t_{CLK(H)}$	High-level clock time		60	–	–	uS
$t_{CLK(L)}$	Low-level clock time		60	–	–	uS
Synchronization						
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay		–	30	–	nS
t_{SYNC_NL}	$\overline{SYNC}$ low time		[2]	–	–	uS
$t_{PD(DRV)}$	Driver propagation delay	V_{LCD}=5V [3]	–	–	30	uS
I^2C bus timing [4]						
f_{SCL}	SCL clock frequency	pin SCL	–	–	400	kHz
t_{LOW}	LOW period of the SCL clock	pin SCL	1.3	–	–	uS
t_{HIGH}	HIGH period of the SCL clock	pin SCL	0.6	–	–	uS
$t_{SU;DAT}$	Data set-up time	pin SDA	100	–	–	nS
$t_{HD;DAT}$	Data hold time	pin SDA	0	–	–	nS
t_{BUF}	Bus free time between STOP & START	pins SCL and SDA	1.3	–	–	uS
$t_{SU;STO}$	Set-up time from STOP condition		0.6	–	–	uS
$t_{HD;STA}$	Hold time (repeated) START condition		0.6	–	–	uS
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6	–	–	uS
t_R	Rise time of both SDA and SCL signals	F_{SCL}=400kHz	–	–	0.3	uS
		F_{SCL}<125Hz	–	–	1.0	
t_F	Fall time of both SDA and SCL signals		–	–	0.3	uS
C_B	Capacitive load for each bus line		–	–	400	pF
$t_{W(SPIKE)}$	Spike pulse width	On the I^2C bus	–	–	50	nS

Note:
[1] Typical output duty factor: 50 % measured at the CLK output pin.
[2] The value is half cycle time.
[3] Not tested in production.
[4] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

CASCADED OPERATION

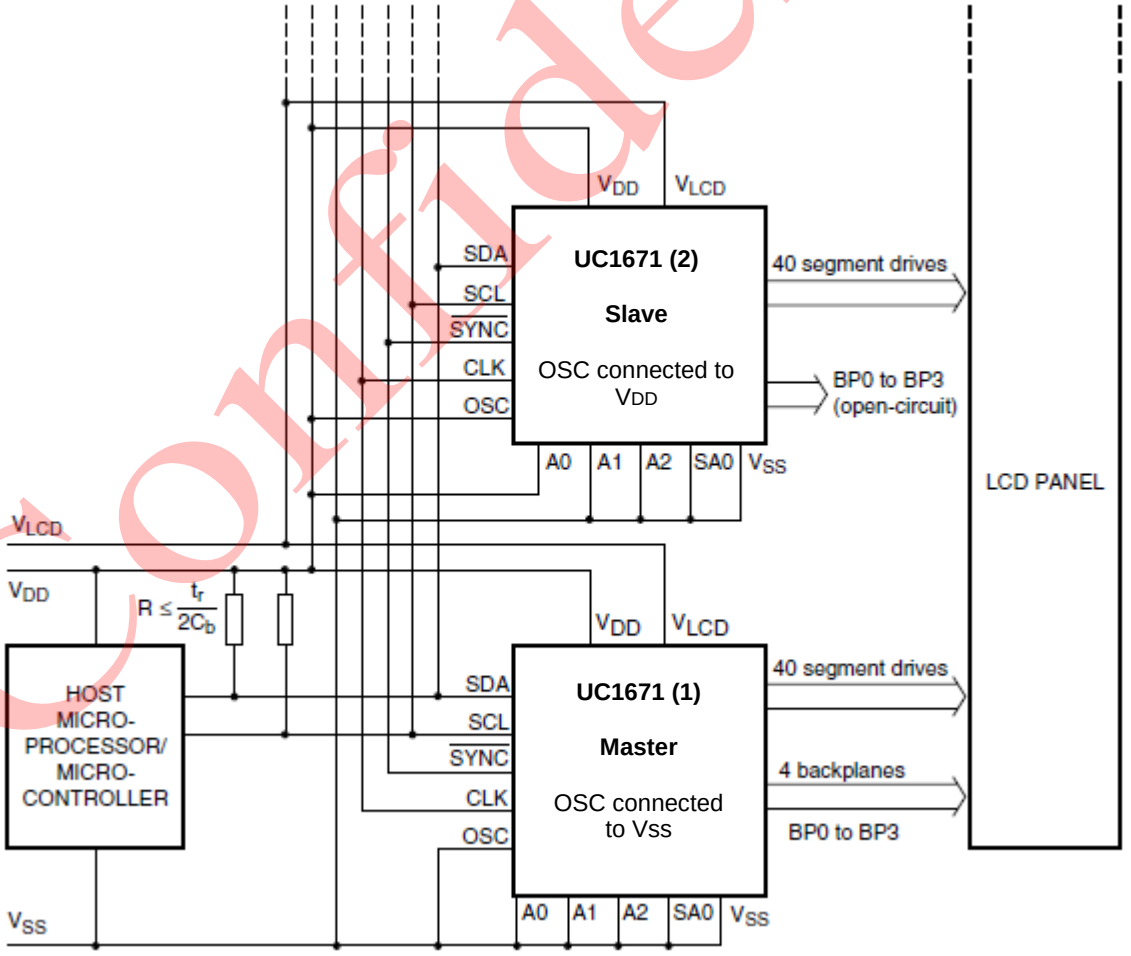
In large display configurations, up to 16 UC1671, can be recognized on the same I²C bus by using the 3-bit hardware sub-address (A0, A1, and A2) and the programmable I²C bus slave address (SA0).

Cluster	SA0	A[2:0]	Device
1	0	000 b	0
		001 b	1
		010 b	2
		011 b	3
		100 b	4
		101 b	5
		110 b	6
		111 b	7

Cluster	SA0	A[2:0]	Device
2	1	000 b	8
		001 b	9
		010 b	10
		011 b	11
		100 b	12
		101 b	13
		110 b	14
		111 b	15

When cascaded UC1671 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other UC1671 of the cascade contribute additional SEG outputs, but their backplane outputs are left open-circuit (See the following Figure).

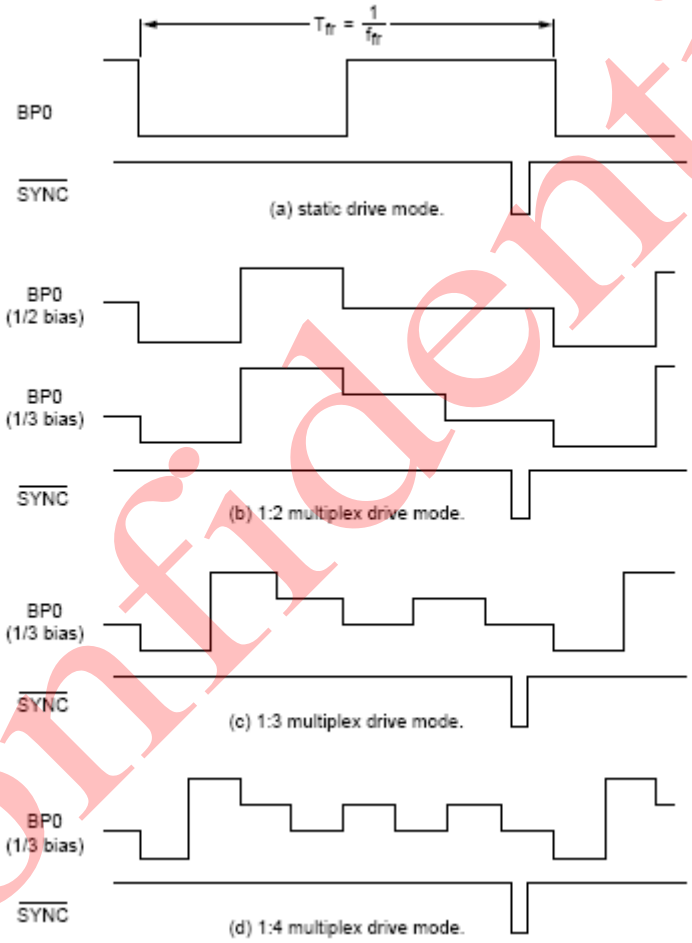
Cascaded UC1671 Configuration



The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded UC1671's. Synchronization is guaranteed after the Power-ON Reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by the definition of a multiplex drive mode when UC1671 with different SA0 levels are cascaded).

$\overline{SYNC}$ is organized as an input/output pin; The output selection is realized as an open-drain driver with an internal pull-up resistor. A UC1671 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first UC1671 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the UC1671 are shown in the Figure below.

Synchronization of the Cascade for the various UC1671 drive modes



The contact resistance between the $\overline{SYNC}$ pins on each cascaded device must be controlled. If the resistance is too high, the device can not synchronize properly; this is particularly applicable to Chip-on-Glass applications. The table below shows the maximum $\overline{SYNC}$ contact resistance allowed for the number of devices in cascade.

Number of devices	Maximum contact resistance
2	6000 Ω
3~5	2200 Ω
6~10	1200 Ω
11~16	700 Ω

The UC1671 can always be cascaded with other devices of the same type or conditionally with other devices of the same family. This allows optimal drive selection for a given number of pixels to display.

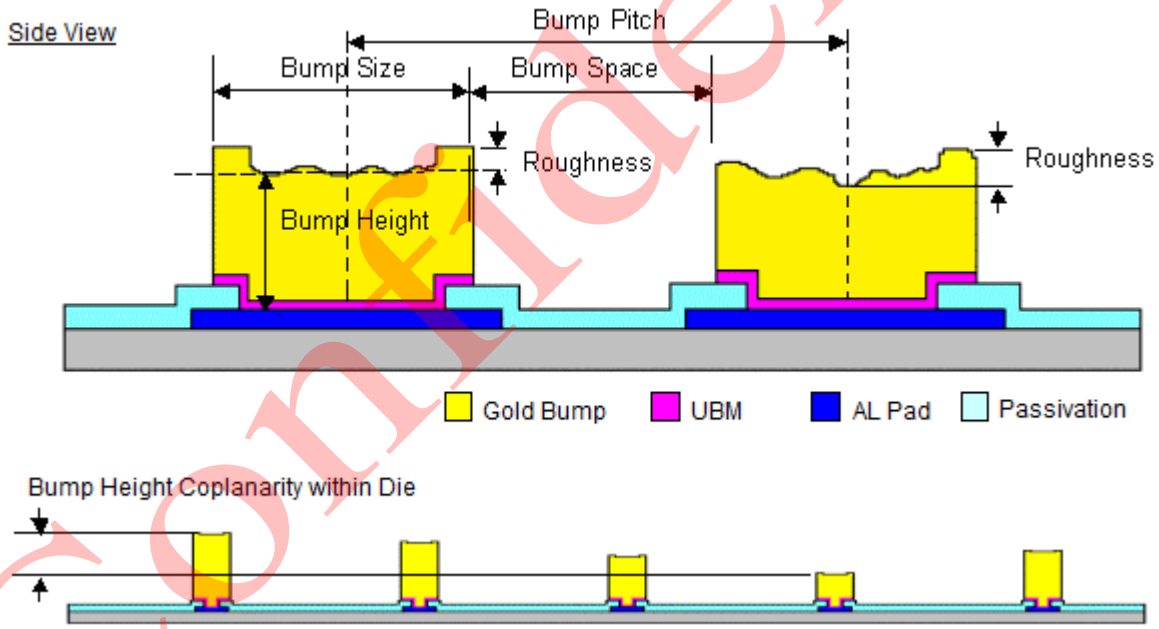
In a cascaded configuration, only one UC1671 master must be used as clock source. All other UC1671's in the cascade must be configured as slave such that they receive the clock from the master.

If an external clock source is used, all UC1671's in the cascade must be configured such as to receive the clock from that external source (pin OSC connected to V_{DD}). Thereby it must be ensured that the clock tree is designed such that on all UC1671's the clock propagation delay from the clock source to all UC1671 in the cascade is as equal as possible since otherwise synchronization artefacts may occur.

In mixed cascading configurations, care has to be taken that the specifications of the individual cascaded devices are met at all times.

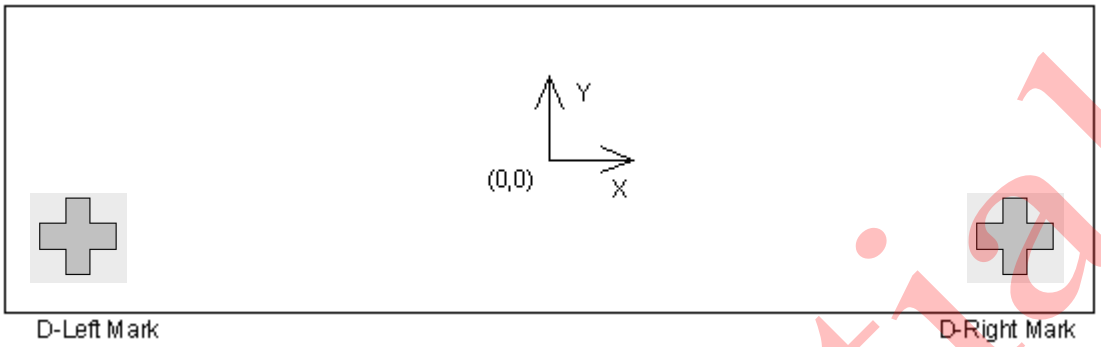
PHYSICAL DIMENSIONS

Die Size:	(2840μM ± 40μM) x (840μM ± 40μM)
Die Thickness:	400μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	9μM ± 3μM (Part Number: UC1671cGAD)
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Bump Size:	30μMx84μM ± 2μM
Bump Pitch:	50μM
Bump Space:	18 ± 3μM
Bump Area:	2520μM^2
Coordinate origin:	Chip center
Pad reference:	Pad center

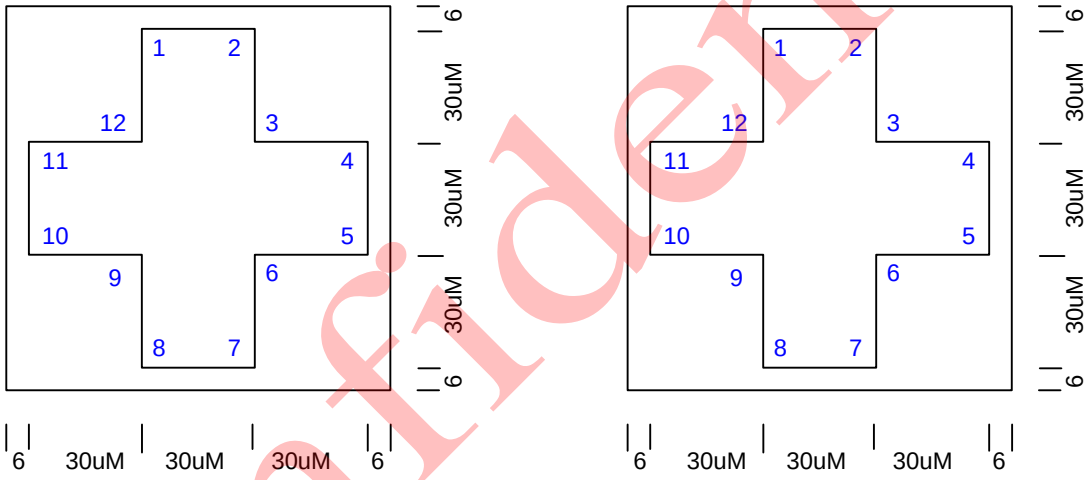


ALIGNMENT MARK INFORMATION

ALIGNMENT MARK POSITION:



ALIGNMENT MARK SHAPES:



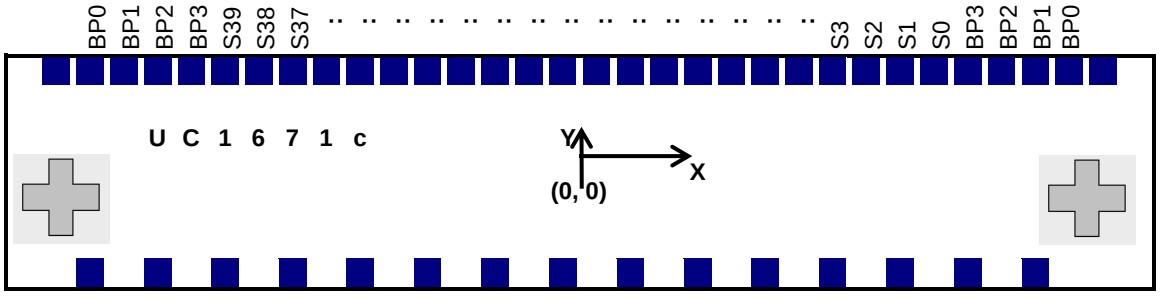
ALIGNMENT MARK COORDINATES:

Point	D-Left mark		D-Right mark	
	X	Y	X	Y
1	-1325	-215	1295	-215
2	-1295	-215	1325	-215
3	-1295	-245	1325	-245
4	-1265	-245	1355	-245
5	-1265	-275	1355	-275
6	-1295	-275	1325	-275
7	-1295	-305	1325	-305
8	-1325	-305	1295	-305
9	-1325	-275	1295	-275
10	-1355	-275	1265	-275
11	-1355	-245	1265	-245
12	-1325	-245	1295	-245

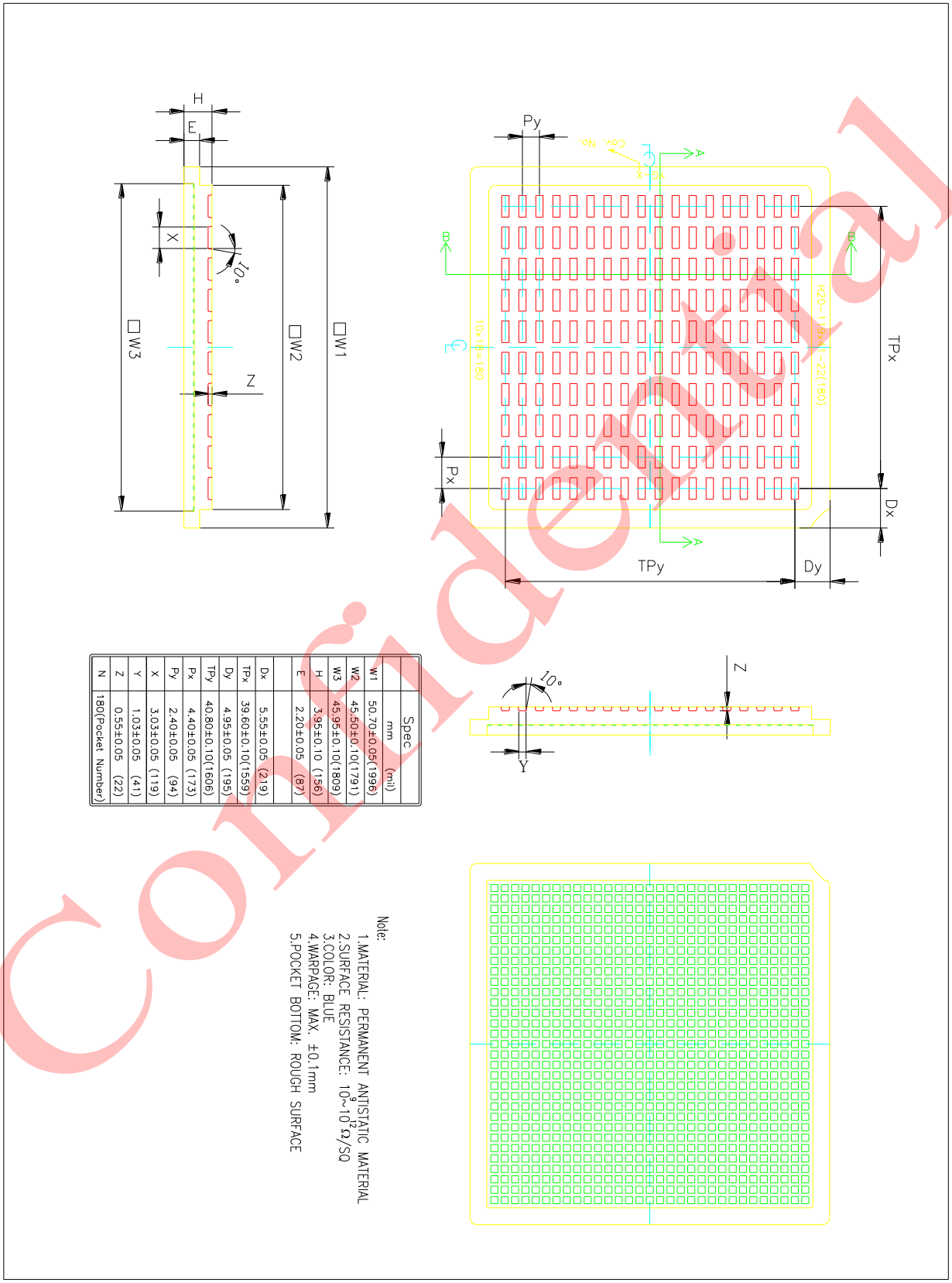
PAD COORDINATES

#	Name	X	Y	W	H
1	DUMMY	-1224	-333	30	84
2	SDA	-1122	-333	30	84
3	SDA	-1020	-333	30	84
4	SCL	-918	-333	30	84
5	SCL	-816	-333	30	84
6	SYNC	-714	-333	30	84
7	CLK	-612	-333	30	84
8	RSTB	-510	-333	30	84
9	VDD	-408	-333	30	84
10	VDD	-306	-333	30	84
11	VDD	-204	-333	30	84
12	OSC	-102	-333	30	84
13	A0	0	-333	30	84
14	A1	102	-333	30	84
15	A2	204	-333	30	84
16	SA0	306	-333	30	84
17	TEST2	408	-333	30	84
18	TEST1	510	-333	30	84
19	VSS	612	-333	30	84
20	VSS	714	-333	30	84
21	VSS	816	-333	30	84
22	VLCD	918	-333	30	84
23	VLCD	1020	-333	30	84
24	VLCD	1122	-333	30	84
25	DUMMY	1224	-333	30	84
26	DUMMY	1275	335	32	80
27	BP0	1225	335	32	80
28	BP1	1175	335	32	80
29	BP2	1125	335	32	80
30	BP3	1075	335	32	80
31	S0	1025	335	32	80
32	S1	975	335	32	80
33	S2	925	335	32	80
34	S3	875	335	32	80
35	S4	825	335	32	80
36	S5	775	335	32	80
37	S6	725	335	32	80
38	S7	675	335	32	80
39	S8	625	335	32	80

#	Name	X	Y	W	H
40	S9	575	335	32	80
41	S10	525	335	32	80
42	S11	475	335	32	80
43	DUMMY	425	335	32	80
44	S12	375	335	32	80
45	S13	325	335	32	80
46	S14	275	335	32	80
47	S15	225	335	32	80
48	S16	175	335	32	80
49	S17	125	335	32	80
50	S18	75	335	32	80
51	S19	25	335	32	80
52	S20	-25	335	32	80
53	S21	-75	335	32	80
54	S22	-125	335	32	80
55	S23	-175	335	32	80
56	S24	-225	335	32	80
57	S25	-275	335	32	80
58	S26	-325	335	32	80
59	S27	-375	335	32	80
60	DUMMY	-425	335	32	80
61	S28	-475	335	32	80
62	S29	-525	335	32	80
63	S30	-575	335	32	80
64	S31	-625	335	32	80
65	S32	-675	335	32	80
66	S33	-725	335	32	80
67	S34	-775	335	32	80
68	S35	-825	335	32	80
69	S36	-875	335	32	80
70	S37	-925	335	32	80
71	S38	-975	335	32	80
72	S39	-1025	335	32	80
73	BP3	-1075	335	32	80
74	BP2	-1125	335	32	80
75	BP1	-1175	335	32	80
76	BP0	-1225	335	32	80
77	DUMMY	-1275	335	32	80



TRAY INFORMATION



REVISION HISTORY

Revision	Content	Date
0.6	(First Release)	Aug. 19, 2020
0.61	The "Mode-set"command is updated.	Mar. 9, 2021
0.62	Remove register default values.	Jun. 25, 2021