General Description

The VK2C23 device is a memory mapping and multi-function LCD controller driver. The Display segments of the device are 224 patterns (56 segments and 4commons) or 416 patterns (52 segments and 8commons). The software configuration feature of the VK2C23 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The VK2C23 device communicates with most microprocessors / microcontrollers via a two-line bidirectional I²C-bus.

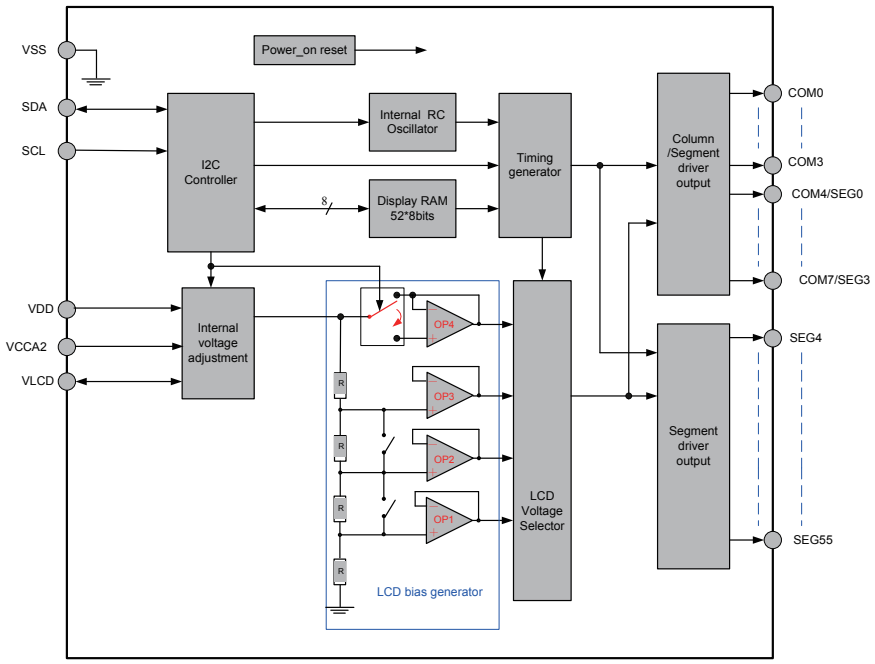
Features

- Operating voltage: 2.4 ~ 5.5V
- Internal 32kHz RC oscillator
- Bias: 1/3 or 1/4; Duty:1/4 or 1/8
- Internal LCD bias generation with voltage-follower buffers
- I²C-bus interface
- Two Selectable LCD frame frequencies: 80Hz or 160Hz
- Up to 52 x 8 bits RAM for display data storage
- Display patterns:
  – 56 x 4 patterns: 56 segments and 4 commons
  – 52 x 8 patterns: 52 segments and 8 commons
- Versatile blinking modes
- R/W address auto increment
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Low power consumption
- Provides V_{LCD} pin to adjust LCD operating voltage
- Manufactured in silicon gate CMOS process
- Package Type: 48LQFP, 64LQFP, Chip and Goldbump chip.

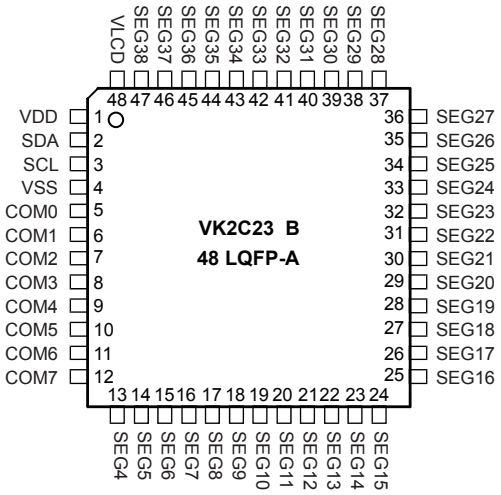
Applications

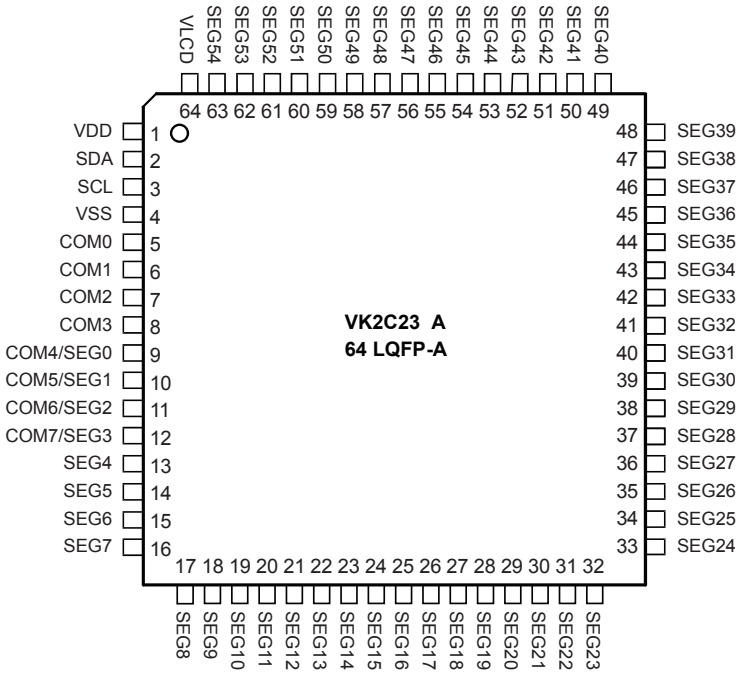
- Electronic meter
- Water meter
- Gas meter
- Heat energy meter
- •Household appliance
- •Games
- •Telephone
- •Consumer electronics

Block Diagram



Pin Assignment



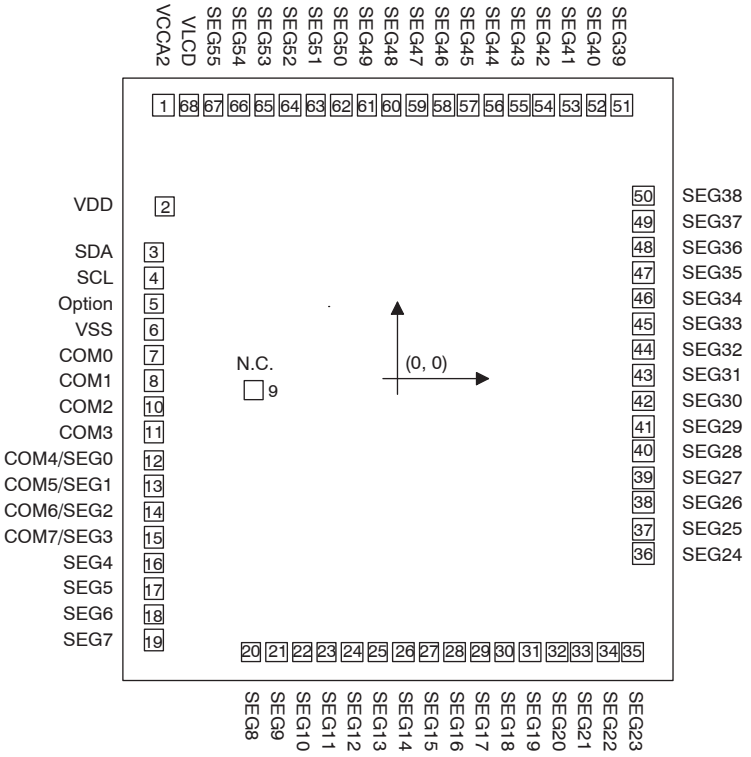


Note: 1. Application at $V_{DD} \leq V_{LCD}$ or $V_{LCD} \leq V_{DD}$.

2. When the 48-pin LQFP package is selected, this device does not support LCD 1/4 duty.

3. The VCCA2 pad is internally connected with the VLCD pad.

Pad assignment for COB



Chip size: 1843 x 2018μm²

Note: 1. The option (pad 5) must be bonded to V_{DD} or floating.

2. The IC substrate should be connected to V_{SS} in the PCB layout artwork.

3. VLCD (pad 68) and VCCA2 (pad 1) must be bonded together for the application at $V_{DD} \le V_{LCD}$ or $V_{LCD} \le V_{DD}$.

Internal voltage adjustment (IVA) set command		VLCD (pad 68)	SEG55 (pad 67)	Note
DE bit	VE bit			
0	0	Input	Null	• VLCD support internal bias voltage.
0	1	Input	Null	• Internal Voltage Adjustment is null • VLCD support internal bias voltage
1	0	Input	Output	• VLCD support internal bias voltage
1	1	Input	Output	• VLCD support internal bias voltage

4. VDD (pad2) and VCCA2 (pad 1) must be bonded together for the application at $V_{LCD} \le V_{DD}$.

Internal voltage adjustment (IVA) set command		VLCD (pad 68)	SEG55 (pad 67)	Note
DE bit	VE bit			
0	0	Input	Null	• VLCD support internal bias voltage.
0	1	Output	Null	• Detect the internal bias voltage • VDD support internal bias voltage
1	0	Floating	Output	• VDD support internal bias voltage
1	1	Floating	Output	• VDD support internal bias voltage

Pad Coordinates for COB

Unit: μm

No	Name	X	Y	No	Name	X	Y
1	VCCA2	-788.05	905.4	35	SEG23	780.15	-905.4
2	VDD	-783.15	572.25	36	SEG24	817.45	-582.35
3	SDA	-817.9	419.55	37	SEG25	817.45	-497.35
4	SCL	-817.9	334.55	38	SEG26	817.45	-412.35
5	OPTION	-817.9	249.55	39	SEG27	817.45	-327.35
6	VSS	-817.9	164.55	40	SEG28	817.45	-242.35
7	COM0	-817.9	79.55	41	SEG29	817.45	-157.35
8	COM1	-817.9	-5.45	42	SEG30	817.45	-72.35
9	N.C.	-484.014	-35.6	43	SEG31	817.45	12.65
10	COM2	-817.9	-90.45	44	SEG32	817.45	97.65
11	COM3	-817.9	-175.45	45	SEG33	817.45	182.65
12	COM4/SEG0	-817.9	-270.35	46	SEG34	817.45	267.65
13	COM5/SEG1	-817.9	-355.35	47	SEG35	817.45	352.65
14	COM6/SEG2	-817.9	-440.35	48	SEG36	817.45	437.65
15	COM7/SEG3	-817.9	-525.35	49	SEG37	817.45	522.65
16	SEG4	-817.9	-613.1	50	SEG38	817.45	607.65
17	SEG5	-817.9	-698.1	51	SEG39	741.95	905.4
18	SEG6	-817.9	-783.1	52	SEG40	656.95	905.4
19	SEG7	-817.9	-868.1	53	SEG41	571.95	905.4
20	SEG8	-494.85	-905.4	54	SEG42	486.95	905.4
21	SEG9	-409.85	-905.4	55	SEG43	401.95	905.4
22	SEG10	-324.85	-905.4	56	SEG44	316.95	905.4
23	SEG11	-239.85	-905.4	57	SEG45	231.95	905.4
24	SEG12	-154.85	-905.4	58	SEG46	146.95	905.4
25	SEG13	-69.85	-905.4	59	SEG47	61.95	905.4
26	SEG14	15.15	-905.4	60	SEG48	-23.05	905.4
27	SEG15	100.15	-905.4	61	SEG49	-108.05	905.4
28	SEG16	185.15	-905.4	62	SEG50	-193.05	905.4
29	SEG17	270.15	-905.4	63	SEG51	-278.05	905.4
30	SEG18	355.15	-905.4	64	SEG52	-363.05	905.4
31	SEG19	440.15	-905.4	65	SEG53	-448.05	905.4
32	SEG20	525.15	-905.4	66	SEG54	-533.05	905.4
33	SEG21	610.15	-905.4	67	SEG55	-618.05	905.4
34	SEG22	695.15	-905.4	68	VLCD	-703.05	905.4

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS} = 0V; V_{DD} =2.4V to 5.5V; Ta = -40 to +85°C. VCCA2 pad is connected to VDD Pad

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3bias, f_{LCD}=80Hz, LCD display on, Internal system oscillator on, DA0~DA3 are set to "0000"	—	25	40	μA
		5V		—	35	50	μA
I_{DD1}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3bias f_{LCD}=80Hz, LCD display off, Internal system oscillator on, DA0~DA3 are set to "0000"	—	2	5	μA
		5V		—	4	10	μA
I_{STB}	Standby Current	3V	No load, V_{LCD}=V_{DD}, LCD display off, Internal system oscillator off,	—	—	1	μA
		5V		—	—	2	μA
V_{IH}	Input high Voltage	—	SDA ,SCL	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input low Voltage	—	SDA, SCL	0	—	0.3V_{DD}	V
I_{IL}	Input leakage current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low level output current	3V	V_{OL}=0.4V SDA	3	—	—	mA
		5V		6	—	—	mA
I_{OL1}	LCD COM Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD COM Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD SEG Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD SEG Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS} = 0V; V_{DD} = 2.4 to 5.5V; Ta= -40 to +85°C. VCCA2 pad is connected to VDD Pad

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD1}	LCD Frame Frequency	4V	1/4 duty, Ta =25°C	72	80	88	Hz
f_{LCD2}	LCD Frame Frequency	4V	1/4 duty, Ta =25°C	144	160	176	Hz
f_{LCD3}	LCD Frame Frequency	4V	1/4 duty,Ta=-40 to +85°C	52	80	124	Hz
f_{LCD4}	LCD Frame Frequency	4V	1/4 duty, Ta=-40 to +85°C	104	160	248	Hz
t_{OFF}	V_{DD} OFF Times	—	V_{DD} drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Slew Rate	—	—	0.05	—	—	V/ms

Note:

- If the conditions of Power on Reset timing are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.
- If the V_{DD} voltage drops below the minimum voltage of operating voltage spec. during operating, the Power on Reset timing conditions must also be satisfied. That is, the V_{DD} voltage must drop to 0V and remain at 0V for 20ms (min.) before rising to the normal operating voltage.

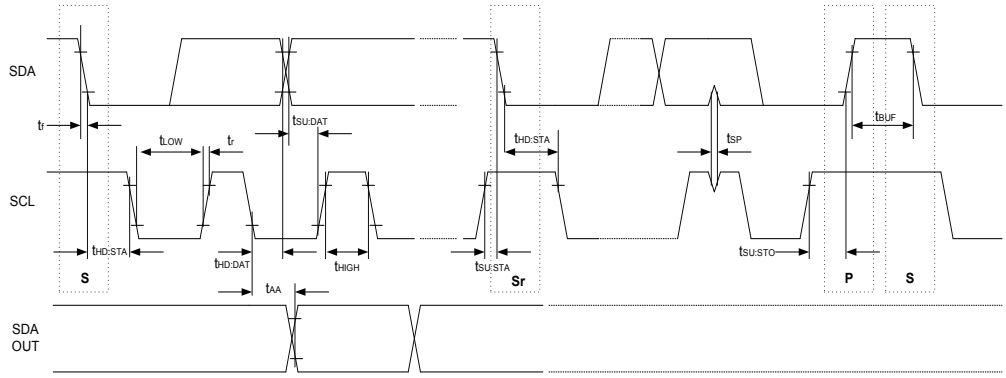
A.C. Characteristics – I²C Interface

Symbol	Parameter	Condition	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	KHZ
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD:STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4	—	0.6	—	μs
$t_{SU:STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rise Time	Note	—	1	—	0.3	μs
t_F	SDA and SCL Fall Time	Note	—	0.3	—	0.3	μs
$t_{SU:STO}$	Stop Condition set-up Time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

I²C Timing



Power On Reset Timing

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common / segment outputs are set to V_{DD} when VCCA2 pad is connected to VDD pad.
- All common / segment outputs are set to V_{LCD} when VCCA2 pad is connected to VLCD pad.
- The drive mode 1/4 duty output and 1/3 bias is selected for 64 pin LQFP package.
- The drive mode 1/8 duty output and 1/3 bias is selected for 48 pin LQFP package.
- The System Oscillator and the LCD bias generator are off state.
- LCD Display is off state.
- Internal voltage adjustment function is enabled.
- The Segment / VLCD shared pin is set as the Segment pin.
- Detection switch for the VLCD pin is disabled.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Display Memory – RAM Structure

The display RAM is static 52 x 8-bits RAM which stores the LCD data. Logic “1” in the RAM bit-map indicates the “on” state of the corresponding LCD segment; similarly, logic 0 indicates the ‘off’ state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The following is a mapping from the RAM data to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55					SEG54					1BH
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM Mapping of 56×4 Display Mode

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55									33H
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM Mapping of 52×8 Display Mode

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

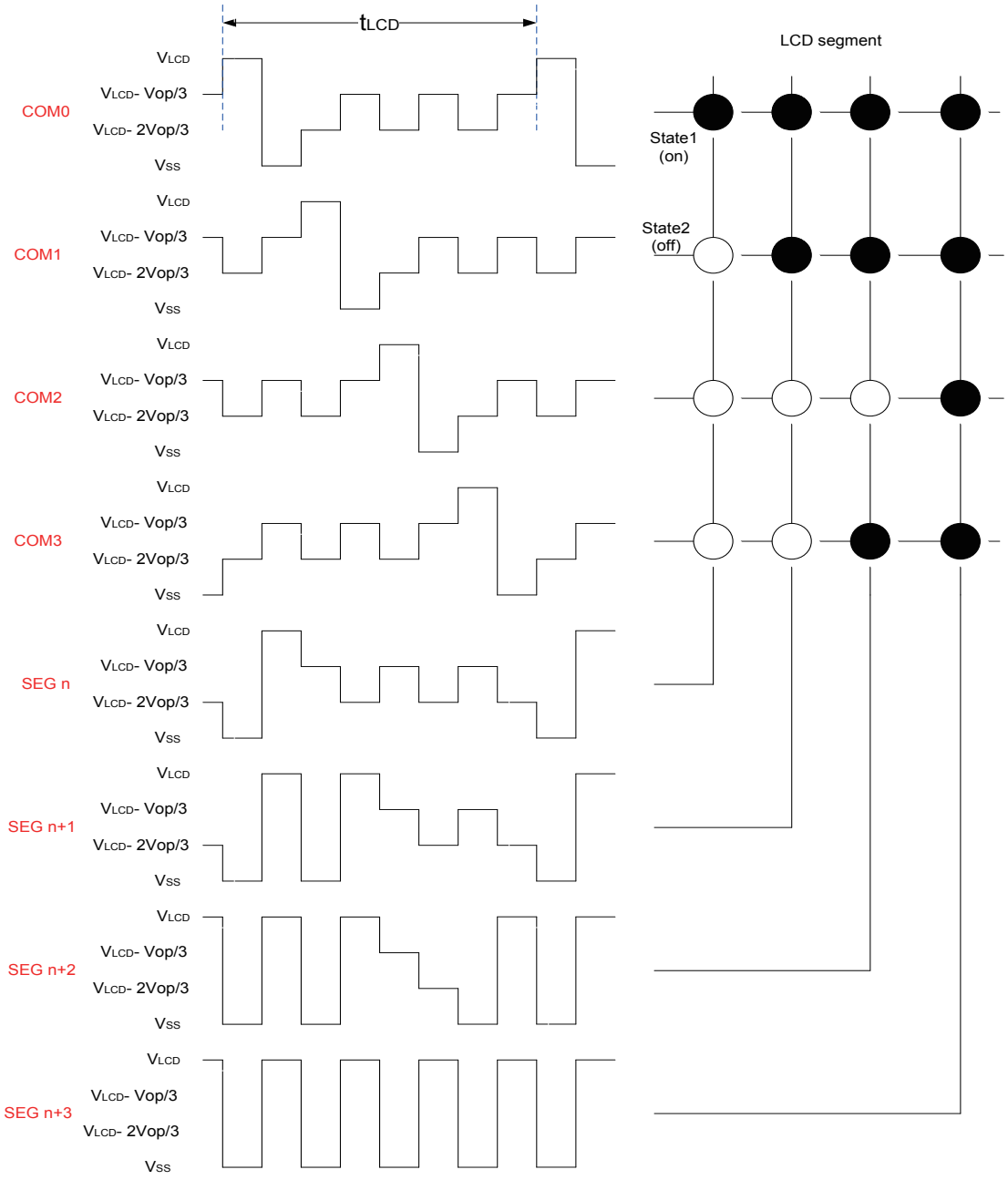
LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from (V_{LCD} – V_{SS}). The LCD voltage may be temperature compensated externally through the Voltage supply to the V_{LCD} pin.

Fractional LCD biasing voltages, known as 1/3 or 1/4 bias voltage, are obtained from an internal voltage divider of four series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of circuits to provide a 1/3bias voltage level configuration.

LCD Drive Mode Waveforms

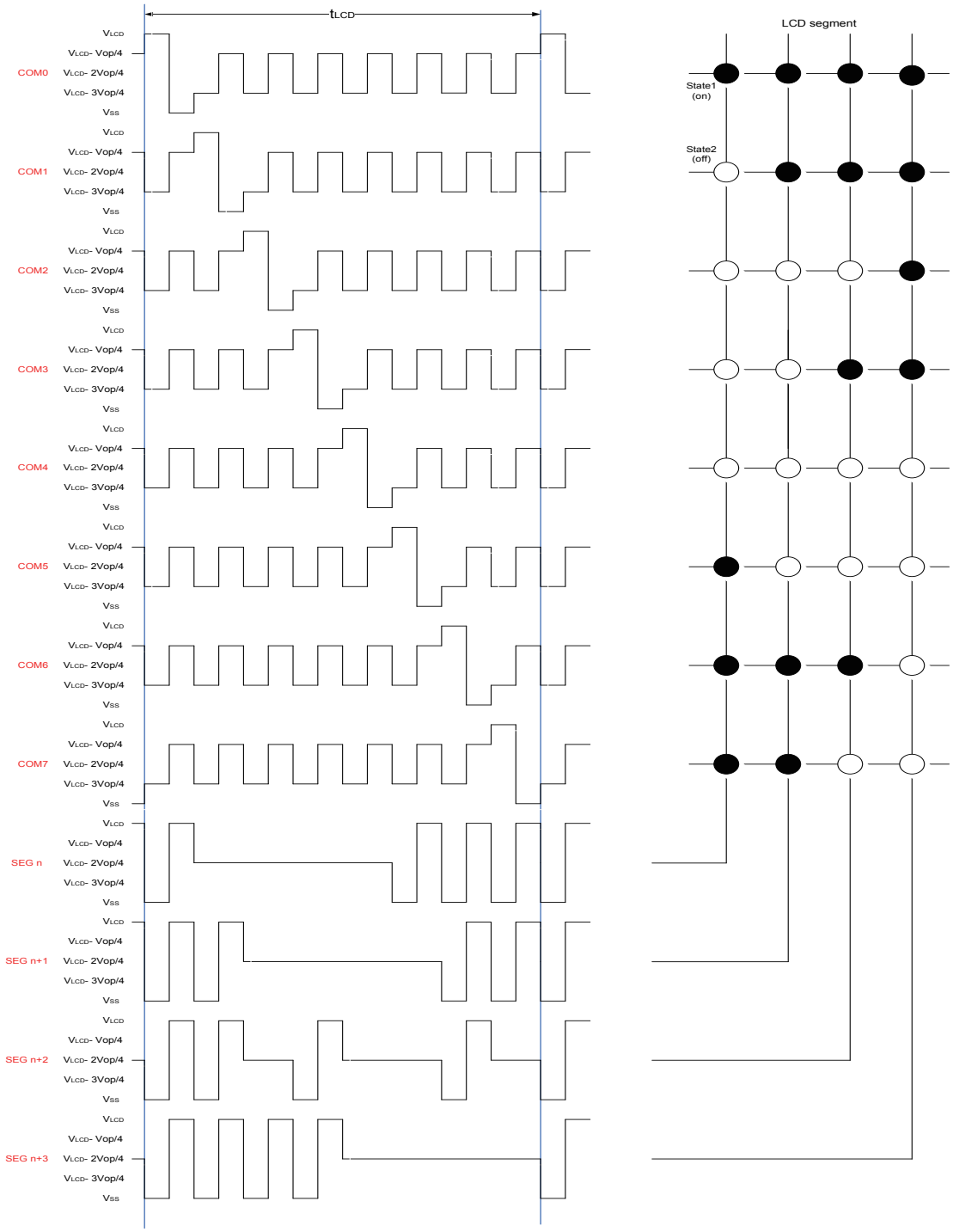
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with1/3 bias (V_{OP}=V_{LCD}-V_{SS})

Note: $t_{LCD}=1/f_{LCD}$

- When the LCD drive mode is selected as 1/8 duty and 1/4bias, the waveform and LCD display is shown as follows:



Waveforms for 1/8 duty drive mode with1/4 bias (V_{OP}=V_{LCD}-V_{SS})

Note: t_{LCD}=1/f_{LCD}

Segment Driver Outputs

The LCD drive section includes 56 segment outputs SEG0~SEG55 or 52 segment outputs SEG4~SEG55 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit when less than 56 or 52 segment outputs are required.

Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 or 8 column outputs COM0~COM7 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 or 8 column outputs are required.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Address pointer command.

Blinker Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blink command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

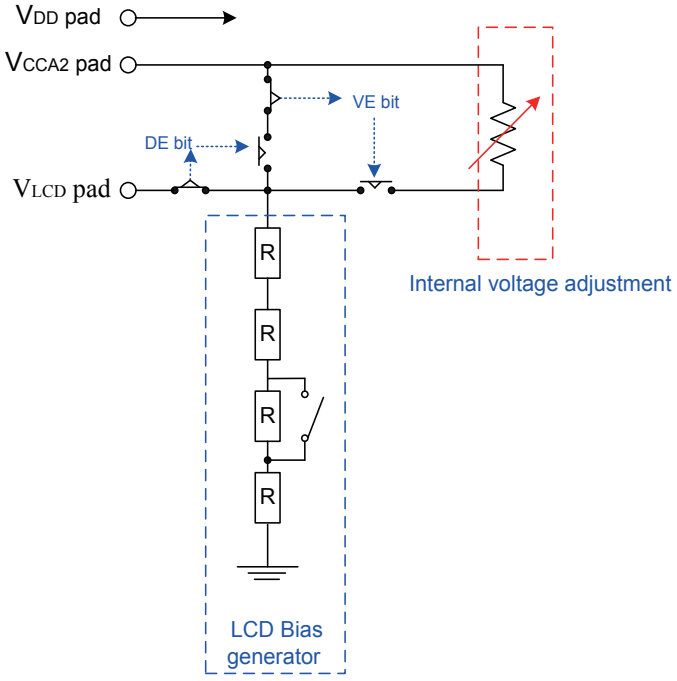
Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	Blink off
1	f_{SYS} / 16384Hz	2
2	f_{SYS} / 32768Hz	1
3	f_{SYS} / 65536Hz	0.5

Frame Frequency

The VK2C23 device provides two frame frequencies selected with Mode set command known as 80Hz and 160Hz respectively.

Internal VLCD Voltage Adjustment

- The internal V_{LCD} adjustment contains four resistors in series and a 4-bit programmable analog switch which can provide sixteen voltage adjustment options using the V_{LCD} voltage adjustment command.
- The internal V_{LCD} adjustment structure is shown in the diagram:



- The relationship between the programmable 4-bit analog switch and the V_{LCD} output voltage is shown in the table:

1. When VCCA2 pad is connected to VDD pad

Bias / DA3~DA0	1/3	1/4	Note
00H	1.000*V_{DD}	1.000*V_{DD}	Default value
01H	0.944*V_{DD}	0.957*V_{DD}	
02H	0.894*V_{DD}	0.918*V_{DD}	
03H	0.849*V_{DD}	0.882*V_{DD}	
04H	0.808*V_{DD}	0.849*V_{DD}	
05H	0.771*V_{DD}	0.818*V_{DD}	
06H	0.738*V_{DD}	0.789*V_{DD}	
07H	0.707*V_{DD}	0.763*V_{DD}	
08H	0.678*V_{DD}	0.738*V_{DD}	
09H	0.652*V_{DD}	0.714*V_{DD}	
0AH	0.628*V_{DD}	0.692*V_{DD}	
0BH	0.605*V_{DD}	0.672*V_{DD}	
0CH	0.584*V_{DD}	0.652*V_{DD}	
0DH	0.565*V_{DD}	0.634*V_{DD}	
0EH	0.547*V_{DD}	0.616*V_{DD}	
0FH	0.529*V_{DD}	0.600*V_{DD}	

2. When VCCA2 pad is connected to VLCD pad

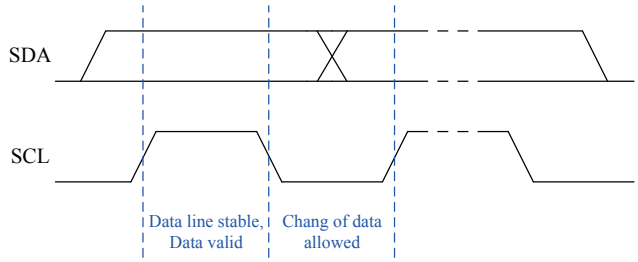
Bias / DA3~DA0	1/3	1/4	Note
00H	1.000*V_{LCD}	1.000* V_{LCD}	Default value
01H	0.944* V_{LCD}	0.957* V_{LCD}	
02H	0.894* V_{LCD}	0.918* V_{LCD}	
03H	0.849* V_{LCD}	0.882* V_{LCD}	
04H	0.808* V_{LCD}	0.849* V_{LCD}	
05H	0.771* V_{LCD}	0.818* V_{LCD}	
06H	0.738* V_{LCD}	0.789* V_{LCD}	
07H	0.707* V_{LCD}	0.763* V_{LCD}	
08H	0.678* V_{LCD}	0.738* V_{LCD}	
09H	0.652* V_{LCD}	0.714* V_{LCD}	
0AH	0.628* V_{LCD}	0.692* V_{LCD}	
0BH	0.605* V_{LCD}	0.672*V_{DD}	
0CH	0.584* V_{LCD}	0.652* V_{LCD}	
0DH	0.565* V_{LCD}	0.634* V_{LCD}	
0EH	0.547* V_{LCD}	0.616* V_{LCD}	
0FH	0.529* V_{LCD}	0.600* V_{LCD}	

I²C Serial Interface

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7KΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

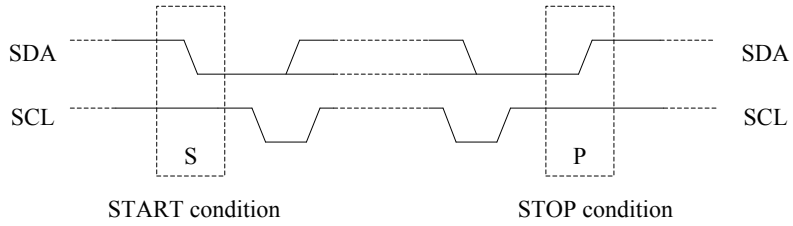
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



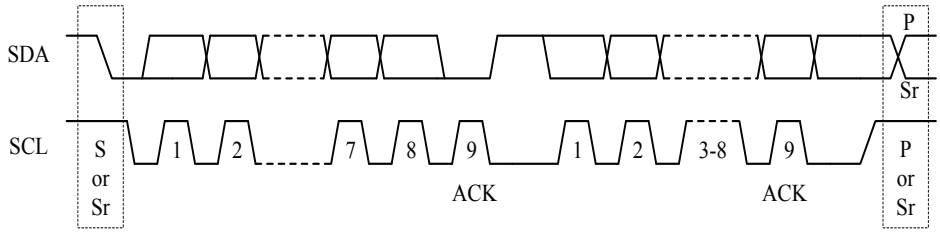
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



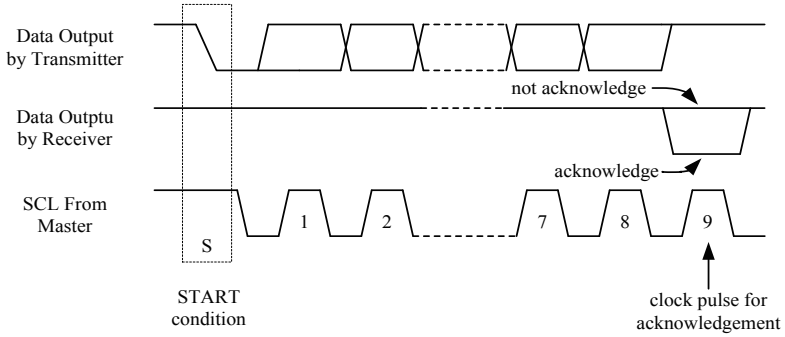
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

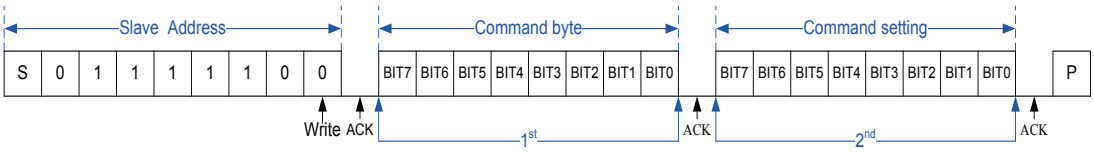
- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- The VK2C23 address bits are "0111110". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA line.

Write Operation

Byte Writes Operation

- **Command Byte**

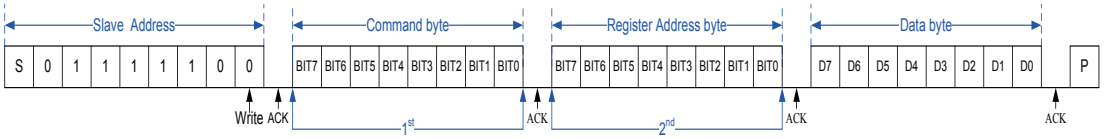
A Command Byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a command setting byte and a STOP condition for a command byte write operation.



Command Byte Write Operation

- **Display RAM Single Data Byte**

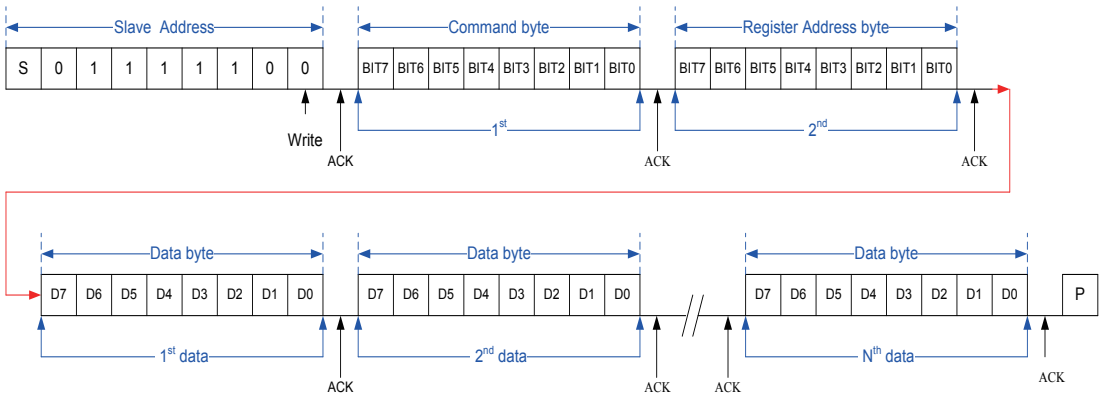
A display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a valid Register Address byte, a Data byte and a STOP condition.



Display RAM Single Data Byte Write Operation

Display RAM Page Write Operation

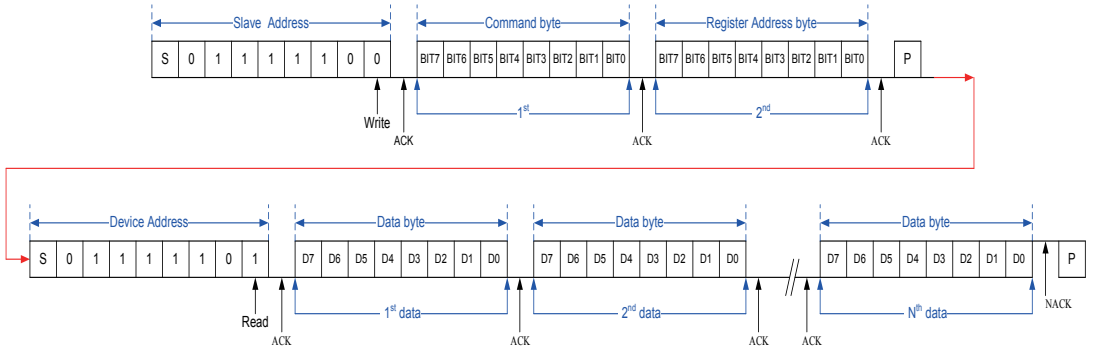
After a START condition the slave address with the R/$\overline{W}$ bit is placed on the bus followed with a command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, which is 1BH for 1/4 duty drive mode or 33H for 1/8 duty drive mode, the address pointer will be reset to 00H.



N Bytes Display RAM Data Write Operation

Display RAM Read Operation

- In this mode, the master reads the VK2C23 data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit ("1"). Then the MSB of the data which was addressed is transmitted first on the I²C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, which is 1Bh for 1/4 duty drive mode or 33H for 1/8 duty drive mode, the address pointer will be reset to 00H.
- This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Command Summary

Display Data Input Command

This command sends data from MCU to memory MAP of the VK2C23 device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Display Data Input/output Command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address of memory map	W	00H

Note:
- Power on status: the address is set to 00H.
- If the programmed command is not defined, the function will not be affected.
- For 1/4 duty drive mode after reaching the memory location 1BH, the pointer will reset to 00H.
- For 1/8 duty drive mode after reaching the memory location 33H, the pointer will reset to 00H.

Drive Mode Command

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Driver mode setting command	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias setting	2nd	X	X	X	X	X	X	Duty	Bias	No matter what “Duty” bit is set, 1/8 duty drive mode is only available for 48 LQFP.	W	00H

Note:

Bit		Duty	Bias
Duty	Bias		
0	0	1/4duty	1/3bias
0	1	1/4duty	1/4bias
1	0	1/8duty	1/3bias
1	1	1/8duty	1/4bias

- Power on status: The drive mode 1/4 duty output and 1/3 bias is selected.
- If the programmed command is not defined, the function will not be affected.

System Mode Command

This command controls the internal system oscillator on/off and display on/off.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/off Setting	2nd	X	X	X	X	X	X	S	E		W	00H

Note:

Bit		Internal System oscillator	LCD Display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

- Power on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

Frame Frequency Command

This command selects the frame frequency.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Note:

Bit	Frame Frequency
F	
0	80Hz
1	160Hz

- Power on status: Frame frequency is set to 80Hz.
- If the programmed command is not defined, the function will not be affected.

Blinking Frequency Command

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Blinking Frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking Frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Note:

Bit		Blinking Frequency
BK1	BK0	
0	0	Blinking off
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) adjustment can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Note	R/W	Def
IVA Command	1st	1	0	0	0	1	0	1	0		W	
IVA Control	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	• The Segment/VLCD shared pin can be programmed via the "DE" bit. • The "VE" bit is used to enable or disable the internal voltage adjustment is supply voltage to bias voltage. • The DA3~DA0 bits can be used to adjust the V_{LCD} output voltage.	W	30H

Note:

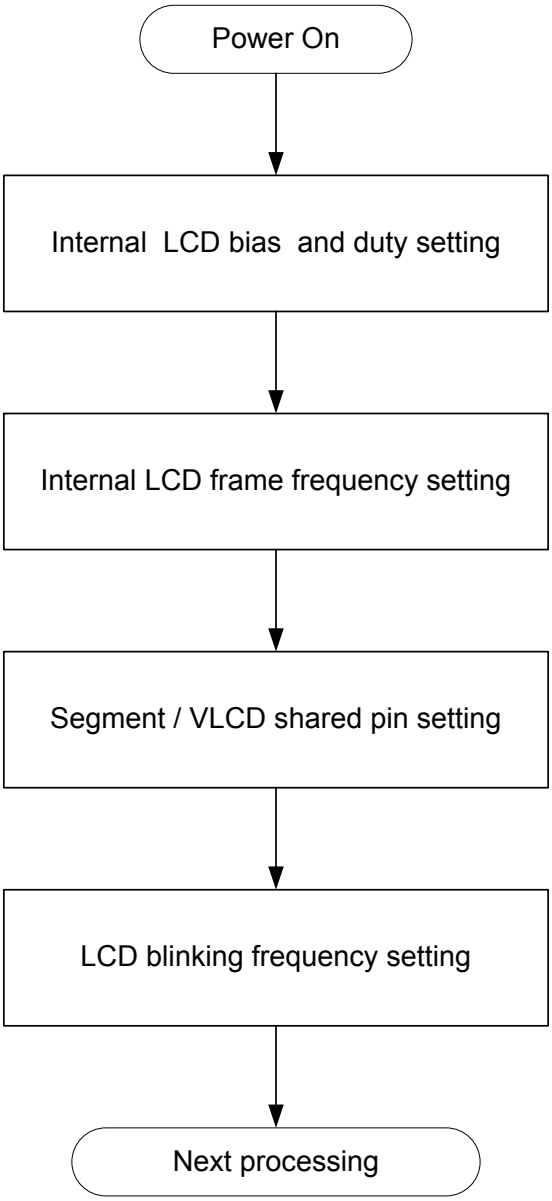
Bit		Segment 55/ VLCD shared pin select	Internal Voltage Adjustment	Note
DE	VE			
0	0	VLCD	off	• The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD. • The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VDD. • If the VLCD pin is connected to the VDD pin, the internal voltage follower (OP4) must be disabled by setting the DA3~DA0 bits as "0000".
0	1	VLCD	on	• When VCCA2 is connected to VLCD, internal voltage adjustment can not be used to adjust internal bias voltage. (Bias voltage is supplied by the external VLCD pin) • When VCCA2 is connected to VDD, internal voltage adjustment can not be used to adjust internal bias voltage when VLCD pin is supplies with external voltage.(Recommend: can not be used) • When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is floating and internal voltage adjustment is enable.(Bias voltage is supplied by the internal voltage adjustment)
1	0	Segment 55	off	• The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD. • The bias voltage is supplied by the external VDD power when VCCA2 is connected to VDD. • The internal voltage-follower (OP4) is disabled automatically and DA3~DA0 don't care.
1	1	Segment 55	on	• When VCCA2 is connected to VLCD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is supplies with external voltage and internal voltage adjustment is enable. (Bias voltage is supplied by the internal voltage adjustment) • When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when internal voltage adjustment is enable.(Bias voltage is supplied by the internal voltage adjustment)

- Power on status: Enable the internal voltage Adjustment and the Segment/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to "0000", the internal voltage-follower (OP4) is disabled. When the DA0~DA3 bits are set to other values except "0000", the internal voltage follower (OP4) is enabled.
- If the programmed command is not defined, the function will not be affected.

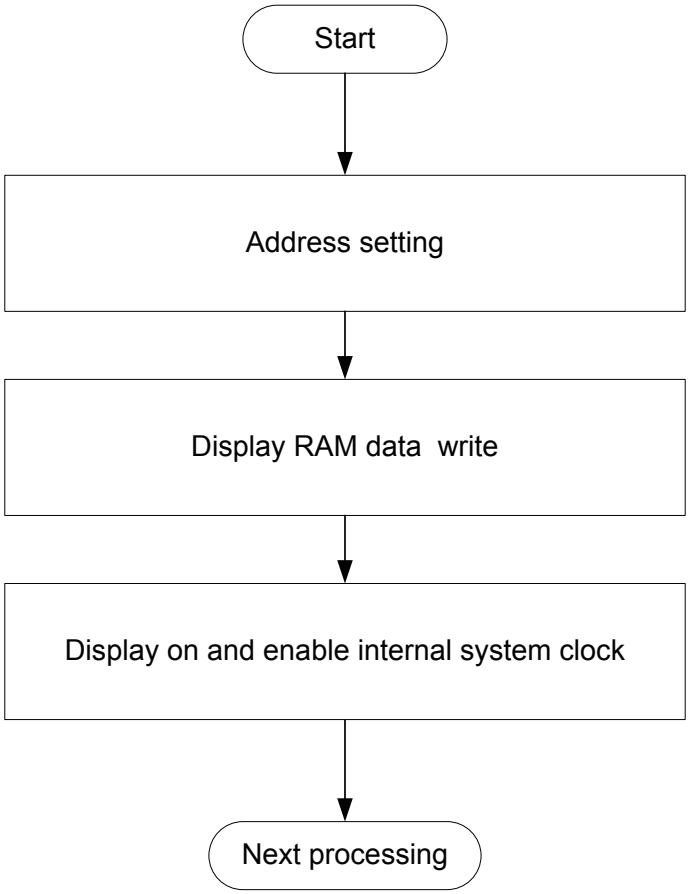
Operation Flowchart

Access procedures are illustrated below by means of the flowcharts.

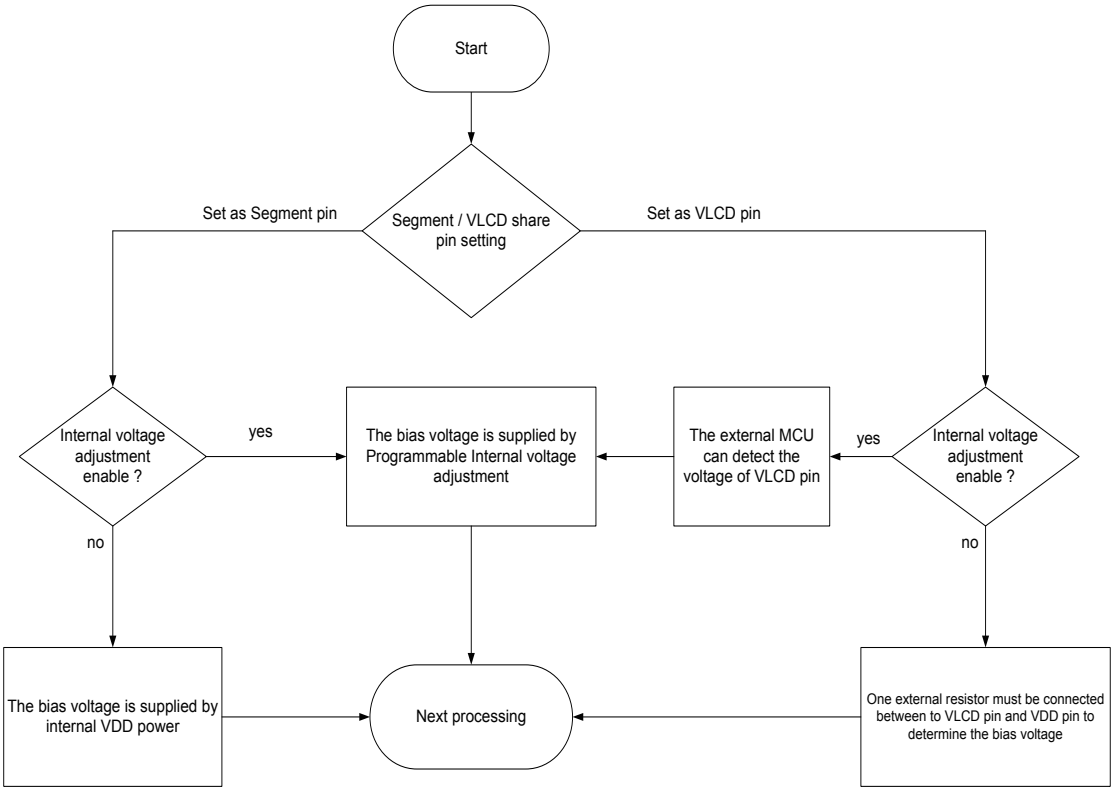
Initialization



Display Data Read/Write (Address Setting)



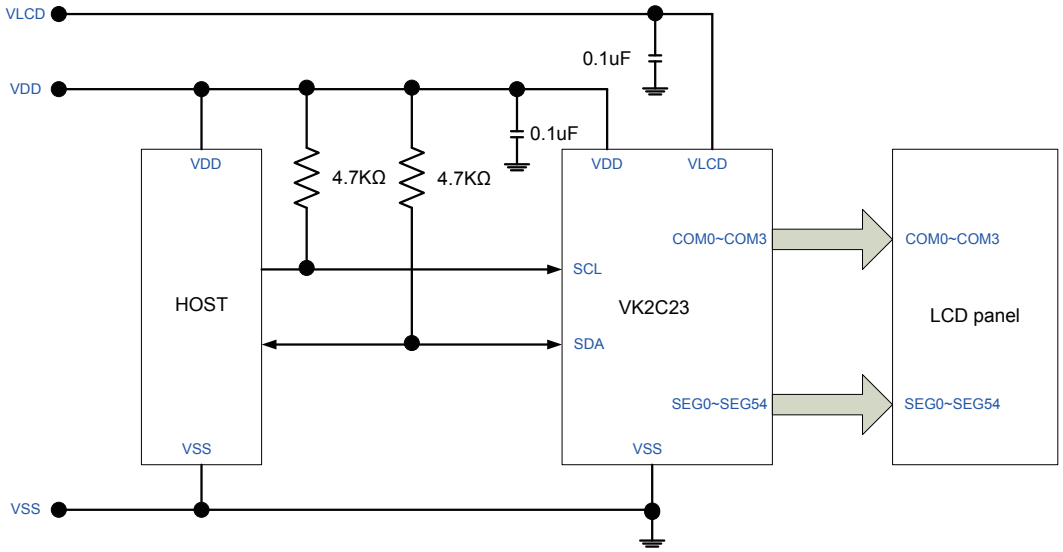
Segment / VLCD Shared Pin and Internal Voltage Adjustment Setting



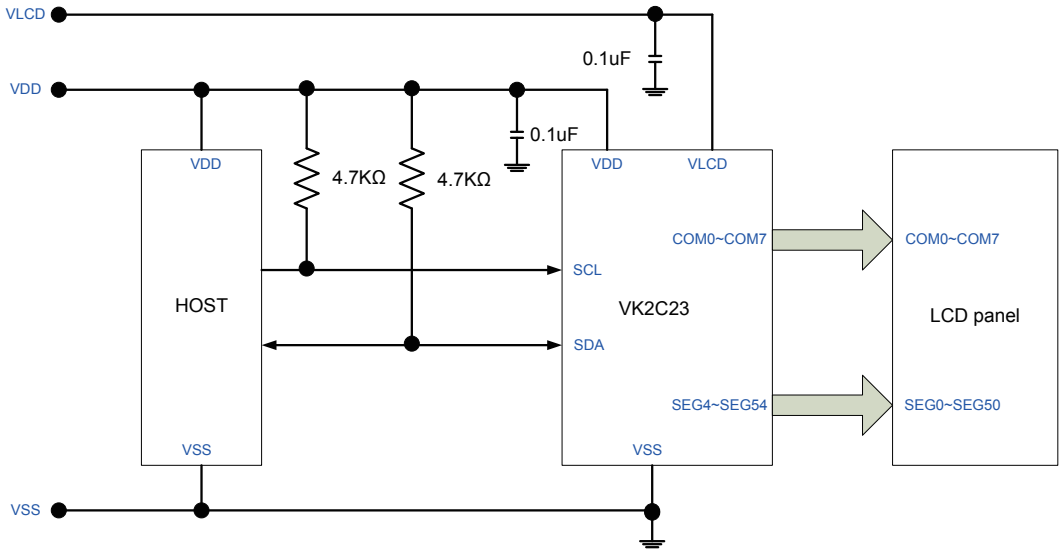
Application Circuits

64-pin Package

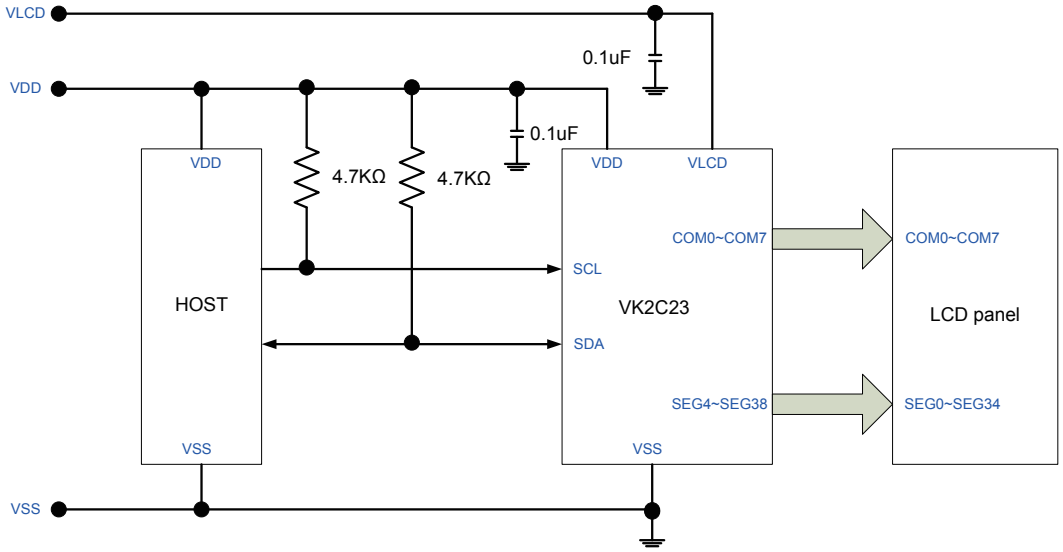
1/4 Duty



1/8 Duty



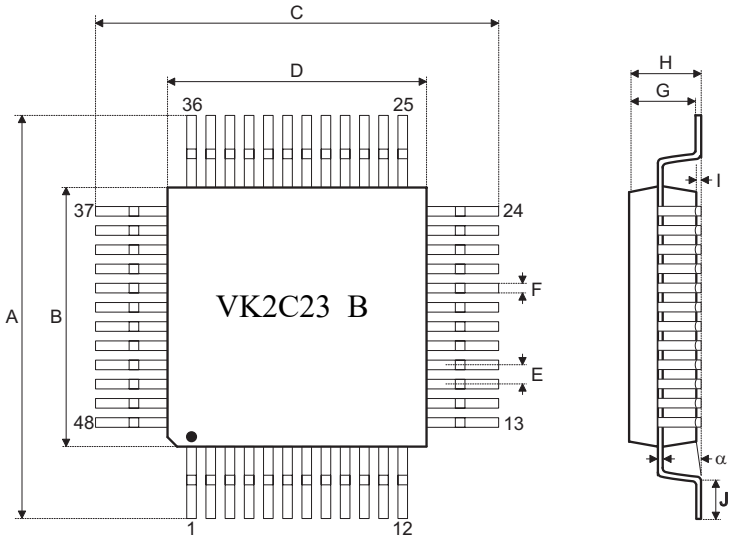
48-pin Package (The 48-pin Package Supports LCD 1/8 Duty only)



Package Information

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

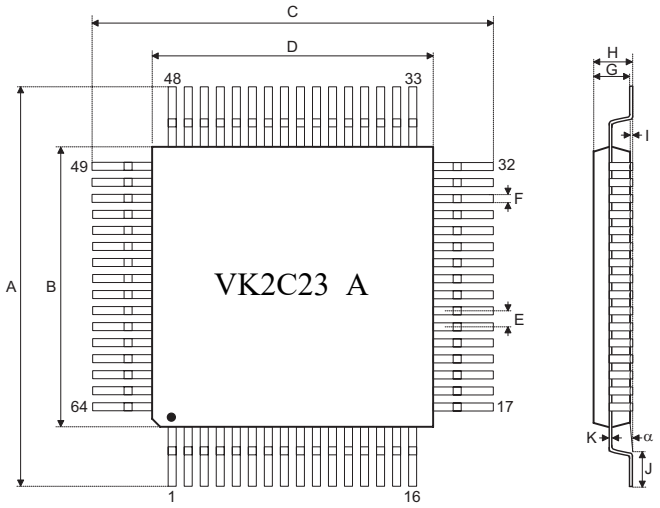
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.4 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°