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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E35RG63248LWAM400-C

Overview:

- 3.5-inch TFT (61.9x91.04mm)
- 320(RGB)x480 pixels
- 8/9/16/18-bit MCU
- 3/4 SPI + 16/18-bit RGB
- Transmissive/Normally Black
- White LED Backlight
- Capacitive Touch Screen
- 400 NITS
- Controllers: TFT ILI9486L, CTP FT6236
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, capacitive touch panel and a backlight unit. The resolution of the 3.5" TFT-LCD contains 320x480 pixels and can display up to 65K/262K colors.

TFT Features

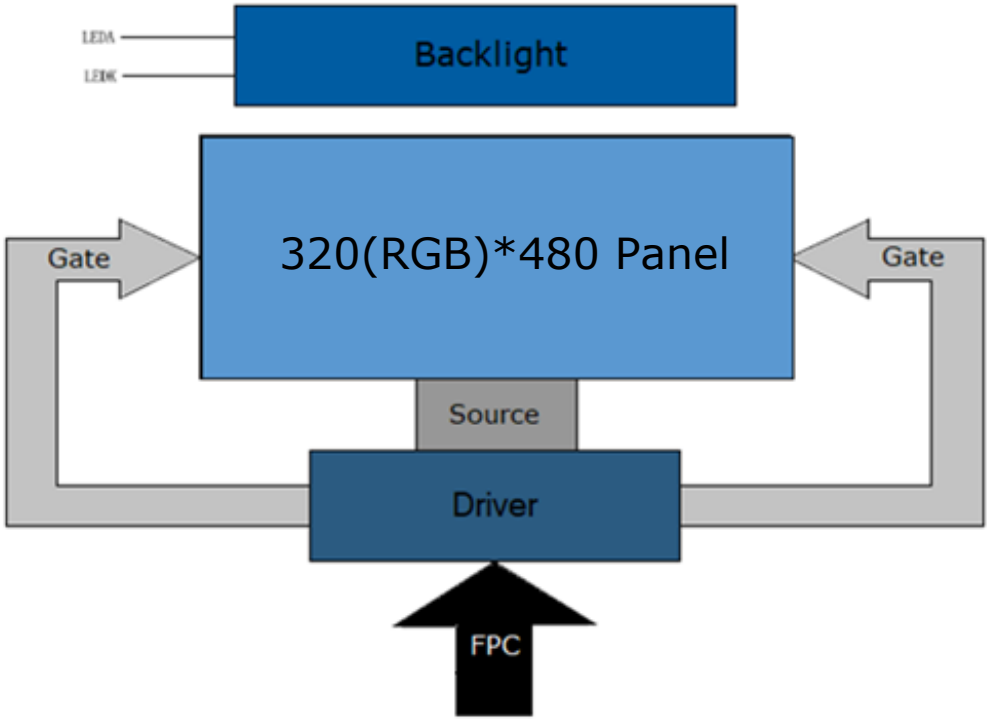
Low Input Voltage: 3.3V (TYP)
Display Colors: 65K/262K
TFT Interfaces: 8/9/16/18-bit MCU
3/4SPI+16/18-bit RGB
CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	48.96 (H) x 73.44 (V) (3.5 inch)	mm	-
CTP View Area	49.96(H)*74.44(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)x480	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153 (H) x 0.153 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9486L	-	-
CTP Driver IC	FT6236	-	-
Display mode	Transmissive/ Normally Black	-	-
Touch mode	Single point and gestures	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

Mechanical Information

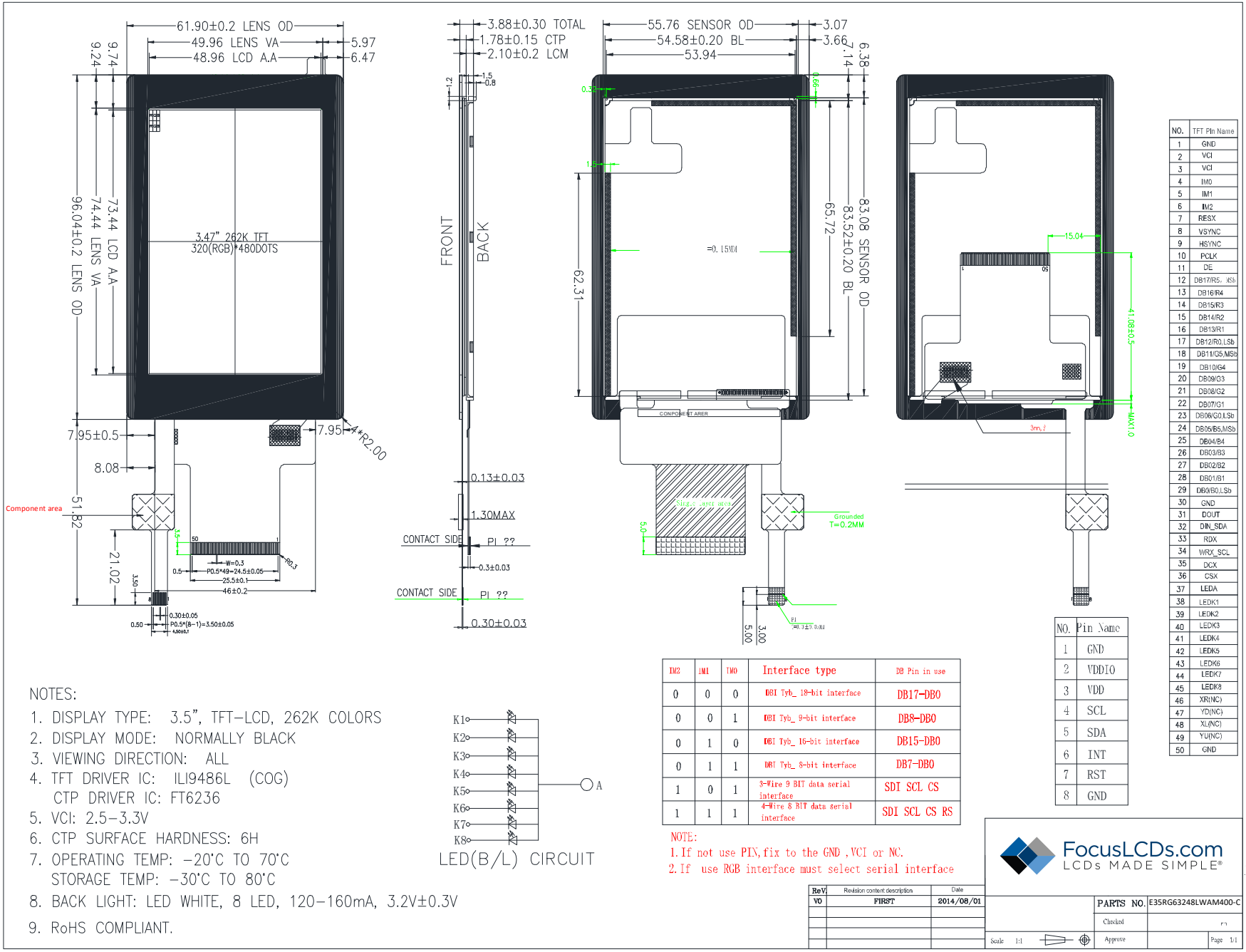
Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)		61.90		mm	-
	Vertical (V)		91.04		mm	-
	Depth (D)		3.88		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline Dimensions

2.1 TFT



NO.	TFT Pin Name
1	GND
2	VCI
3	VCI
4	IM0
5	IM1
6	IM2
7	RESX
8	VSYNC
9	HSYNC
10	PCLK
11	DE
12	DB17/R5, MSb
13	DB16/R4
14	DB15/R3
15	DB14/R2
16	DB13/R1
17	DB12/R0,LSb
18	DB11/G5,MSb
19	DB10/G4
20	DB09/G3
21	DB08/G2
22	DB07/G1
23	DB06/G0,LSb
24	DB05/B5,MSb
25	DB04/B4
26	DB03/B3
27	DB02/B2
28	DB01/B1
29	DB0/B0,LSb
30	GND
31	DOUT
32	DIN_SDA
33	RDX
34	WRX_SCL
35	DCX
36	CSX
37	LEDA
38	LEDK1
39	LEDK2
40	LEDK3
41	LEDK4
42	LEDK5
43	LEDK6
44	LEDK7
45	LEDK8
46	XR(NC)
47	YD(NC)
48	XL(NC)
49	YU(NC)
50	GND

NO.	Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:

1. DISPLAY TYPE: 3.5", TFT-LCD, 262K COLORS
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. TFT DRIVER IC: ILI9486L (COG)
   CTP DRIVER IC: FT6236
5. VCI: 2.5-3.3V
6. CTP SURFACE HARDNESS: 6H
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. BACK LIGHT: LED WHITE, 8 LED, 120-160mA, 3.2V±0.3V
9. RoHS COMPLIANT.

LED(B/L) CIRCUIT

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Typ_ 18-bit interface	DB17-DB0
0	0	1	DBI Typ_ 9-bit interface	DB8-DB0
0	1	0	DBI Typ_ 16-bit interface	DB15-DB0
0	1	1	DBI Typ_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , VCI or NC.
2. If use RGB interface must select serial interface

ReV.	Revision content description	Date
V0	FIRST	2014/08/01

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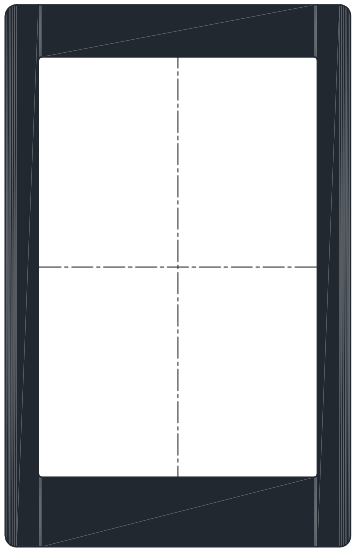
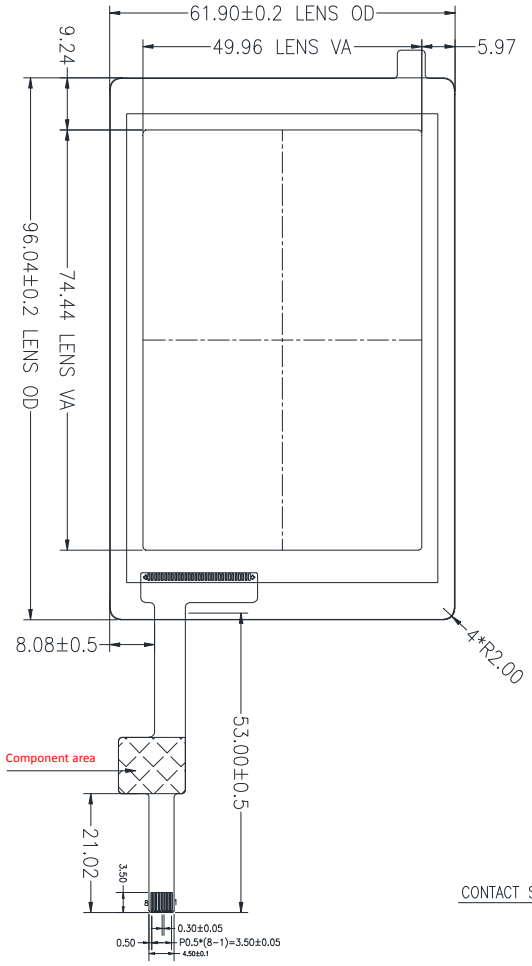
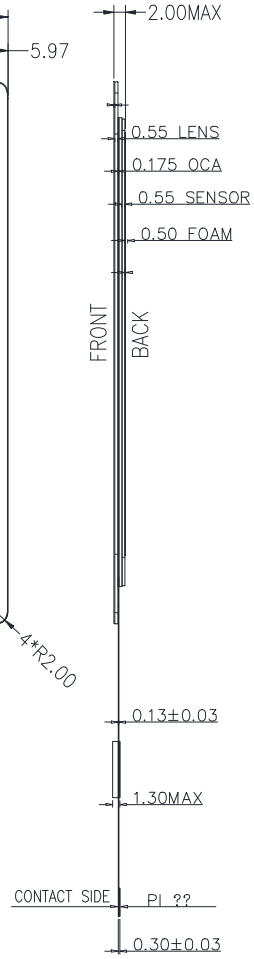
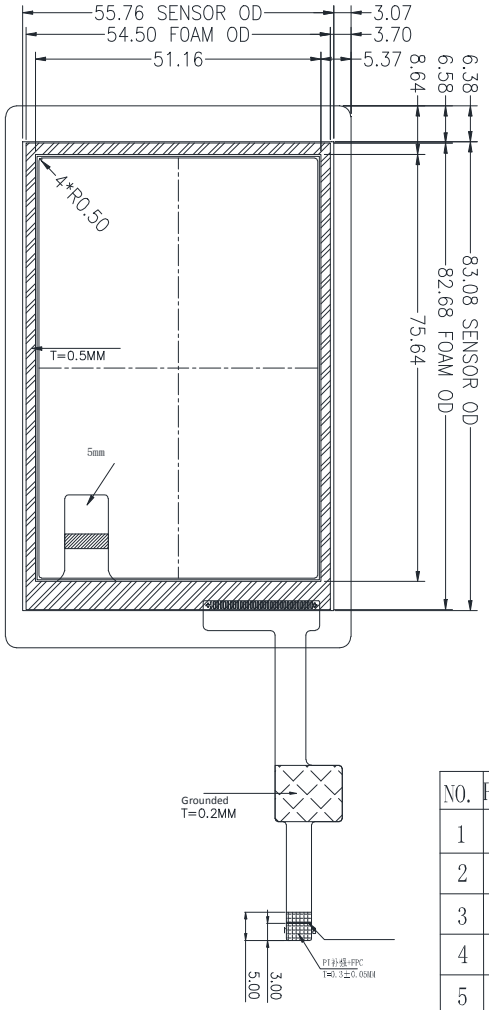
2.2 CTP









FRONT SIDE BACK

NO.	Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:
1.DRIVER IC: FT6236
2.WORKING VOLTAGE: 3.3V
3.LIGHT TRANSMISSION: ≥86%
4.SURFACE HARDNESS: 6H
5.OPERATING TEMP: −20℃~+70℃, ≤90%RH
6.STORAGE TEMP: −30℃~+80℃, ≤90%RH
7.UNMARKED TOLERANCE±0.2mm
8.PRECISE DIMENSION IN<>

ReV	Revision content description	Date
A	FIRST	2013/03/29

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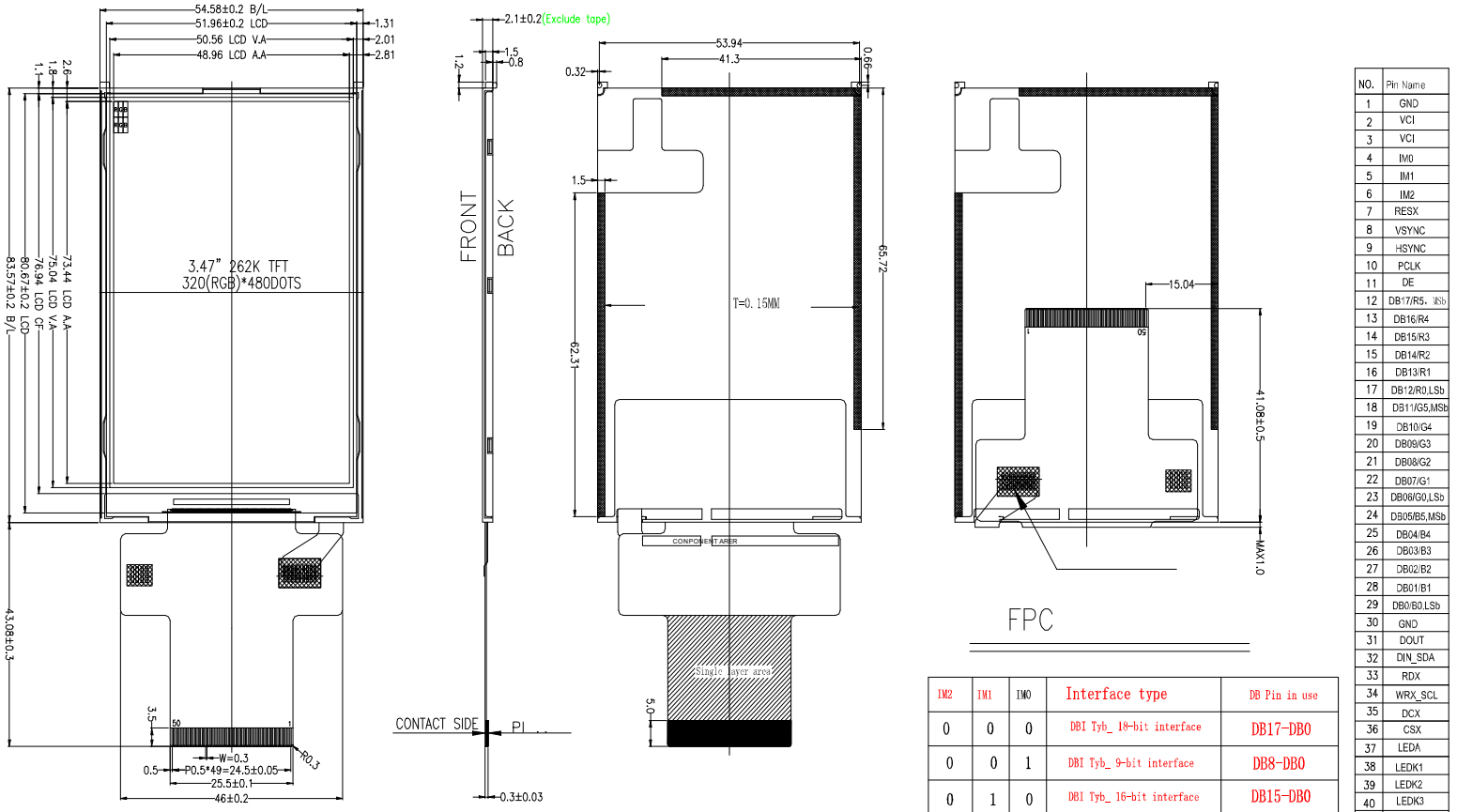
2.3 TFT+CTP



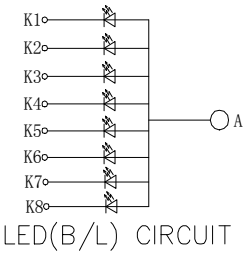
NO.	Pin Name
1	GND
2	VCI
3	VCI
4	IM0
5	IM1
6	IM2
7	RESX
8	VSYNC
9	HSYNC
10	PCLK
11	DE
12	DB17/R5, MSb
13	DB16/R4
14	DB15/R3
15	DB14/R2
16	DB13/R1
17	DB12/R0,LSb
18	DB11/G5,MSb
19	DB10/G4
20	DB09/G3
21	DB08/G2
22	DB07/G1
23	DB06/G0,LSb
24	DB05/B5,MSb
25	DB04/B4
26	DB03/B3
27	DB02/B2
28	DB01/B1
29	DB0/B0,LSb
30	GND
31	DOUT
32	DIN_SDA
33	RDX
34	WRX_SCL
35	DCX
36	CSX
37	LEDA
38	LEDK1
39	LEDK2
40	LEDK3
41	LEDK4
42	LEDK5
43	LEDK6
44	LEDK7
45	LEDK8
46	XR(NC)
47	YD(NC)
48	XL(NC)
49	YU(NC)
50	GND

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0
0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0
0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

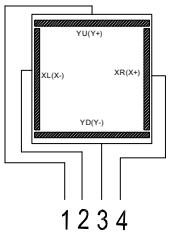
NOTE:
1. If not use PIN, fix to the GND , VCI or NC.
2. If use RGB interface must select serial interface

NOTES:

1. DISPLAY TYPE: 3.5", TFT-LCD, 262K COLORS
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. DRIVER IC: ILI9486L (COG)
5. VCI: 2.5-3.3V
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 8 LED, 120-160mA, 3.2V±0.3V
8. RoHS COMPLIANT.



LED(B/L) CIRCUIT



ReV	Revision content description	Date
A	FIRST	2012/07/06
B		2012/07/14

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3. Input Terminal Pin Assignment

3.1 TFT

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	VCI	Analog power supply (3.3V)	P
3	VCI	Analog power supply (3.3V)	P
4	IM0	Select Interface mode signal	I
5	IM1		
6	IM2		
7	RESET	Reset pin. Setting low initializes the LSI. Must be reset after power is supplied.	I
8	VSYNC	Frame synchronizing signal for DPI I/F mode. Connect to GND if not used.	I
9	HSYNC	Line synchronizing signal for DPI I/F mode. Connect to GND if not used.	I
10	PCLK	Pixel clock signal for DPI I/F mode. If not used, connect to GND.	I
11	DE	Data enable signal for DPI I/F mode. If not used, connect to GND.	I
12-29	DB17-DB0	Data bus pins. 18-bit bi-directional data bus. 8-bit bus: DB7-DB0 9-bit bus: DB8-DB0 16-bit bus: DB15-DB0 18-bit bus: DB17-DB0 When operating in MIPI DPI mode, it is an 18-bit RGB data bus. 6-bit bus: DB5-DB0 16-bit bus: DB15-DB0 18-bit but: DB17-DB0 If not used, connect to GND.	I/O
30	GND	Ground	P
31	DOUT	Serial data output pin in serial system interface. If not used leave open.	O
32	DIN_SDA	Serial data input pin or input/output pin in serial I/F. Data is input on the rising edge of the SCL signal. If not used, connect to GND.	I
33	RDX	DBI Type-B: Serves as read signal and read data at the low level. If not used connect to IOVCC.	I
34	WRX_SCL	DBI Type-B: Serves as a write signal and write data at the low level. DBI Type-C: Serves as SCL (Serial clock). If not used, connect to GND.	I
35	DCX	Data/Command selection pin. If not used, connect to GND.	I
36	CSX	Chip select signal. Low: chip can be accessed. High: chip cannot be accessed. If not used, connect to GND.	I
37	LEDA	Anode pin of backlight	P
38-45	LEDK1-LEDK8	Cathode pin of backlight	P
46	XR	Touch panel right glass terminal	A/D
47	YD	Touch panel bottom film terminal	A/D
48	XL	Touch panel left glass terminal	A/D
49	YU	Touch panel top film terminal	A/D
50	GND	Ground	P

I: Input, O: Output, P: Power

3.2 CTP

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	VDDIO	I/O power supply voltage	P
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host	I
7	RST	External reset. Low is active.	I
8	GND	Ground	P

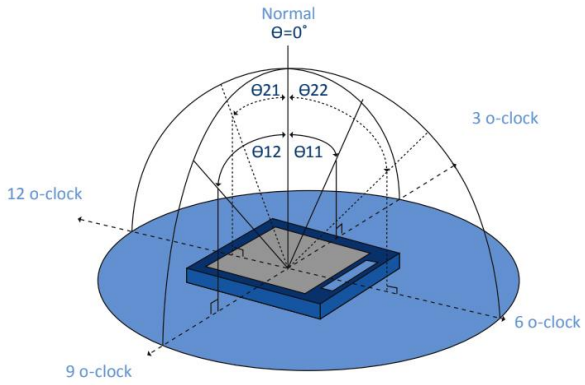
4. LCD Optical Characteristics

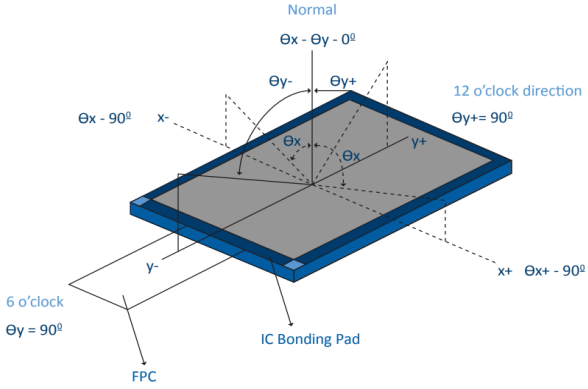
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ=0 Normal viewing angle	400	500	--	%	(2)
Response Time	Rising	TR+TF		--	35	50	msec	(4)
	Falling							
Transmittance		T		3.86	4.40	--	%	(5)
Color Filter Chromaticity	White	W_X		0.275	0.295	0.315		(5)(6)
		W_Y		0.297	0.317	0.337		
	Red	R_X		0.640	0.660	0.680		
		R_Y		0.297	0.317	0.337		
	Green	G_X		0.240	0.260	0.280		
		G_Y		0.555	0.575	0.595		
	Blue	B_X		0.121	0.141	0.161		
		B_Y		0.055	0.075	0.095		
Viewing Angle	Hor.	ΘL	CR≥10	--	80	--	degree	(1)(6)
		ΘR		--	80	--		
	Ver.	ΘT		--	80	--		
		ΘB		--	80	--		
Option View Direction		FREE						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



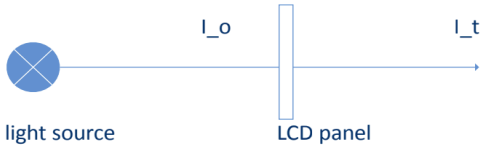


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

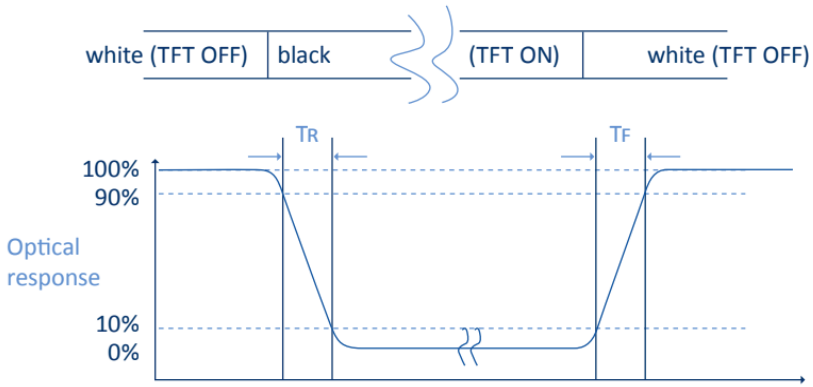
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io}\ x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

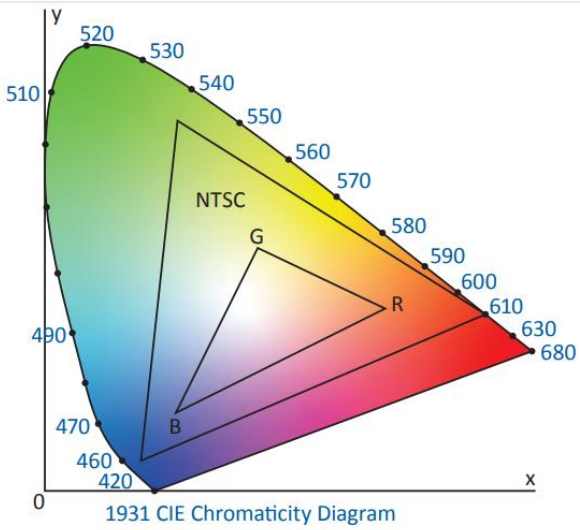
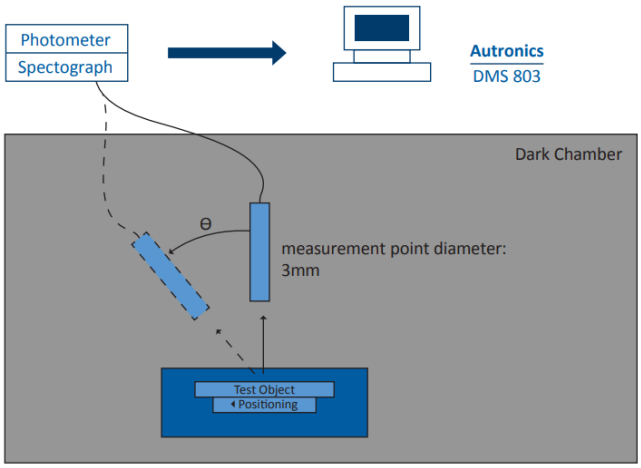


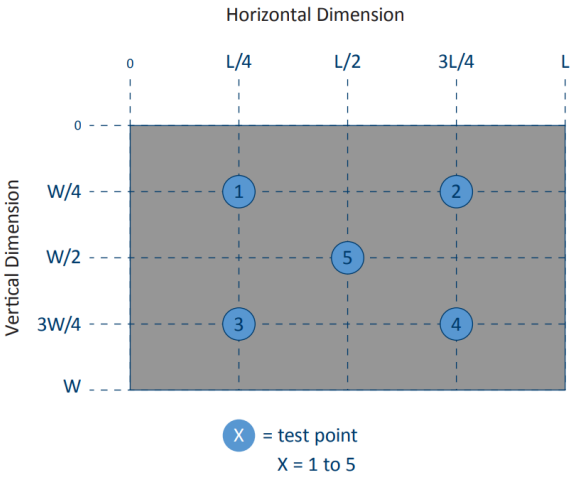
Fig. 1931 CIE chromacity diagram

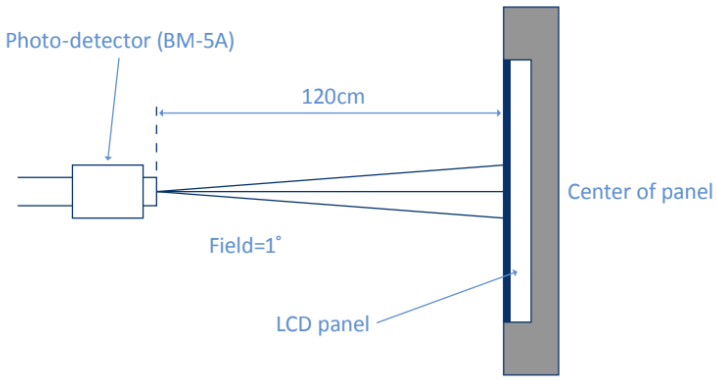
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.2	V
Digital Interface Supply Voltage	iovcc	-0.3	VDD	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	3.0	3.3	4.2	V	
Digital Interface Supply Voltage	iovcc	1.65	3.3	4.2	V	
Normal Mode Current Consumption	IDD	--	10	--	mA	
Level Input Voltage	VIH	0.7VDDIO	--	VDDIO	V	
	VIL	GND	--	0.3VDDIO	V	
Level Output Voltage	VOH	0.8VDDIO	--	VDDIO	V	
	VOL	GND	--	0.2VDDIO	V	

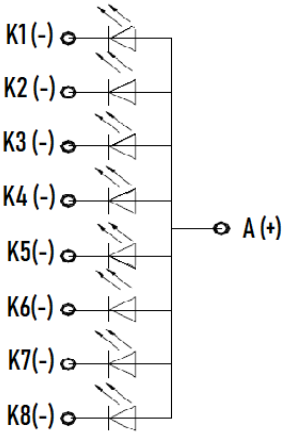
5.3 LED Backlight Characteristics

The backlight system is edge lighting type with 8 chips LED.

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	120	160	--	mA	
Forward Voltage	V_F	2.9	3.2	3.4	V	
LCM Luminance	LV	400	--	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

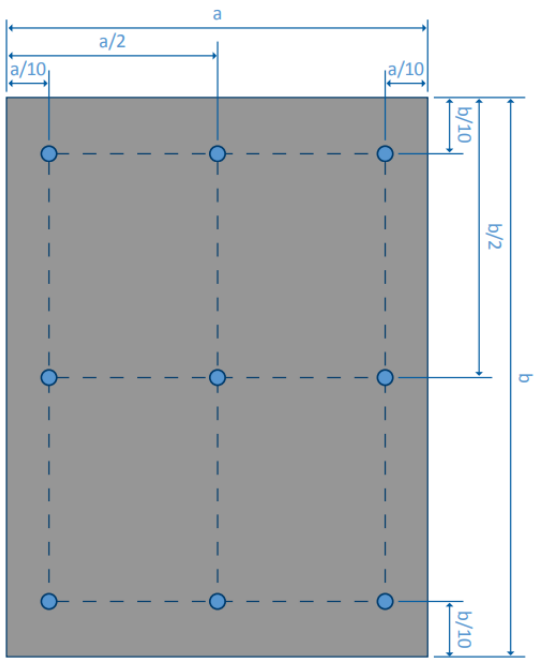
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 160mA. The LED lifetime could be decreased if operating IL is larger than 160mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:

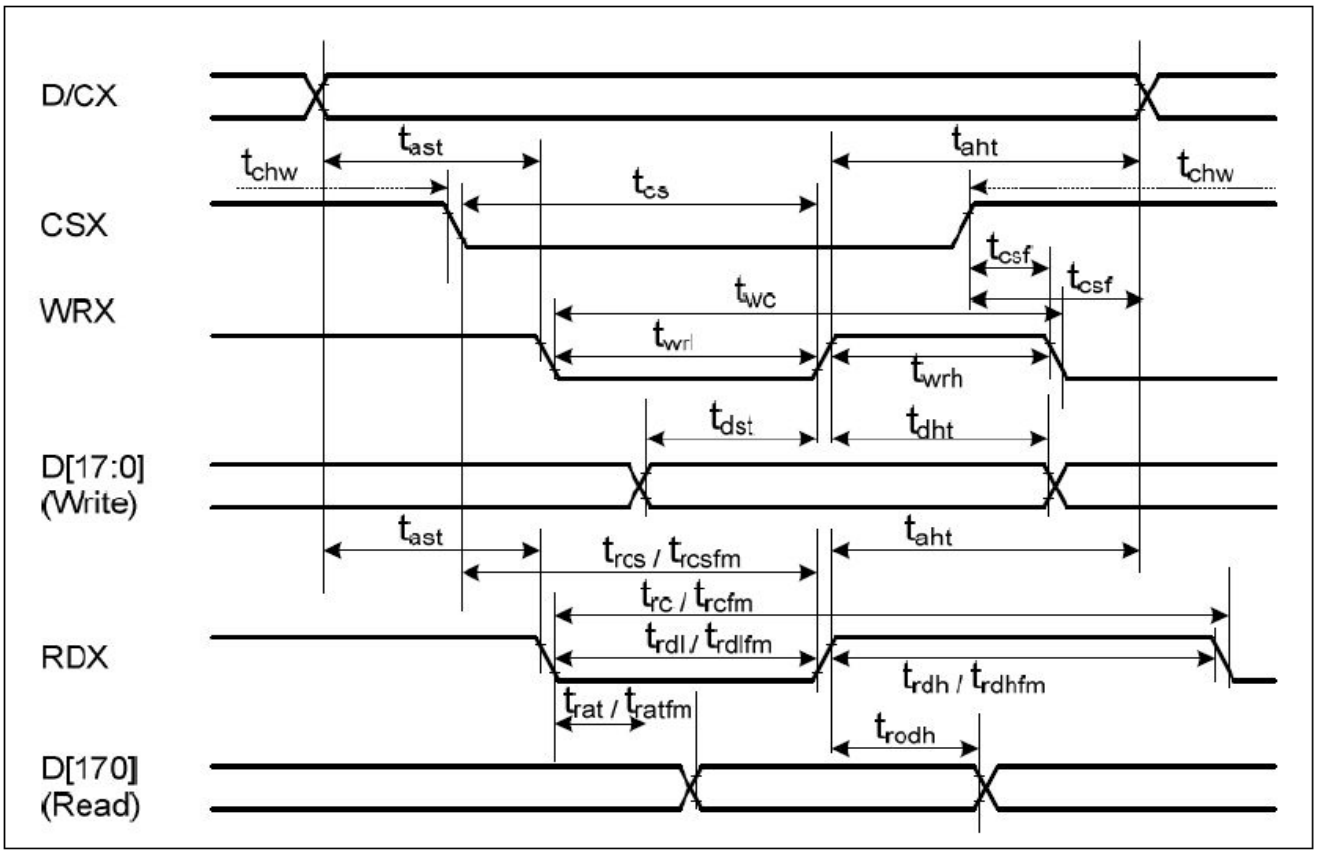


$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

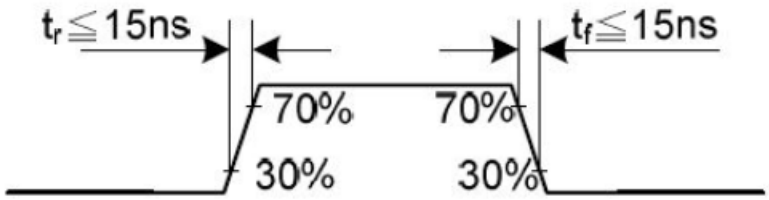
6. TFT AC Characteristics

6.1 DBI Type B (18/16/9/8 bit) Interface Timing Characteristics (8080-series)

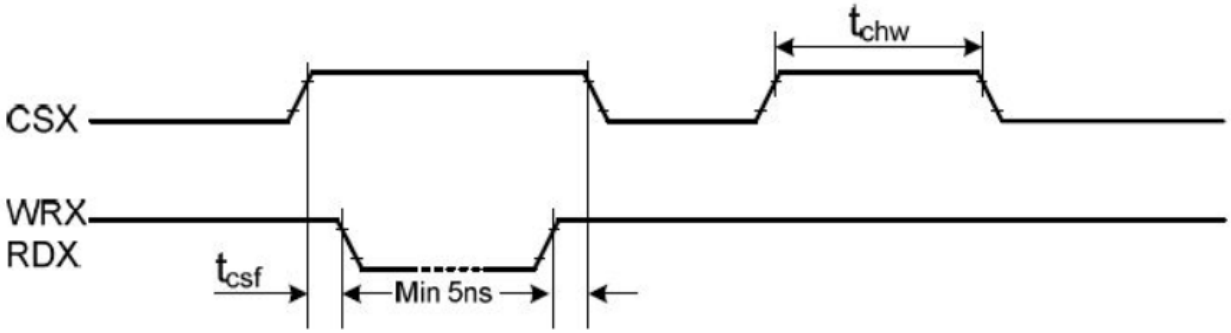


Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	that	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX “H’ pulse width	0	-	ns	
	tcs	Chip select setup time (Write)	15	-	ns	
	trcs	Chip select setup time (Read ID)	45	-	ns	
	trcsfm	Chip select setup time (Read FM)	355	-	ns	
	tcsf	Chip select wait time (Write/Read)	0	-	ns	
WRX	twc	Write cycle	50	-	ns	
	twrh	Write control pulse H duration	15	-	ns	
	twrl	Write control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read cycle (FM)	450	-	ns	When read from frame memory
	trdhfm	Read control H duration (FM)	90	-	ns	
	trdlfm	Read control L duration (FM)	355	-	ns	
RDX(ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read control pulse H duration	90	-	ns	
	trdl	Read control pulse L duration	45	-	ns	
DB[17:0] DB[15:0] DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

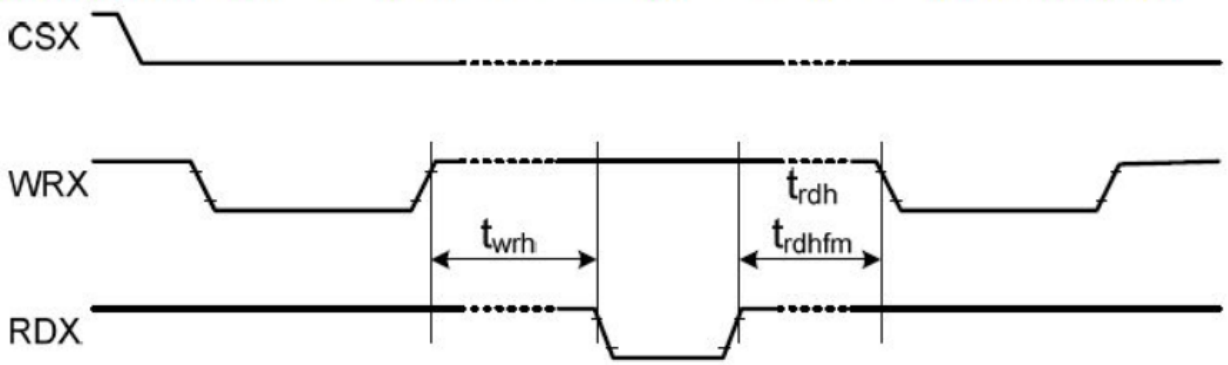
Note: (1) Ta = -30 to 70˚, IOVCC = 1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=DGND=0V



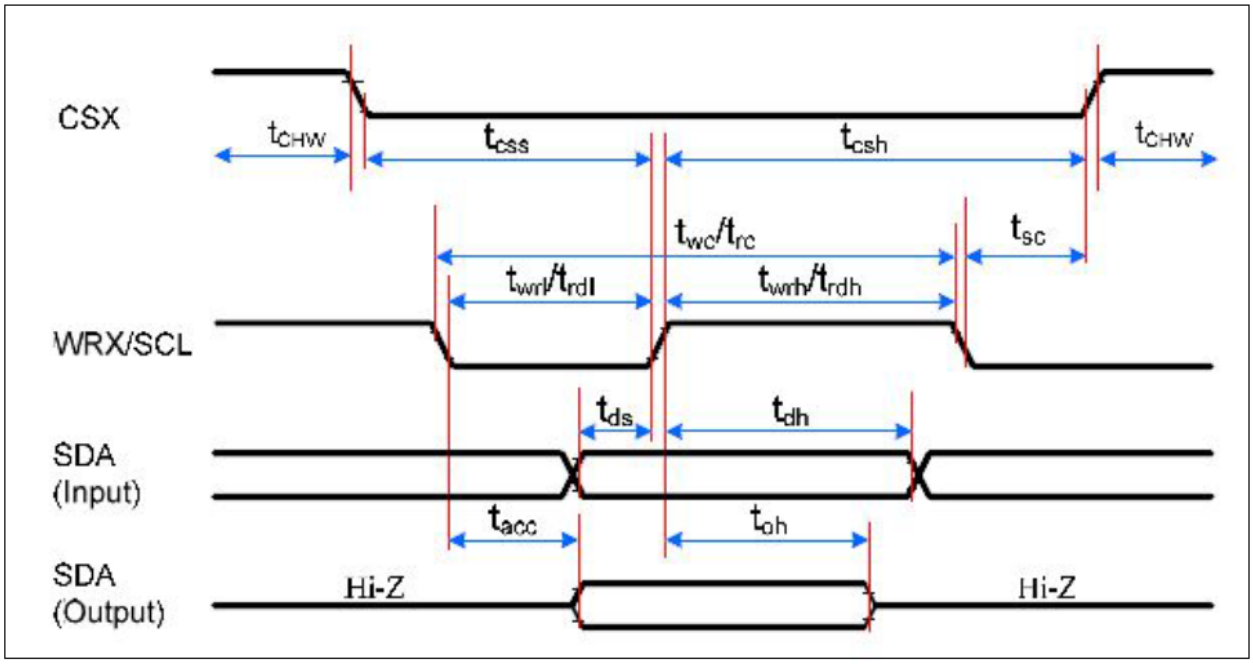
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



(3) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

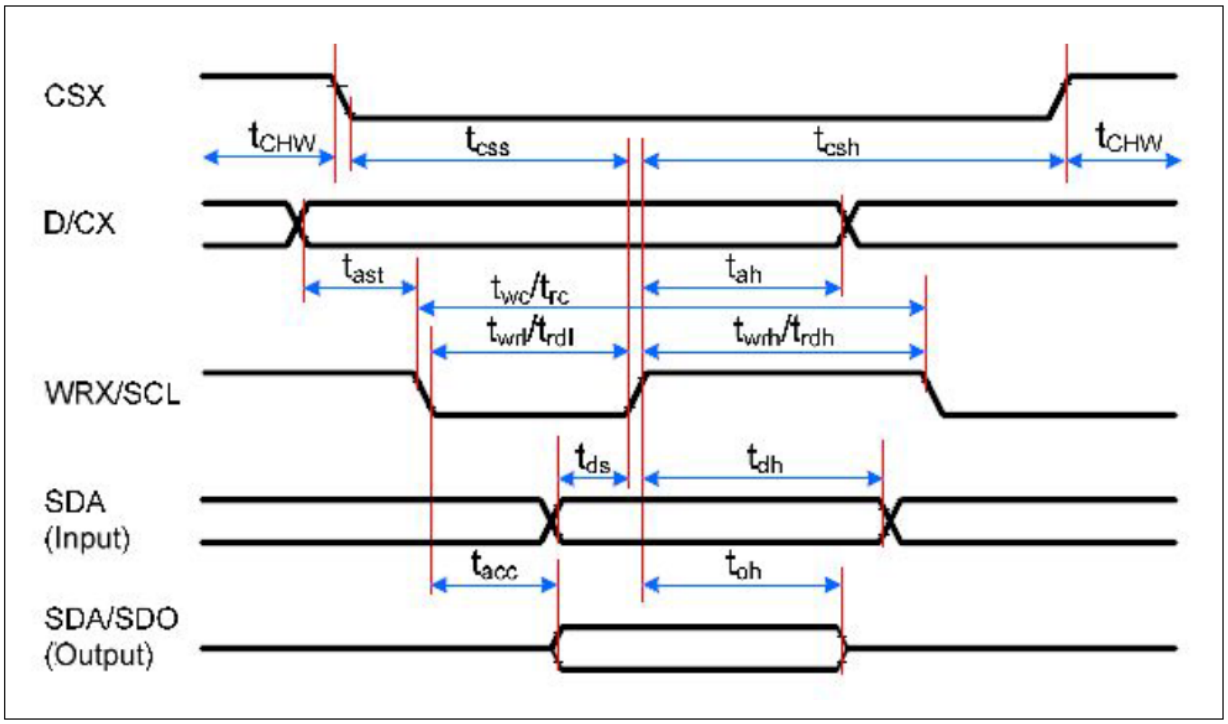


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)



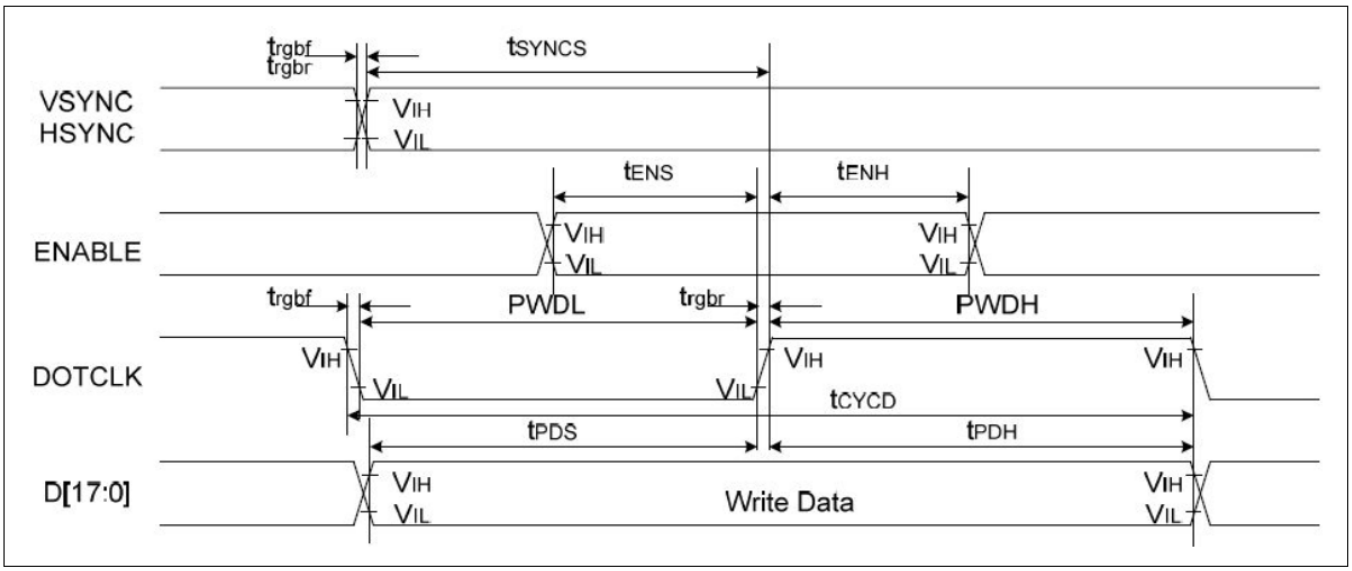
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H pulse width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL H pulse width (Write)	15	-	ns	
	twrl	SCL L pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	When read ID data
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For max, CL=30pF For mini, CL=8pF
	toh	Output disale time (Read)	15	50	ns	

6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

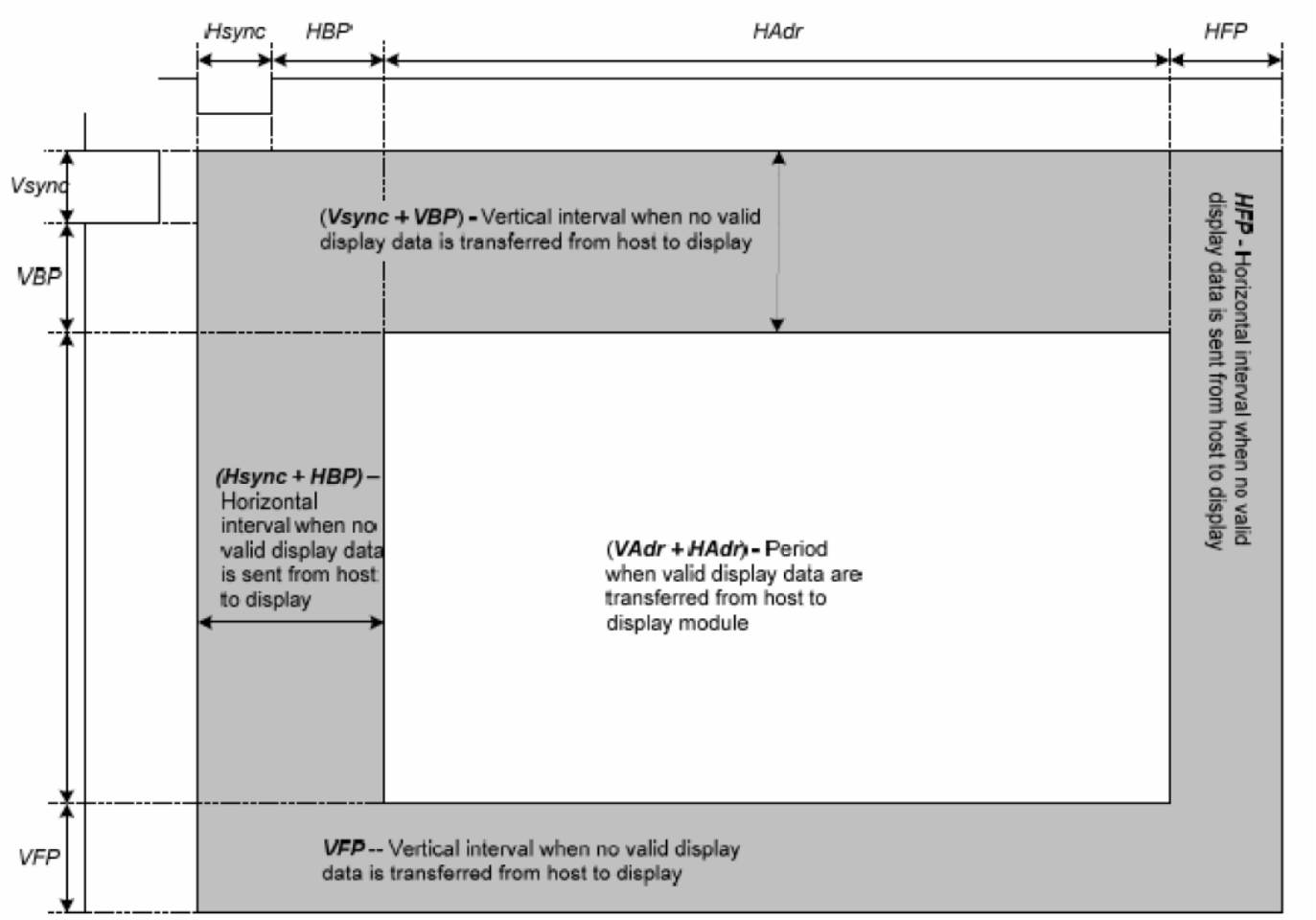


Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H pulse width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL H pulse width (Write)	15	-	ns	
	twrl	SCL L pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For max, CL=30pF
	toh	Output disale time (Read)	15	50	ns	For mini, CL=8pF

6.4 Parallel 18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC/ HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	tENS	ENABLE setup time	15	-	ns	
	tENH	ENABLE hold time	15	-	ns	
DB[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	66	-	ns	
	trgbr,trgbf	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	



Parameters	Symbols	Min	Typ.	Max	Units
PCLK cycle	PCLKcyc	100	80	66.6	Ns
Horiontal synchronization	Hsync	3	3	-	PCLK
Horizontal back porch	HBP	3	3	-	PCLK
Horizontal address	HAdr	-	320	-	PCLK
Horizontal front porch	HFP	3	3	-	PCLK
Vertical synchronization	Vsync	2	2	-	Line
Vertical back porch	VBP	2	2	-	Line
Vertical address	Vadr	-	480	-	Line
Vertical front porch	VFP	2	2	-	Line
Vertical frequency(*)		50	60	80	Hz
Horizontal frequency(*)		-	33	-	kHz
PCLK frequency(*)		10	12.5	15	MHz

Notes:

(1) Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr +VFP.

(2) Horizontal period (one line) shall be equal to the sum Hsync + HBP +HAdr + HFP.

(3) Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pizels are transferred between the host processor and the display module.

6.5 Reset Timing

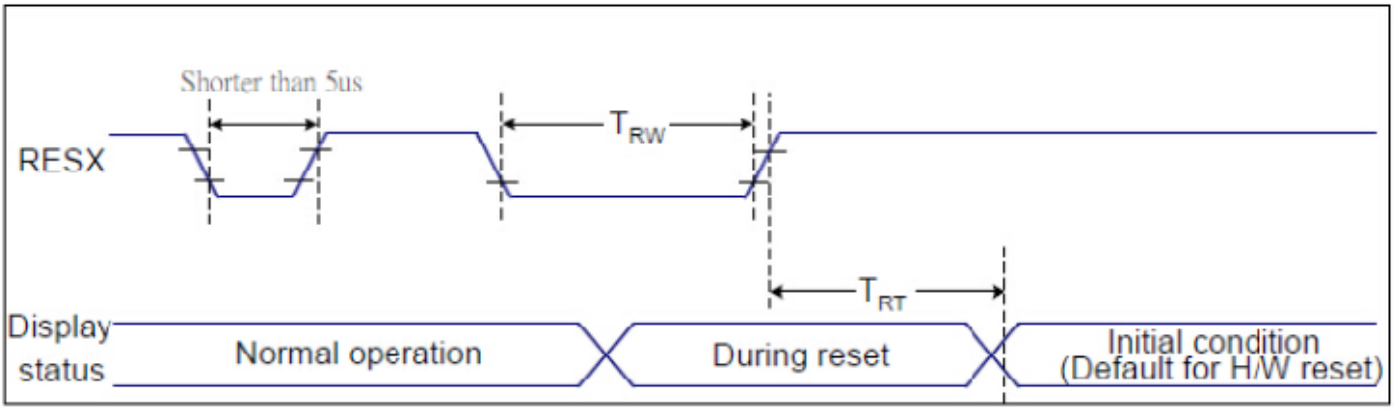


Figure 6.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

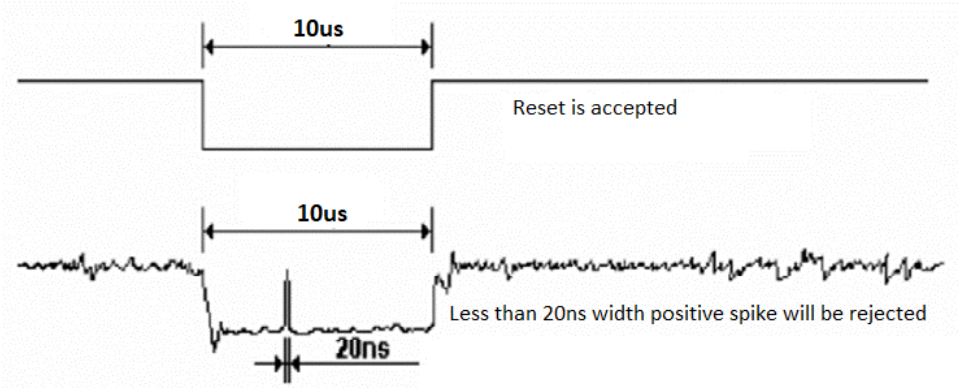
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating Temperature	T	-20	+70	℃	-
Storage Temperature	T_{ST}	-30	+80	℃	-

Note: If used beyond the absolute maximum ratings, FT6236 may permanently damage. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

7.1.2 DC Electrical Characteristics (Ta=25℃)

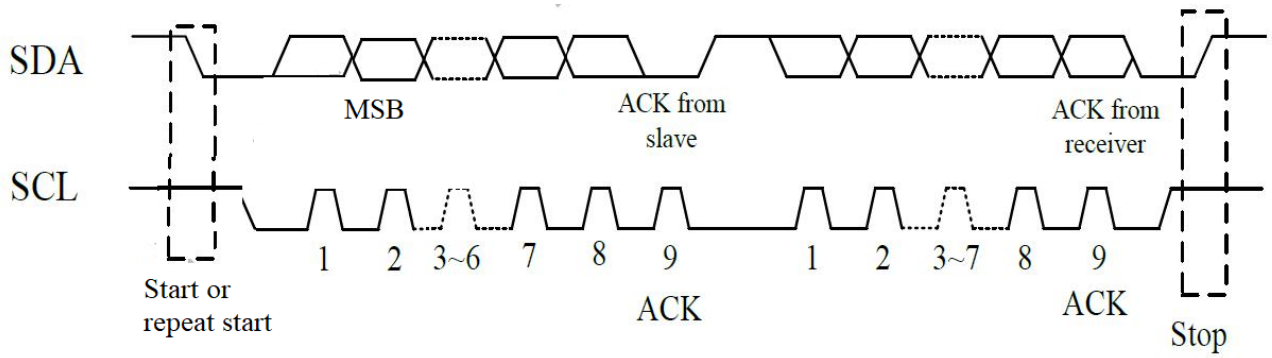
Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode current consumption	I_{OPr}	VDD=2.8V Ta=25℃ MCLK=17.5MHz		4		mA	
Monitor mode current consumption	I_{mon}			1.5		mA	
Sleep mode current consumption	I_{sip}			50		uA	
Level input voltage	V_{IH}		0.7VDDIO		VDDIO	V	
	V_{IL}		-0.3		0.3VDDIO	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	0.7VDDIO			V	
	V_{OL}	I_{OL}=0.1mA			0.3VDDIO	V	

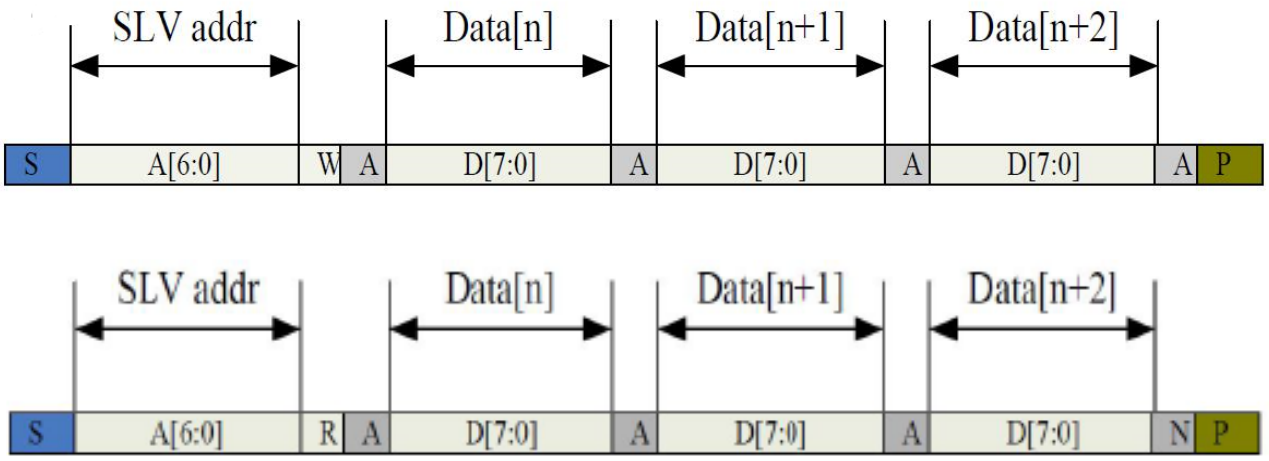
7.1.3 AC Characteristics

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA=2.8V; Ta=25℃	34.65	35	35.35	MHz	
Sensor acceptable clock	ftx	VDDA=2.8V; Ta=25℃	0	100	300	kHz	
Sensor output rise time	Ttxr	VDDA=2.8V; Ta=25℃	-	100	-	Ns	
Sensor input fall time	Ttxf	VDDA=2.8V; Ta=25℃	-	80	-	Ns	
Sensor input voltage	Trxi	VDDA=2.8V; Ta=25℃	-	5	-	V	

7.1.4 I2C Interface

The I2C is always configured in the slave mode. The data transfer format is shown below.





The following table lists the meanings of the mnemonics used in the above figures.

Mnemonics	Description
S	I2C start or I2C restart
A [6:0]	Slave address
R/W	Read/Write bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	Stop: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	kHz
Bus free time between a stop and start condition	4.7	-	us
Hold time (repeated) start condition	4.0	-	us
Data setup time	250	-	us
Setup time for a repeated start condition	4.7	-	us
Setup time for stop condition	4.0	-	us

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.