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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E45RA-RW245-R

Overview:

- 4.5-inch TFT (61.54x110.09)
- 480 854
- 3SPI + /24 k8" @
- ‡ u erature
- Top View

- Transmissive
- Resistive Touch Panel
- 245 NITS
- TFT IC: ILI9806E
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, 4-wire resistive touch panel, and a backlight unit. The resolution of the 4.5" TFT-LCD contains 480(RGB)x854 pixels and can display up to 16.7M colors.

TFT Features

Low Input Voltage: 3.3V
Display Colors: 16.7M
Interface: 3SPI+16/18/24-bit RGB

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	55.44(H) x 98.64(V) (4.5 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	480(RGB)x854	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.1155 (H)x0.1155(V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ILI9806E	-	-
TFT Interface	3SPI+16/18/24-bit RGB	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20-+70	°C	-
Storage temperature	-30-+80	°C	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		61.54		mm	-
	Vertical (V)		110.09		mm	-
	Depth (D)		3.60		mm	-
	Weight		TBD		g	

1. Outline Dimensions

Pin NO. table (left):

Pin NO.	Assignment
1	YU
2	XL
3	YD
4	XR

Main dimension callouts:
- 61.54±0.2 BL OUT
- 60.94±0.2 TP OD
- 56.14 TP AA
- 55.44 LCD AA
- 0.30
- 2.70
- 3.05
- 0.20
- 2.30
- 2.65
- YU
- 4.46" TN
- 480RGB X 854
- XL / XR
- YD
- 110.09±0.2 BL OUT
- 109.49±0.2 TP OD
- 99.34 TP AA
- 98.64 LCD AA
- 4.50
- 20.03±0.5
- 47.8±0.5
- 3.50
- 45
- W=0.30
- P0.5*44=22.00±0.05
- 19.27±0.3
- 23.00±0.1
- 52.54±0.5

Side view (FRONT / BACK):
- 3.60±0.2(TP+LCM)
- 2.55±0.2(LCM)
- 1.2MAX
- 0.13±0.03 FPC
- 0.30±0.03(Conduct+Stiffener)

Back view:
- 9.77±0.5
- 45
- 45.61±0.5
- 1.00MAX
- FPC
- 5.00
- 3.00

RGB Interface

RGB Interface	DB Pins Used
16 Bit RGB interface	DB20-DB16, DB13-DB8, DB4-DB0
18 Bit RGB interface	DB21-DB16, DB13-DB8, DB5-DB0
24 Bit RGB interface	DB23-DB0

Pin Assignment (right table)

NO.	Pin Name
1	XR
2	YD
3	XL
4	YU
5	GND
6	GND
7	VCI
8	IOVCC
9	SDO
10	SDI
11	SCL
12	CS
13	RESET
14	DB23(R7)
15	DB22(R6)
16	DB21(R5)
17	DB20(R4)
18	DB19(R3)
19	DB18(R2)
20	DB17(R1)
21	DB16(R0)
22	DB15(G7)
23	DB14(G6)
24	DB13(G5)
25	DB12(G4)
26	DB11(G3)
27	DB10(G2)
28	DB9(G1)
29	DB8(G0)
30	DB7(B7)
31	DB6(B6)
32	DB5(B5)
33	DB4(B4)
34	DB3(B3)
35	DB2(B2)
36	DB1(B1)
37	DB0(B0)
38	DE
39	PCLK
40	HSYNC
41	VSYNC
42	NC
43	LEDK
44	NC
45	LEDA

NOTES:

1. DISPLAY TYPE: 4.46", TFT-LCD(16:9)
2. DISPLAY MODE: NORMALLY WHITE(TN)
3. VIEWING DIRECTION: 12 o'clock
4. DRIVER IC: ILI9806E (COG)
5. VCI: 3.3V(TYP), IOVCC: 1.65-3.3V
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 8 LED, 40mA, 12.8±0.2V
8. RoHS COMPLIANT.

LEDA — LEDK

CIRCUIT DIAGRAM

FOCUS LCDs — LCDs MADE SIMPLE®

TOLERANCE		DRAWING NAME		
		PARTS NO.	E45RA-RW245-R	
TOLERANCE UNLESS	X.X±0.3	Drawn		Unit
OTHERWISE SPECIFIED	X.XX±0.2	Checked		mm
Scale 1:1		Approve		Page 1/1

2.   Block Diagram

Backlight

LEDA
LEDK

480(RGB)*854 Panel

Gate

Gate

Source

Driver

FPC

3. Input TFT Terminal Pin Assignment

Recommended TFT Connector: FH12S-45S-0.5SH(55) | Recommended RTP Connector: FH33-4S-1SH(10)

NO.	Symbol	Description	I/O
1	XR	Touch panel right glass terminal	A/D
2	YD	Touch panel bottom film terminal	A/D
3	XL	Touch panel left glass terminal	A/D
4	YU	Touch panel top film terminal	A/D
5	GND	Ground	P
6	GND	Ground	P
7	VCI	Supply voltage (3.3V)	P
8	IOVCC	I/O power supply voltage (1.65-3.3V)	P
9	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal.	O
10	SDI	SPI input pin. The data is latched on the rising edge of the SCL signal.	I
11	SCL	SPI clock signal.	I
12	CS	Chip select signal. Low enabled.	I
13	RESET	Reset signal of the device. Low enabled.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus for RGB interface.	I/O
38	DE	Data enable signal for the RGB interface.	I
39	DOTCLK	Dot clock signal for the RGB interface.	I
40	HSYNC	Line synchronizing signal for the RGB interface	I
41	VSYNC	Frame synchronizing signal for the RGB interface	I
42	NC	Not connected	
43	LEDK	Cathode pin of the backlight	P
44	NC	Not connected	
45	LEDA	Anode pin of the backlight	P

I: Input, O: Output, P: Power

4. LCD Optical Characteristics

4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%		--	58	--	%	(3)
Contrast Ratio		CR		--	800	--	%	(2)
Response Time	Rising	T_R		--	4	8	ms	(4)
	Falling	TF		--	12	24		
Color Filter Chromaticity	White	W_X	θ=0 Normal viewing angle	0.273	0.313	0.353		(5)(6)
		W_Y		0.290	0.330	0.370		
	Red	R_X		0.604	0.624	0.644		
		R_Y		0.327	0.357	0.377		
	Green	G_X		0.343	0.363	0.383		
		G_Y		0.569	0.589	0.609		
	Blue	B_X		0.128	0.148	0.168		
		B_Y		0.055	0.075	0.095		
Viewing Angle	Hor.	ΘL	CR≥10	60	70	--	degrees	(1)(6)
		ΘR		60	70	--		
	Ver.	ΘT		60	70	--		
		ΘB		40	60	--		
Option View Direction		12:00						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
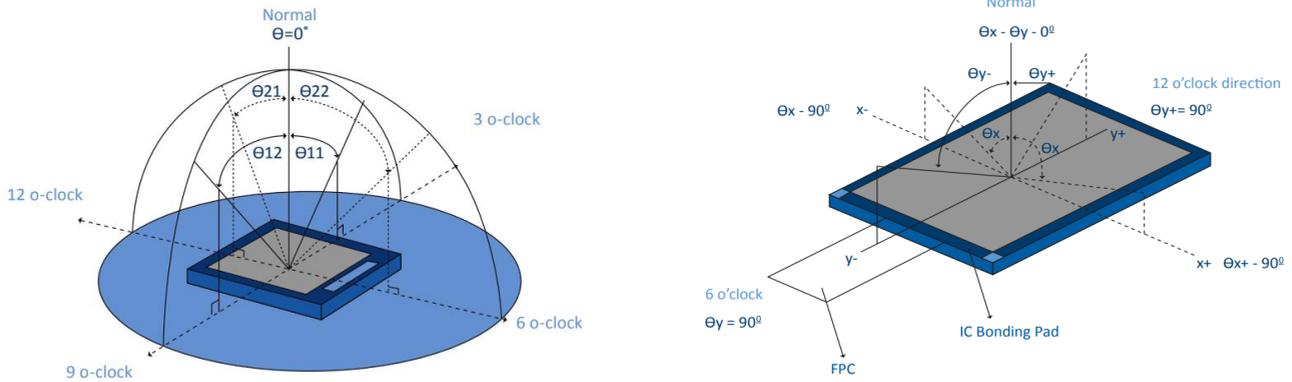
(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} \, x \, 100\%$$
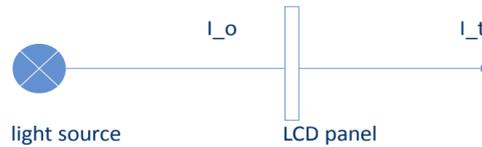
Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.

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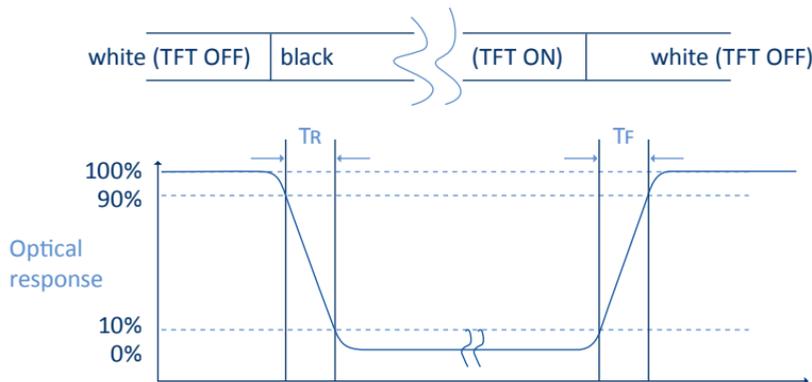
(5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
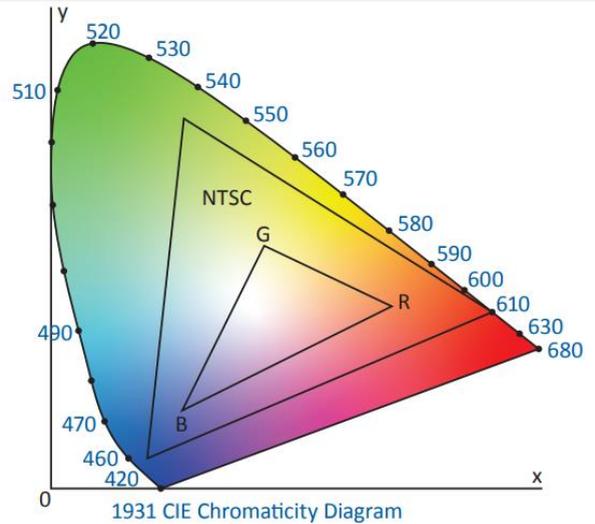

Fig. 1931 CIE chromacity diagram

Color gamut: $S = \dfrac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.
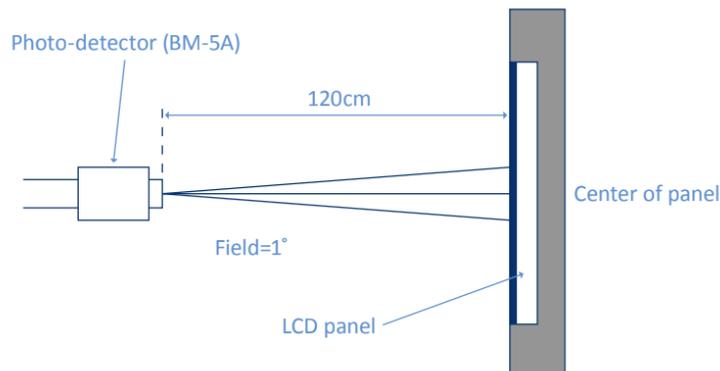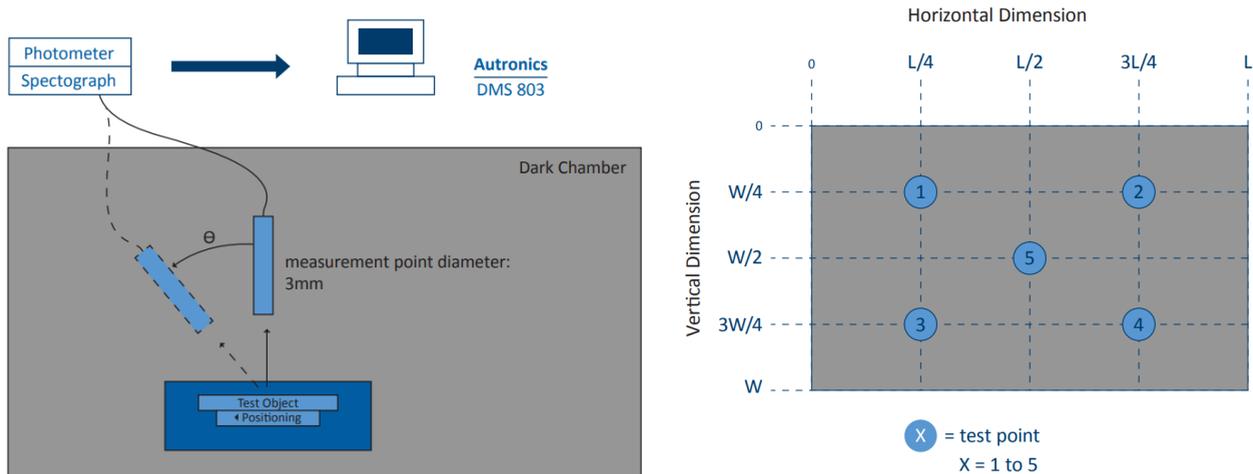
5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.2	V
Digital Interface Supply Voltage	IOVCC	-0.3	3.3	
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8/3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current	IDD	--	26	--	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC	V	
	VIL	GND	--	0.3IOVCC	V	
Level Output Voltage	VOH	0.8IOVCC	--	IOVCC	V	
	VOL	GND	--	0.2IOVCC	V	

5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	30	40	--	mA	
Forward Voltage	VF	--	12.8	--	V	
LCM Luminance	LV	245	--	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 8 white LEDs.

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.
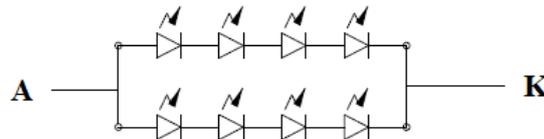
Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:
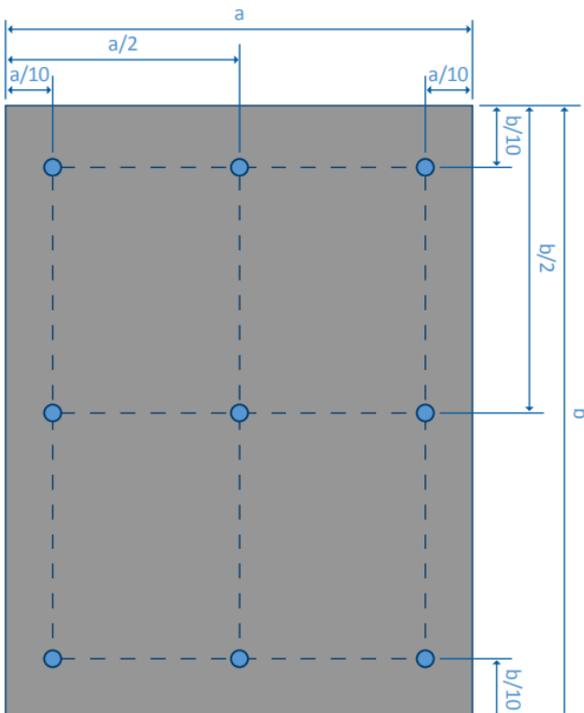
$$Luminance = \frac{(Total\ Luminance\ of\ 9\ points)}{9}$$

$$Uniformity = \frac{minimum\ luminance\ in\ 9\ points(1\text{-}9)}{maximum\ luminance\ in\ 9\ points(1\text{-}9)}$$

6. AC Characteristic

6.1 Parallel RGB Interface Characteristics
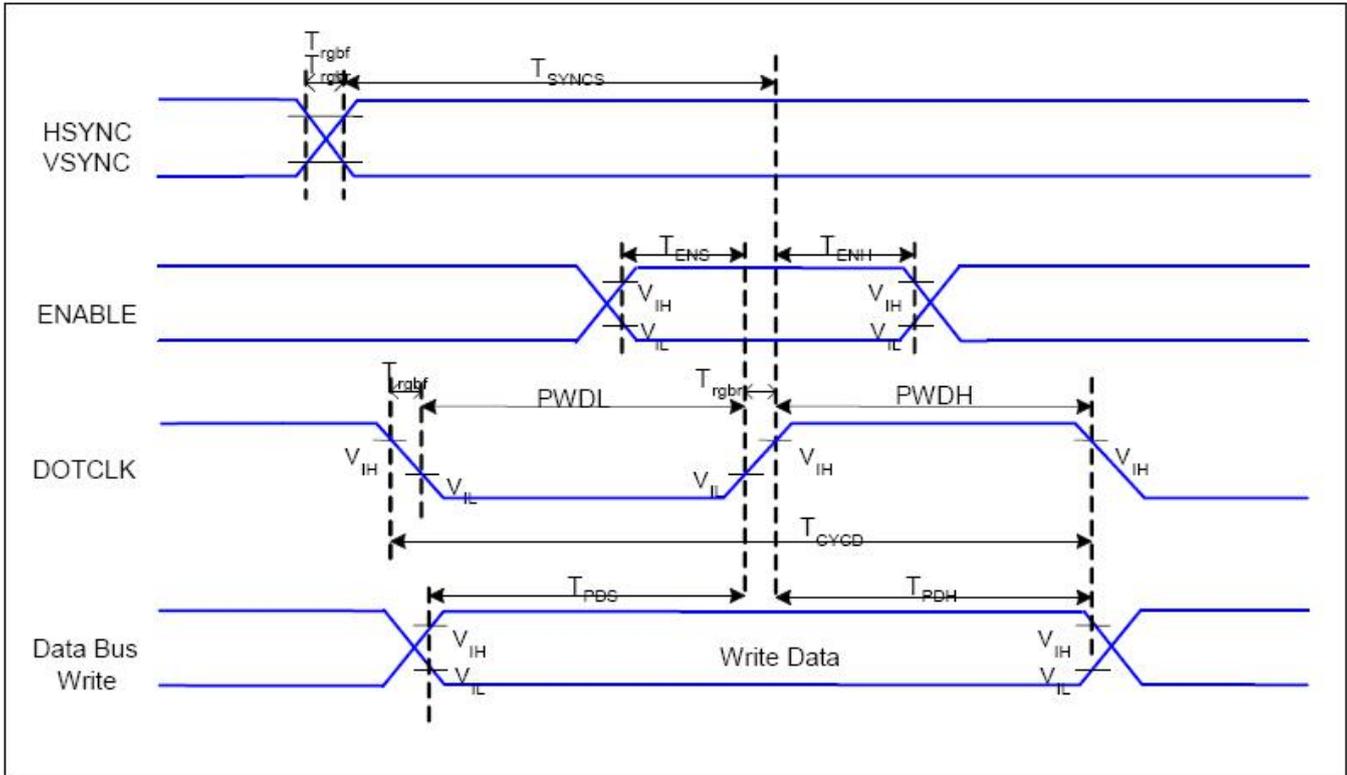
Figure 6.1: Parallel RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	13	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	13	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	28	-	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK Rise/Fall Time	-	15	ns	
DB	T_{PDS}	DB Data Setup Time	5	-	ns	
	T_{PDH}	DB Data Hold Time	5	-	ns	

Table 6.1: Parallel RGB Interface Timing Characteristics
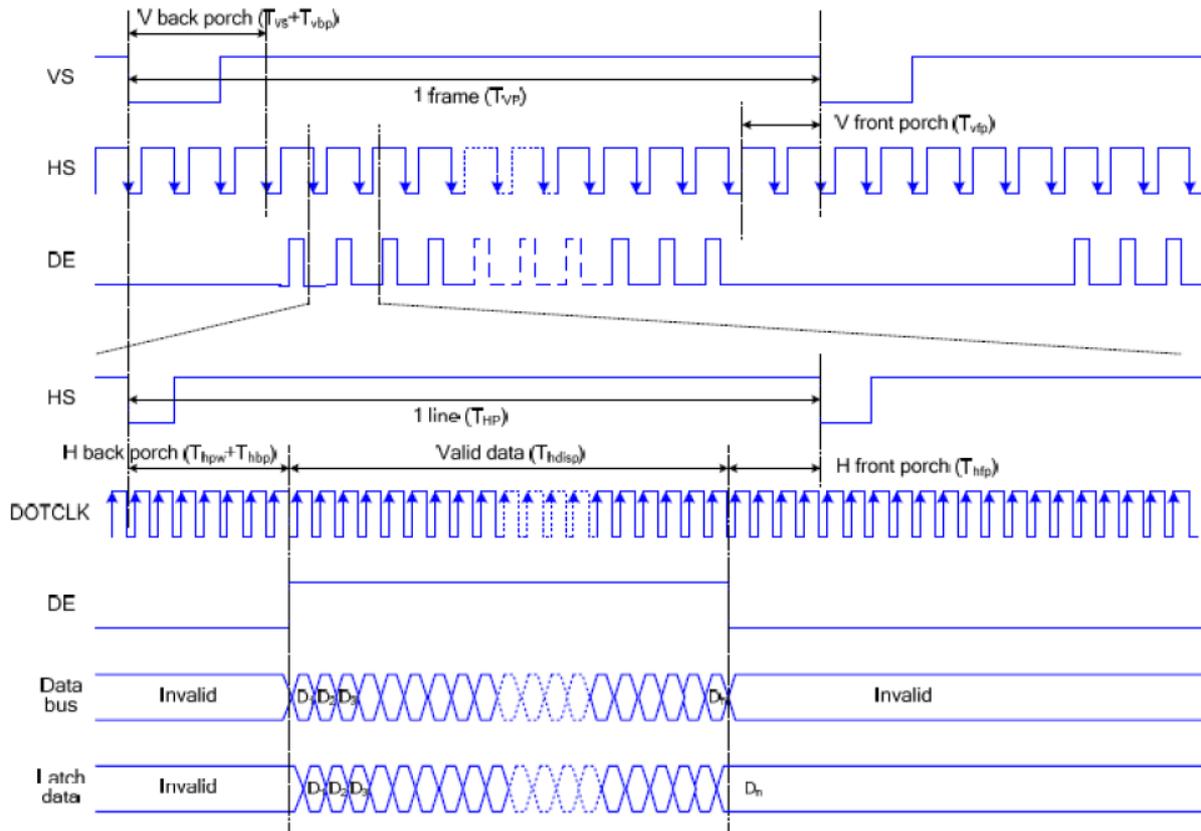
Note: The setting of front porch and back porch in host must match that in IC as this mode.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frame Rate	FR		54	--	66	fps
Horizontal sync width	hpw		1	--	--	DCLK
Horizontal back porch	hbp		2	--	126	DCLK
Horizontal Active Area	HACT		--	480	--	DCLK
Horizontal front porch	hfp		2	--	--	DCLK
Vertical sync width	vs		1	--	126	Line
Vertical back porch	vbp		1	--	126	Line
Vertical front porch	vfp		1	--	255	Line
Vertical Active Area	VACT		--	854	--	Line
DOTCLK	DCLK		16.6	--	41.7	MHz

6.2 Display Serial Interface Characteristics (3-line SPI system)
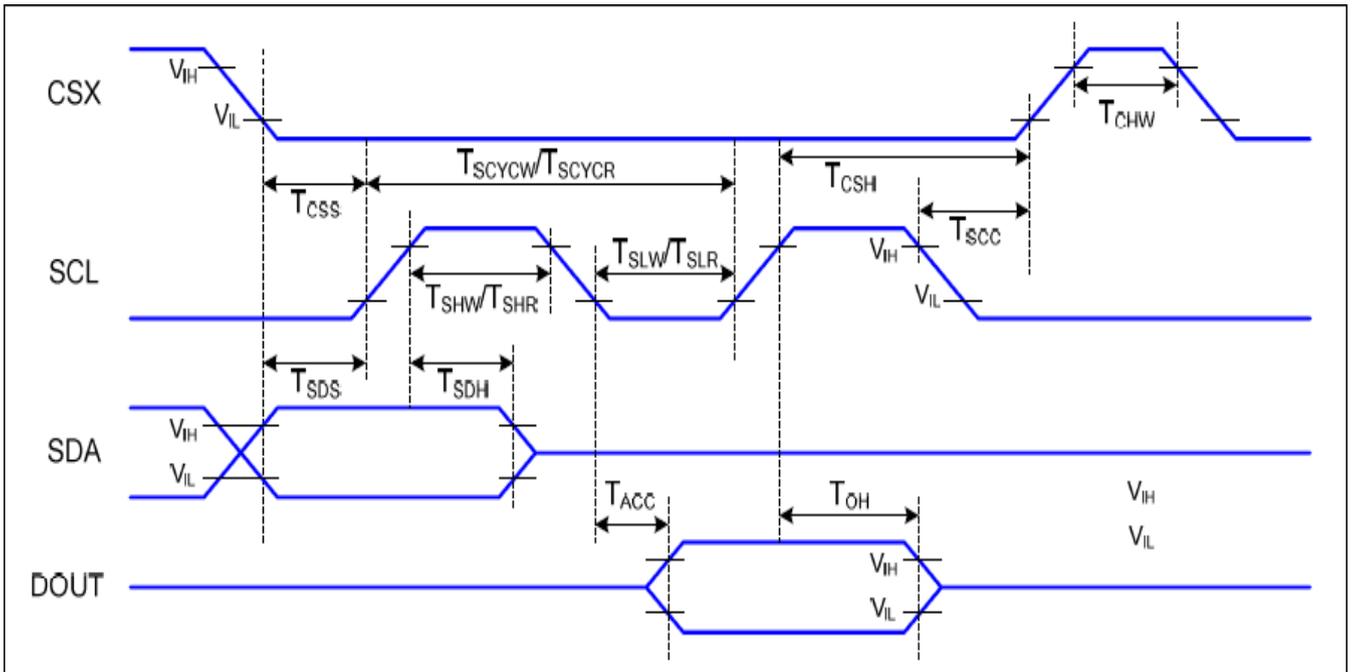
Figure 6.2: Serial Interface 3-SPI Timing Diagram

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C^o

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	15		ns	
	T_{SCC}	Chip select hold time (read)	15		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	30		ns	
	T_{SHW}	SCL "H" pulse width (write)	10		ns	
	T_{SLW}	SCL "L" width (write)	10		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10			
DOUT	T_{ACC}	Access time	10	50	ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50		

Table 6.2: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.3   Reset Timing
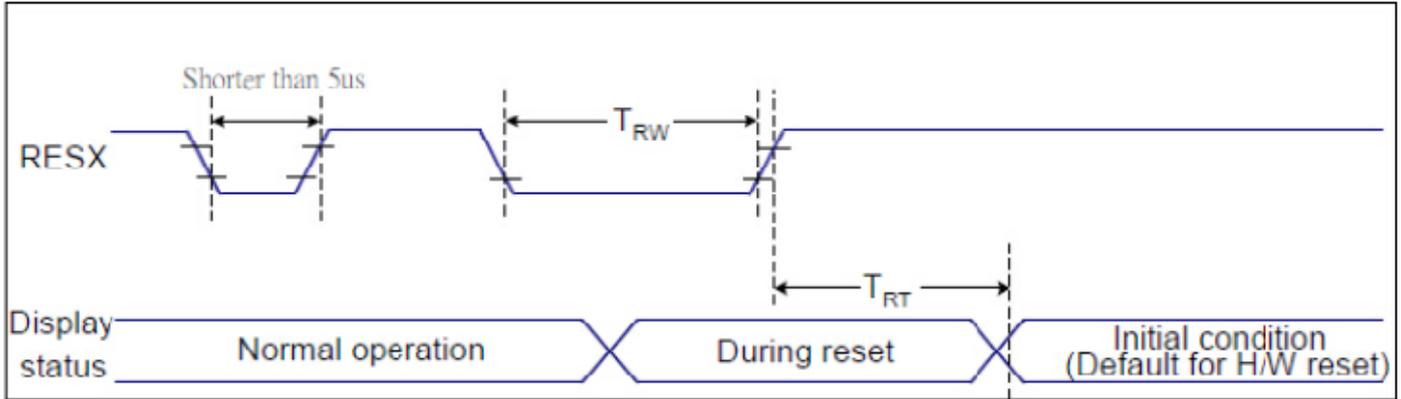

Figure 6.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
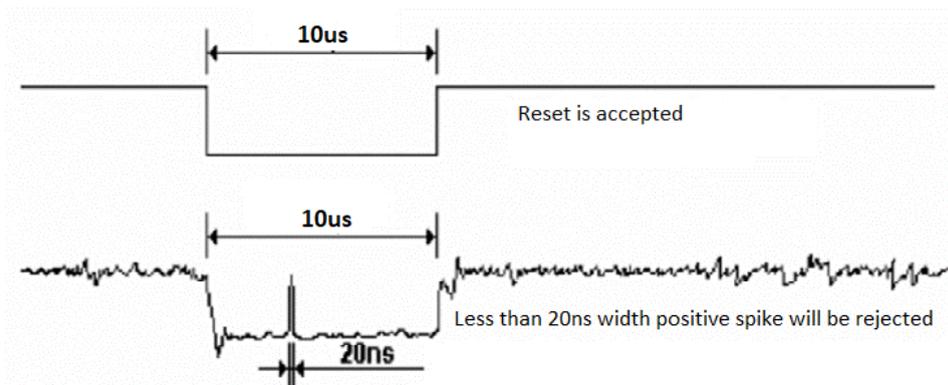
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.