FOCUS LCDs
LCDs MADE SIMPLE®

ISO 9001
QUALITY MANAGEMENT

MEDICAL | INDUSTRIAL | DEFENSE | AGRICULTURE | FOOD SERVICE

G120160A-FT0-DS123

Product Description

- 120x160 Graphic LCD
- FSTN Positive
- 63.50x74.00mm Module
- Parallel and SPI Interfaces
- No Backlight

- Transflective
- Special Temp Range
- 3.0V
- LCD IC: UC1610i
- RoHS Compliant

LCD@FocusLCDs.com | 480-503-4295

Revision History

Date	Rev. No	Page	Summary
12/04/2025	1.0	All	First issue

Graphic LCD Features

Resolution: 120x160 Dots
Interface(s): Parallel and SPI
RoHS Compliant.

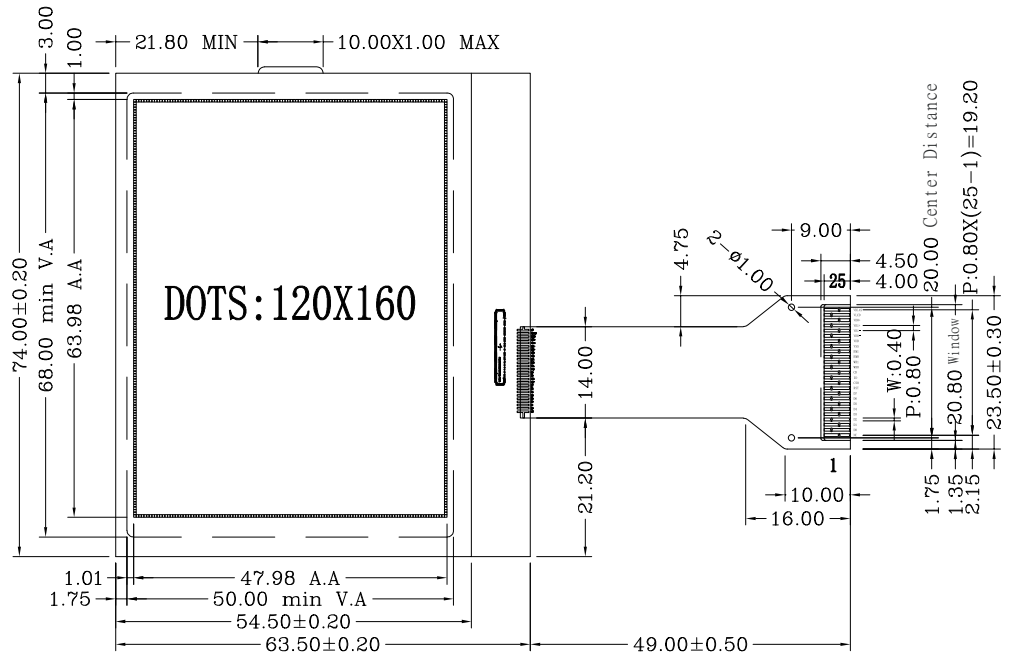
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	50.0 (H) x 68.0 (V)	mm	--
LCD Type	FSTN Positive	--	--
Viewing Angle	12:00	O'Clock	--
Polarizer	Transflective	--	--
Backlight Type	None	--	--
Backlight Color	N/A	--	--
LCD IC	UC1610i	--	--
Drive Mode	1/120 Duty, 1/12 Bias	--	--
Operating Temperature	-30 to +80	°C	--
Storage Temperature	-35 to +85	°C	--

Mechanical Information

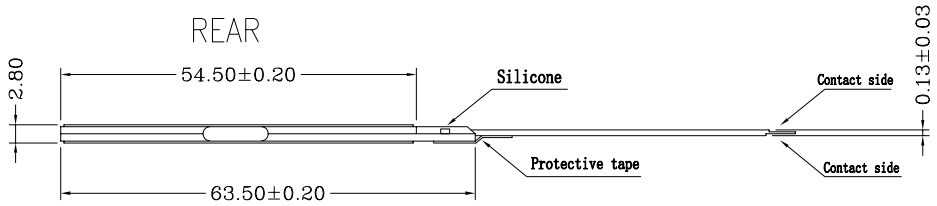
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	63.50	--	mm	--
	Vertical (V)	--	74.00	--	mm	--
	Depth (D)	--	2.80	--	mm	--
Weight		--	28	--	g	Approximate

1. Outline Dimensions

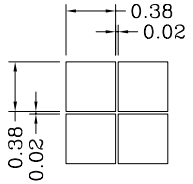
Rev.	Description	Date
1.0	First	11/19/2025
2.0	Updated viewing angle	12/04/2025



REAR



FRONT



NO	PIN
1	NC
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	RST
11	CS0
12	ID
13	CD
14	WR0
15	WR1
16	BM0
17	BM1
18	VSS
19	VDD
20	VB0-
21	VB1-
22	VB1+
23	VB0+
24	VLCD
25	VBIAS

NOTES:
1. DISPLAY TYPE: 120x160 FSTN GRAPHIC LCD
2. POLARIZER: TRANSFLECTIVE, POSITIVE MODE
3. VIEWING ANGLE: 12:00
4. OPERATING TEMPERATURE: -30°C TO +80°C
   STORAGE TEMPERATURE: -35°C TO +85°C
5. DRIVE METHOD: 1/120 DUTY, 1/12 BIAS, VDD 3.0V,
6. LCD IC: UC1610i
7. BACKLIGHT: N/A
8. ROHS COMPLIANT.

Model Name: G120160A-FT0-DS123		FOCUS LCDs LCDs MADE SIMPLE®
General Tol: ±0.2		
Approvals	Date	Drawing No.: / Scale:
DWN:		
CHK:		Size: / Unit: mm / Page: 1/1
APP:		

2. Input Terminal Pin Assignment

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>1</td><td>NC</td><td>No connection.</td><td>--</td></tr>
<tr><td>2-9</td><td>D0-D7</td><td>Bi-directional bus for both serial and parallel host interfaces.</td><td>I/O</td></tr>
<tr><td>10</td><td>RST</td><td>When RST=”L”, all control registers are re-initialized by their default states.</td><td>I</td></tr>
<tr><td>11</td><td>CS0</td><td>Chip Select.
Chip is selected when CS1=”H” and CS0 = “L”.</td><td>I</td></tr>
<tr><td>12</td><td>ID</td><td>ID pin is for production control. The connection will affect the content of D[7] when using Get Status command.</td><td>I</td></tr>
<tr><td>13</td><td>CD</td><td>Select control data or display data for read/write operation.</td><td>I</td></tr>
<tr><td>14</td><td>WR0</td><td rowspan="2">WR[1:0] controls the read/write operation of the host interface.
<table>
<tr><th colspan="2">Mode</th><th>WR[1:0]</th></tr>
<tr><td rowspan="2">Parallel</td><td>8080</td><td>RD, WR</td></tr>
<tr><td>6800</td><td>EN, R/W</td></tr>
<tr><td rowspan="4">Serial</td><td>S8</td><td>11</td></tr>
<tr><td>S8uc</td><td>11</td></tr>
<tr><td>S9</td><td>00</td></tr>
<tr><td>I²C</td><td>11</td></tr>
</table></td><td rowspan="2">I</td></tr>
<tr><td>15</td><td>WR1</td></tr>
<tr><td>16</td><td>BM0</td><td rowspan="2">Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:
<table>
<tr><th colspan="2">Mode</th><th>BM[1:0]</th><th>D[7:6]</th></tr>
<tr><td>8080</td><td rowspan="2">8-bit</td><td>10</td><td>Data</td></tr>
<tr><td>6800</td><td>11</td><td>Data</td></tr>
<tr><td>8080</td><td rowspan="2">4-bit</td><td>00</td><td>00</td></tr>
<tr><td>6800</td><td>01</td><td>00</td></tr>
<tr><td colspan="2">4-wire SPI w/ 8-bit token (S8: conventional)</td><td>00</td><td>10</td></tr>
<tr><td colspan="2">3-wire SPI w/ 8-bit token (S8uc: ultra-compact)</td><td>00</td><td>11</td></tr>
<tr><td colspan="2">3-wire SPI w/ 9-bit token (S9: conventional)</td><td>01</td><td>10</td></tr>
<tr><td colspan="2">2-wire I²C</td><td>01</td><td>11</td></tr>
</table></td><td rowspan="2">I</td></tr>
<tr><td>17</td><td>BM1</td></tr>
<tr><td>18</td><td>VSS</td><td>Ground.</td><td>P</td></tr>
<tr><td>19</td><td>VDD</td><td>Power.</td><td>P</td></tr>
<tr><td>20</td><td>VB0-</td><td rowspan="4">LCD bias voltages.
These are the voltage sources to provide SEG driving currents.
These voltages are generated internally.
Connect capacitors of CBX value between VBX+ and VBX–.</td><td rowspan="4">P</td></tr>
<tr><td>21</td><td>VB1-</td></tr>
<tr><td>22</td><td>VB1+</td></tr>
<tr><td>23</td><td>VB0+</td></tr>
<tr><td>24</td><td>VLCD</td><td>High voltage LCD power supply.</td><td>P</td></tr>
<tr><td>25</td><td>VBIAS</td><td>This is the reference voltage to generate the actual SEG driving voltage.</td><td>I</td></tr>
</table>

3. LCD Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit
Contrast Ratio		CR	--	--	5	--	--
Response Time	On	T_{on}	--	--	150	250	ms
	Off	T_{off}		--	180	300	ms
Viewing Angle $C_r \geq 2$, 25°C	Hor.	Θ_L	Φ=270°, 9H	--	55	--	degree
		Θ_R	Φ=90°, 3H	--	55	--	
	Ver.	Θ_T	Φ=180°, 12H	--	70	--	
		Θ_B	Φ=0°, 6H	--	40	--	

4. TFT Electrical Characteristics

4.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	4.0	V
	V0-XV0	-0.3	18.0	V
Input Voltage	V_{IN}	-0.4	VDD+0.5	V
Operating Temperature	T_{OP}	-30	+80	°C
Storage Temperature	T_{ST}	-35	+85	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
LCD Driving Voltage		VLCD	--	--	13.4	--	V
Supply Voltage		VDD	VDD-GND	2.6	3.0	3.4	V
Input Voltage	H Level	V_{IH}	--	0.8VDD	--	--	V
	L Level	V_{IL}	--	--	--	0.2VDD	V

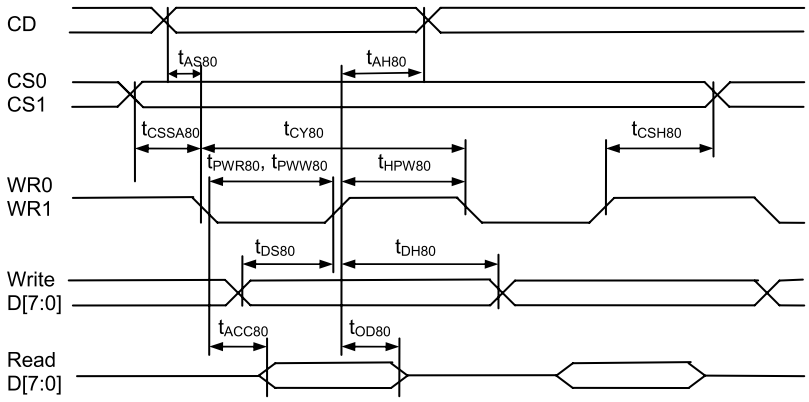
Condition:

1. VDD = 3.0V
2. 1/120 Duty, 1/12 Bias

5. Module Function

5.1 Timing Characteristics

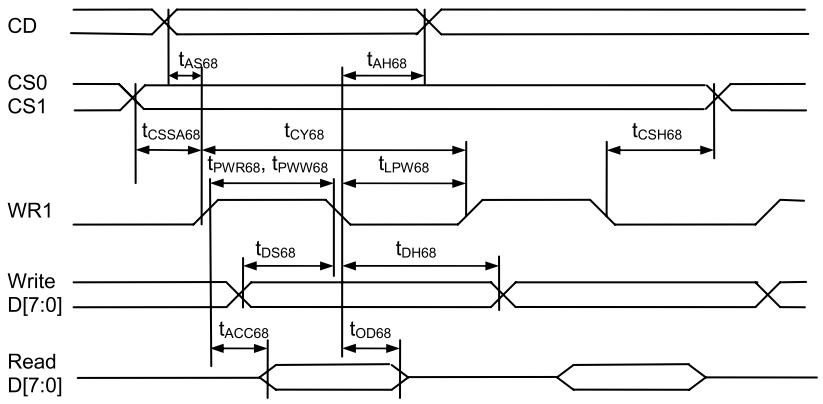
System Bus Timing for 8080 MCU Interface



Symbol	Signal	Description	Condition	Min.	Max.	Unit
($2.5V \le V_{DD} < 3.465V$, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		5 15	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5	–	nS
t_{CY80}	WR1 / WR0	System cycle time	(8-bit bus) (4-bit bus)	170 / 110 170 / 110	–	nS
t_{PWR80} / t_{PWW80}		Pulse width	(8-bit bus) (4-bit bus)	70 / 40 70 / 40		
t_{HPW80}		High pulse width	(8-bit bus) (4-bit bus)	70 / 40 70 / 40		
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		30 15	–	nS
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 25	60	nS
($1.8V \le V_{DD} < 2.5V$, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		10 30	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10	–	nS
t_{CY80}	WR1 / WR0	System cycle time	(8-bit bus) (4-bit bus)	310 / 190 310 / 190	–	nS
t_{PWR80} / t_{PWW80}		Pulse width	(8-bit bus) (4-bit bus)	140 / 80 140 / 80		
t_{HPW80}		High pulse width	(8-bit bus) (4-bit bus)	140 / 80 140 / 80		
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		60 30	–	nS
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 50	–	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

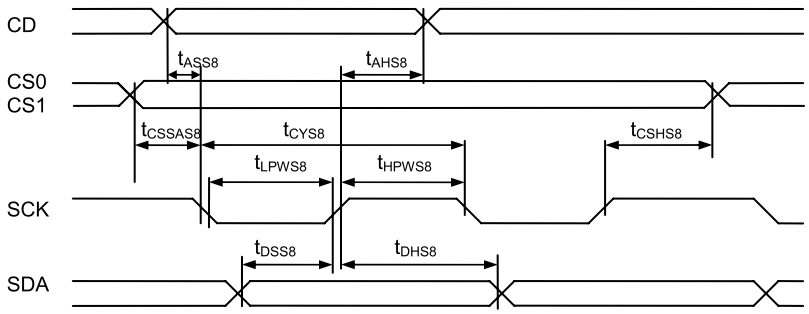
System Bus Timing for 6800 MCU Interface



Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		5 15	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS
t_{CY68}	WR1	System cycle time	(8-bit bus) (4-bit bus)	170 / 110 170 / 110	–	nS
t_{PWR68} / t_{PWW68}		Pulse width	(8-bit bus) (4-bit bus)	70 / 40 70 / 40		
t_{LPW68}		Low pulse width	(8-bit bus) (4-bit bus)	70 / 40 70 / 40		
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 25	60	nS
(1.8V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		10 30	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10		nS
t_{CY68}	WR1	System cycle time	(8-bit bus) (4-bit bus)	310 / 190 310 / 190	–	nS
t_{PWR68} / t_{PWW68}		Pulse width	(8-bit bus) (4-bit bus)	140 / 80 140 / 80		
t_{LPW68}		Low pulse width	(8-bit bus) (4-bit bus)	140 / 80 140 / 80		
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		60 30	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 50		nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

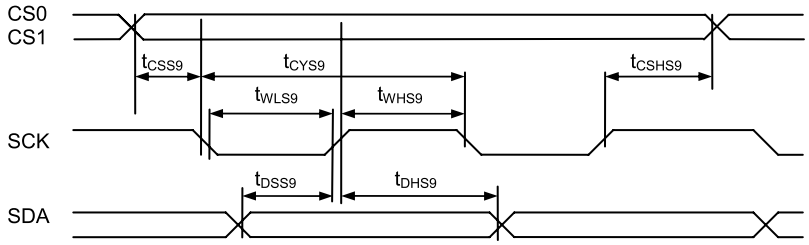
Serial Bus Timing for S8 / S8uc



Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		5 20	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 15	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width	tr, tf ≤ 15	155 63 62	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
(1.8V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		10 45	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 30	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width	tr, tf ≤ 15	280 125 125	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		60 40	–	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

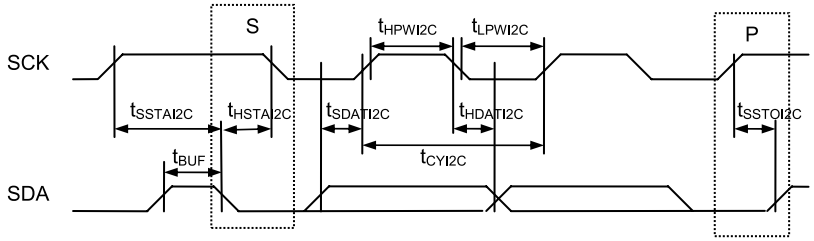
Serial Bus Timing for S9



Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width	tr, tf ≤ 15	110 40 40	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
(1.8V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width	tr, tf ≤ 15	190 80 80	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		60 40	–	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

Serial Bus Timing for I²C



Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C}	SCK	SCK cycle time	tr, tf ≤ 15	280	–	nS
t_{LPWI2C}		Low pulse width		125	–	nS
t_{HPWI2C}		High pulse width		125	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		25	–	nS
t_{HDAI2C}		Data hold time		10	–	nS
$t_{SSTAI2C}$		START Setup time		25	–	nS
$t_{HSTAI2C}$		STAR Hold time		20	–	nS
$t_{SSTOI2C}$		STOP setup time		25	–	nS
(1.8V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C}	SCK	SCK cycle time	tr, tf ≤ 15	330	–	nS
t_{LPWI2C}		Low pulse width		150	–	nS
t_{HPWI2C}		High pulse width		150	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		40	–	nS
t_{HDAI2C}		Data hold time		10	–	nS
$t_{SSTAI2C}$		START Setup time		25	–	nS
$t_{HSTAI2C}$		STAR Hold time		35	–	nS
$t_{SSTOI2C}$		STOP setup time		25	–	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

Reset Timing Characteristic

(1.8V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
t_{RW}	RST	Reset low pulse width		1	–	µS

5.2 LCM Application

Please see information on pages 31-35 of the data sheet for LCD controller UC1610i. The data sheet can be found here: *https://focuslcds.com/wp-content/uploads/Drivers/UC1610i.pdf*

5.3 Command Table

The following is a list of host commands supported by UC1610i:

C/D: 0 Control, 1 Data; W/R: 0 Write cycle, 1 Read cycle; D7-D0: # Useful data bits, "-" Don't care

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Page Address	0	0	0	1	1	#	#	#	#	#	Set PA[4:0]	0
11	Set V_BIAS Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	B2H
		0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[8:7]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
20	Set LCD Gray Shade	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	00b
21	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
22	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
23	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
24	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
25	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
26	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
31	Set Window Program Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[4:0]	0
		0	0	-	-	-	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
33	Set Window Program Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[4:0]	31
		0	0	-	-	-	#	#	#	#	#		
34	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

6. Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.