FOCUS LCDs
LCDs MADE SIMPLE®

ISO 9001
QUALITY MANAGEMENT

MEDICAL | INDUSTRIAL | DEFENSE | AGRICULTURE | FOOD SERVICE

G128128A-FTW-LW63

Product Description

- 128x128 Graphic LCD
- FSTN Positive
- 71.30x75.41mm Module
- Parallel and SPI Interfaces
- White LED Backlight

- Transflective
- Wide Temp Range
- 3.0V
- LCD IC: ST75160
- RoHS Compliant

LCD@FocusLCDs.com | 480-503-4295

Revision History

Date	Rev. No	Page	Summary
08/15/2025	1.0	All	First issue

Graphic LCD Features

Resolution: 128x128 Dots
Interface(s): Parallel and SPI
RoHS Compliant.

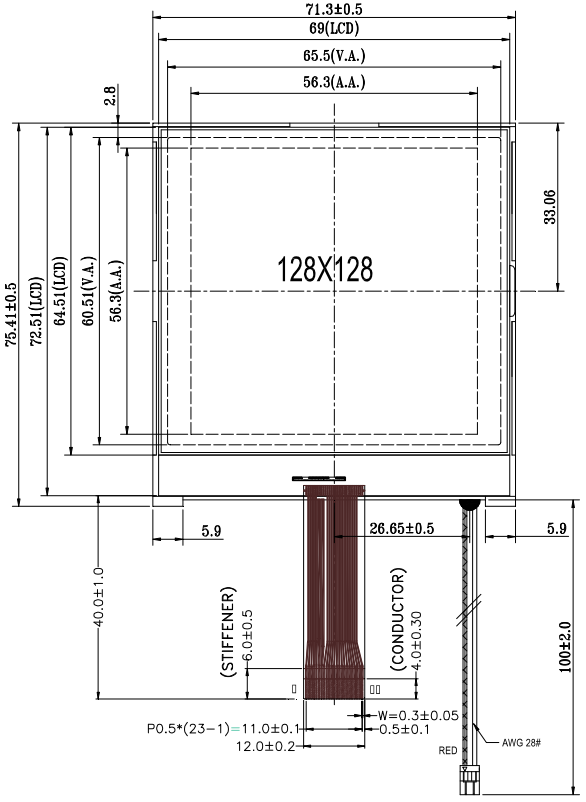
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	65.50 (H) x 60.51 (V)	mm	--
LCD Type	FSTN Positive	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transflective	--	--
Backlight Type	LED	--	--
Backlight Color	White	--	--
LCD IC	ST75160	--	--
Drive Mode	1/128 Duty, 1/12 Bias	--	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

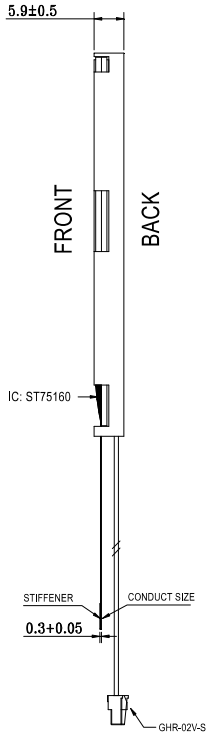
Mechanical Information

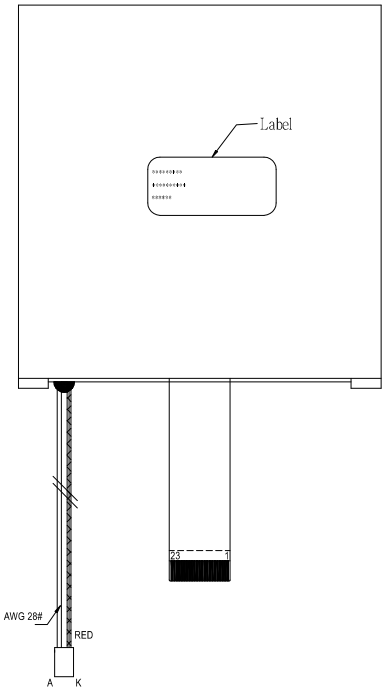
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	71.30	--	mm	--
	Vertical (V)	--	75.41	--	mm	--
	Depth (D)	--	5.90	--	mm	--
Weight		--	TBD	--	g	--

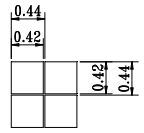
1. Outline Dimensions

Rev.	Description	Date
1.0	First	08/15/2025





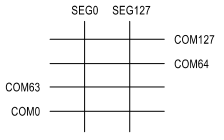




DOTS SCALE:1/10

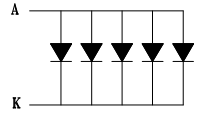
Pin Assignment:

NO	PIN
1	VG
2	V0
3	XV0
4	CA1P
5	CA1N
6	VDD
7	VSS
8	IF2
9	IF1
10	IF0
11	CSB
12	A0
13	ERD
14	RWR
15	RST
16	D0
17	D1
18	D2
19	D3
20	D4
21	D5
22	D6
23	D7



COM & SEG LAYOUT

WHITE LED BACKLIGHT



NOTES:
1. DISPLAY TYPE: 128x128 FSTN GRAPHIC LCD
2. POLARIZER: TRANSFLECTIVE, POSITIVE MODE
3. VIEWING ANGLE: 6:00
4. OPERATING TEMPERATURE: -20°C TO +70°C
   STORAGE TEMPERATURE: -30°C TO +80°C
5. DRIVE METHOD: 1/128 DUTY,1/12 BIAS,VDD 3.0V,VLCD 13.5V
6. LCD IC: ST75160
7. BACKLIGHT: WHITE LED, 5 LEDS, 45mA, 3.3V
8. ROHS COMPLIANT.

Model Name: G128128A-FTW-LW63		
General Tol: ±0.3		
Approvals	Date	
DWN:		
CHK:		
APP:		

FOCUS LCDs
LCDs MADE SIMPLE®

Drawing No.:
Scale:
Size:
Unit: mm
Page: 1/1

2. Input Terminal Pin Assignment

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>1</td><td>VG</td><td>VG is the power of SEG-drivers.</td><td>P</td></tr>
<tr><td>2</td><td>V0</td><td>Positive operating voltage of COM-drivers.</td><td>P</td></tr>
<tr><td>3</td><td>XV0</td><td>Negative operating voltage of COM-drivers.</td><td>P</td></tr>
<tr><td>4</td><td>CA1P</td><td rowspan="2">DC/DC voltage converter. Connect a capacitor between CA1P and CA1N.</td><td rowspan="2">O</td></tr>
<tr><td>5</td><td>CA1N</td></tr>
<tr><td>6</td><td>VDD</td><td>Power supply for LCM (+3.0V).</td><td>P</td></tr>
<tr><td>7</td><td>VSS</td><td>Ground.</td><td>P</td></tr>
<tr><td>8
9
10</td><td>IF2
IF1
IF0</td><td>These pins select interface operation mode.
<table><tr><th>IF2</th><th>IF1</th><th>IF0</th><th>Description</th></tr><tr><td>L</td><td>L</td><td>L</td><td>4-line serial interface</td></tr><tr><td>L</td><td>L</td><td>H</td><td>I²C serial interface</td></tr><tr><td>L</td><td>H</td><td>L</td><td>8-bit 6800 parallel interface</td></tr><tr><td>L</td><td>H</td><td>H</td><td>8-bit 8080 parallel interface</td></tr><tr><td>H</td><td>L</td><td>L</td><td>9-bit 3-line serial interface</td></tr></table>Note: Refer to Parallel / Serial Interface for detailed information.</td><td>I</td></tr>
<tr><td>11</td><td>CSB</td><td>Chip select input pin.
CSB="L": This chip is selected and the MPU interface is active.
CSB="H": This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).
There is no CSB pin in I²C interface and it should be fixed to “L” by VSS1.</td><td>I</td></tr>
<tr><td>12</td><td>A0</td><td>It determines whether the access is related to data or command.
A0 = "H": Indicates that D[7:0] are display data;
A0 = "L": Indicates that D[7:0] are control data.
There is no A0 pin in 3-Line SPI and I2C interface. A0 should be fixed to "H" by VDD1.</td><td>I</td></tr>
<tr><td>13</td><td>ERD</td><td>Read/Write execution control pin (only used in parallel interface).
This pin is not used in serial interfaces and should be connected to VDD1.<table><tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr><tr><td>6800-series</td><td>E</td><td>Read/Write control input pin.
R/W=”H”: When E is “H”, data bus is in output status.
R/W=”L”: The data are latched at the falling edge of the E signal.</td></tr><tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr></table></td><td>I</td></tr>
</table>

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>14</td><td>RWR</td><td>Read/Write execution control pin (only used in parallel interface).
This pin is not used in serial interfaces and should be connected to VDD1.
<table>
<tr><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read/Write control input pin.
R/W=”H“: read.
R/W=”L“: write.</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table></td><td>I</td></tr>
<tr><td>15</td><td>RST</td><td>Reset input pin.
When RST is "L", internal initialization procedure is executed.</td><td>I</td></tr>
<tr><td>16-23</td><td>D0~D7</td><td>When using 8-bit parallel interface: 8080 or 6800 mode
8 bit bi-directional data bus.
Connect to the data bus of 8-bit microprocessor.
When CSB is “H”, D[7:0] are high impedance.

When using serial interface : 4-line SPI or 3-line SPI mode
D[7:4] : fix to “H” by VDD1.
D[3:1] : serial input/output data (SDA).
D[0] : serial input clock (SCL).
<u>D1 to D3 must be connected together (SDA)</u>
When CSB is “H”, D[7:0] are high impedance.

When using serial interface : I²C interface
D[7] : SA[1], I²C slave address bit. Must be connected to VDD1 or VSS1.
D[6] : SA[0], I²C slave address bit. Must be connected to VDD1 or VSS1.
D[5:4] : fix to “H” by VDD1.
D[3:2] : SDA_OUT, serial data and acknowledge output for the I²C interface. D[1] : SDA_IN, serial input data.
D[0] : SCL, serial input clock.
<u>D1 to D3 must be connected together (SDA)</u>
<u>CSB must be fixed to “L” by VSS1.</u></td><td>I/O</td></tr>
</table>

3. LCD Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit
Contrast Ratio		CR	Ta=25°C	2	5	--	--
Response Time	On	T_{on}		--	150	250	ms
	Off	T_{off}		--	200	300	ms
Viewing Angle	Hor.	Θ_L	Φ=270°, 9H	50	60	--	degree
		Θ_R	Φ=90°, 3H	50	60	--	
	Ver.	Θ_T	Φ=180°, 12H	30	40	--	
		Θ_B	Φ=0°, 6H	50	60	--	

4. TFT Electrical Characteristics

4.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	VDD	0.3	3.6	V
Input Voltage	V_{IN}	VSS	VDD	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
LCD Driving Voltage		VLCD	--	13.2	13.5	13.8	V
Supply Voltage		VDD	--	2.7	3.0	3.3	V
Input Voltage	H Level	V_{IH}	--	2.2	--	VDD	V
	L Level	V_{IL}	--	0	--	0.6	V
Output Voltage	H Level	V_{OH}	--	2.4	--	--	V
	L Level	V_{OL}	--	--	--	0.4	V

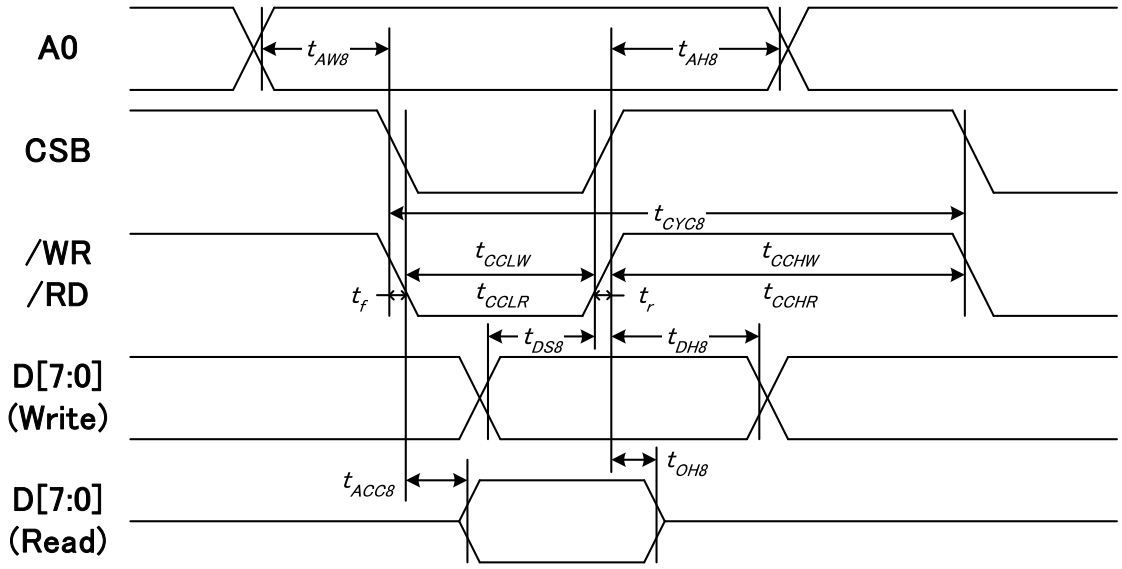
Condition:

1. VDD = 3.0V
2. 1/128 Duty, 1/12 Bias

5. Module Function

5.1 Timing Characteristics

System Bus Timing for 8080 MCU Interface

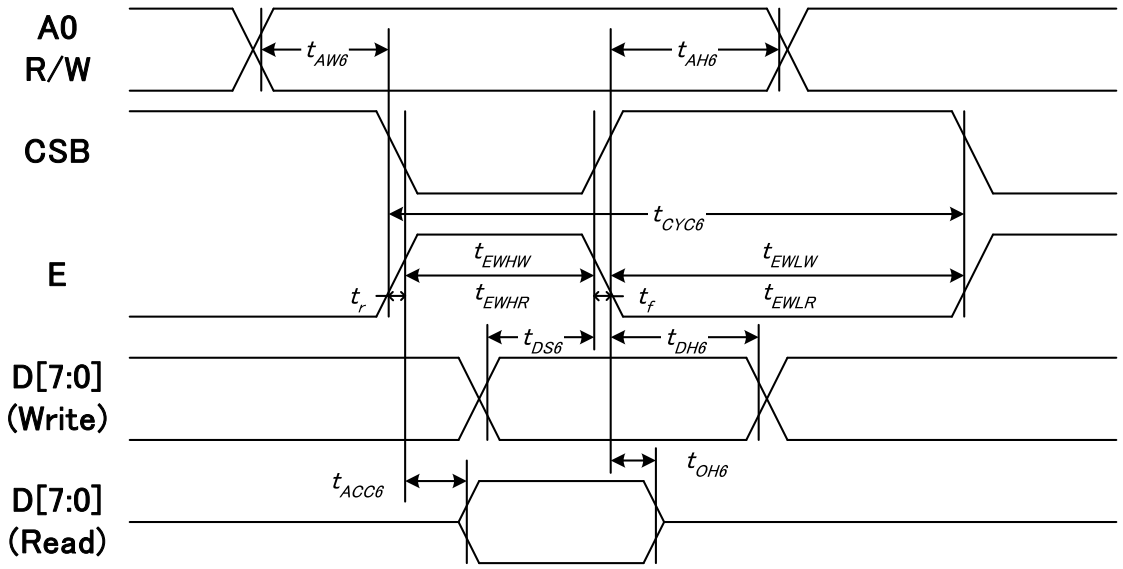


(VDD1 = 1.8~3.3V, Ta = –30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW8}		20	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time (WRITE)	/WR	t_{CYC8}		160	—	
/WR L pulse width (WRITE)		t_{CCLW}		70	—	
/WR H pulse width (WRITE)		t_{CCHW}		70	—	
System cycle time (READ)	/RD	t_{CYC8}		400		
/RD L pulse width (READ)		t_{CCLR}		180		
/RD H pulse width (READ)		t_{CCHR}		180		
WRITE Data setup time	D[7:0]	t_{DS8}		15	—	
WRITE Data hold time		t_{DH8}		15	—	
READ access time		t_{ACC8}	CL=30pF	—	100	
READ Output disable time		t_{OH8}	CL=30pF	10	100	

Note:
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2. All timing is specified using 20% and 80% of VDD1 as the reference.

System Bus Timing for 6800 MCU Interface

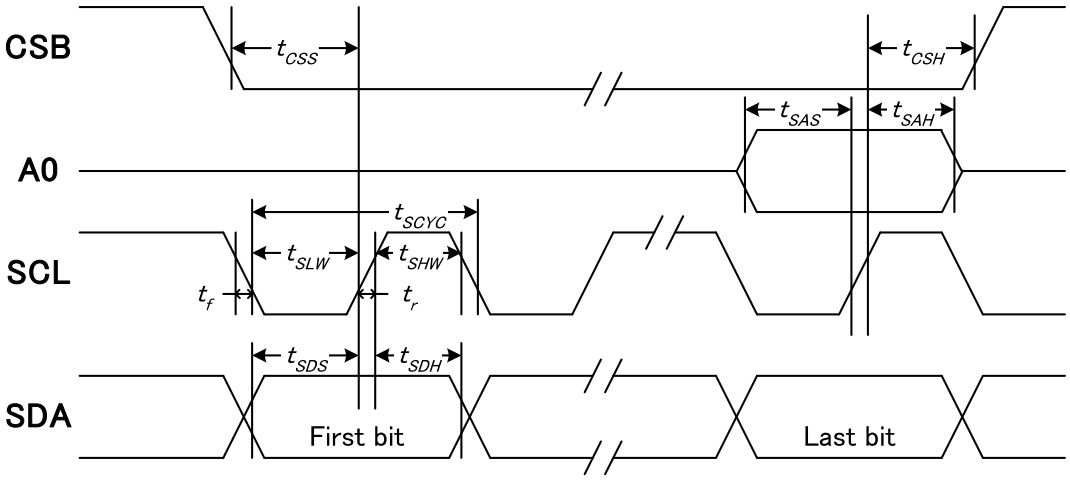


(VDD1 = 1.8~3.3V, Ta = –30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW6}		20	—	ns
Address hold time		t_{AH6}		0	—	
System cycle time (WRITE)	E	t_{CYC6}		160	—	
Enable L pulse width (WRITE)		t_{EWLW}		70	—	
Enable H pulse width (WRITE)		t_{EWHW}		70	—	
System cycle time (READ)		t_{CYC6}		400		
Enable L pulse width (READ)		t_{EWLR}		180	—	
Enable H pulse width (READ)		t_{EWHR}		180		
Write data setup time	D[7:0]	t_{DS6}		15	—	
Write data hold time		t_{DH6}		15	—	
Read data access time		t_{ACC6}	CL=30pF	—	100	
Read data output disable time		t_{OH6}	CL=30pF	10	110	

Note:
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2. All timing is specified using 20% and 80% of VDD1 as the reference.

System Bus Timing for 4-Line SPI MCU Interface



(VDD1 = 1.8~3.3V, Ta = –30~85°C)

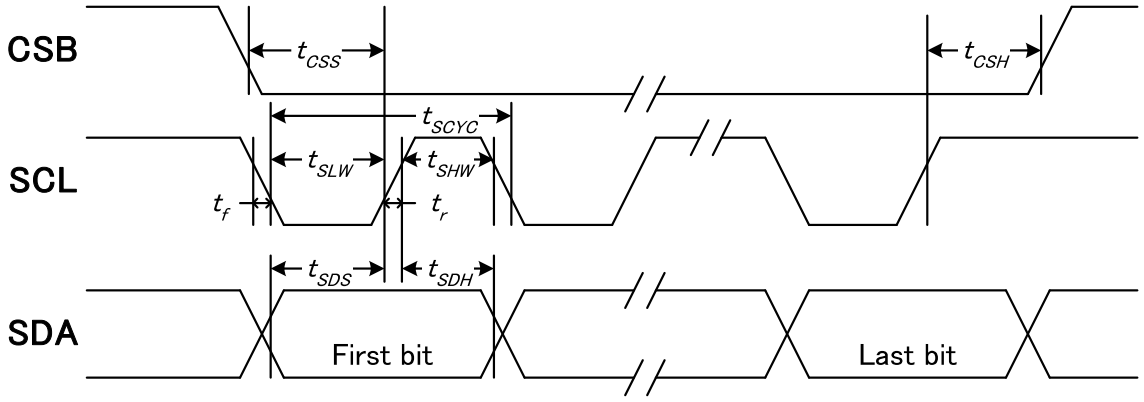
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCLK	t_{SCYC}		80	—	ns
SCLK “H” pulse width		t_{SHW}		30	—	
SCLK “L” pulse width		t_{SLW}		30	—	
Address setup time	A0	t_{SAS}		20	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SDA	t_{SDS}		20	—	
Data hold time		t_{SDH}		20	—	
CSB-SCLK time	CSB	t_{CSS}		20	—	
CSB-SCLK time		t_{CSH}		20	—	
CS “H” pulse width		t_{CHW}		0	—	

Note:

*1. The input signal rise time and fall time (t_r, t_f) are specified as 15ns or less.

*2. All timing is specified using 20% and 80% of VDD1 as the standard.

System Bus Timing for 3-Line SPI MCU Interface



(VDD1 = 1.8~3.3V, Ta = –30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		80	—	ns
SCL “H” pulse width		t_{SHW}		30	—	
SCL “L” pulse width		t_{SLW}		30	—	
Data setup time	SDA	t_{SDS}		20	—	
Data hold time		t_{SDH}		20	—	
CSB-SCL time	CSB	t_{CSS}		20	—	
CSB-SCL time		t_{CSH}		20	—	

Note:

*1. The input signal rise time and fall time (t_r, t_f) are specified as 15ns or less.

*2. All timing is specified using 20% and 80% of VDD1 as the standard.

5.2 LCM Application

Please see information on pages 96-100 of the data sheet for LCD controller ST75160. The data sheet can be found here: *https://focuslcds.com/wp-content/uploads/Drivers/ST75160.pdf*

5.3 Command Table

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
1.Extension Command	0	0	0	0	1	1	EXT1	0	0	EXT0	Set extension instruction
Ext[1:0]=0,0 (Extension Command 1)											
2.Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
3.Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
4.All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
5.Display Control	0	0	1	1	0	0	1	0	1	0	Set display control CLD :Set CL dividing ratio DT[7:0] : Set the number of duty LF[4:0] : Set N-line inversion counter FI : Set the inversion type of frame at the end of common scan cycle
	1	0	0	0	0	0	0	CLD	0	0	
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
	1	0	0	0	0	LF4	FI	LF3	LF2	LF1	
6.Power Save	0	0	1	0	0	1	0	1	0	SLP	Set power save mode SLP=0: Sleep out mode SLP=1: Sleep in mode
7.Set Page Address	0	0	0	1	1	1	0	1	0	1	Set page address Starting page address: 00h <= YS <= 27h Ending page address: YS <= YE <= 27h
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
8.Set Column Address	0	0	0	0	0	1	0	1	0	1	Set column address Starting column address: 00h <= XS <= 9Fh Ending column address: XS <= XE <= 9Fh
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
9.Data Scan Direction	0	0	1	0	1	1	1	1	0	0	Set normal/ inverse display of address and address scan direction
	1	0	0	0	0	0	0	MV	MX	0	
10.Write Data	0	0	0	1	0	1	1	1	0	0	Write data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
11.Read Data	0	0	0	1	0	1	1	1	0	1	Read data from DDRAM (Only for parallel interface and I²C)
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
12.Partial In	0	0	1	0	1	0	1	0	0	0	Set partial area Starting partial display address: 00h <= PTS <= 9Fh Ending partial display address: 00h <= PTE <= 9Fh
	1	0	PTS7	PTS6	PTS7	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	
13.Partial Out	0	0	1	0	1	0	1	0	0	1	Exit the partial mode
14.Read/Modify/Write In	0	0	1	1	1	0	0	0	0	0	Enable read modify write
15.Read/Modify/Write Out	0	0	1	1	1	0	1	1	1	0	Disable read modify write
16.Scroll Area	0	0	1	0	1	0	1	0	1	0	Set scroll areaTL[7:0] : Set top line addressBL[7:0] : Set bottom line addressNSL[7:0] : Number of specified lineSCM[1:0] : Area scroll mode
	1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	
	1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	
	1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	
	1	0	0	0	0	0	0	0	SCM1	SCM0	
17.Set Start Line	0	0	1	0	1	0	1	0	1	1	Set scroll start address 00h <= SL <= 9Fh
	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	
18.OSC ON	0	0	1	1	0	1	0	0	0	1	Turn on the internal oscillator
19.OSC OFF	0	0	1	1	0	1	0	0	1	0	Turn off the internal oscillator
20.Power Control	0	0	0	0	1	0	0	0	0	0	Power circuit operation VB=0: OFF, VB=1: ON VF=0: OFF, VF=1: ON VR=0: OFF, VR=1: ON
	1	0	0	0	0	0	VB	0	VF	VR	
21.Set Vop	0	0	1	0	0	0	0	0	0	1	Set Vop
	1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	0	0	0	0	0	Vop8	Vop7	Vop6	
22.Vop Control	0	0	1	1	0	1	0	1	1	VOL	Control Vop VOL=0: Vop increase one step VOL=1: Vop decrease one step
23.Read Register Mode	0	0	0	1	1	1	1	1	0	REG	Set read register mode REG=0: read the register value of Vop[5:0] REG=1: read the register value of Vop[8:6]
24.Nop	0	0	0	0	1	0	0	1	0	1	No operation
25.Read Status (Parallel and I²C)	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read status byte (Parallel and I²C)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
26.Read Status (4-Line and 3-Line SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte (4-Line and 3-Line SPI)
	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
27.Data Format Select	0	0	0	0	0	0	1	DO	0	0	DO=0; LSB on bottom (Default) DO=1; LSB on top
28.Display Mode	0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
	1	0	0	0	0	1	0	0	0	DM	
29.Set ICON	0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON RAM ICON=1 ; Enable ICON RAM ICON=0 ; Disable ICON RAM
Ext[1:0]=0,1 (Extension Command 2)											
30. Set Gray Level	0	0	0	0	1	0	0	0	0	0	Set gray scale level GL[4:0]: Set Light Gray Level GD[4:0]: Set Dark Gray Level
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
31.Analog Circuit Set	0	0	0	0	1	1	0	0	1	0	Set analog circuit BE[1:0]: Booster efficiency set BS[2:0]: Set bias ratio
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	BE1	BE0	
	1	0	0	0	0	0	0	BS2	BS1	BS0	
32.Booster Level	0	0	0	1	0	1	0	0	0	1	Set booster level BST=0 : X8 BST=1 : X10
	1	0	1	1	1	1	1	0	1	BST	
33. Driving Select	0	0	0	1	0	0	0	0	0	DS	Power type DS=0: Internal (Default) DS=1 :External

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
34.Auto Read Control	0	0	1	1	0	1	0	1	1	1	Set auto-read instruction XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
35.OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR/RD	0	0	0	0	0	
36.OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
37.OTP Write	0	0	1	1	1	0	0	0	1	0	OTP write
38.OTP Read	0	0	1	1	1	0	0	0	1	1	OTP read
39.OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=1: Disable OTP Selection Ctrl=0: Enable OTP Selection
	1	0	1	Ctrl	0	1	1	0	0	1	
40.OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	1	1	1	1	
41.Frame Rate	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range
	1	0	0	0	0	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	0	0	0	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	0	0	0	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	0	0	0	FRD4	FRD3	FRD2	FRD1	FRD0	
42.Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
43.Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	1	1	1	1	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	
Ext[1:0]=1,1 (Extension Command 4)											
44.Enable OTP	0	0	1	1	0	1	0	1	1	0	Enable OTP EOTP =0 ; Disable (Default) EOTP =1 ; Enable
	1	0	0	0	0	EOTP	0	0	0	0	

6. Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.