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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic Display Module

Part Number

G12864I-FTW-DW63

Overview:

- 128x64 Graphic LCD
- FSTN Positive
- 76.00x48.50mm Module
- Parallel and SPI Interfaces
- White LED Backlight
- Transflective
- Wide Temp Range
- 3.0V
- LCD IC: ST7567
- RoHS Compliant

Graphic LCD Features

Resolution: 128x64 Dots
Interface(s): Parallel and SPI
RoHS Compliant.

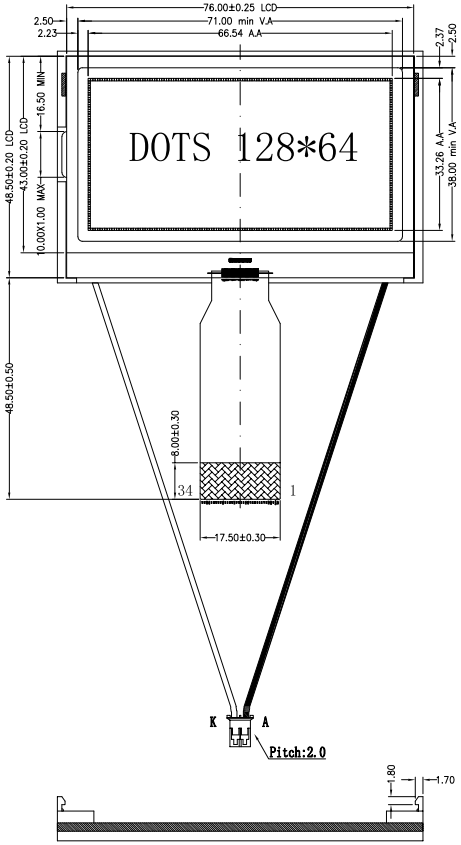
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	71.0 (H) x 38.0 (V)	mm	--
LCD Type	FSTN Positive	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transflective	--	--
Backlight Type	LED	--	--
Backlight Color	White	--	--
LCD IC	ST7567	--	--
Drive Mode	1/65 Duty, 1/9 Bias	--	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

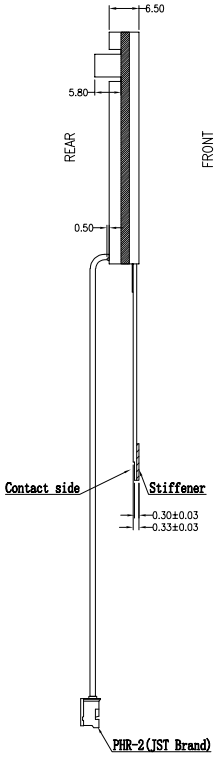
Mechanical Information

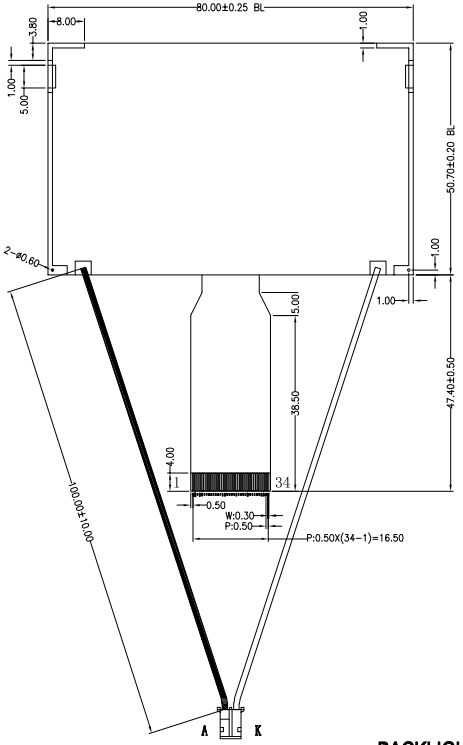
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	76.00	--	mm	--
	Vertical (V)	--	48.50	--	mm	--
	Depth (D)	--	6.50	--	mm	--
Weight		--	25.40	--	g	Approximate

1. Outline Dimensions

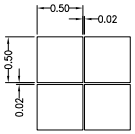
Rev.	Description	Date
1.0	First	2025.05.07



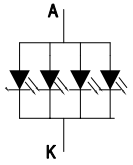




NO	PIN
1	CSB
2	RSTB
3	A0
4	RWR
5	ERD
6	D0
7	D1
8	D2
9	D3
10	D4
11	D5
12	D6
13	D7
14	VDD
15	VSS
16	NC
17	NC
18	NC
19	V0
20	XV0
21	NC
22	NC
23	NC
24	NC
25	VM0
26	NC
27	NC
28	NC
29	VG
30	NC
31	C86
32	PSB
33	NC
34	NC



BACKLIGHT CIRCUIT



NOTES:
1. DISPLAY TYPE: 128x64 FSTN GRAPHIC LCD
2. POLARIZER: TRANSFLECTIVE, POSITIVE MODE
3. VIEWING ANGLE: 6:00
4. OPERATING TEMPERATURE: -20°C TO +70°C
   STORAGE TEMPERATURE: -30°C TO +80°C
5. DRIVE METHOD: 1/65 DUTY, 1/9 BIAS, VDD 3.0V, VLCD 8.7V
6. LCD IC: ST7567
7. BACKLIGHT: WHITE LED, 4 LEDS, IF=60mA, VF=3.0V
8. ROHS COMPLIANT.

Model Name: G12864I-FTW-DW63		
General Tol: ±0.3		
Approvals	Date	
DWN:		
CHK:		
APP:		

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Drawing No.:		Scale:
Size:		Unit: mm / Page: 1/1

2. Input Terminal Pin Assignment

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>1</td><td>CSB</td><td>Chip select input pin. Interface access is enabled when CSB is “L”.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td>I</td></tr>
<tr><td>2</td><td>RSTB</td><td>Hardware reset input pin. When RSTB is “L”, internal initialization
is executed and the internal registers will be initialized.</td><td>I</td></tr>
<tr><td>3</td><td>A0</td><td>It determines whether the access is related to data or command.
A0=“H” : Indicates that signals on D[7:0] are display data.
A0=“L” : Indicates that signals on D[7:0] are command.</td><td>I</td></tr>
<tr><td>4</td><td>RWR</td><td>Read/Write execution control pin.
When PSB is “H”, RWR is not used in serial interface and should fix to “H” by VDD1 or VDDH.
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin.
R/W=”H”: read.
R/W=”L”: write.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table></td><td>I</td></tr>
<tr><td>5</td><td>ERD</td><td>Read/Write execution control pin.
When PSB is “H”, ERD is not used in serial interface and should fix to “H” by VDD1 or VDDH.
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table></td><td>I</td></tr>
<tr><td rowspan="2">6-13</td><td rowspan="2">D0-D7</td><td>When using 8-bit parallel interface: (6800 or 8080 mode) 8-bit bi-directional data bus.
Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td>I/O</td></tr>
<tr><td>When using serial interface: 4-LINE
D7=SDA : Serial data input. D6=SCL : Serial clock input. D[5:0] are not used and should connect to “H” by VDD1 or VDDH.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td>I</td></tr>
<tr><td>14</td><td>VDD</td><td>Power supply.</td><td>P</td></tr>
<tr><td>15</td><td>VSS</td><td>Ground.</td><td>P</td></tr>
<tr><td>16-18</td><td>NC</td><td>Not connected.</td><td>--</td></tr>
<tr><td>19</td><td>V0</td><td>V0 is the LCD driving voltage for common circuits at negative frame.</td><td>P</td></tr>
<tr><td>20</td><td>XV0</td><td>XV0 is the LCD driving voltage for common circuits at positive frame.</td><td>P</td></tr>
<tr><td>21-24</td><td>NC</td><td>Not connected.</td><td>--</td></tr>
<tr><td>25</td><td>VM0</td><td>VM is the LCD driving voltage for common circuits.</td><td>P</td></tr>
</table>

<table>
<tr><td>26-28</td><td>NC</td><td>Not connected.</td><td>--</td></tr>
<tr><td>29</td><td>VG</td><td>VG is the LCD driving voltage for segment circuits.</td><td>P</td></tr>
<tr><td>30</td><td>NC</td><td>Not connected.</td><td>--</td></tr>
<tr><td>31</td><td>C86</td><td>C86 selects the microprocessor type in parallel interface mode.
<table>
<tr><th>PSB</th><th>C86</th><th>Selected Interface</th></tr>
<tr><td>H</td><td>H</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>H</td><td>L</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>L</td><td>X</td><td>Serial 4-Line SPI Interface</td></tr>
</table></td><td>I</td></tr>
<tr><td>32</td><td>PSB</td><td>PSB selects the interface type: Serial or Parallel.</td><td>I</td></tr>
<tr><td>33-34</td><td>NC</td><td>Not connected.</td><td>--</td></tr>
</table>

I: Input, O: Output, P: Power

3. LCD Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit
Contrast Ratio		CR	--	--	5	--	--
Response Time	On	T_{on}	--	--	150	250	ms
	Off	T_{off}		--	180	300	ms
Viewing Angle $C_r \geq 2$, 25°C	Hor.	Θ_L	Φ=270°, 9H	--	55	--	degree
		Θ_R	Φ=90°, 3H	--	55	--	
	Ver.	Θ_T	Φ=180°, 12H	--	40	--	
		Θ_B	Φ=0°, 6H	--	70	--	

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	VDD	0.3	4.0	V
	Vout	0.3	16.0	V
Input Voltage	Vin	VSS-0.3	VDD+0.3	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
LCD Driving Voltage		VLCD	--	--	8.7	--	V
Supply Voltage		VDD	VDD-GND	--	3.0	--	V
Input Voltage	H Level	V_{IH}	--	0.7VDD	--	VDD	V
	L Level	V_{IL}	--	VSS	--	0.3VDD	V

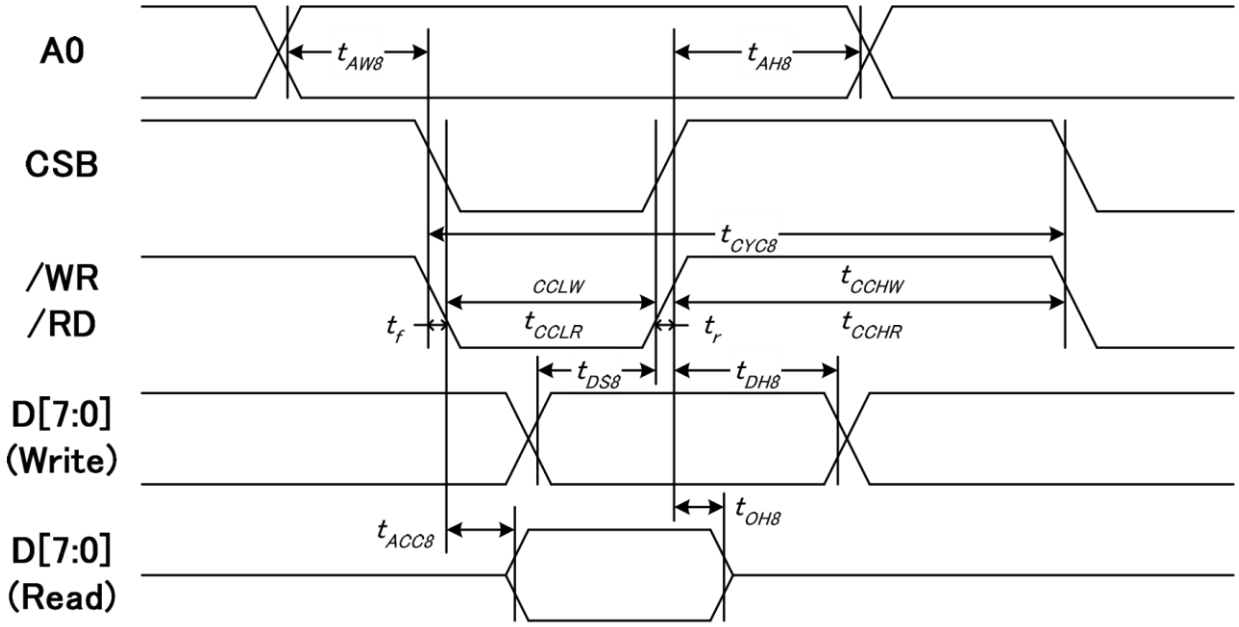
Condition:

1. VDD = 3.0V
2. 1/65 Duty, 1/9 Bias

5. Module Function

5.1 Timing Characteristics

System Bus Timing for 8080 MCU Interface



(VDD1=3.3V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		10	—	
System cycle time	/WR	t_{CYC8}		240	—	
/WR L pulse width (WRITE)		t_{CCLW}		80	—	
/WR H pulse width (WRITE)		t_{CCHW}		80	—	
/RD L pulse width (READ)	/RD	t_{CCLR}		140		
/RD H pulse width (READ)		t_{CCHR}		80		
WRITE data setup time	D[7:0]	t_{DS8}		40	—	
WRITE data hold time		t_{DH8}		20	—	
READ access time		t_{ACC8}	CL=16pF	—	70	
READ output disable time		t_{OH8}	CL=16pF	5	50	

System Bus Timing for 8080 MCU Interface (continued)

(VDD1=2.8V, Ta=25°C)

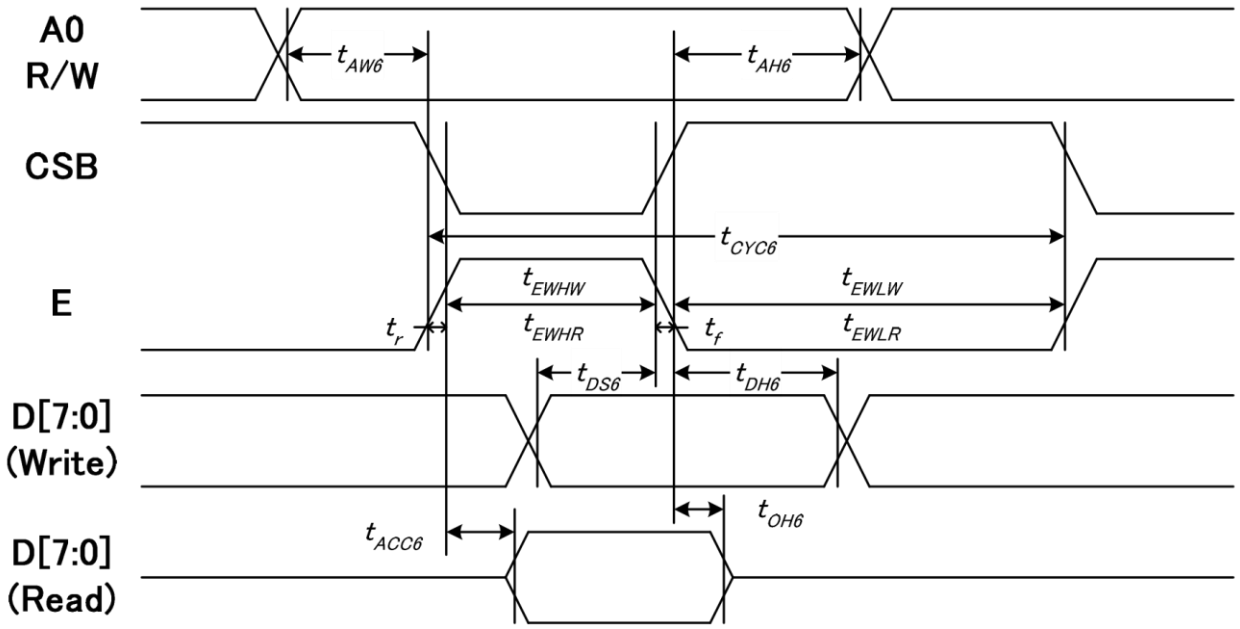
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time	/WR	t_{CYC8}		400	—	
/WR L pulse width (WRITE)		t_{CCLW}		220	—	
/WR H pulse width (WRITE)		t_{CCHW}		180	—	
/RD L pulse width (READ)	/RD	t_{CCLR}		220		
/RD H pulse width (READ)		t_{CCHR}		180		
WRITE data setup time	D[7:0]	t_{DS8}		40	—	
WRITE data hold time		t_{DH8}		20	—	
READ access time		t_{ACC8}	CL=16pF	—	140	
READ output disable time		t_{OH8}	CL=16pF	10	100	

(VDD1=1.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW8}		0	—	ns
Address hold time		t_{AH8}		0	—	
System cycle time	/WR	t_{CYC8}		640	—	
/WR L pulse width (WRITE)		t_{CCLW}		360	—	
/WR H pulse width (WRITE)		t_{CCHW}		280	—	
/RD L pulse width (READ)	/RD	t_{CCLR}		360		
/RD H pulse width (READ)		t_{CCHR}		280		
WRITE data setup time	D[7:0]	t_{DS8}		80	—	
WRITE data hold time		t_{DH8}		20	—	
READ access time		t_{ACC8}	CL=16pF	—	240	
READ output disable time		t_{OH8}	CL=16pF	10	200	

Note:
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2. All timing is specified using 20% and 80% of VDD1 as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Timing for 6800 MCU Interface



(VDD=3.3V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW6}		0	—	ns
Address hold time		t_{AH6}		10	—	
System cycle time	E	t_{CYC6}		240	—	
Enable L pulse width (WRITE)		t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)		t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
Write data setup time	D[7:0]	t_{DS6}		40	—	
Write data hold time		t_{DH6}		10	—	
Read data access time		t_{ACC6}	CL=16pF	—	70	
Read data output disable time		t_{OH6}	CL=16pF	5	50	

System Bus Timing for 6800 MCU Interface (continued)

(VDD=2.8V, Ta=25°C)

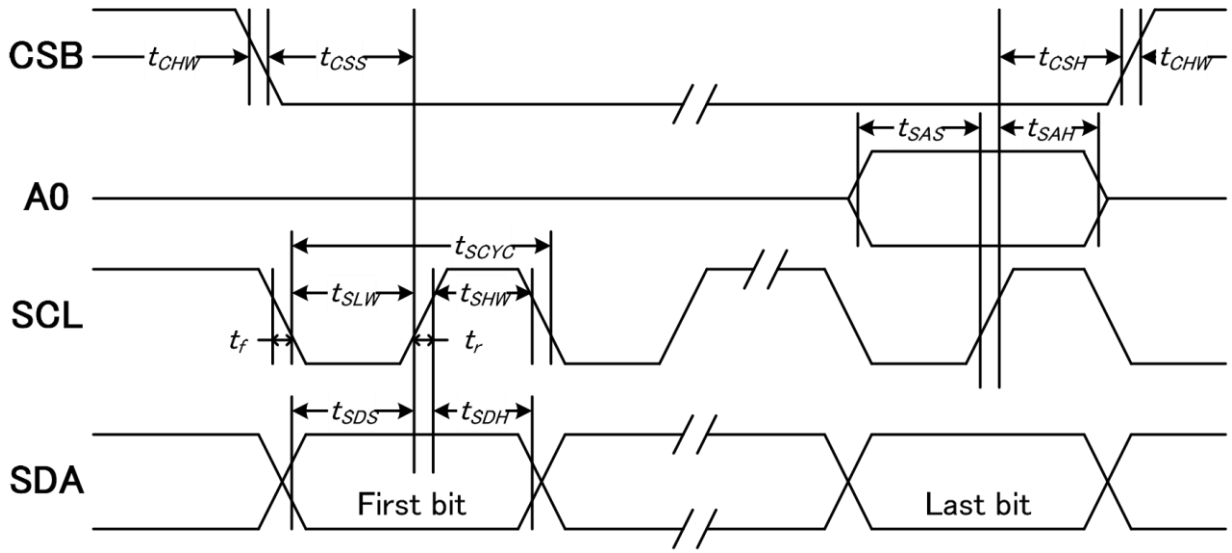
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW6}		0	—	ns
Address hold time		t_{AH6}		0	—	
System cycle time	E	t_{CYC6}		400	—	
Enable L pulse width (WRITE)		t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)		t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180		
Write data setup time	D[7:0]	t_{DS6}		40	—	
Write data hold time		t_{DH6}		20	—	
Read data access time		t_{ACC6}	CL=16pF	—	140	
Read data output disable time		t_{OH6}	CL=16pF	10	100	

(VDD=1.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address setup time	A0	t_{AW6}		0	—	ns
Address hold time		t_{AH6}		0	—	
System cycle time	E	t_{CYC6}		640	—	
Enable L pulse width (WRITE)		t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)		t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280		
Write data setup time	D[7:0]	t_{DS6}		80	—	
Write data hold time		t_{DH6}		20	—	
Read data access time		t_{ACC6}	CL=16pF	—	240	
Read data output disable time		t_{OH6}	CL=16pF	10	200	

Note:
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2. All timing is specified using 20% and 80% of VDD1 as the reference.
*3. t_{EWLW} and t_{EWLR} are specified as the overlap between CSB being “L” and E.

System Bus Timing for 4-Line SPI MCU Interface



(VDD=3.3V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCLK	t_{SCYC}		50	—	ns
SCLK “H” pulse width		t_{SHW}		25	—	
SCLK “L” pulse width		t_{SLW}		25	—	
Address setup time	A0	t_{SAS}		20	—	
Address hold time		t_{SAH}		10	—	
Data setup time	SDA	t_{SDS}		20	—	
Data hold time		t_{SDH}		10	—	
CSB-SCLK time	CSB	t_{CSS}		20	—	
CSB-SCLK time		t_{CSH}		40	—	

(VDD=2.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCLK	t_{SCYC}		100	—	ns
SCLK “H” pulse width		t_{SHW}		50	—	
SCLK “L” pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		30	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SDA	t_{SDS}		30	—	
Data hold time		t_{SDH}		20	—	
CSB-SCLK time	CSB	t_{CSS}		30	—	
CSB-SCLK time		t_{CSH}		60	—	

System Bus Timing for 4-Line SPI MCU Interface (continued)

(VDD=1.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCLK	t_{SCYC}		200	—	ns
SCLK “H” pulse width		t_{SHW}		80	—	
SCLK “L” pulse width		t_{SLW}		80	—	
Address setup time	A0	t_{SAS}		60	—	
Address hold time		t_{SAH}		30	—	
Data setup time	SDA	t_{SDS}		60	—	
Data hold time		t_{SDH}		30	—	
CSB-SCLK time	CSB	t_{CSS}		40	—	
CSB-SCLK time		t_{CSH}		100	—	

Note:

*1. The input signal rise time and fall time (t_r, t_f) are specified as 15ns or less.

*2. All timing is specified using 20% and 80% of VDD1 as the standard.

5.2 LCM Application

Please see information on pages 43-45 of the data sheet for LCD controller ST7567. The data sheet can be found here: https://focuslcds.com/wp-content/uploads/Drivers/ST7567.pdf

5.3 Command Table

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4) Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Test	0	0	1	1	1	1	1	1	1	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

5.4 Initialization Code

```
Void lcd_init(void)
      {
RES=1;
delays(10);
 RES=0;
 delays(10);
 RES=1;
 delays(50);
          writecommand(0xE2);
 delay(10);
          writecommand(0xA2);//0xa2
          writecommand(0xA0);//0xa0
          writecommand(0xC0);//0xc0
          writecommand(0x24);//vop
          writecommand(0x81);//vop
          writecommand(0x23);//vop
          writecommand(0x2F);//0x2f
          writecommand(0xB0);//0xb0
          writecommand(0xAF);//0xaf
          ritecommand(0xA6);//0xa6
}
```

6. Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.