Ph. 480-503-4295 | LCD@FocusLCDs.com

TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic OLED Module

Part Number

O12864A-GLB-YW3

Overview:

- 128x64 Graphic OLED
- Blue Pixel Color
- 26.70x19.26mm Module
- 6800/8080 Parallel, 3/4-Wire SPI, I2C Interfaces
- Anti-glare Polarizer
- Wide Temp Range
- 2.8V
- LCD IC: SSD1306
- RoHS Compliant

Graphic OLED LCD Features

Resolution: 128x64 Dots
Interface(s): 6800/8080 Parallel, 3/4-Wire SPI, I2C
RoHS Compliant

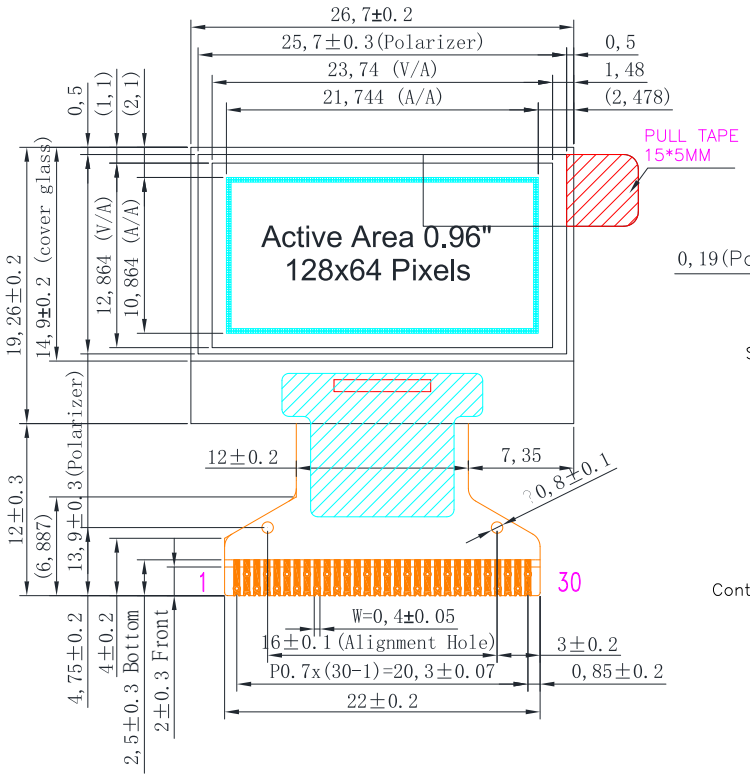
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	23.74 (H) x 12.86 (V)	mm	--
Pixel Color	Blue	--	--
Viewing Angle	All	degrees	--
Polarizer	Anti-glare	--	--
Controller IC	SSD1306	--	--
Operating Temperature	-40 to +70	°C	--
Storage Temperature	-40 to +85	°C	--
Voltage	2.8	V	--
Resolution	128x64	--	--

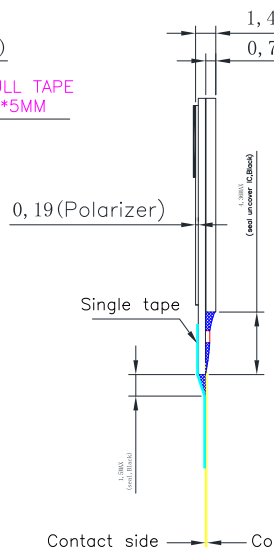
Mechanical Information

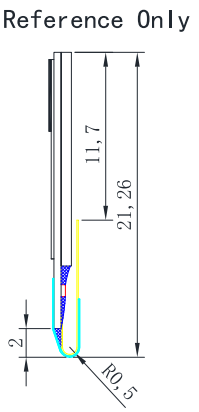
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	26.70	--	mm	--
	Vertical (V)	--	19.26	--	mm	--
	Depth (D)	--	1.41	--	mm	--
Weight		--	1.5	--	g	Approximate

1. Outline Dimensions

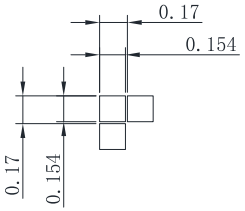
Rev.	Description	Date
1.0	First	2017.08.26

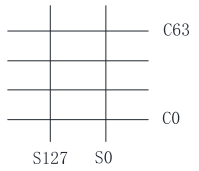






NO	PIN
1	NC(GND)
2	C2P
3	C2N
4	C1P
5	C1N
6	VBAT
7	NC
8	VSS
9	VDD
10	BS0
11	BS1
12	BS2
13	CS#
14	RES#
15	D/C#
16	R/W#
17	E/RD#
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	VCOMH
28	VCC
29	VLSS
30	NC(GND)





NOTES:
1. DISPLAY TYPE: 128x64 WHITE GRAPHIC OLED
2. POLARIZER: ANTI-GLARE
3. VIEWING ANGLE: ALL VIEW
4. OPERATING TEMPERATURE: -40°C TO +70°C
   STORAGE TEMPERATURE: -40°C TO +85°C
5. CONTROLLER IC: SSD1306
6. ROHS COMPLIANT.

Model Name: O12864A-GLB-YW3			
General Tol: ±0.3			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm
APP:			Page: 1/1

2. Input Terminal Pin Assignment

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>Reserved pin. It should be connected to VSS.</td><td>--</td></tr>
<tr><td>2</td><td>C2P</td><td rowspan="4">C1P/C1N - Pin for charge pump capacitor.
C2P/C2N - Pin for charge pump capacitor.
Connect to each other with a capacitor.
They must be floated when the charge pump not use.</td><td rowspan="4">I</td></tr>
<tr><td>3</td><td>C2N</td></tr>
<tr><td>4</td><td>C1P</td></tr>
<tr><td>5</td><td>C1N</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power supply for charge pump regulator circuit.
It must be connected to external source when charge pump is used.
It must be float when charge pump is not used.</td><td>P</td></tr>
<tr><td>7</td><td>NC</td><td>No connection.</td><td>--</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td><td>P</td></tr>
<tr><td>9</td><td>VDD</td><td>Power supply pin for core logic operation.</td><td>P</td></tr>
<tr><td>10</td><td>BS0</td><td rowspan="3">MCU bus interface pin selection
<table>
<tr><th>BS0</th><th>BS1</th><th>BS2</th><th>MPU Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>4-wire serial interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>6800-parallel interface (8 bit)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I2C interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080-parallel interface (8 bit)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>3-wire serial interface</td></tr>
</table></td><td rowspan="3">I</td></tr>
<tr><td>11</td><td>BS1</td></tr>
<tr><td>12</td><td>BS2</td></tr>
<tr><td>13</td><td>CS#</td><td>Chip select input pin. Active “L”.</td><td>I</td></tr>
<tr><td>14</td><td>RES#</td><td>Hardware reset input pin. Active “L”.</td><td>I</td></tr>
<tr><td>15</td><td>D/C#</td><td>This is Data/Command control pin.
When the pin is pulled HIGH, the data at D[7:0] is data.
When the pin is pulled LOW, the data at D[7:0] is command.
In I2C mode, this pin acts as SA0 for slave address section.
When 3-wire serial interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>16</td><td>R/W#</td><td>This is Read/Write control input pin.
8080: data write enable; 6800: read/write select pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>17</td><td>E/RD#</td><td>This is Read/write control input pin.
8080: data read enable; 6800: read/write enable pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>18-25</td><td>D0~D7</td><td>These are 8-bit bi-directional data bus to be connected to microprocessor’s data bus.
When serial interface mode is selected, D2 should be kept NC, D1 will be the serial data input: SDIN, D0 will be the serial clock input: SCLK.
When I2C mode is selected, D2, D1 should be tied together and serve as SDA and D0 is the serial clock input: SCL.</td><td>I/O</td></tr>
<tr><td>26</td><td>IREF</td><td>Current reference for brightness adjustment.
This is segment output current reference pin.
A resistor should be connected between this pin and VSS.
Set the current at 12.5 uA maximum.</td><td>I</td></tr>
<tr><td>27</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.</td><td>O</td></tr>
<tr><td>28</td><td>VCC</td><td>Power supply for OLED driving voltage.
A capacitor should be connected between this pin and VSS, when charge pump is used.
It must be connected to external source when charge pump is not used.</td><td>P</td></tr>
<tr><td>29</td><td>VLSS</td><td>This is an analog ground pin. It should be connected to VSS externally.</td><td>P</td></tr>
<tr><td>30</td><td>NC(GND)</td><td>Reserved pin. It should be connected to VSS.</td><td>--</td></tr>
</table>

I: Input, O: Output, P: Power

3. OLED Optical Characteristics

Parameter	Min	Typ.	Max	Units	Comments
Normal Mode Current (IBAT) (Charge Pump)	--	26	32	mA	All pixels on (1)
	--	9	15	mA	20% Pixels on (1)
Standby Mode Current (IBAT) (Charge Pump)	--	4.5	5	mA	Standby mode 10% pixels on (2)
IDD Sleep Mode Current	--	--	10	µA	Sleep mode current (3)
IBAT Sleep Mode Current (Charge Pump)	--	-	10	µA	Sleep mode current (3)
Normal Luminance (Charge Pump)	80	105	--	cd/m²	Display average
Standby Luminance (Charge Pump)	90	--	--	cd/m²	Display average
CIEx (White)	0.10	0.14	0.18	--	x,y (CIE 1931)
CIEy (White)	0.20	0.24	0.28	--	
Dark Room Contrast	2000:1	--	--	--	--
Viewing Angle	160	--	--	degrees	--
Response Time	--	10	--	µs	--

***(1)** Normal mode condition:*
(charge pump) VBAT =3.6V; Contrast setting: 0x66, Frame rate: 105Hz, Duty setting: 1/64.
***(2)** Standby mode condition:*
(charge pump) VBAT =3.6V; Contrast setting: 0x00, Frame rate: 105Hz, Duty setting: 1/64.
***(3)** Sleep mode condition:*
When send 0xae command OLED display off and memory data will be maintained.
***(4)** Wake up condition:*
When send 0xaf commend OLED will be turned on.

4. Electrical Characteristics

4.1 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Logic Supply Voltage		VDD	Ta=25°C	1.65	--	3.3	V
Charge Pump Regulator Supply Voltage		VBAT	Ta=25°C	3.5	--	4.2	V
Operating Voltage (For Panel) (Charge Pump)		VCC	Ta=25°C	7.0	7.5	--	V
Input Voltage	H Level	V_{IH}	--	0.8*VDD	--	--	V
	L Level	V_{IL}	--	--	--	0.2*VDD	V
Output Voltage	H Level	V_{OH}	I_{OUT} =100µA 3.3MHz	0.9*VDD	--	--	V
	L Level	V_{OL}	I_{OUT} =100µA 3.3MHz	--	---	0.1*VDD	V

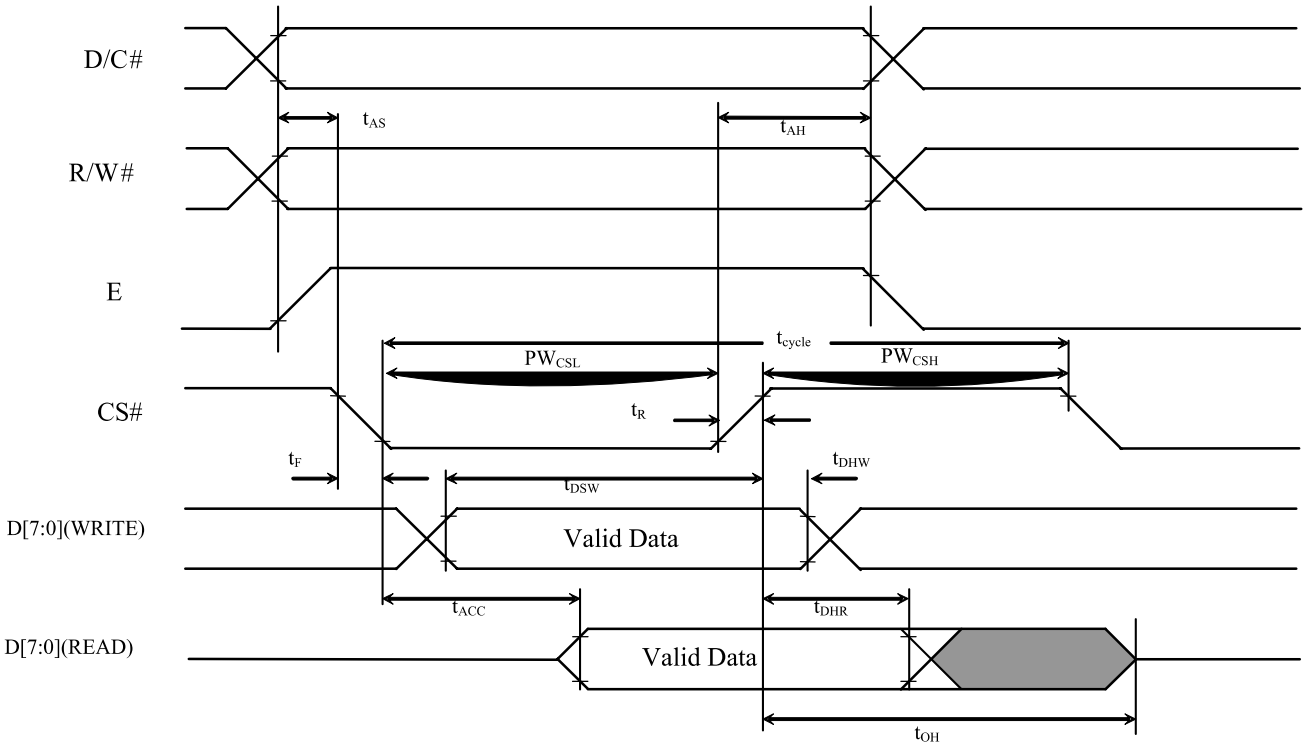
5. Module Function

5.1 Timing Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	0	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	7	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	PW_{CSL}	120	--	--	ns
Chip Select Low Pulse Width (write)		60	--	--	ns
Chip Select High Pulse Width (read)	PW_{CSH}	60	--	--	ns
Chip Select High Pulse Width (write)		60	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns

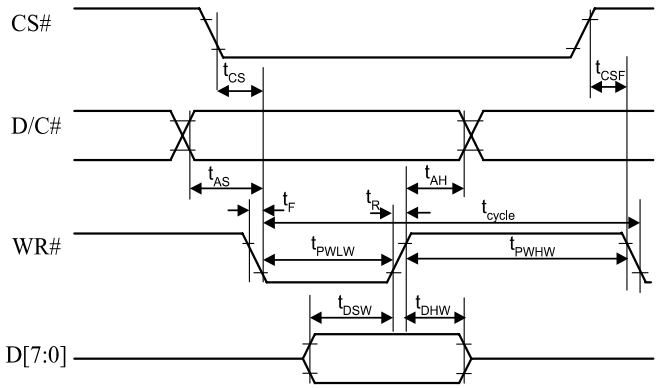


8080-Series MCU Parallel Interface Timing Characteristics

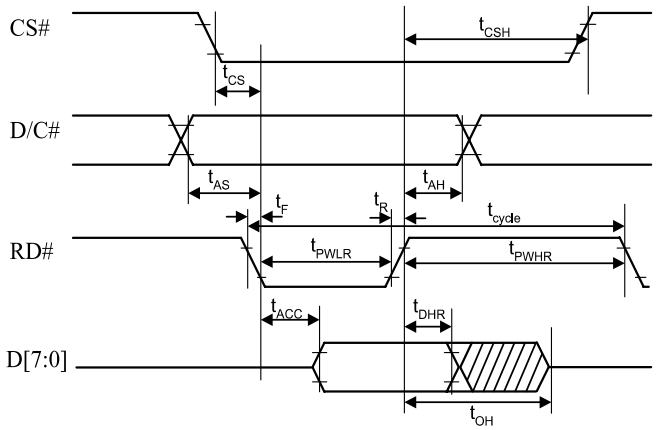
(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	10	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	7	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	t_{PWLR}	120	--	--	ns
Chip Select Low Pulse Width (write)	t_{PWLW}	60	--	--	ns
Chip Select High Pulse Width (read)	t_{PWHR}	60	--	--	ns
Chip Select High Pulse Width (write)	t_{PWHW}	60	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns
Chip Select Setup Time	t_{CS}	0	--	--	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	--	--	ns
Chip Select Hold Time	t_{CSF}	20	--	--	ns

Write Cycle



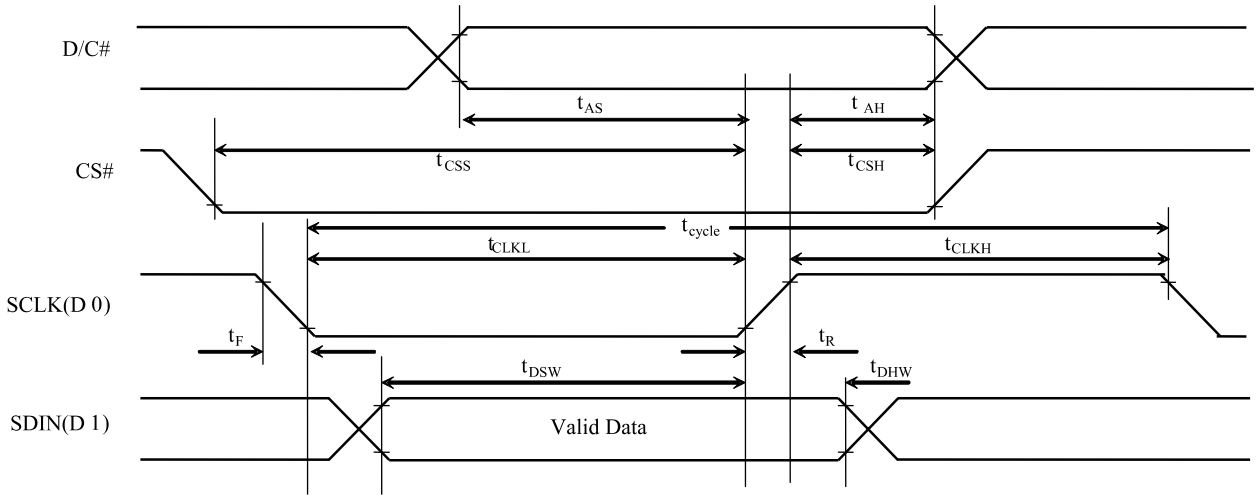
Read cycle

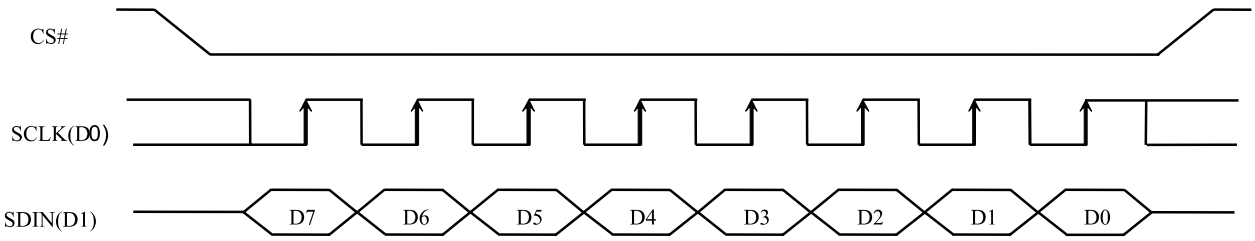


4-wire Serial Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Address Setup Time	t_{AS}	15	--	--	ns
Address Hold Time	t_{AH}	15	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	10	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	20	--	--	ns
Clock High Time	t_{CLKH}	20	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns

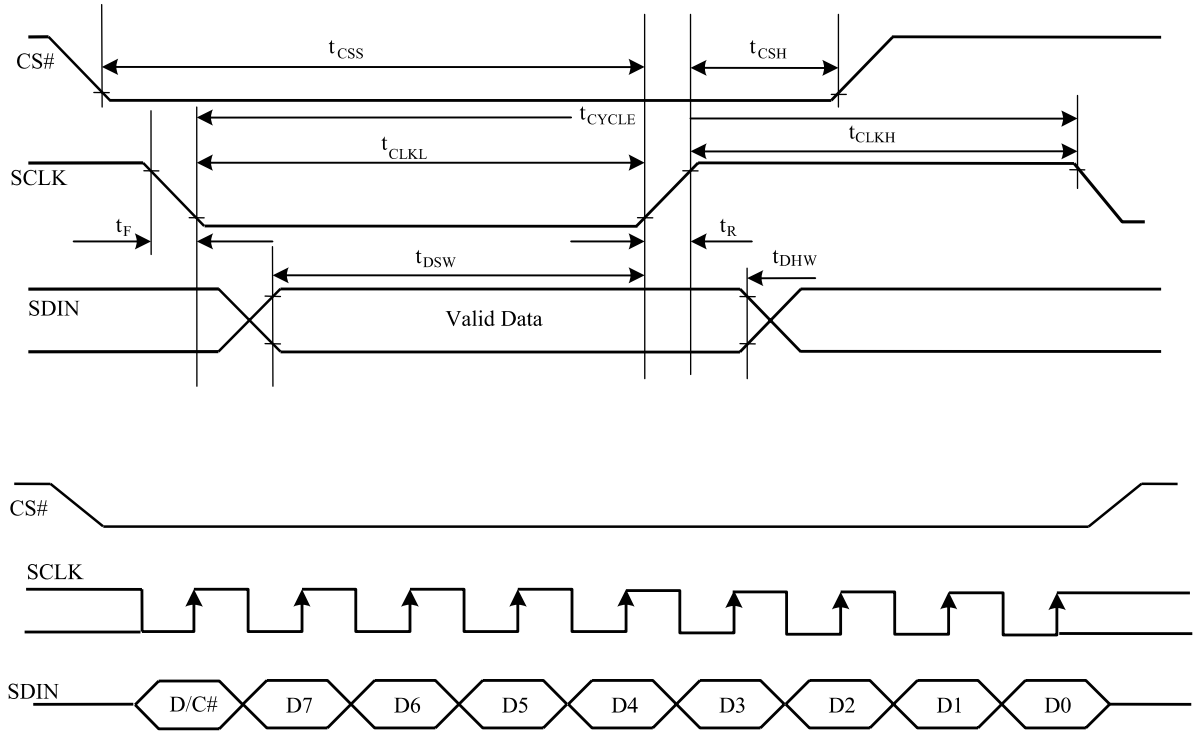




3-wire Serial Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

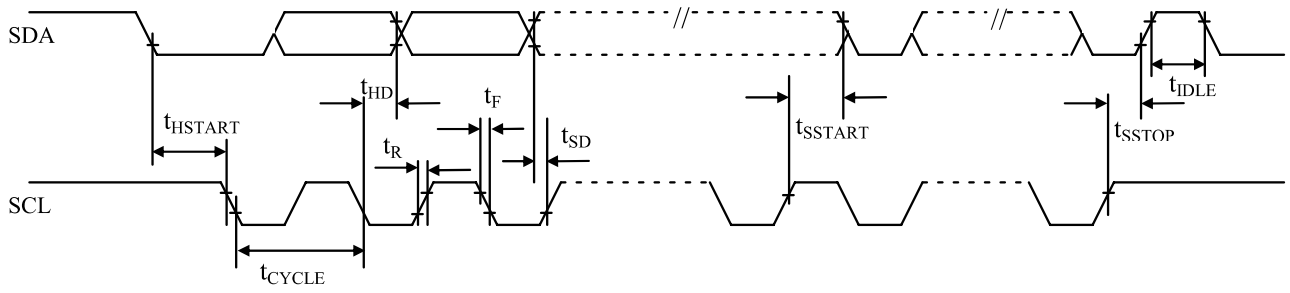
Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	10	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	20	--	--	ns
Clock High Time	t_{CLKH}	20	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns



I2C interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	2.5	--	--	µs
Start Condition Hold Time	t_{HSTART}	0.6	--	--	µs
Data Hold Time (for “SDAOUT” pin)	t_{DH}	0	--	--	ns
Data Hold Time (for “SDAIN” pin)		300	--	--	ns
Data Setup Time	t_{SD}	100	--	--	ns
Start Condition Setup Time (Only relevant for a repeated start condition)	t_{SSTART}	0.6	--	--	µs
Stop Condition Setup Time	t_{SSTOP}	0.6	--	--	µs
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns
Idle Time Before A New Transmission Can Start	t_{IDLE}	1.3	--	--	µs



5.2 LCM Application

Please see information on page 55 of the data sheet for OLED controller SSD1306. The data sheet can be found here: https://focuslcds.com/wp-content/uploads/Drivers/SSD1306.pdf

5.3 Command Table

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0 0 0	26/27 A[7:0] B[2:0] C[2:0] D[2:0] E[7:0] F[7:0]	0 0 * * * 0 1	0 0 * * * 0 1	1 0 * * * 0 1	0 0 * * * 0 1	0 0 * * * 0 1	1 0 B_2 C_2 D_2 0 1	1 0 B_1 C_1 D_1 0 1	X_0 0 B_0 C_0 D_0 0 1	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0
0
0
0
0</td><td>29/2A
A[2:0]
B[2:0]
C[2:0]
D[2:0]
E[5:0]</td><td>0
0
*
*
*
*</td><td>0
0
*
*
*
*</td><td>1
0
*
*
*
E_5</td><td>0
0
*
*
*
E_4</td><td>1
0
*
*
*
E_3</td><td>0
0
B_2
C_2
D_2
E_2</td><td>X_1
0
B_1
C_1
D_1
E_1</td><td>X_0
0
B_0
C_0
D_0
E_0</td><td>Continuous Vertical and Horizontal Scroll Setup</td><td>29h, X1X0=01b : Vertical and Right Horizontal Scroll
2Ah, X1X0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column)
A[7:0] : Dummy byte

B[2:0] : Define start page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency<table><tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr><tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr></table>
D[2:0] : Define end page address<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>The value of D[2:0] must be larger or equal to B[2:0]

E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =3Fh refer to offset =63 rows

Note
(1) No continuous vertical scrolling is available.</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate Scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
<tr><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Activate Scroll</td><td>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:

Valid command sequence 1: 26h ;2Fh.
Valid command sequence 2: 27h ;2Fh.
Valid command sequence 3: 29h ;2Fh.
Valid command sequence 4: 2Ah ;2Fh.

For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</td></tr>
</table>

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) Note (1) This command is only for horizontal or vertical addressing mode.

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) Note (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. Note (1) This command is only for page addressing mode

4. Hardware Configuration (Panel Resolution & Layout Related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET). A1h, X[0]=1b: column address 127 is mapped to SEG0.
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX). A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1]. C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0. Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d. The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration.

5. Timing & Driving Scheme Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1). A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b. Range:0000b~1111b. Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-Charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h). A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h).
0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	A[6:4] / Hex code / V COMH deselect level 000b / 00h / ~ 0.65 x VCC 010b / 20h / ~ 0.77 x VCC (RESET) 011b / 30h / ~ 0.83 x VCC
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation.

Note

(1) "" stands for "Don't care".*

6. Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.