Ph. 480-503-4295 | LCD@FocusLCDs.com

TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic OLED Module

Part Number

O12864C-GW-YW3

Overview:

- 128x64 Graphic OLED
- White Pixel Color
- 42.04x27.22mm Module
- 6800/8080 Parallel, 3/4-Wire SPI, I2C Interfaces
- Anti-glare Polarizer
- Wide Temp Range
- 2.8V
- LCD IC: SSD1309Z
- RoHS Compliant

Graphic OLED LCD Features

Resolution: 128x64 Dots
Interface(s): 6800/8080 Parallel, 3/4-Wire SPI, I2C
RoHS Compliant

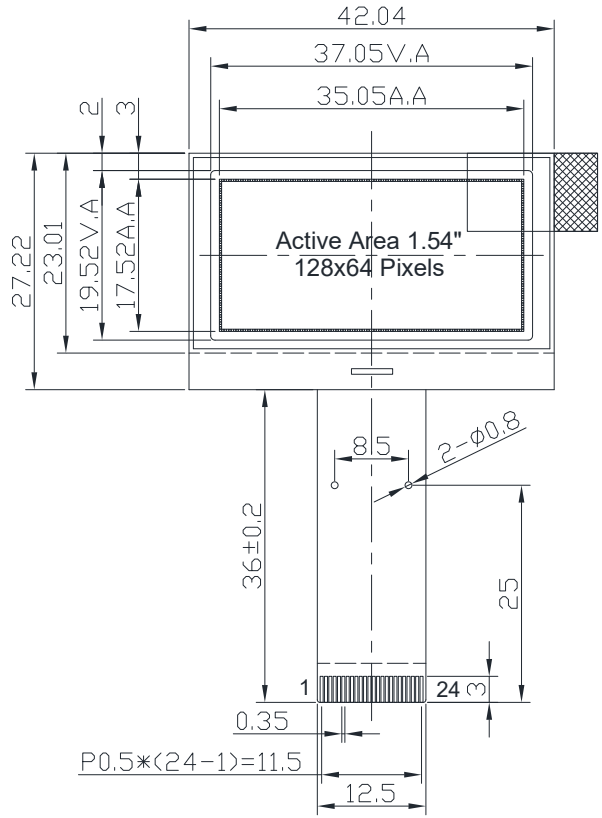
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	37.50 (H) x 19.52 (V)	mm	--
Pixel Color	White	--	--
Viewing Angle	All	degrees	--
Polarizer	Anti-glare	--	--
Controller IC	SSD1309Z	--	--
Operating Temperature	-40 to +70	°C	--
Storage Temperature	-40 to +85	°C	--
Voltage	2.8	V	--
Resolution	128x64	--	--

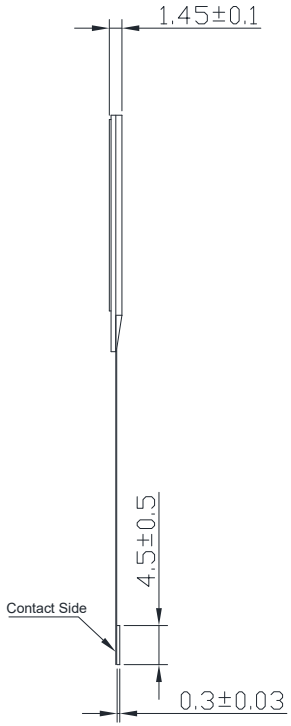
Mechanical Information

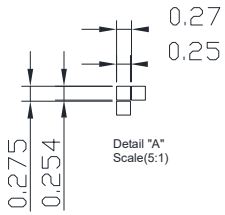
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	42.04	--	mm	--
	Vertical (V)	--	27.22	--	mm	--
	Depth (D)	--	1.45	--	mm	--
Weight		--	3.35	--	g	Approximate

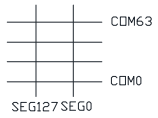
1. Outline Dimensions

Rev.	Description	Date
1.0	First	2017.08.26









COM & SEG LAYOUT

NO	PIN
1	NC(GND)
2	VLSS
3	VSS
4	NC
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	R/W#
12	E/RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	NC(GND)

NOTES:
1. DISPLAY TYPE: 128x64 WHITE GRAPHIC OLED
2. POLARIZER: ANTI-GLARE
3. VIEWING ANGLE: ALL VIEW
4. OPERATING TEMPERATURE: -40°C TO +70°C
   STORAGE TEMPERATURE: -40°C TO +85°C
5. CONTROLLER IC: SSD1309Z
6. ROHS COMPLIANT.

Model Name: O12864A-GW-YW3		FOCUS LCDs LCDs MADE SIMPLE®	
General Tol: ±0.3			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm / Page: 1/1
APP:			

2. Input Terminal Pin Assignment

<table>
<tr><th>NO.</th><th>Symbol</th><th>Description</th><th>I/O</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>Reserved pin. It should be connected to VSS.</td><td>--</td></tr>
<tr><td>2</td><td>VLSS</td><td>This is an analog ground pin. It should be connected to VSS externally.</td><td>P</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td><td>P</td></tr>
<tr><td>4</td><td>NC</td><td>No connection.</td><td>--</td></tr>
<tr><td>5</td><td>VDD</td><td>Power supply pin for core logic operation.</td><td>P</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">MCU bus interface pin selection<table><tr><th>BS1</th><th>BS2</th><th>MPU Interface Mode</th></tr><tr><td>0</td><td>0</td><td>4-wire serial interface</td></tr><tr><td>0</td><td>1</td><td>6800-parallel interface (8 bit)</td></tr><tr><td>1</td><td>0</td><td>I2C interface</td></tr><tr><td>1</td><td>1</td><td>8080-parallel interface (8 bit)</td></tr></table></td><td rowspan="2">I</td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>Chip select input pin. Active “L”.</td><td>I</td></tr>
<tr><td>9</td><td>RES#</td><td>Hardware reset input pin. Active “L”.</td><td>I</td></tr>
<tr><td>10</td><td>D/C#</td><td>This is Data/Command control pin.
When the pin is pulled HIGH, the data at D[7:0] is data.
When the pin is pulled LOW, the data at D[7:0] is command.
In I2C mode, this pin acts as SA0 for slave address section.
When 3-wire serial interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>11</td><td>R/W#</td><td>This is Read/Write control input pin.
8080: data write enable; 6800: read/write select pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>12</td><td>E/RD#</td><td>This is Read/write control input pin.
8080: data read enable; 6800: read/write enable pin.
When serial or I2C interface is selected, this pin must be connected to VSS.</td><td>I</td></tr>
<tr><td>13-20</td><td>D0~D7</td><td>These are 8-bit bi-directional data bus to be connected to microprocessor’s data bus.
When serial interface mode is selected, D2 should be kept NC, D1 will be the serial data input: SDIN, D0 will be the serial clock input: SCLK.
When I2C mode is selected, D2, D1 should be tied together and serve as SDA and D0 is the serial clock input: SCL.</td><td>I/O</td></tr>
<tr><td>21</td><td>IREF</td><td>Current reference for brightness adjustment.
This is segment output current reference pin.
A resistor should be connected between this pin and VSS.
Set the current at 12.5 uA maximum.</td><td>I</td></tr>
<tr><td>22</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.</td><td>P</td></tr>
<tr><td>23</td><td>VCC</td><td>Power supply for OLED driving voltage.
A capacitor should be connected between this pin and VSS, when charge pump is used.
It must be connected to external source when charge pump is not used.</td><td>P</td></tr>
<tr><td>24</td><td>NC(GND)</td><td>Reserved pin. It should be connected to VSS.</td><td>--</td></tr>
</table>

I: Input, O: Output, P: Power

3. Electrical Characteristics

3.2 DC Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Supply Voltage for Display	VCC		12	12.5	13	V
High Level Input	VIH		0.8*VDD	--	--	V
Low Level Input	VIL		--	--	0.2*VDD	V
High Level Output	VOH	IOUT = 100μA, 3.3MHz	0.9*VDD	--	--	V
Low Level Output	VOL	IOUT = 100μA, 3.3MHz	--	--	0.1*VDD	V
VDD Supply Current VDD =2.8V, VCC = 12, IREF = 10uA , No Panel attached, Display ON, All ON,	IDD	Contrast = 0xFFh	--	90	110	uA
VCC Supply Current VDD = 2.8V, VCC =12, IREF =10uA, No Panel attached, Display ON, All ON	ICC		--	450	580	uA
Segment Output Current, VDD = 2.8V, VCC =12V, IREF=10uA, Display ON.	ISEG	Contrast = 0xFFh	280	310	340	uA
		Contrast = 0xAFh	--	215	--	
		Contrast = 0x7Fh	--	155	--	
		Contrast = 0x3Fh	--	78	--	
		Contrast = 0x0Fh	20	--	--	
Sleep Mode Current for VDD	IDD,SLEEP	VDD = 1.65V~3.3V, VCC = 7V~16V Display OFF, No panel attached	--	--	10	uA
Sleep Mode Current for VCC	ICC SLEEP	VDD = 1.65V~3.3V, VCC = 7V~16V Display OFF, No panel attached	--	--	10	uA

3.2 Electrical Specifications

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Normal Mode Current Consumption		All pixels on	1	17	25	mA
Standby Mode Current Consumption		Standby mode 10% pixels on	--	0.5	1.5	mA
Normal Mode Power Consumption		All pixels on	--	71.5	97.5	mW
Standby Mode Power Consumption		Standby mode 10% pixels on	--	6.5	19.5	mW
Brightness	Lbr	--	90	110	--	Cd/m²
C.I.E. (White)	(X),(Y)	C.I.E. 1931	0.24 0.28	0.28 0.32	0.32 0.36	
Dark Room Contrast	CR	--	2000:1	--	--	
Viewing Angle		--	160	--	--	degree

Note:
VDD is 2.8V,set VDD selection (0xad)=(0x40),
VDD is 1.8V,set VDD selection (0xad)=(0x60) contrast setting is shown below.
***(1)** Normal mode condition:*
-Driving Voltage : 12V
-Contrast setting : 0x3e
-Frame rate : 105Hz
-Duty setting : 1/64
***(2)** Standby mode condition:*
-Driving Voltage : 12V
-Contrast setting : 0x00
-Frame rate : 105Hz
-Duty setting : 1/64

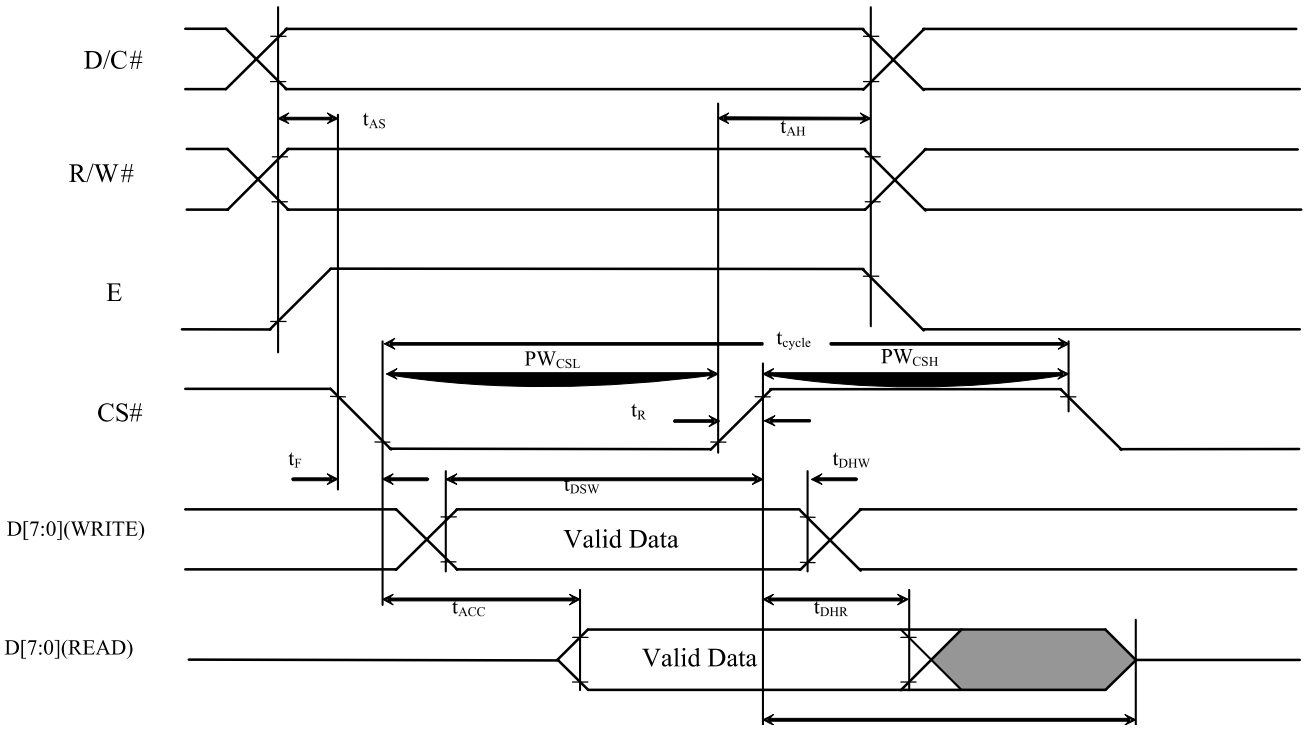
4. Module Function

4.1 Timing Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	20	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Data Write Time	t_{DW}	80	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	20	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	PW_{CSL}	120	--	--	ns
Chip Select Low Pulse Width (write)		60	--	--	ns
Chip Select High Pulse Width (read)	PW_{CSH}	60	--	--	ns
Chip Select High Pulse Width (write)		60	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns

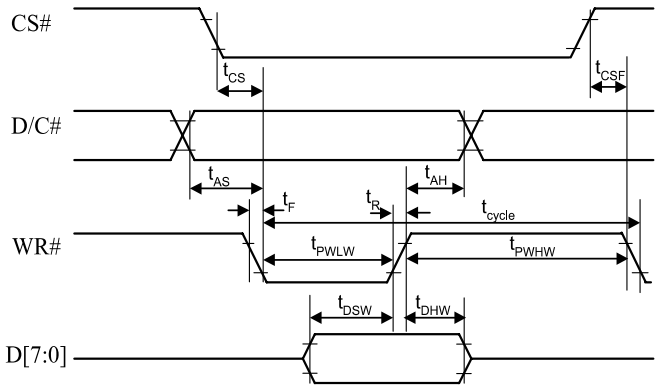


8080-Series MCU Parallel Interface Timing Characteristics

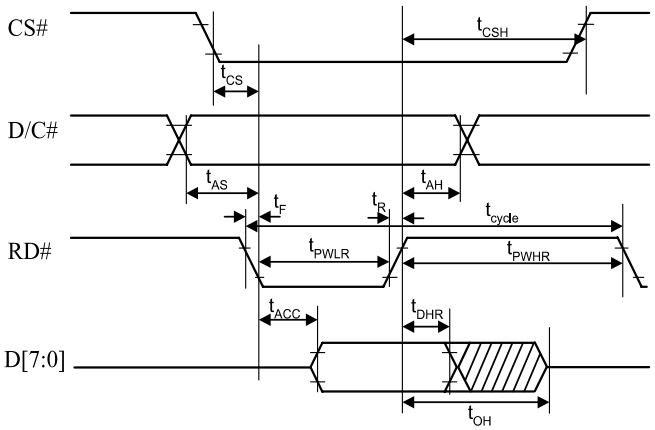
(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	10	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Data Write Time	t_{DW}	70	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	t_{PWLR}	120	--	--	ns
Chip Select Low Pulse Width (write)	t_{PWLW}	60	--	--	ns
Chip Select High Pulse Width (read)	t_{PWHR}	60	--	--	ns
Chip Select High Pulse Width (write)	t_{PWHW}	60	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns
Chip Select Setup Time	t_{CS}	0	--	--	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	--	--	ns
Chip Select Hold Time	t_{CSF}	20	--	--	ns

Write Cycle



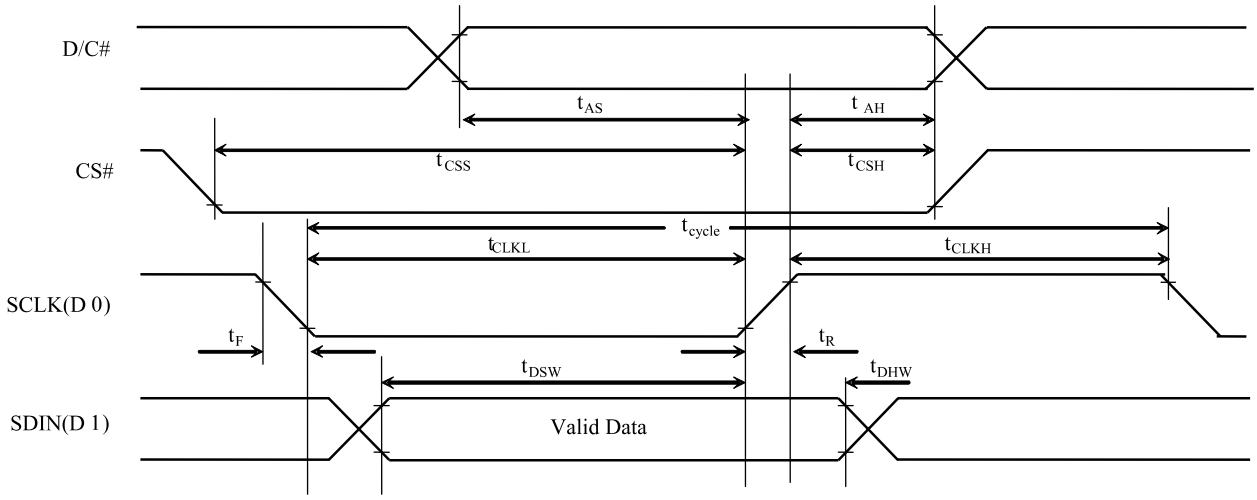
Read cycle

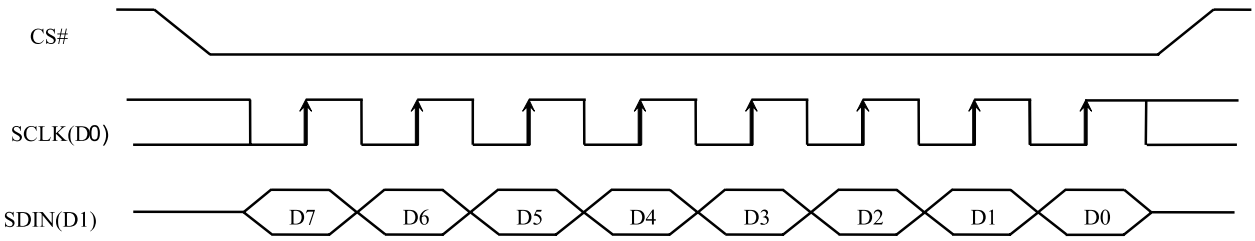


4-wire Serial Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Address Setup Time	t_{AS}	15	--	--	ns
Address Hold Time	t_{AH}	15	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	50	--	--	ns
Data Write Time	t_{DW}	55	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	50	--	--	ns
Clock High Time	t_{CLKH}	50	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns

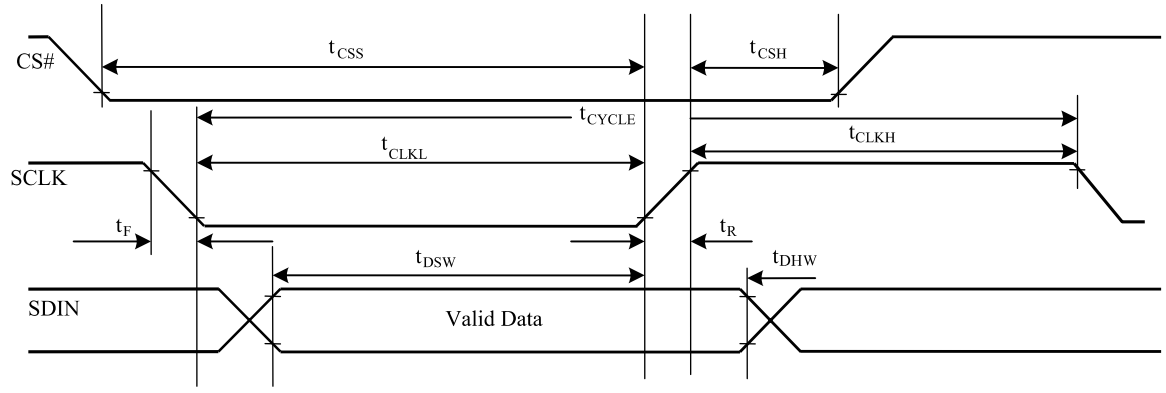


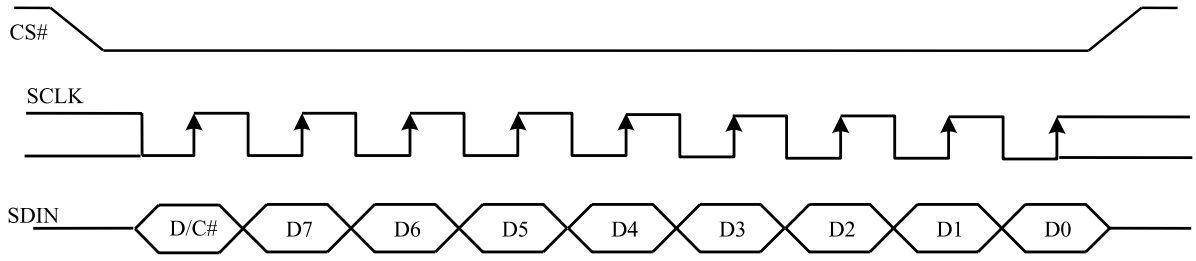


3-wire Serial Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	50	--	--	ns
Data Write Time	t_{DW}	55	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	50	--	--	ns
Clock High Time	t_{CLKH}	50	--	--	ns
Rise Time	t_R	--	--	40	ns
Fall Time	t_F	--	--	40	ns

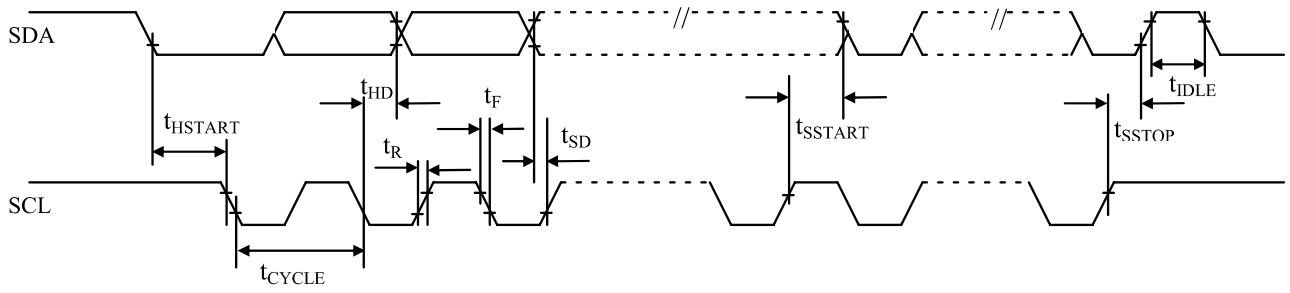




I²C interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	2.5	--	--	µs
Start Condition Hold Time	t_{HSTART}	0.6	--	--	µs
Data Hold Time (for “SDAOUT” pin)	t_{DH}	0	--	--	ns
Data Hold Time (for “SDAIN” pin)		300	--	--	ns
Data Setup Time	t_{SD}	100	--	--	ns
Start Condition Setup Time (Only relevant for a repeated start condition)	t_{SSTART}	0.6	--	--	µs
Stop Condition Setup Time	t_{SSTOP}	0.6	--	--	µs
Rise Time	t_R	--	--	300	ns
Fall Time	t_F	--	--	300	ns
Idle Time Before A New Transmission Can Start	t_{IDLE}	1.3	--	--	µs



4.2 LCM Application

Please see information on page 55 of the data sheet for OLED controller SSD1309Z. The data sheet can be found here: https://focuslcds.com/wp-content/uploads/Drivers/SSD1309Z.pdf

4.3 Command Table

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status A[2]=ob unlock OLED driver IC MCU interface from entering command (RESET) A[2]=1b, lock OLED driver IC MCU interface from entering command Note(1): The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll A[7:0] : Dummy byte (Set as 00h) Horizontal scroll by 1 column B[2:0] : Define start page address
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

C[2:0] : Set time interval between each scroll step in terms of frame frequency

000b – 5 frames	100b – 2 frames
001b – 64 frames	101b – 3 frames
010b – 128 frames	110b – 4 frames
011b – 256 frames	111b – 1 frame

D[2:0] : Define end page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

E[7:0]:Dummy byte (Set as 00h)
F[7:0]: Define the start column (RESET=00h)
G[7:0]:Define the end column address (RESET=7Fh)

Notes:
(1)The value of D[2:0] must be larger or equal to B[2:0]
(2)The value of G[7:0] must be larger or equal to F[7:0]

<table>
<tr><th colspan="12">2. Scrolling Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0
0
0
0
0
0
0</td><td>29/2A
A[0]
B[2:0]
C[2:0]
D[2:0]
E[5:0]
F[7:0]
G[7:0]</td><td>0
*
*
*
*
*
F_7
G_7</td><td>0
*
*
*
*
*
F_6
G_6</td><td>1
*
*
*
*
E_5
F_5
G_5</td><td>0
*
*
*
*
E_4
F_4
G_4</td><td>1
*
*
*
*
E_3
F_3
G_3</td><td>0
*
B_2
C_2
D_2
E_2
F_2
G_2</td><td>X_1
*
B_1
C_1
D_1
E_1
F_1
G_1</td><td>X_0
A_0
B_0
C_0
D_0
E_0
F_0
G_0</td><td>Continuous Vertical and Horizontal Scroll Setup</td><td>29h, X1X0=01b : Vertical and Right Horizontal Scroll
2Ah, X1X0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column)
A[0]: Set number of column scroll offset

B[2:0] : Define start page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency
<table><tr><td>000b – 5 frames</td><td>100b – 2 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 3 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 4 frames</td></tr><tr><td>011b – 256 frames</td><td>111b – 1 frame</td></tr></table>
D[2:0] : Define end page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>
E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =3Fh refer to offset =63 rows
F[7:0]: Define the start column (RESET=00h)
G[7:0]: Define the end column address (RESET=7Fh)

Note
(1) The value of D[2:0] must be larger than or equal to B[2:0]
(2)The value of G[7:0] must be larger than or equal to F[7:0]</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate Scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
<tr><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Activate Scroll</td><td>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:

Valid command sequence 1: 26h ;2Fh.
Valid command sequence 2: 27h ;2Fh.
Valid command sequence 3: 29h ;2Fh.
Valid command sequence 4: 2Ah ;2Fh.

For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</td></tr>
</table>

2. Scrolling Command Table

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0
0</td><td>A3
A[5:0]
B[6:0]</td><td>1
*
*</td><td>0
*
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>0
A_3
B_3</td><td>0
A_2
B_2</td><td>1
A_1
B_1</td><td>1
A_0
B_0</td><td>Set Vertical Scroll Area</td><td>A[5:0]: Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET=0]

B[6:0]: Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET=64]

Note:
(1)A[5:0]+B[6:0]<=MUX ratio
(2)B[6:0]<= MUX ratio
(3a)Vertical scrolling offset (E[5:0] in 29H/2AH)<B[6:0]
(3b)Set display start line ($X_5X_4X_3X_3X_2X_1X_0$ OF 40H~7Fh)
(4)The last row of the scroll area shifts to the first row of the scroll area
(5)For 64d MUX display
A[5:0]=0,B[6:0]=64: Whole area scrolls
A[5:0]=0,B[6:0]<64: Top area scrolls
A[5:0]+B[6:0]<64: Central area scrolls
A[5:0]+B[6:0]=64: Bottom area scrolls
(6)When vertical scrolling is enabled by command 29h/2Ah, the vertical scroll area is defined by this command</td></tr>
<tr><td>0
0
0
0
0
0
0
0</td><td>2C/2D
A[7:0]
B[2:0]
C[7:0]
D[2:0]
E[7:0]
F[7:0]
G[7:0]</td><td>0
0
*
0
*
0
F_7
G_7</td><td>0
0
*
0
*
0
F_6
G_6</td><td>1
0
*
0
*
0
F_5
G_5</td><td>0
0
*
0
*
0
F_4
G_4</td><td>1
0
*
0
*
0
F_3
G_3</td><td>1
0
B_2
0
D_2
0
F_2
G_2</td><td>0
0
B_1
0
D_1
0
F_1
G_1</td><td>X_0
0
B_0
1
D_0
0
F_0
G_0</td><td>Content Scroll Setup</td><td>2Ch, X[0]=0, Right horizontal scroll by one column
2Dh, X[0]=1, Left horizontal scroll by one column
A[7:0]: Dummy byte (set as 00h)
Horizontal scroll by 1 column
B[2:0] : Define start page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>C[7:0] : Dummy byte (set as 01h)
D[2:0] : Define end page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>E[7:0]: Dummy byte (set as 00h)
F[7:0]: Define the start column (RESET=00h)
G[7:0]: Define the end column address (RESET=7Fh)

Note:
(1)The value of D[2:0] must be larger than or equal to B[2:0]
(2)The value of G[7:0] must be larger than F[7:0]
(3)A delay time of 2/FrameFreq must be set if sending the command of 2Ch/2Dh consecutively</td></tr>
</table>

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-127d, (RESET=0d) B[7:0]: Column end address, range : 0-127d, (RESET =127d) Note (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) Note (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. Note (1) This command is only for page addressing mode

4. Hardware Configuration (Panel Resolution & Layout Related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET). A1h, X[0]=1b: column address 127 is mapped to SEG0.
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX). A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1]. C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0. Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d. The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration. A[5]=0b (RESET), Disable COM left/right remap A[5]=1b, Enable COM left/right re map
0 0	DC A[1:0]	1 0	1 0	0 0	1 0	1 0	1 0	0 A_1	0 A_0	Set GPIO	A[1:0]GPIO: 00 pin HiZ, input disabled 01 pin HiZ, input enabled 10 pin output LOW [RESET] 11 pin output HIGH

<table>
<tr><th colspan="12">5. Timing & Driving Scheme Setting Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0</td><td>D5
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>1
A_4</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Display Clock Divide Ratio/Oscillator Frequency</td><td>A[3:0] : Define the divide ratio (D) of the display clocks (DCLK):
Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1).

A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b.
Range:0000b~1111b.
Frequency increases as setting value increases.</td></tr>
<tr><td>0
0</td><td>D9
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Pre-Charge Period</td><td>A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h).

A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h).</td></tr>
<tr><td>0
0</td><td>DB
A[5:2]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
0</td><td>1
0</td><td>Set V_{COMH} Deselect Level</td><td>
<table>
<tr><td>A[5:2]</td><td>Hex code</td><td>V COMH deselect level</td></tr>
<tr><td>0000b</td><td>00h</td><td>~ 0.64 x VCC</td></tr>
<tr><td>1101b</td><td>34h</td><td>~ 0.78 x VCC (RESET)</td></tr>
<tr><td>1111b</td><td>3Ch</td><td>~ 0.84 x VCC</td></tr>
</table>
</td></tr>
</table>

Note

(1) "" stands for "Don't care".*

Bit Pattern	Command	Description
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Status Register Read	D[7]: Reserved D[6]: "1" for display OFF/"0" for display ON D[5]: Reserved D[4]: Reserved D[3]: Reserved D[2]: Reserved D[1]: Reserved D[0]: Reserved

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

5. Cautions and Handling Precautions

5.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

5.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.