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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic OLED Module

Part Number

O25664A-GGS-YW3

Overview:

- 256x64 Graphic OLED
- Monochrome with 16 Gray Scales
- 84.00x25.80mm Module
- 6800/8080 Parallel, 3/4-Wire Serial Interfaces
- Anti-glare Polarizer
- Wide Temp Range
- 3.0V
- LCD IC: SSD1322U
- RoHS Compliant

Graphic OLED LCD Features

Resolution: 128x64 Dots
Interface(s): 6800/8080 Parallel, 3/4-Wire Serial
RoHS Compliant

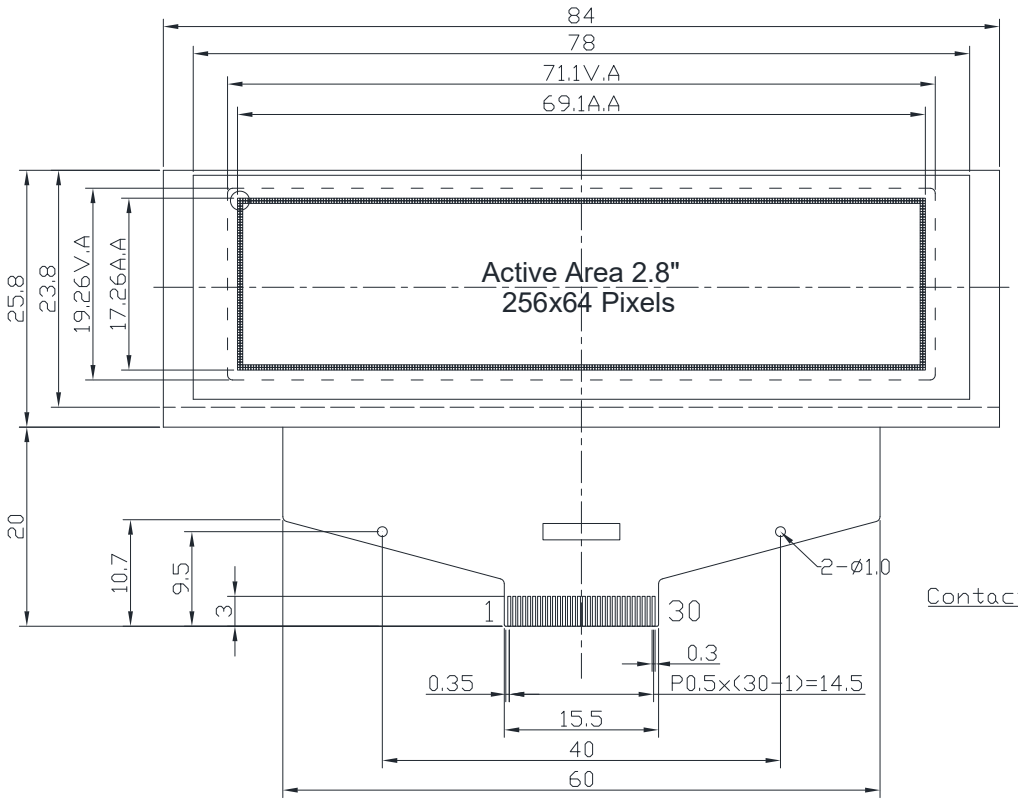
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	71.10 (H) x 19.26 (V)	mm	--
Pixel Color	White	--	--
Viewing Angle	All	degrees	--
Polarizer	Anti-glare	--	--
Controller IC	SSD1322U	--	--
Operating Temperature	-40 to +70	°C	--
Storage Temperature	-40 to +85	°C	--
Voltage	3.0	V	--
Resolution	256x64	--	--

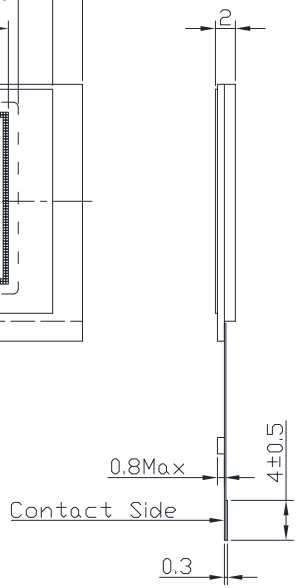
Mechanical Information

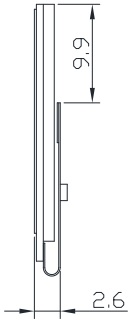
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	84.00	--	mm	--
	Vertical (V)	--	25.80	--	mm	--
	Depth (D)	--	2.00	--	mm	--
Weight		--	9.1	--	g	Approximate

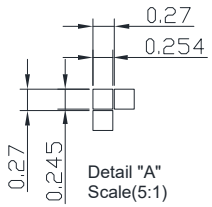
1. Outline Dimensions

Rev.	Description	Date
1.0	First	2017.08.26









NO	PIN
1	NC
2	VSS
3	VCC
4	VCOMH
5	VLSS
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E/RD#
15	R/W#
16	BS0
17	BS1
18	DC#
19	CS#
20	RES#
21	FR
22	IREF
23	NC
24	VDDIO
25	VDD
26	VCI
27	VSL
28	VLSS
29	VCC
30	NC

NOTES:
1. DISPLAY TYPE: 256x64 MONOCHRIME WITH 16 GRAY SCALE GRAPHIC OLED
2. POLARIZER: ANTI-GLARE
3. VIEWING ANGLE: ALL VIEW
4. OPERATING TEMPERATURE: -40°C TO +70°C
   STORAGE TEMPERATURE: -40°C TO +85°C
5. CONTROLLER IC: SSD1322U
6. ROHS COMPLIANT.

Model Name: O25664A-GGS-YW3		FOCUS LCDs LCDs MADE SIMPLE®	
General Tol: ±0.3			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm / Page: 1/1
APP:			

2. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	N.C.(GND)	Reserved pin (supporting pin). The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.	--
2	VSS	Ground of logic circuit. This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.	P
3	VCC	Power supply for OEL panel. These are the most positive voltage supply pin of the chip. They must be connected to external source.	P
4	VCOMH	Voltage output high level for COM signal. This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and Vss.	P
5	VLSS	Ground of analog circuit. These are the analog ground pins. They should be connected to VSS externally.	P
6~13	D7~D0	Host data input/output bus. These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.	I/O
14	E/RD#	Read/Write enable or read. This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.	I
15	R/W#	Read/Write select or write. This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.	I
16	BS0	Communicating protocol select. These pins are MCU interface selection input. See the following table: BS0=1;BS1=0: 3-wire SPI; BS0=0;BS1=0:4-wire SPI; BS0=1;BS1=1:8-bit 68XX Parallel; BS0=0;BS1=1:8-bit 80XX Parallel;	I
17	BS1		
18	D/C#	Data/Command control. This pin is Data/Command control pin. When the pin is pulled high, the input at D7~DO is treated as display data. When the pin is pulled low, the input at D7~DO will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire serial mode is selected, this pin must be connected to VSS. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.	I
19	CS#	Chip select. This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.	I

20	RES#	Power reset for controller and driver. This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.	I
21	FR	Frame frequency triggering signal. This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.	O
22	IREF	Current reference for brightness adjustment. This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10 A maximum.	I
23	N.C.	Reserved pin. The N.C. pin between function pins is reserved for compatible and flexible design.	--
24	VDDIO	Power supply for I/O pin. This pin is a power supply pin of I/O buffer. It should be connected to VcI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals...) pull high, they should be connected to VDDIO.	P
25	VDD	Power supply for core logic circuit. This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.	P
26	VCI	Power supply for operation. This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.	P
27	VSL	Voltage output low level for SEG signal. This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.	P
28	VLSS	Ground of analog circuit. These are the analog ground pins. They should be connected to Vss externally.	P
29	VCC	Power supply for OEL panel. These are the most positive voltage supply pin of the chip. They must be connected to external source.	P
30	N.C.(GND)	Reserved pin (supporting pin). The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.	--

3. Absolute Maximum Ratings

Characteristics	Symbol	Notes	Min	Max	Unit
Supply Voltage (Operation)	VCI	1,2	-0.5	4	V
Supply Voltage (Logic)	VDD	1,2	-0.5	2.75	V
Supply Voltage (I/O Pins)	VDDIO	1,2	-0.5	VCI	V
Supply Voltage (Display)	VCC	1,2	-0.5	16	V
Operating Current for VCC	ICC	1,2	--	60	mA
Operating Temprature	TCP	3	-40	85	℃
Storage Temprature	TSTG	3	-40	90	℃
Lifetime (100 cd/m^2)		4	15,000	--	Hour
Liftime (80 cd/m^2)		4	25,000	--	Hour

Notes:

(1) *All the above voltages are on the basis of "VSS=0V".*

(2) *When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to section 3." optics & electrical characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.*

(3) *The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.*

(4) *VCC=12.0V, TA=2580℃, checkerboard. Software configuration follow section 4.5 initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.*

3.1 Optical Characteristics

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Brightness	LBR		80	100	--	Cd/m^2
CIE (White)	X	CIE 1931	0.25	0.29	0.33	V
CIE (White)	Y	CIE 1931	0.27	0.31	0.35	V
Dark Room Contrast	CR		--	>10,000:1	--	V
Viewing Angle			--	Free	--	Degree

4. Electrical Characteristics

4.1 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage (Operation)		VCI	--	2.4	2.8	3.5	V
Supply Voltage (Logic)		VDD	--	2.4	2.5	2.6	V
Supply Voltage (I/O Pins)		VDDIO	--	1.65	1.8	VCI	V
Supply Voltage (Display)		VCC	Note 5	11.5	12.0	12.5	V
Input Voltage	H Level	V_{IH}	--	0.8*VDD	--	VDDIO	V
	L Level	V_{IL}	--	0	--	0.2*VDD	V
Output Voltage	H Level	V_{OH}	I_{OUT} =100μA	0.9*VDD	--	VDDIO	V
	L Level	V_{OL}	I_{OUT} =100μA	0	--	0.1*VDD	V
Operating Current for VCC		ICC	Note 6	--	15.6	19.5	mA
			Note 7	--	26.1	32.7	
			Note 8	--	44.7	55.9	
Operating Current for VCI		ICI	--	--	180	300	uA
Sleep Mode Current (VCI)		ICI, Sleep	--	--	20	100	uA
Sleep Mode Current (VDDIO)		IDDIO,Sleep	--	--	2	10	uA

Notes:

(5) *Brightness (Lbr) and Supply Voltage for Display (Vcc) are subject to the change of the panel characteristics and the customer's request.*

(6) *VcI=2.8V, Vcc= 12.0V, 30% Display Area Turn on.*

(7) *VcI=2.8V, Vcc= 12.0V, 50% Display Area Turn on.*

(8) *VcI= 2.8V, Vcc=12.0V, 100% Display Area Turn on.*

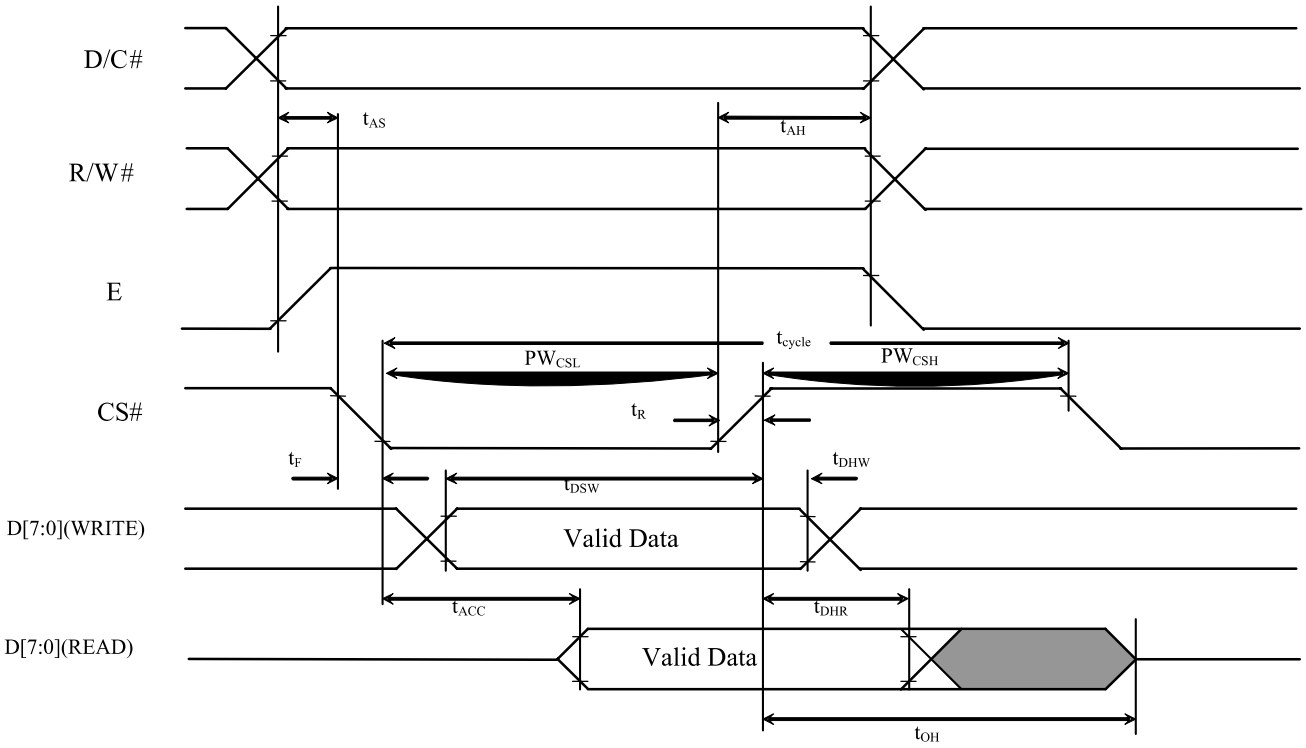
5. Module Function

5.1 Timing Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 3.3V, Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	10	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	7	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	PW_{CSL}	120	--	--	ns
Chip Select Low Pulse Width (write)		60	--	--	ns
Chip Select High Pulse Width (read)	PW_{CSH}	60	--	--	ns
Chip Select High Pulse Width (write)		60	--	--	ns
Rise Time	t_R	--	--	15	ns
Fall Time	t_F	--	--	15	ns

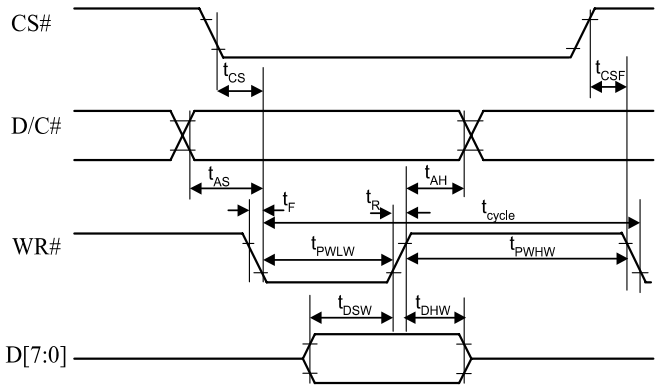


8080-Series MCU Parallel Interface Timing Characteristics

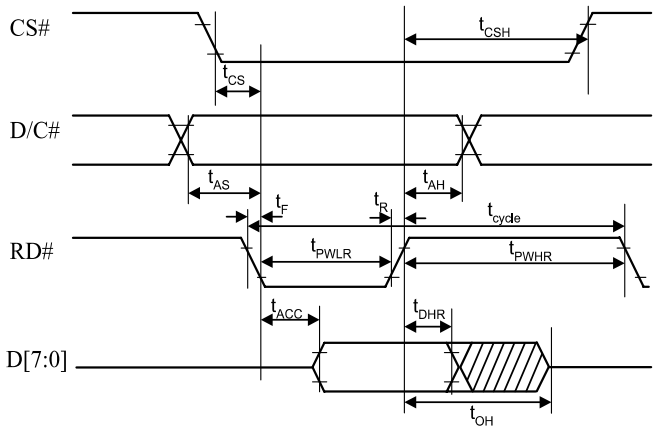
(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 3.3V Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	300	--	--	ns
Address Setup Time	t_{AS}	10	--	--	ns
Address Hold Time	t_{AH}	0	--	--	ns
Write Data Setup Time	t_{DSW}	40	--	--	ns
Write Data Hold Time	t_{DHW}	7	--	--	ns
Read Data Hold Time	t_{DHR}	20	--	--	ns
Output Disable Time	t_{OH}	--	--	70	ns
Access Time	t_{ACC}	--	--	140	ns
Chip Select Low Pulse Width (read)	t_{PWLR}	150	--	--	ns
Chip Select Low Pulse Width (write)	t_{PWLW}	60	--	--	ns
Chip Select High Pulse Width (read)	t_{PWHR}	60	--	--	ns
Chip Select High Pulse Width (write)	t_{PWHW}	60	--	--	ns
Rise Time	t_R	--	--	15	ns
Fall Time	t_F	--	--	15	ns
Chip Select Setup Time	t_{CS}	0	--	--	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	--	--	ns
Chip Select Hold Time	t_{CSF}	20	--	--	ns

Write Cycle



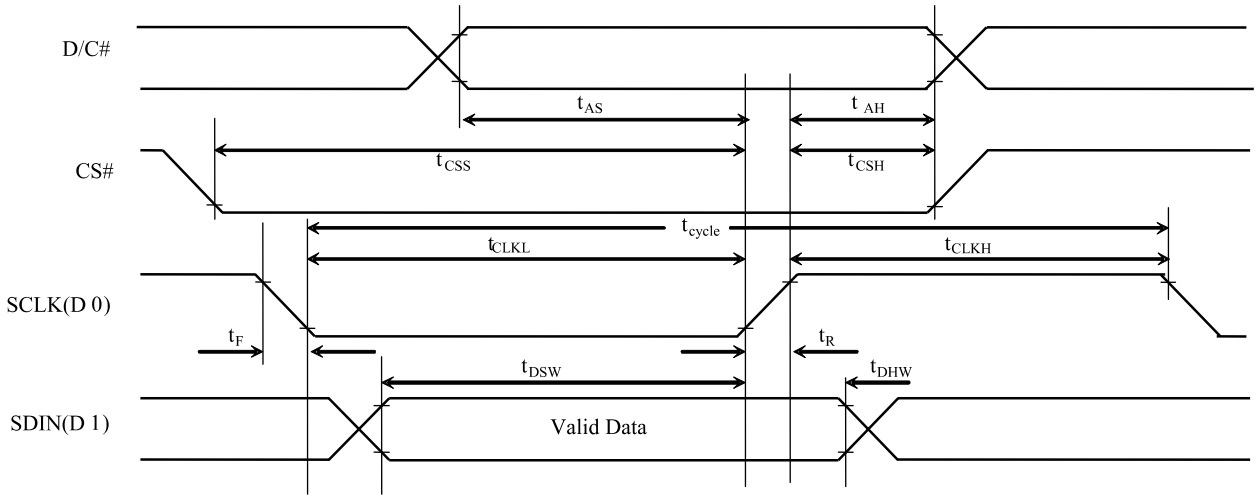
Read cycle

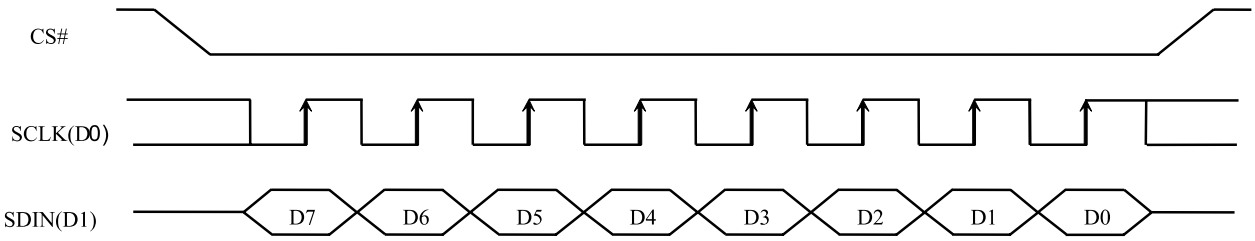


4-wire Serial Interface Timing Characteristics

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 3.3V Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Address Setup Time	t_{AS}	15	--	--	ns
Address Hold Time	t_{AH}	15	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	10	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	20	--	--	ns
Clock High Time	t_{CLKH}	20	--	--	ns
Rise Time	t_R	--	--	15	ns
Fall Time	t_F	--	--	15	ns

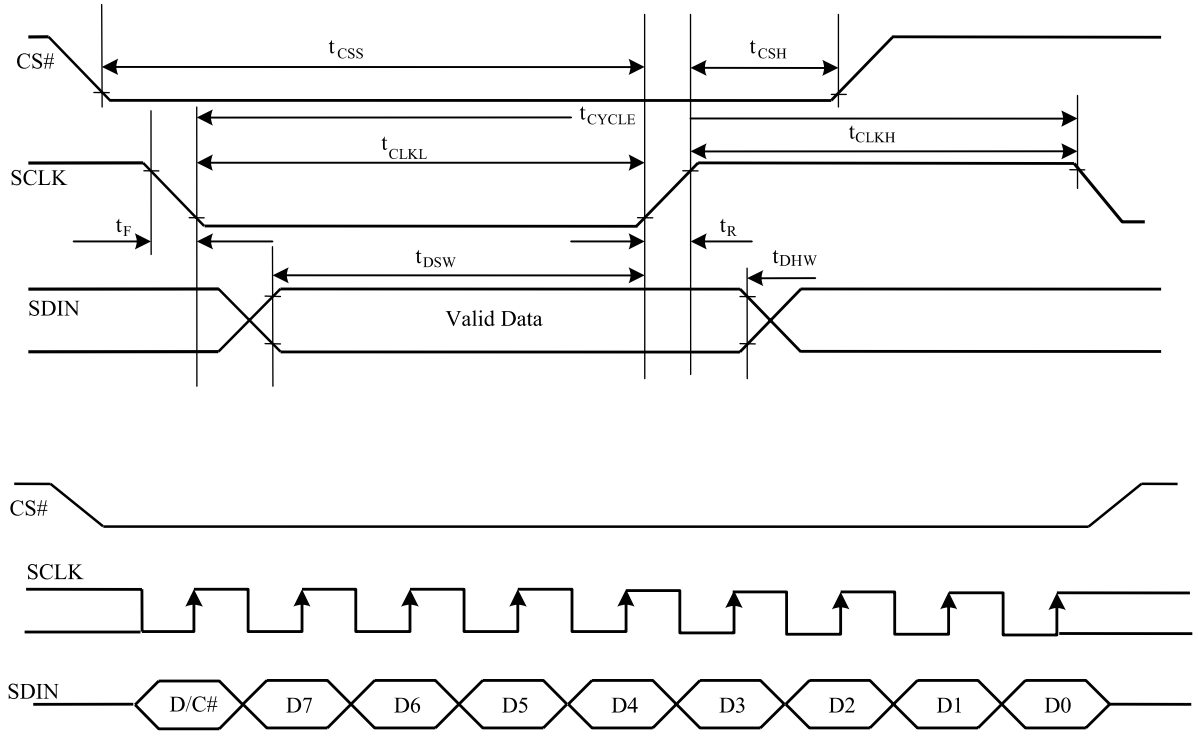




3-wire Serial Interface Timing Characteristics

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 3.3V Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
Clock Cycle Time	t_{cycle}	100	--	--	ns
Chip Select Setup Time	t_{CSS}	20	--	--	ns
Chip Select Hold Time	t_{CSH}	10	--	--	ns
Write Data Setup Time	t_{DSW}	15	--	--	ns
Write Data Hold Time	t_{DHW}	15	--	--	ns
Clock Low Time	t_{CLKL}	20	--	--	ns
Clock High Time	t_{CLKH}	20	--	--	ns
Rise Time	t_R	--	--	15	ns
Fall Time	t_F	--	--	15	ns



5.2 LCM Application

Please see information on page 55 of the data sheet for OLED controller SSD1322 and equivalents. The data sheet can be found here: https://focuslcds.com/wp-content/uploads/Drivers/SSD1322.pdf

5.3 Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>A2
A[6:0]</td><td>1
*</td><td>0
A_6</td><td>1
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Display Offset</td><td>Set vertical scroll by COM from 0-127
The value is reset to 00H after RESET</td></tr>
<tr><td>0</td><td>A4~A7</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Display Mode</td><td>A4h = Entire Display OFF, all pixels turns OFF in GS level 0
A5h = Entire Display ON, all pixels turns ON in GS level 15
A6h = Normal Display [reset]
A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)</td></tr>
<tr><td>0
1
1</td><td>A8
A[6:0]
B[6:0]</td><td>1
0
0</td><td>0
A_6
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>1
A_3
B_3</td><td>0
A_2
B_2</td><td>0
A_1
B_1</td><td>0
A_0
B_0</td><td>Enable Partial Display</td><td>This command turns ON partial mode. The partial mode display area is defined by the following two parameters,
A[6:0]: Address of start row in the display area
B[6:0]: Address of end row in the display area,
where B[6:0] must be ≥ A[6:0]</td></tr>
<tr><td>0</td><td>A9</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Exit Partial Display</td><td>This command is sent to exit the Partial Display mode</td></tr>
<tr><td>0
1</td><td>AB
A[0]</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
A_0</td><td>Function Selection</td><td>A[0]=0b, Select external V_{DD}
A[0]=1b, Enable internal V_{DD} regulator [reset]</td></tr>
<tr><td>0</td><td>AE~AF</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>X_0</td><td>Set Sleep mode ON/OFF</td><td>AEh = Sleep mode ON (Display OFF)
AFh = Sleep mode OFF (Display ON)</td></tr>
<tr><td>0
1</td><td>B1
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Phase Length</td><td>A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow:
<table>
<tr><th>A[3:0]</th><th>Phase 1 period</th></tr>
<tr><td>0000</td><td>invalid</td></tr>
<tr><td>0001</td><td>invalid</td></tr>
<tr><td>0010</td><td>5 DCLKs</td></tr>
<tr><td>0011</td><td>7 DCLKs</td></tr>
<tr><td>0100</td><td>9 DCLKs [reset]</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1111</td><td>31 DCLKs</td></tr>
</table>
A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:
<table>
<tr><th>A[7:4]</th><th>Phase 2 period</th></tr>
<tr><td>0000</td><td>invalid</td></tr>
<tr><td>0001</td><td>invalid</td></tr>
<tr><td>0010</td><td>invalid</td></tr>
<tr><td>0011</td><td>3 DCLKs</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>0111</td><td>7 DCLKs [reset]</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1111</td><td>15 DCLKs</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=0101b]</td></tr>
<tr><td>0
1
1</td><td>B4
A[1:0]
B[7:3]</td><td>1
1
B_7</td><td>0
0
B_6</td><td>1
1
B_5</td><td>1
0
B_4</td><td>0
0
B_3</td><td>1
0
1</td><td>0
A_1
0</td><td>0
A_0
1</td><td>Display Enhancement A</td><td>A[1:0] = 00b: Enable external VSL
A[1:0] = 10b: Internal VSL [reset]

B[7:3] = 11111b: Enhanced low GS display quality
B[7:3] = 10110b: Normal [reset]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
.....
1000b 8 dclks [reset]
.....
1111b 15 dclks</td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>B8</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="10">Set Gray Scale Table</td><td rowspan="10">The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)

A1[7:0]: Gamma Setting for GS1,
A2[7:0]: Gamma Setting for GS2,
:
A14[7:0]: Gamma Setting for GS14,
A15[7:0]: Gamma Setting for GS15

Note
(1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15

Refer to Section 8.8 for details

(2) The setting must be followed by the Enable Gray Scale Table command (00h)</td></tr>
<tr><td>1</td><td>A1[7:0]</td><td>$A1_7$</td><td>$A1_6$</td><td>$A1_5$</td><td>$A1_4$</td><td>$A1_3$</td><td>$A1_2$</td><td>$A1_1$</td><td>$A1_0$</td></tr>
<tr><td>1</td><td>A2[7:0]</td><td>$A2_7$</td><td>$A2_6$</td><td>$A2_5$</td><td>$A2_4$</td><td>$A2_3$</td><td>$A2_2$</td><td>$A2_1$</td><td>$A2_0$</td></tr>
<tr><td>1</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>1</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>1</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>1</td><td>A14[7:0]</td><td>$A14_7$</td><td>$A14_6$</td><td>$A14_5$</td><td>$A14_4$</td><td>$A14_3$</td><td>$A14_2$</td><td>$A14_1$</td><td>$A14_0$</td></tr>
<tr><td>1</td><td>A15[7:0]</td><td>$A15_7$</td><td>$A15_6$</td><td>$A15_5$</td><td>$A15_4$</td><td>$A15_3$</td><td>$A15_2$</td><td>$A15_1$</td><td>$A15_0$</td></tr>
<tr><td>0</td><td>B9</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Select Default Linear Gray Scale table</td><td>The default Linear Gray Scale table is set in unit of DCLK's as follow

GS0 level pulse width = 0;
GS1 level pulse width = 0;
GS2 level pulse width = 8;
GS3 level pulse width = 16;
:
:
GS14 level pulse width = 104;
GS15 level pulse width = 112

Refer to Section 8.8 for details</td></tr>
<tr><td>0
1</td><td>BB
A[4:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Pre-charge voltage</td><td>Set pre-charge voltage level.[reset = 17h]

<table><tr><th>A[4:0]</th><th>Hex code</th><th>pre-charge voltage</th></tr><tr><td>00000</td><td>00h</td><td>0.20 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>11111</td><td>1Fh</td><td>0.60 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>BE
A[2:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>1
0</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set V_{COMH}</td><td>Set COM deselect voltage level [reset = 04h]

<table><tr><th>A[2:0]</th><th>Hex code</th><th>V_{COMH}</th></tr><tr><td>000</td><td>00h</td><td>0.72 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>100</td><td>04h</td><td>0.80 x V_{CC} [reset]</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>111</td><td>07h</td><td>0.86 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>C1
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Contrast Current</td><td>A[7:0]: Contrast current value, range:00h~FFh,
i.e. 256 steps for I_{SEG} current [reset = 7Fh]</td></tr>
</table>

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]
0 1	CA A[6:0]	1 *	1 A_6	0 A_5	0 A_4	1 A_3	0 A_2	1 A_1	0 A_0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]
0 1 1	D1 A[5:4] 20	1 1 0	1 0 0	0 A_5 1	1 A_4 0	0 0 0	0 0 0	0 1 0	1 0 0	Display Enhancement B	A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

Note

(1) "" stands for "Don't care".*

6. Cautions and Handling Precautions

6.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

6.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%.
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.